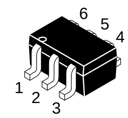
MDC3238T1

Integrated Dual Inductive Load Driver



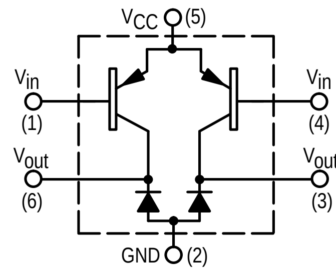
CASE 419B–01
SC–70/SOT–363

Application circuit designs are moving toward the consolidation of device count and into smaller packages. The new SOT–363 package is a solution which simplifies circuit design, reduces device count, and reduces board space by integrating a few discrete devices into one small six–leaded package. The SOT–363 is ideal for low–power surface mount applications where board space is at a premium, such as portable products.

This device is intended to replace an array of four to eight discrete components in an integrated SOT–363 package.

- Optimized to Switch Inductive Pager/Phone Loads Such as Motors, Lamps and Speakers from a 0.9 to 1.7 V Rail
- Low $V_{CE(sat)}$ Performance
- Internal Output Clamp Diodes
- Provide a Robust Driver Interface between Inductive Load and Sensitive Logic Circuits

INTERNAL CIRCUIT DIAGRAM



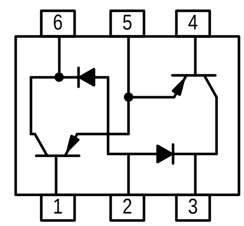
Applications include:

- Pager Silent Alert Motor
- Pager E/M Acoustic Transducers

Ordering Information:

- MDC3238T1: 8 mm, 7–inch/3,000 Unit Tape and Reel
- MDC3238T3: 8 mm, 13–inch/10,000 Unit Tape and Reel

INTERNAL CIRCUIT DIAGRAM



MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	15	Vdc
Collector–Base Voltage	V_{CBO}	15	Vdc
Emitter–Base Voltage	V_{EBO}	5.0	Vdc
Collector–Current — Continuous	I_C	200	mAdc
Diode Reverse Voltage	V_R	8.0	Vdc

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Total Device Dissipation	P_D	150	mW
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	833	°C/W
Junction and Storage Temperature	T_J, T_{stg}	–55 to 150	°C

DEVICE MARKING

MDC3238T1 = E8

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector–Emitter Breakdown Voltage (I_C = 1.0 mAdc, I_B = 0 mAdc)	$V_{(BR)CEO}$	15	—	—	Vdc
Collector–Base Breakdown Voltage (I_C = 10 μAdc, I_E = 0 mAdc)	$V_{(BR)CBO}$	15	—	—	Vdc
Emitter–Base Breakdown Voltage (I_C = 10 μAdc, I_C = 0 mAdc)	$V_{(BR)EBO}$	5.0	—	—	Vdc
ON CHARACTERISTICS					
DC Current Gain (I_C = 100 mAdc, V_{BE} = 5.0 Vdc)	h_{FE}	100	—	400	—
Collector–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 1.0 mAdc)	$V_{CE(sat)}$	—	—	0.175	Vdc
Base–Emitter Saturation Voltage (I_C = 100 mAdc, I_B = 1.0 mAdc)	$V_{BE(sat)}$	—	—	0.900	Vdc
SMALL–SIGNAL CHARACTERISTICS					
Current–Gain — Bandwidth Product (I_C = 50 mAdc, V_{CE} = 5.0 Vdc, f = 20 MHz)	f_T	100	—	—	MHz
Output Capacitance (V_{CB} = 10 Vdc, f = 1.0 MHz)	C_{obo}	—	—	18	pF
Input Capacitance (V_{EB} = 0.5 Vdc, f = 1.0 MHz)	C_{ibo}	—	—	105	pF
DIODE CHARACTERISTICS					
Reverse Breakdown Voltage ($I_{(BR)}$ = 100 μAdc)	$V_{(BR)}$	8.0	—	—	Vdc
Forward Voltage (I_F = 50 mAdc)	V_F	—	—	1.0	Vdc
Reverse Recovery Time (I_F = I_R = 10 mAdc)	t_{rr}	—	—	25	ns

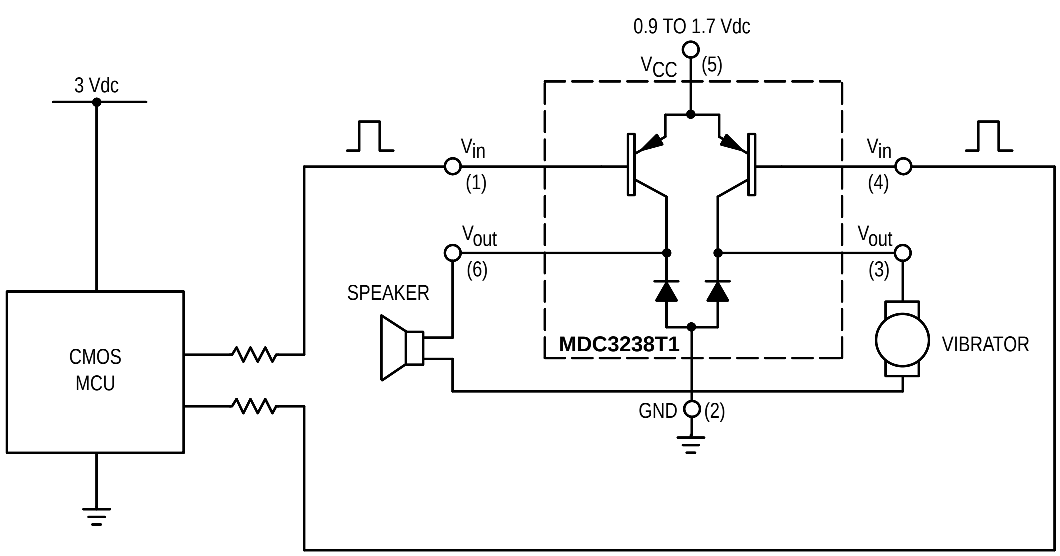


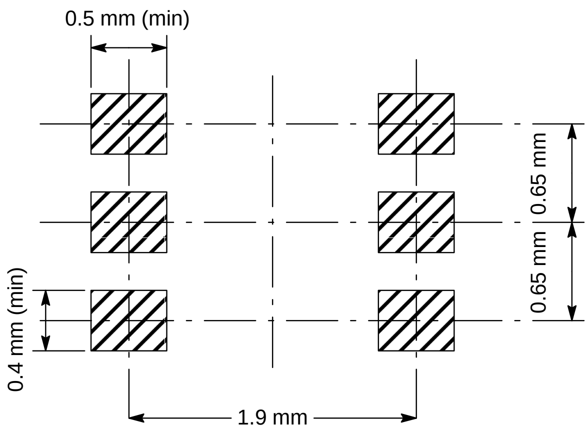
Figure 1. Multiple Loads With Dual Inductive Load Driver

INFORMATION FOR USING THE SOT–363 SURFACE MOUNT PACKAGE

MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.

SOT–363



SOT–363 POWER DISSIPATION

The power dissipation of the SOT–363 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, T_A. Using the values provided on the data sheet for the SOT–363 package, P_D can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature T_A of 25°C, one can calculate the power dissipation of the device which in this case is 120 milliwatts.

$$P_D = \frac{120°C - 25°C}{833°C/W} = 120 \text{ milliwatts}$$

The 833°C/W for the SOT–363 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 120 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–363 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

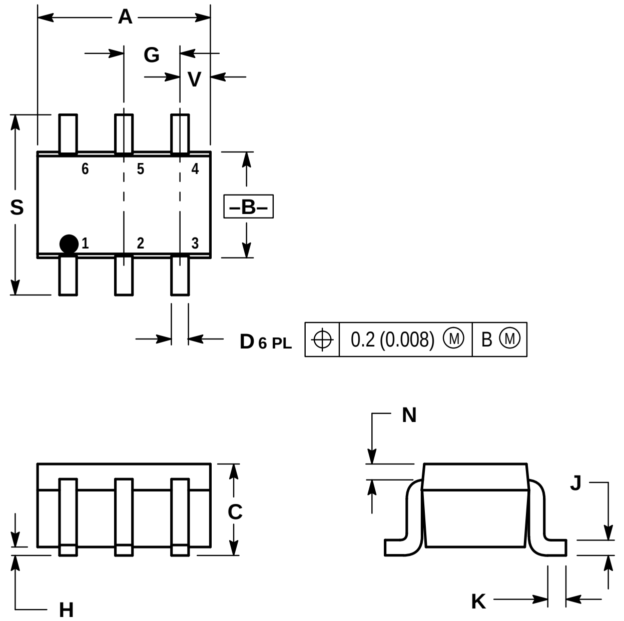
SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES MIN	INCHES MAX	MILLIMETERS MIN	MILLIMETERS MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	—	0.004	—	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20
V	0.012	0.016	0.30	0.40

CASE 419B–01
ISSUE C

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