

## 6 Output PCI Express\* Buffer with CLKREQ# Function

### Recommended Application:

1-to-6 Zero-delay or fanout buffer for PCI Express

### Output Features:

- 6 - 0.7V current mode differential output pairs (HSCL)
- SMBus for complete device control

### Key Specifications:

- Cycle-to-cycle jitter < 40ps
- Output-to-output skew < 30 ps

### Features/Benefits:

- CLKREQ# pin for outputs 1 and 4/output enable for Express Card applications
- PLL or bypass mode/PLL can dejitter incoming clock
- Selectable PLL bandwidth/minimizes jitter peaking in downstream PLL's
- Spread Spectrum Compatible/tracks spreading input clock for low EMI
- SMBus Interface/unused outputs can be disabled

### Pin Configuration

PLL_BW	1	28	VDDA
CLK_INT	2	27	GNDA
CLK_INC	3	26	IREF
CLKREQ1#	4	25	**CLKREQ4#
PCIEXT0	5	24	PCIEXT5
PCIEXC0	6	23	PCIEXC5
VDD	7	22	VDD
GND	8	21	GND
PCIEXT1	9	20	PCIEXT4
PCIEXC1	10	19	PCIEXC4
PCIEXT2	11	18	PCIEXT3
PCIEXC2	12	17	PCIEXC3
VDD	13	16	VDD
SMBDAT	14	15	SMBCLK

**ICS9DB106**

### Note:

Pins preceded by '\*\*' have internal 120K ohm pull down resistors

### 28-pin SSOP & TSSOP

## Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	PLL_BW	IN	3.3V input for selecting PLL Band Width 0 = low, 1 = high
2	CLK_INT	IN	"True" reference clock input.
3	CLK_INC	IN	"Complimentary" reference clock input.
4	**CLKREQ1#	IN	Output enable for PCI Express output pair '1' 0 = enabled, 1 = tri-stated
5	PCIEXT0	OUT	True clock of differential PCI_Express pair.
6	PCIEXC0	OUT	Complement clock of differential PCI_Express pair.
7	VDD	PWR	Power supply, nominal 3.3V
8	GND	IN	Ground pin.
9	PCIEXT1	OUT	True clock of differential PCI_Express pair.
10	PCIEXC1	OUT	Complement clock of differential PCI_Express pair.
11	PCIEXT2	OUT	True clock of differential PCI_Express pair.
12	PCIEXC2	OUT	Complement clock of differential PCI_Express pair.
13	VDD	PWR	Power supply, nominal 3.3V
14	SMBDAT	I/O	Data pin of SMBUS circuitry, 5V tolerant
15	SMBCLK	IN	Clock pin of SMBUS circuitry, 5V tolerant
16	VDD	PWR	Power supply, nominal 3.3V
17	PCIEXC3	OUT	Complement clock of differential PCI_Express pair.
18	PCIEXT3	OUT	True clock of differential PCI_Express pair.
19	PCIEXC4	OUT	Complement clock of differential PCI_Express pair.
20	PCIEXT4	OUT	True clock of differential PCI_Express pair.
21	GND	PWR	Ground pin.
22	VDD	PWR	Power supply, nominal 3.3V
23	PCIEXC5	OUT	Complement clock of differential PCI_Express pair.
24	PCIEXT5	OUT	True clock of differential PCI_Express pair.
25	**CLKREQ4#	IN	Output enable for PCI Express output pair '4' 0 = enabled, 1 = tri-stated
26	IREF	OUT	This pin establishes the reference current for the differential current-mode output pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current. 475 ohms is the standard value.
27	GNDA	PWR	Ground pin for the PLL core.
28	VDDA	PWR	3.3V power for the PLL core.

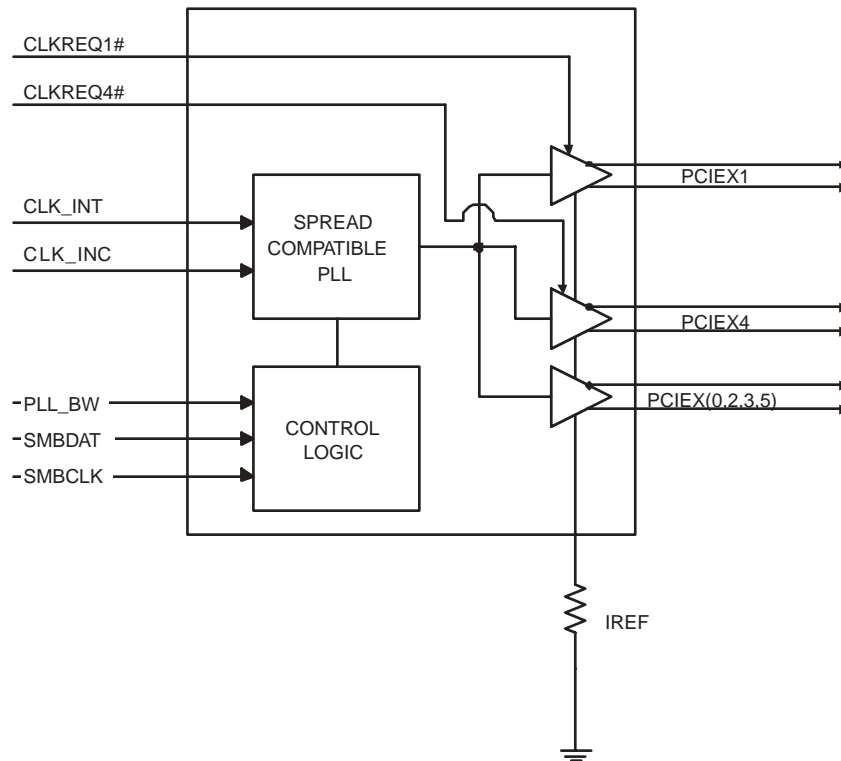
**Note:**

Pins preceded by \*\*\* have internal 120K ohm pull down resistors

### General Description

The **ICS9DB106** zero-delay buffer supports PCI Express clocking requirements. The **ICS9DB106** is driven by a differential SRC output pair from an ICS CK409/CK410-compliant main clock generator such as the ICS952601 or ICS954101. It attenuates jitter on the input clock and has a selectable PLL bandwidth to maximize performance in systems with or without Spread-Spectrum clocking. An SMBus interface allows control of the PLL bandwidth and bypass options, while 2 clock request (OE#) pins make the **ICS9DB106** suitable for Express Card applications.

### Block Diagram



### Power Groups

Pin Number		Description
VDD	GND	
7, 13, 16, 22	8,21	PCI Express Outputs
TBD	TBD	SMBUS
N/A	27	IREF
28	27	Analog VDD & GND for PLL core

### Absolute Max

Symbol	Parameter	Min	Max	Units
VDDA	3.3V Core Supply Voltage		$V_{DD} + 0.5V$	V
VDD	3.3V Output Supply Voltage	GND - 0.5	$V_{DD} + 0.5V$	V
Ts	Storage Temperature	-65	150	°C
Tambient	Ambient Operating Temp	0	70	°C
Tcase	Case Temperature		115	°C
ESD prot	Input ESD protection human body model	2000		V

### Electrical Characteristics - Input/Supply/Common Output Parameters

T<sub>A</sub> = 0 - 70°C; Supply Voltage V<sub>DD</sub> = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	Notes
Input High Voltage	V <sub>IH</sub>	3.3 V +/-5%	2		V <sub>DD</sub> + 0.3	V	1
Input Low Voltage	V <sub>IL</sub>	3.3 V +/-5%	V <sub>SS</sub> - 0.3		0.8	V	1
Input High Current	I <sub>IH</sub>	V <sub>IN</sub> = V <sub>DD</sub>	-5		5	uA	1
Input Low Current	I <sub>IL1</sub>	V <sub>IN</sub> = 0 V; Inputs with no pull-up resistors	-5			uA	1
	I <sub>IL2</sub>	V <sub>IN</sub> = 0 V; Inputs with pull-up resistors	-200			uA	1
Operating Supply Current	I <sub>DD3,3OP</sub>	Full Active, C <sub>L</sub> = Full load;		130	150	mA	1
		all differential pairs tri-stated		30	40	mA	1
Input Frequency	F <sub>i</sub>	V <sub>DD</sub> = 3.3 V	99	100	101	MHz	
Pin Inductance	L <sub>pin</sub>				7	nH	1
Input Capacitance	C <sub>IN</sub>	Logic Inputs			5	pF	1
	C <sub>OUT</sub>	Output pin capacitance			4.5	pF	1
Clk Stabilization	T <sub>STAB</sub>	From VDD reaching 3.1V and input clock stable			1.8	ms	1
Input Spread Spectrum Modulation Frequency		Triangular Modulation	30		33	kHz	1
SMBus Voltage	V <sub>DD</sub>		2.7		5.5	V	1
Low-level Output Voltage	V <sub>OL</sub>	@ I <sub>PULLUP</sub>			0.4	V	1
Current sinking at V <sub>OL</sub> = 0.4 V	I <sub>PULLUP</sub>		4			mA	1
SCLK/SDATA Clock/Data Rise Time	T <sub>RI2C</sub>	(Max VIL - 0.15) to (Min VIH + 0.15)			1000	ns	1
SCLK/SDATA Clock/Data Fall Time	T <sub>FI2C</sub>	(Min VIH + 0.15) to (Max VIL - 0.15)			300	ns	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

### Electrical Characteristics - PCIeX 0.7V Current Mode Differential Outputs

$T_A = 0 - 70^\circ\text{C}$ ;  $V_{DD} = 3.3\text{ V} \pm 5\%$ ;  $C_L = 2\text{pF}$ ,  $R_S = 33.2\Omega$ ,  $R_P = 49.9\Omega$   $I_{REF} = 9$ ,

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Current Source Output Impedance	$Z_o^1$	$V_O = V_x$	3000			$\eta$	1
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660		850	mV	1,3
Voltage Low	VLow		-150		150		1,3
Max Voltage	Vovs	Measurement on single ended signal using absolute value.			1150	mV	1,3
Min Voltage	Vuds		-300				1,3
Crossing Voltage (abs)	Vcross(abs)		250		550	mV	1,3
Crossing Voltage (var)	d-Vcross	Variation of crossing over all edges			140	mV	1,3
Long Accuracy	ppm	see Tperiod min-max values			0	ppm	1,2
Average period	$T_{period}$	100.00MHz nominal	9.9970		10.0030	ns	2
		100.00MHz spread	9.9970		10.0533	ns	2
Absolute min period	$T_{absmin}$	100.00MHz nominal/spread	9.8720			ns	1,2
Rise Time	$t_r$	$V_{OL} = 0.175\text{V}$ , $V_{OH} = 0.525\text{V}$	175		700	ps	1
Fall Time	$t_f$	$V_{OH} = 0.525\text{V}$ , $V_{OL} = 0.175\text{V}$	175		700	ps	1
Rise Time Variation	d- $t_r$				125	ps	1
Fall Time Variation	d- $t_f$				125	ps	1
Input to Output Delay	$t_{pd}$	PLL Mode.	100		150	ps	1
	$t_{pdby}$	Bypass mode	3.2		3.7	ns	1
Duty Cycle	$d_{t3}$	Measurement from differential waveform	45		55	%	1
Output-to-Output Skew	$t_{sk3}$	$V_T = 50\%$			30	ps	1
Jitter, Cycle to cycle	$t_{jyc-cyc}$	PLL mode, Measurement from differential waveform			40	ps	1
		BYPASS mode as additive jitter			25	ps	1

<sup>1</sup>Guaranteed by design and characterization, not 100% tested in production.

<sup>2</sup>All Long Term Accuracy and Clock Period specifications are guaranteed with the assumption that the input clock complies with CK409/CK410 accuracy requirements

<sup>3</sup> $I_{REF} = V_{DD}/(3 \times R_R)$ . For  $R_R = 475\Omega$  (1%),  $I_{REF} = 2.32\text{mA}$ .  $I_{OH} = 6 \times I_{REF}$  and  $V_{OH} = 0.7\text{V}$  @  $Z_O = 50\Omega$ .



**SMBusTable: Device Control Register, READ/WRITE ADDRESS (DC/DD)**

Byte 0		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		SW_EN	Enables SMBus Control	RW	PLL controlled by SMBus registers	PLL controlled by device pins	1
Bit 6	-		RESERVED		RW	-	-	X
Bit 5	-		RESERVED		RW	-	-	X
Bit 4	-		RESERVED		RW	-	-	X
Bit 3	-		RESERVED		RW	-	-	X
Bit 2	-		RESERVED		RW	-	-	X
Bit 1	-		PLL BW #adjust	Selects PLL Bandwidth	RW	Low BW	High BW	1
Bit 0	-		PLL Enable	Bypasses PLL for board test	RW	PLL bypassed (fan out mode)	PLL enabled (ZDB mode)	1

**SMBusTable: Output Enable Register**

Byte 1		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-		RESERVED		RW	-	-	X
Bit 6	-		RESERVED		RW	-	-	X
Bit 5	24,23		PCIEX5	Output Control	RW	Disable	Enable	1
Bit 4	-		RESERVED		RW	-	-	X
Bit 3	18,17		PCIEX3	Output Control	RW	Disable	Enable	1
Bit 2	11,12		PCIEX2	Output Control	RW	Disable	Enable	1
Bit 1	-		RESERVED		RW	-	-	X
Bit 0	5,6		PCIEX0	Output Control	RW	Disable	Enable	1

**SMBusTable: Function Select Register**

Byte 2		Pin #	Name	Control Function	Type	0	1	PWD
Bit 7			RESERVED		RW	-	-	X
Bit 6			RESERVED		RW	-	-	X
Bit 5	-		RESERVED		RW	-	-	X
Bit 4	-		RESERVED		RW	-	-	X
Bit 3	-		RESERVED		RW	-	-	X
Bit 2	-		RESERVED		RW	-	-	X
Bit 1	-		RESERVED		RW	-	-	X
Bit 0	-		RESERVED		RW	-	-	X



**SMBusTable: Vendor & Revision ID Register**

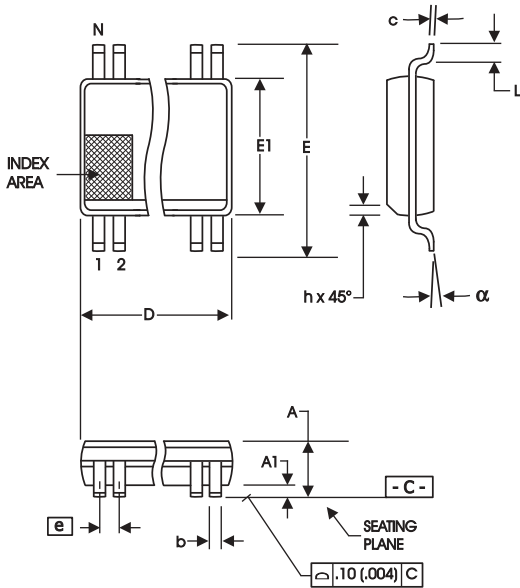
Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	X
Bit 6	-	RID2		R	-	-	X
Bit 5	-	RID1		R	-	-	X
Bit 4	-	RID0		R	-	-	X
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

**SMBusTable: DEVICE ID**

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Device ID = 06 Hex		R	-	-	0
Bit 6	-			R	-	-	0
Bit 5	-			R	-	-	0
Bit 4	-			R	-	-	0
Bit 3	-			R	-	-	0
Bit 2	-			R	-	-	1
Bit 1	-			R	-	-	1
Bit 0	-			R	-	-	0

**SMBusTable: Byte Count Register**

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is 06 = 6 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	0
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	0



**209 mil SSOP**

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	2.00	--	.079
A1	0.05	--	.002	--
A2	1.65	1.85	.065	.073
b	0.22	0.38	.009	.015
c	0.09	0.25	.0035	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	7.40	8.20	.291	.323
E1	5.00	5.60	.197	.220
e	0.65 BASIC		0.0256 BASIC	
L	0.55	0.95	.022	.037
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°

**VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.90	10.50	.390	.413

Reference Doc.: JEDEC Publication 95, MO-150

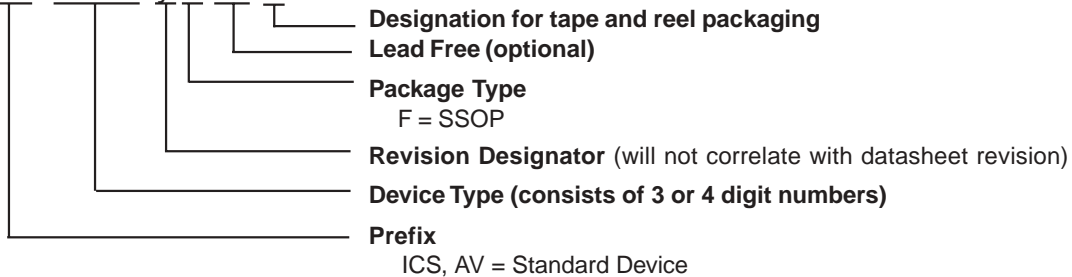
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**Ordering Information**

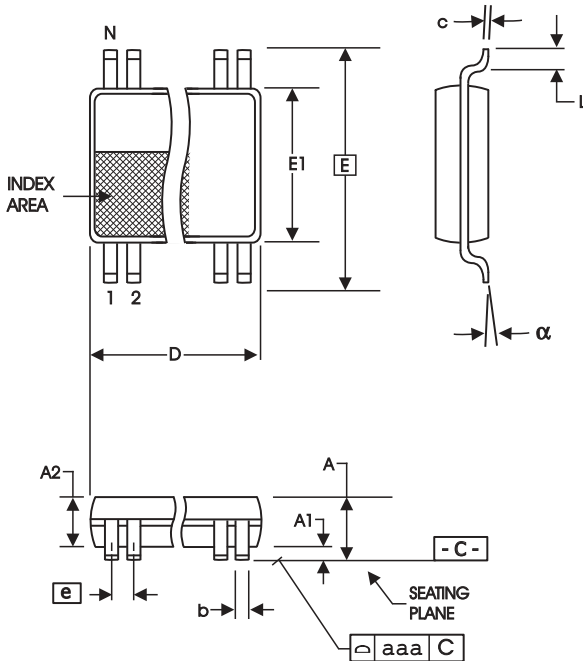
**ICS9DB106yFLF-T**

Example:

**ICS XXXX y F LF-T**







**4.40 mm. Body, 0.65 mm. Pitch TSSOP**  
**(173 mil) (25.6 mil)**

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
a	0°	8°	0°	8°
aaa	--	0.10	--	.004

**VARIATIONS**

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

Reference Doc.: JEDEC Publication 95, MO-153

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**Ordering Information**

**ICS9DB106yGLF-T**

Example:

**ICS XXXX yG LF-T**

