

Framing and Line Interface Component for PCM 30 and PCM 24 FALC54

PEB 2254 Version 1.4

Delta Sheet 10.97

This document describes the **FALC54 V1.4** in relation to **FALC54 V1.3** and hence is a **Delta Sheet** which references the **FALC54 V1.3 Data Sheet 11.96** and the **FALC54 V1.3 Errata Sheet 06.97**

All of the original FALC54 V1.3 features have been retained. Also the FALC54 V1.4 is pin and software compatible to FALC54 V1.3.

All of the erratas described in the FALC54 V1.3 Errata Sheet are removed except the following two:

- LIM2 Register is writeable but not readable.
- Corruption of received data by internal generated cross talk noise in digital line interface mode:

If the digital line interface mode LIM1.DRS = 1 is programmed and one of the following line codes is selected FMR0.RC1/0 = 11,10 or 01 it might be happen that data received on pin RDIP/ RDIP or ROID are modified by internal generated cross talk noise. The receiver will lose its synchronization.

Workaround: To avoid the internal cross talk noise an additional capacitor between 680 and max. 5000 picofarads should be connected between pin 3 (REFR) and Ground (VSSR). The capacitor is parallel to the 12 KOHM resistance.

Please refer also to the Addendum / Corrections 10.97 to the Data Sheet 11.96.

Software Compatibility to FALC54 V1.3

The FALC54 V1.4 is software compatible to FALC54 V1.3 with the following exceptions.

- Register VSTR : FALC54 V1.4 = 02_H
- Due to the fact the Errata:
'Receive Data Input Sense (only PCM30 Mode and CMI Code)'
has been corrected, the corresponding configuration bit (RC0.RDIS) now operates as

described in the Data Sheet. To obtain correct functionality the above mentioned bit needs (and must) not be inverted anymore as described by the workaround in the FALC54 V1.3 Errata Sheet.

Boundary Scan Changes

Due to the incrementing of the version number programming of the boundary scan has to be changed.

Identification Register : 32 bit

Version: 2 H

Part Number: 0027 H

manufacturer: 083 H