PM4344

TQUAD

QUADRUPLE T1 FRAMER

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CONTENTS

LIST OF REGISTERS

LIST OF FIGURES

LIST OF TABLES

1 FEATURES

- Integrates four full-featured T1 framers and transmitters in a single device for terminating duplex DS-1 signals.
- Software and functionally compatible with the PM4341A T1XC Single T1 Transceiver.
- Provides digital jitter attenuation programmable for either the transmit or receive directions.
- Provides an 8-bit microprocessor bus interface for configuration, control, and status monitoring.
- Low power CMOS technology
- Available in a 128 pin PQFP package.

Each one of four receiver sections:

- Recovers clock and data using a digital phase locked loop for high jitter tolerance. A direct clock input is provided to allow clock recovery to be by-passed.
- Accepts dual rail or single rail digital PCM inputs.
- Supports B8ZS or AMI line code.
- Accepts gapped data streams to support higher rate demultiplexing.
- Frames to SF, ESF, T1DM (DDS), and SLC®96 format DS1 signals.
- Provides loss of signal detection, and red, yellow, and AIS alarm detection. Red, yellow, and AIS alarms are integrated as per industry specifications.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window.
- Provides programmable in-band loopback code detection.
- Supports line and path performance monitoring according to AT&T and ANSI specifications. Accumulators are provided for counting:

- ESF CRC-6 errors to 333 per second;
- Framing bit errors to 31 per second;
- Line code violations to 4095 per second; and
- Loss of frame or change of frame alignment events to 7 per second.

- Provides ESF bit-oriented code detection, and an HDLC interface for terminating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Extracts the data link in ESF, T1DM (DDS) or SLC®96 modes.
- Supports fractional T1 channel extraction.
- Provides a two-frame elastic store buffer for jitter and wander attenuation that performs controlled slips and indicates slip occurrence and direction.
- Provides robbed bit signaling extraction, with optional data inversion, programmable idle code substitution, digital milliwatt code substitution, bit fixing, and 2 superframes of signaling debounce on a per-channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Optionally provides dual rail digital PCM output signals to allow BPV transparency. Also supports unframed mode.
- Supports transfer of PCM and signaling data to 1.544 Mbit/s, 2.048 Mbit/s, 12.352Mbit/s or 16.384Mbit/s backplane buses.

Each one of four transmitter sections:

- Formats data to SF, ESF, T1DM (DDS), and SLC®96 format DS1 signals.
- Optionally accepts dual rail digital PCM inputs to allow BPV transparency. Also supports unframed mode and framing bit, CRC, or data link by-pass.
- Supports transfer of PCM and signaling data from 1.544 Mbit/s, 2.048 Mbit/s, 12.352Mbit/s or 16.384Mbit/s backplane buses.

- Provides signaling insertion, programmable idle code substitution, digital milliwatt code substitution, and data inversion on a per channel basis.
- Provides trunk conditioning which forces programmable trouble code substitution and signaling conditioning on all channels or on selected channels.
- Provides minimum ones density through Bell (bit 7), GTE or DDS zero code suppression on a per channel basis.
- Detects violations of the ANSI T1.403 12.5% pulse density rule over a moving 192 bit window or optionally stuffs ones to maintain minimum ones density.
- Allows insertion of framed or unframed in-band loopback code sequences.
- Allows insertion of a data link in ESF, T1DM (DDS) or SLC®96 modes.
- Supports fractional T1 channel insertion.
- Supports transmission of the alarm indication signal (AIS) or the yellow alarm signal in all formats.
- Provides ESF bit-oriented code generation and an HDLC interface for generating the ESF data link.
- Supports polled, interrupt-driven, or DMA servicing of the HDLC interface.
- Provides a digital phase locked loop for generation of a low jitter transmit clock.
- Provides a FIFO buffer for jitter attenuation and rate conversion in the transmitter. FIFO full or empty indication allows for bit-stuffing in higher rate multiplexing applications.
- Supports B8ZS or AMI line code.
- Provides dual rail or single rail digital PCM output signals.

2 APPLICATIONS

- T1 Channel Service Units (CSU) and Data Service Units (DSU)
- T1 Channel Banks and Multiplexers
- Digital Private Branch Exchanges (PBX)
- Digital Access and Cross-Connect Systems (DACS) and Electronic DSX Cross-Connect Systems (EDSX)
- T1 Frame Relay Interfaces
- T1 ATM Interfaces
- ISDN Primary Rate Interfaces (PRI)
- SONET Byte Synchronous VT1.5 Mappers
- Test Equipment

3 REFERENCES

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9. Bell Communications Research - Alarm Indication Signal Requirements and Objectives, TR-TSY-000191 Issue 1, May 1986.

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14. Bell Communications Research - Transport Systems Generic Requirements (TSGR): Common Requirement, TR-TSY-000499, Issue 5, December, 1993.

15. AT&T - Digital Channel Bank - Requirements And Objectives, PUB43801, November 1982.

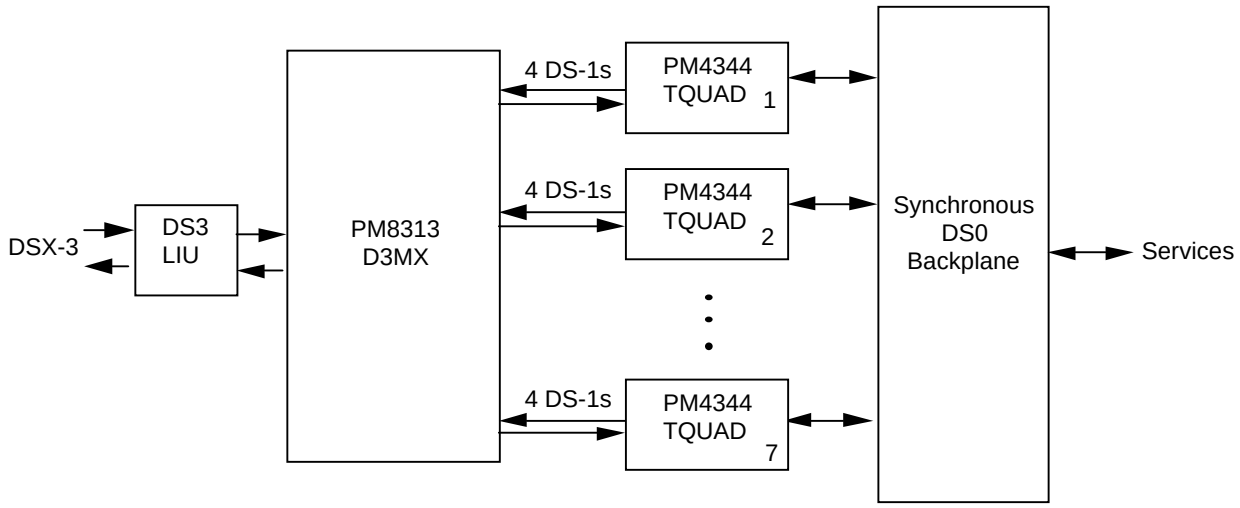
16. AT&T - Digital Channel Bank - Requirements And Objectives - Addendum 1, PUB43801A, January 1985.

17. AT&T - Requirements For Interfacing Digital Terminal Equipment To Services Employing The Extended Superframe Format, TR 54016, September, 1989.

18. AT&T, TR 62411 - Accunet T1.5 - "Service Description and Interface Specification" December, 1990.

4 APPLICATION EXAMPLES

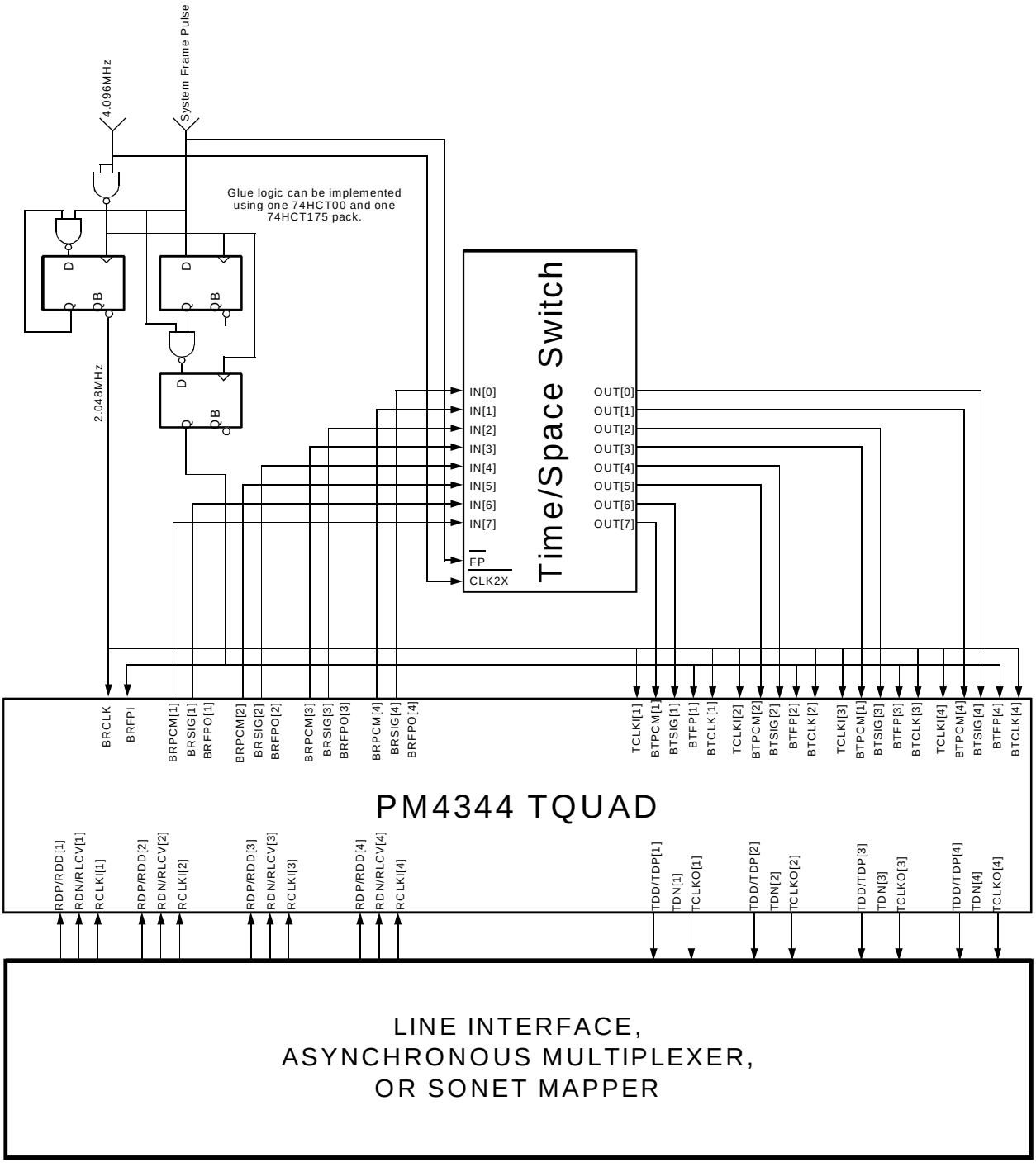
Figure 1 - Example 1. DS-3 Terminal Multiplexer/Channel Bank



Example 1 shows a DS-3 Terminal Multiplexer/Channel Bank using 7 TQUAD devices, PMC-Sierra's PM8313 D3MX M13 Multiplexer, and Silicon System's SSI 78P236 DS-3 Line Interface Unit.

The seven TQUAD chips are each configured to transmit and receive four 1.544MHz DS-1 signals to and from the D3MX. The DS-0 backplane data can be transmitted or recovered using either the 1.544MHz or 2.048MHz backplane data rate or from 12.352MHz or 16.384MHz multiplexed backplane data streams.

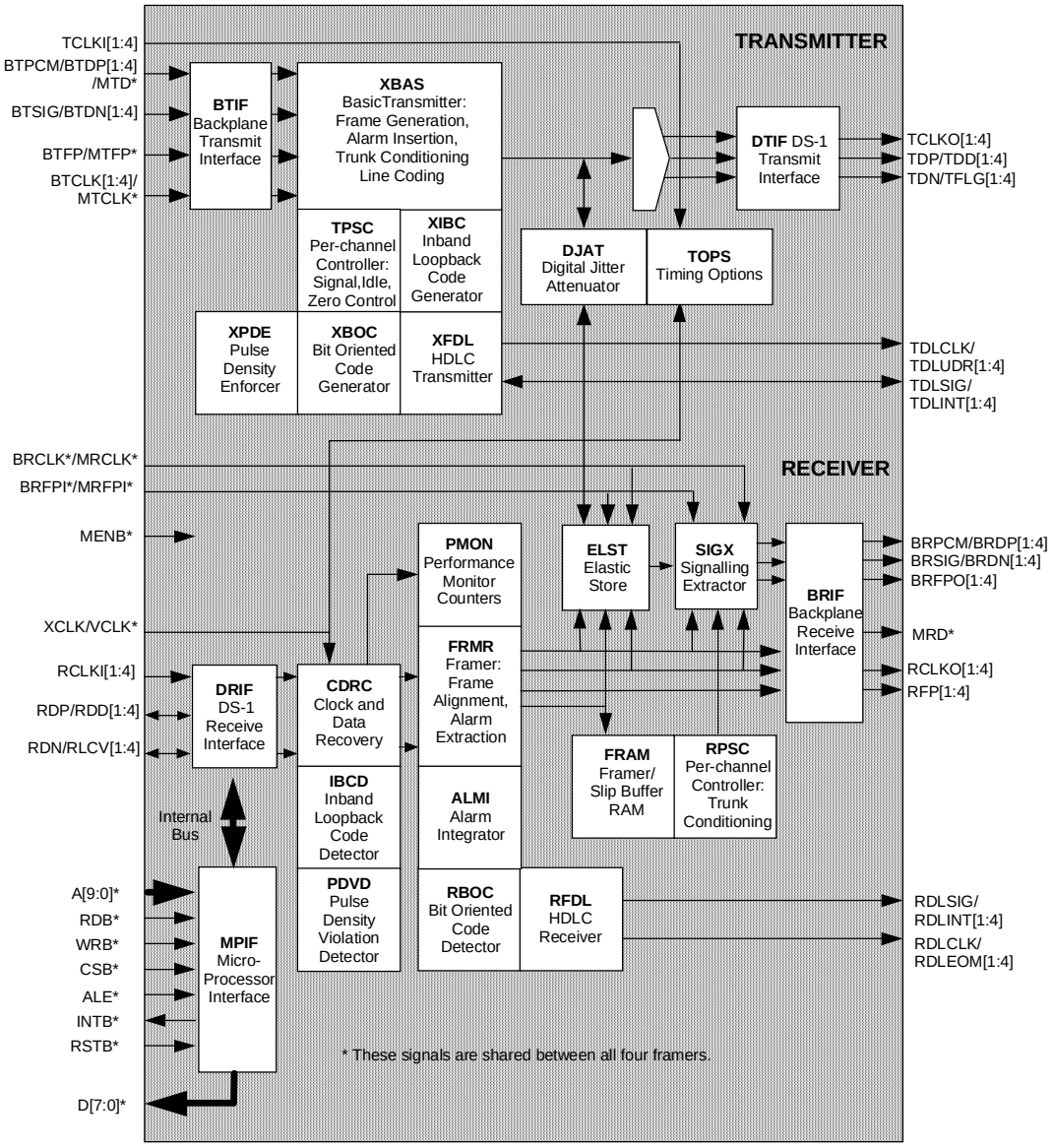
Figure 2 - Example 2. DSX-1/0 Cross-connect



Example 2 shows a DSX 1/0 Cross-Connect using a TQUAD chip and a Digital Time/Space Switch to implement a simple 1/0 cross-connect. An alternate architecture could use two Digital Time/Space Switches, one as a voice switch and the other as a signaling switch, and 2 TQUADs to cross-connect eight T1s. (Note: a true implementation would require redundancy in the switch core.)

In this example, the TQUAD chips are programmed to receive and generate the same framing format, using the 2.048 MHz backplane data rate. The "system frame pulse" signal is stretched through the two D-FF into a pulse of 488ns duration, which is used to frame align the data out of each framer through the elastic store and to provide frame alignment indication to the transmitters. The raw system frame pulse signal is used to indicate frame alignment synchronization to the Digital Time/Space Switch. Another D-FF is configured as a toggle to generate a 2.048MHz clock from the system 4.096MHz clock source, synchronized to the system frame pulse.

5 BLOCK DIAGRAM



6 DESCRIPTION

The PM4344 Quaduple T1 Framer (TQUAD) is a feature-rich device suitable for use in many T1 systems with a minimum of external circuitry. Each of the framers and transmitters is independently software configurable, allowing feature selection without changes to external wiring.

On the receive side, the TQUAD recovers clock and data and can be configured to frame to any of the common DS-1 signal formats: SF, ESF, T1DM (DDS), or SLC®96. The TQUAD also supports detection of various alarm conditions such as loss of signal, pulse density violation, red alarm, yellow alarm, and AIS alarm. The TQUAD detects and indicates the presence of yellow and AIS patterns and also integrates yellow, red, and AIS alarms as per industry specifications.

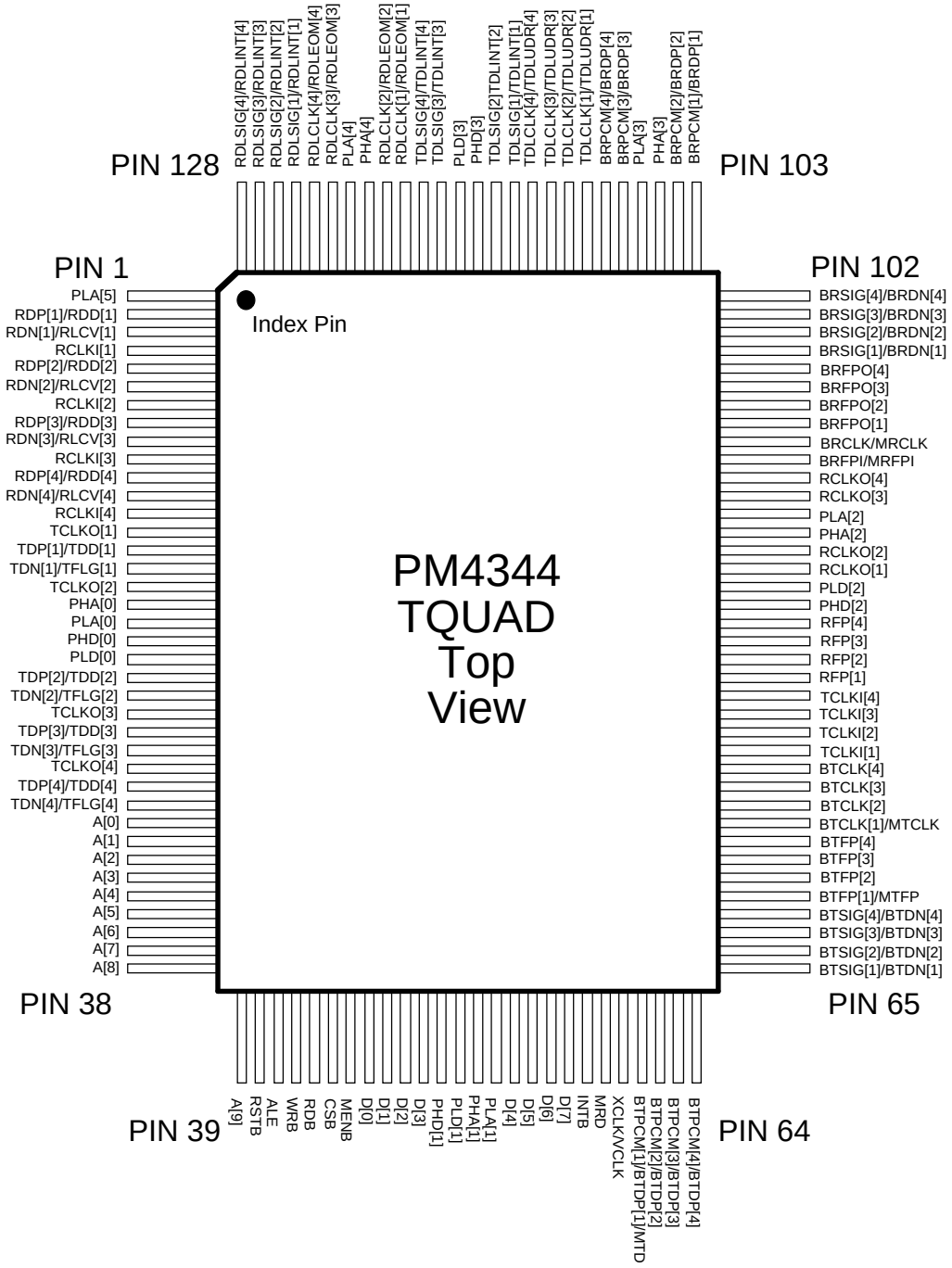
Performance monitoring with accumulation of CRC-6 errors, framing bit errors, line code violations, and loss of frame events is provided. The TQUAD also detects the presence of in-band loopback codes, ESF bit oriented codes, and detects and terminates HDLC messages on the ESF data link. An elastic store for slip buffering and adaptation to backplane timing is provided, as is a signaling extractor that supports signaling debounce, signaling freezing, idle code substitution, digital milliwatt tone substitution, data inversion, and signaling bit fixing on a per-channel basis. Receive side data and signaling trunk conditioning is also provided.

On the transmit side, the TQUAD generates framing for SF, ESF, T1DM (DDS), and SLC®96 DS1 formats, or framing can be optionally disabled. The TQUAD supports signaling insertion, idle code substitution, digital milliwatt tone substitution, data inversion, and zero code suppression on a per-channel basis. The zero code suppression is selectable to Bell (bit 7), GTE, or DDS standards, and can also be disabled. Transmit side data and signaling trunk conditioning is provided. The TQUAD can also generate in-band loopback codes, ESF bit oriented codes, and transmit HDLC messages on the ESF data link. The TQUAD can generate a low jitter transmit clock and provides a FIFO for transmit jitter attenuation. When not used for jitter attenuation, the full or empty status of this FIFO is made available to facilitate higher order multiplexing applications by controlling bit-stuffing logic.

The TQUAD provides a parallel microprocessor interface for controlling the operation of the TQUAD device. Serial PCM interfaces allow 1.544 Mbit/s or 2.048 Mbit/s backplanes to be directly supported. Tolerance of gapped clocks allows other backplane rates to be supported with a minimum of external logic. Optional bit interleaved multiplexing of the individual serial streams supports 12.352 Mbit/s and 16.384 Mbit/s backplanes.

7 PIN DIAGRAM

The TQUAD is packaged in a 128-pin plastic QFP package having a body size of 14mm by 20mm and a pin pitch of 0.5mm.



8 PIN DESCRIPTION

Pin Name	Type	Pin No.	Function
MENB	Input	45	Multiplex Enable (MENB). When this input is asserted low, the four sets of PCM and signaling streams are combined into a single bit interleaved 12.352 Mbits/ or 16.384 Mbit/s serial stream. In the transmit direction, all data is expected on MTD with alignment indicated by MTFP. MTD and MTFP are sampled on the rising edge of MTCLK. In the receive direction, data is presented on MRD aligned with MRFPI. MRFPI is sampled on the rising edge of MRCLK and MRD is updated on the falling edge of MRCLK. When this input is deasserted high, each PCM and signaling stream has its own dedicated pin. MENB has an integral pull-up.
RDP[1] RDP[2] RDP[3] RDP[4] /	Input	2 5 8 11	Receive Positive Line Pulse (RDP[4:1]). These inputs are available when the TQUAD is configured to receive dual-rail formatted data. The RDP[4:1] inputs may be enabled for either RZ or NRZ waveforms. When enabled for NRZ, this input may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1]. When enabled for RZ, the clocks are recovered from the corresponding RDP[4:1] and RDN[4:1] inputs.
RDD[1] RDD[2] RDD[3] RDD[4]			Receive Digital DS-1 Signal (RDD[4:1]). When the TQUAD is configured to receive single-rail data, these inputs may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1].

Pin Name	Type	Pin No.	Function
RDN[1] RDN[2] RDN[3] RDN[4] / RLCV[1] RLCV[2] RLCV[3] RLCV[4]	Input	3 6 9 12	Receive Digital Negative Line Pulse (RDN[4:1]). These inputs are available when the TQUAD is configured to receive dual-rail formatted data. The RDN[4:1] inputs may be enabled for either RZ or NRZ waveforms. When enabled for NRZ, these inputs may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1]. When enabled for RZ, the clocks are recovered from the corresponding RDP[4:1] and RDN[4:1] inputs. Receive Line Code Violation Indication (RLCV[4:1]). When the TQUAD is configured to receive single-rail data, this input may be enabled to be sampled on the rising or falling edge of the corresponding RCLKI[4:1].
RCLKI[1] RCLKI[2] RCLKI[3] RCLKI[4]	Input	4 7 10 13	Receive Line Clock Inputs (RCLKI[4:1]). Each input is an externally recovered 1.544 MHz line clock that may be enabled to sample the RDP[x] and RDN[x] inputs on its rising or falling edge when the input format is enabled for dual-rail NRZ; or to sample the RDD[x] and RLCV[x] inputs on its rising or falling edge when the input format is enabled for single-rail.
RCLKO[1] RCLKO[2] RCLKO[3] RCLKO[4]	Output	87 88 91 92	Recovered PCM Clock Output (RCLKO[4:1]). Each output signal is the recovered 1.544 MHz clock, synchronized to the XCLK signal. Each RCLKO[x] signal is recovered from the RDP[x] and RDN[x] inputs (if the input format is dual-rail RZ) or from the RCLKI[x] input (if the input format is NRZ). When the ELST is by-passed or the RCLKOSEL register bit is set, BRPCM[x] and BRSIG[x] are updated on the falling edge of the associated RCLKO[x]. As an option, the digital attenuator's smooth 1.544 MHz clock may be presented on RCLKO[x]. See the Operations Section for details on this application.

Pin Name	Type	Pin No.	Function
RFP[1] RFP[2] RFP[3] RFP[4]	Output	81 82 83 84	Receive Frame Pulse (RFP[4:1]). The RFP[x] outputs are intended as a timing references. When the TQUAD is configured for receive frame pulse output, each RFP[x] output pulses high for 1 RCLKO[x] cycle once per frame. When configured for receive superframe output, each RFP[x] pulses high for 1 RCLKO[x] cycle once per 12 or 24 frame superframe. Each RFP[x] is updated on the falling edge of the associated RCLKO[x]. RFP[x] should not be used when register bit RCLKOSEL is set to a logic 1.
RDLSIG[1] RDLSIG[2] RDLSIG[3] RDLSIG[4] / RDLINT[1] RDLINT[2] RDLINT[3] RDLINT[4]	Output	125 126 127 128	Receive Data Link Signal (RDLSIG[4:1]). The RDLSIG[4:1] signals are available on these outputs when the associated internal HDLC receiver (RFDL) is disabled from use, or, optionally, when fractional T1 is extracted. When the TQUAD is configured to receive ESF formatted data, each RDLSIG[x] contains the data stream extracted from the facility data link; when the TQUAD is configured to receive SF formatted data, each RDLSIG[x] output is held low; when the TQUAD is configured to receive T1DM, each RDLSIG[x] reflects the value of the R-bit in the T1DM sync word; when the TQUAD is configured for SLC®96, each RDLSIG[x] contains the value of the Fs framing bits. When fractional T1 is enabled for extraction, each RDLSIG[x] contains the contents of a sub-set of the 24 channels. Each RDLSIG[x] is updated on the falling edge of the associated RDLCLK[x]. Receive Data Link Interrupt (RDLINT[4:1]). The RDLINT[4:1] signals are available on these outputs when the associated RFDL is enabled. Each RDLINT[x] goes high when an event occurs which changes the status of the associated HDLC receiver.

Pin Name	Type	Pin No.	Function
RDLCLK[1] RDLCLK[2] RDLCLK[3] RDLCLK[4] /	Output	119 120 123 124	Receive Data Link Clock (RDLCLK[4:1]). The RDLCLK[4:1] signals are available on these outputs when the associated internal HDLC receiver (RFDL) is disabled from use, or, optionally, when fractional T1 is extracted. The rising edge of RDLCLK[x] can be used to sample the data-link data or the fractional T1 data on the associated RDLSIG[x] when the internal HDLC receiver is disabled or when fractional T1 is enabled respectively. When the TQUAD is configured to receive SF formatted data with fractional T1 disabled, the RDLCLK[x] output is held low.
RDLEOM[1] RDLEOM[2] RDLEOM[3] RDLEOM[4]			Receive Data Link End of Message (RDLEOM[4:1]). The RDLEOM[4:1] signals are available on these outputs when the associated RFDL is enabled. Each RDLEOM[x] goes high when the last byte of a received sequence is read from the associated RFDL FIFO buffer, or when the FIFO buffer is overrun.
BRPCM[1] BRPCM[2] BRPCM[3] BRPCM[4] /	Output	103 104 107 108	Backplane Receive PCM (BRPCM[4:1]). The BRPCM[4:1] signals are available on this output when the backplane is configured for single-rail output. Each BRPCM[x] signal contains the recovered data stream passed through ELST, SIGX, and the RPSC. When the ELST is not by-passed or the RCLKOSEL register bit is not set, the BRPCM[x] stream is aligned to the backplane timing and is updated on the falling edge of the associated BRCLK. When the ELST is by-passed or the RCLKOSEL register bit is set, BRPCM[x] is aligned to the receive line timing and is updated on the falling edge of the associated RCLKO[x].
BRDP[1] BRDP[2] BRDP[3] BRDP[4]			Backplane Receive Positive Line Pulse (BRDP[4:1]). The BRDP[4:1] signals are available on these outputs when the backplane is configured for dual-rail output. Each BRDP[x] NRZ output represents the RZ receive digital positive pulse signal extracted from the input bipolar signal. BRDP[x] is updated on the falling edge of the associated RCLKO[x].

Pin Name	Type	Pin No.	Function
MRD	Output	59	Multiplexed Receive Data (MRD). When the multiplex enable (MENB) input is asserted low, the four sets of PCM and signaling streams are bit interleaved into a single 12.352 Mbit/s or 16.384 Mbit/s serial stream presented on MRD aligned with MRFPI. MRFPI is sampled on the rising edge of MRCLK and MRD is updated on the falling edge of MRCLK. When MENB input is deasserted high, each PCM and signaling stream has its own dedicated pin and MRD is unused.
BRSIG[1] BRSIG[2] BRSIG[3] BRSIG[4]	Output	99 100 101 102	Backplane Receive Signaling (BRSIG[4:1]). The BRSIG[4:1] signals are available on these outputs when the backplane is configured for single-rail output. Each BRSIG[x] contains the extracted signaling bits for each channel in the frame, repeated for the entire superframe. Each channel's signaling bits are valid in bit locations 5,6,7,8 of the channel and are channel-aligned with the BRPCM[x] data stream. When the ELST is not by-passed or the RCLKOSEL register bit is not set, the BRSIG[x] stream is aligned to the backplane timing and is updated on the falling edge of BRCLK. When the ELST is by-passed or the RCLKOSEL register bit is set, BRSIG[x] is aligned to the receive line timing and is updated on the falling edge of the associated RCLKO[x].
BRDN[1] BRDN[2] BRDN[3] BRDN[4]			Backplane Receive Negative Line Pulse (BRDN[4:1]). The BRDN[4:1] signals are available on these outputs when the backplane is configured for dual-rail output. Each BRDN[x] NRZ output represents the RZ receive digital negative pulse signal extracted from the input bipolar signal. BRDN[x] is updated on the falling edge of the associated RCLKO[x].

Pin Name	Type	Pin No.	Function
BRFPO[1] BRFPO[2] BRFPO[3] BRFPO[4]	Output	95 96 97 98	Backplane Frame Pulse Output (BRFPO[4:1]). When the TQUAD is configured for backplane receive frame pulse output, each BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed or the RCLKOSEL register bit is set) during bit 1 of each 193-bit frame, indicating the frame alignment of the BRPCM[x] data stream. When configured for backplane receive superframe output, each BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed or the RCLKOSEL register bit is set) during bit 1 of frame 1 of the 12 or 24 frame superframe, indicating the superframe alignment of the BRPCM[x] data stream. When configured for backplane alternate receive superframe output, each BRFPO[x] pulses high for 1 BRCLK cycle (or 1 RCLKO[x] cycle if ELST is by-passed or the RCLKOSEL register bit is set) during bit 1 of frame 1 of every second 12 or 24 frame superframe, indicating the superframe alignment of the BRPCM[x] data stream. This alternate superframe indication is useful for performing format conversion from SF to ESF while maintaining the same superframe alignment. BRFPO[x] is updated on the falling edge of the associated BRCLK or RCLKO[x].
BRCLK	Input	94	Backplane Receive Clock (BRCLK). When the multiplex enable (MENB) input is deasserted high, this clock should be either 1.544MHz or 2.048MHz with optional gapping for adaptation to non-uniform backplane data streams. BRCLK is common to all four framers. The TQUAD may be configured to ignore the BRCLK input and use the RCLKO[x] signal in its place when the ELST is bypassed or the RCLKOSEL register bit is set.
MRCLK			Multiplex Receive Clock (MRCLK). When the multiplex enable (MENB) input is asserted low, this clock should be 12.352 MHz or 16.384 MHz. MRFPI is sampled on the rising edge of MRCLK and MRD is updated on the rising edge of MRCLK. The multiplexed bus can not be used if the ELST is bypassed or the RCLKOSEL register bit is set.

Pin Name	Type	Pin No.	Function
BRFPI	Input	93	Backplane Frame Pulse Input (BRFPI). When the multiplex enable (MENB) input is deasserted high, this input is used to frame align the received data to the system backplane. BRFPI is common to all four framers. If frame alignment only is required, a pulse at least 1 BRCLK cycle wide must be provided on each BRFPI every 193 bit times (or 256 bit times if the 2.048 Mbit/s rate is selected). If receive signaling alignment is required, receive signaling alignment must be enabled, and a pulse at least 1 BRCLK cycle wide must be provided on BRFPI every 12 or 24 frame times. BRFPI is sampled on the rising edge of BRCLK.
MRFPI			Multiplexed Frame Pulse Input (MRFPI). When the multiplex enable (MENB) input is asserted low, this input aligns all four sets of PCM and signaling streams to allow bit interleaved multiplexing. If frame alignment only is required, a pulse at least 1 MRCLK cycle wide must be provided on each MRFPI every 1544 bit times (or 2048 bit times if the 16.384 Mbit/s rate is selected). If receive signaling alignment is required, receive signaling alignment must be enabled, and a pulse at least 1 MRCLK cycle wide must be provided on MRFPI every 12 or 24 frame times. MRFPI is sampled on the rising edge of MRCLK.

Pin Name	Type	Pin No.	Function
BTPCM[1] BTPCM[2] BTPCM[3] BTPCM[4] /	Input	61 62 63 64	Backplane Transmit PCM (BTPCM[4:1]). The non-return to zero, digital data streams to be transmitted are input on these pins when the backplane is configured for non-multiplexed single-rail input. The BTPCM[x] signal is sampled on the rising edge of the associated BTCLK[x].
BTDP[1] BTDP[2] BTDP[3] BTDP[4]			Backplane Transmit Positive Line Pulse (BTDP[4:1]). The positive pulse of the dual-rail signals to be transmitted is input on these pins when the backplane is configured for non-multiplexed dual-rail input. In dual-rail input mode, the BTDP[x] input by-passes the transmitter and is fed directly into the DJAT. BTDP[x] is sampled on the rising edge of the associated BTCLK[x].
MTD			Multiplexed Transmit Data (MTD). MTD shares a pin with BTPCM[1]. BTPCM[4:2] are unused when the multiplex enable (MENB) input is asserted low. When the multiplex enable (MENB) input is asserted low, the four sets of PCM and signaling streams are expected in a single bit interleaved 12.352 Mbits/ or 16.384 Mbit/s serial stream. Frame alignment is indicated by MTFP. MTD is sampled on the rising edge of MTCLK.

Pin Name	Type	Pin No.	Function
BTSIG[1] BTSIG[2] BTSIG[3] BTSIG[4] /	Input	65 66 67 68	Backplane Transmit Signaling (BTSIG[4:1]). The BTSIG[4:1] input signals contain the signaling bits for each channel in the transmit data frame, repeated for the entire superframe. Each signal is input on the BTSIG[x] pin when the backplane is configured for non-multiplexed single-rail input. Each channel's signaling bits are in bit locations 5,6,7,8 of the channel and are channel-aligned with the BTPCM[x] data stream. BTSIG[x] is sampled on the rising edge of the associated BTCLK[x].
BTDN[1] BTDN[2] BTDN[3] BTDN[4]			Backplane Transmit Negative Line Pulse (BTDN[4:1]). The negative pulse of the dual-rail signal to be transmitted is input on these pins when the backplane is configured for non-multiplexed dual-rail input. In dual-rail input mode, the BTDN[x] input by-passes the transmitter and is fed directly into the DJAT. BTDN[x] is sampled on the rising edge of the associated BTCLK[x]. These inputs are unused when the multiplex enable (MENB) input is asserted low
BTFP[1] BTFP[2] BTFP[3] BTFP[4]	Input	69 70 71 72	Backplane Transmit Frame Pulse (BTFP[4:1]). These inputs are used to frame align the transmitters to the system backplane. If frame alignment only is required, a pulse at least 1 BTCLK[x] cycle wide must be provided on BTFP[x] every 193 bit times. If superframe alignment is required, transmit superframe alignment must be enabled, and a pulse at least 1 BTCLK[x] cycle wide must be provided on BTFP[x] every 12 or 24 frame times. If frame alignment is not required, BTFP[x] may be tied to logic high or low.
MTFP			Multiplexed Transmit Frame Pulse (MTFP). MTFP shares a pin with BTFP[1]. BTFP[4:2] are unused when the multiplex enable (MENB) input is asserted low. When the multiplex enable (MENB) input is asserted low, MTFP indicates the frame alignment of the bit interleaved PCM and signaling streams. MTFP is sampled on the rising edge of MTCLK.

Pin Name	Type	Pin No.	Function
BTCLK[1] BTCLK[2] BTCLK[3] BTCLK[4]	Input	73 74 75 76	Backplane Transmit Clock (BTCLK[4:1]). These clocks should be either 1.544MHz or 2.048MHz with optional gapping for adaptation from non-uniform backplane data streams. The TQUAD may be configured to ignore the BTCLK[x] input and use the associated RCLKO[x] signal in its place.
MTCLK			Multiplexed Transmit Clock (MTCLK). MTCLK shares a pin with BTCLK[1]. BTCLK[4:2] are unused when the multiplex enable (MENB) input is asserted low. When the multiplex enable (MENB) input is asserted low, this clock should be 12.352 MHz or 16.384 MHz. MTFP and MTD are sampled on the rising edge of MTCLK.
TDLSIG[1] TDLSIG[2] TDLSIG[3] TDLSIG[4]/	I/O	113 114 117 118	Transmit Data Link Signal (TDLSIG[4:1]). The TDLSIG[4:1] signals are input on this pin when the associated internal HDLC transmitter (XFDL) is disabled from use, or if fractional T1 insertion is selected. When the TQUAD is configured to transmit ESF formatted data, each TDLSIG[x] is the source for the data stream to be inserted into the ESF data link. When the TQUAD is configured to transmit SLC®96 formatted data, each TDLSIG[x] input is the source for the Fs framing bits; when the TQUAD is configured to transmit T1DM with R-bit replacement, each TDLSIG[x] is the source of the R-bit in the T1DM sync word. If fractional T1 insertion is enabled, TDLSIG[x] is the data source for the T1 channels enabled by the Channel Select registers. TDLSIG[x] is sampled on the rising edge of the associated TDLCLK[x]. The TDLSIG[x] pins have integral pull-ups.
TDLINT[1] TDLINT[2] TDLINT[3] TDLINT[4]			Transmit Data Link Interrupt (TDLINT[4:1]). The TDLINT[4:1] signals are output on these pins when the associated XFDL is enabled. Each TDLINT[x] goes high when the last data byte written to the XFDL has been set up for transmission and processor intervention is required to either write control information to end the message, or to provide more data.

Pin Name	Type	Pin No.	Function
TDLCLK[1] TDLCLK[2] TDLCLK[3] TDLCLK[4]/	Output	109 110 111 112	Transmit Data Link Clock (TDLCLK[4:1]). The TDLCLK[4:1] signals are available on this output when the associated internal HDLC transmitter (XFDL) is disabled from use, or if fractional T1 insertion is selected. The rising edge of TDLCLK[x] is used to sample the data-link or fractional T1 data stream contained on the associated TDLSIG[x] input. When the TQUAD is configured to transmit SF formatted data with fractional T1 disabled, the TDLCLK[x] output is held low.
TDLUDR[1] TDLUDR[2] TDLUDR[3] TDLUDR[4]			Transmit Data Link Underrun (TDLUDR[4:1]). The TDLUDR[4:1] signals are available on this output when the associated XFDL is enabled. TDLUDR[x] goes high when the processor has failed to service the TDLINT[x] interrupt before the transmit buffer is emptied.
TCLKO[1] TCLKO[2] TCLKO[3] TCLKO[4]	Output	14 17 24 27	Transmit Clock Output (TCLKO[4:1]). The TDP[4:1], TDN[4:1], and TDD[4:1] outputs may be enabled to be updated on the rising or falling edge of the TCLKO[4:1] outputs. TCLKO[x] is a 1.544 MHz clock that is adequately jitter and wander free in absolute terms to permit an acceptable DS-1 signal to be generated. Depending on the configuration of the TQUAD, TCLKO[x] may be derived from TCLKI[x], RCLKO[x], or BTCLK[x], with or without jitter attenuation.
TDP[1] TDP[2] TDP[3] TDP[4] /	Output	15 22 25 28	Transmit Digital Positive Line Pulse (TDP[4:1]). These signals are available on the output when the TQUAD is configured to transmit dual-rail data. The TDP[x] signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of the associated TCLKO[x].
TDD[1] TDD[2] TDD[3] TDD[4]			Transmit DS-1 Signal (TDD[4:1]). These signals are available on the output when configured to transmit single-rail data. The TDD[x] signal may be enabled to be updated on the rising or falling edge of the associated TCLKO[x].

Pin Name	Type	Pin No.	Function
TDN[1] TDN[2] TDN[3] TDN[4] / TFLG[1] TFLG[2] TFLG[3] TFLG[4]	Output	16 23 26 29	Transmit Digital Negative Line Pulse (TDN[4:1]). These signals are available on the output when the TQUAD is configured to transmit dual-rail data. The TDN[x] signal can be formatted for either RZ or NRZ waveforms, and can be enabled to be updated on the rising or falling edge of the associated TCLKO[x]. Transmit FIFO Flag (TFLG[4:1]). These signals are available when configured to transmit single-rail data. The TFLG[x] output indicates when the transmit rate conversion FIFO in DJAT is nearing an empty or a full condition. Either indication may be selected. This output may be enabled to be updated on the rising or falling edge of the associated TCLKO[x].
TCLKI[1] TCLKI[2] TCLKI[3] TCLKI[4]	Input	77 78 79 80	Transmit Clock Input (TCLKI[x]). This input signal is used to generate the TCLKO[x] clock signal. Depending upon the configuration of the TQUAD, TCLKO[x] may be derived directly from TCLKI[x] by dividing TCLKI[x] by 8, or TCLKO[x] may be derived from TCLKI[x] after jitter attenuation. If TCLKI[x] is jitter-free when divided down to 8 kHz, then it is possible to derive TCLKO[x] from TCLKI[x] when TCLKI[x] is a multiple of 8 kHz (i.e. Nx8 kHz, for N equals 1 to 256). The TQUAD may be configured to ignore the TCLKI[x] input and utilize BTCLK[x] or RCLKO[x] instead. RCLKO[x] is also substituted for TCLKI[x] if line loopback is enabled.
XCLK/ VCLK	Input	60	Crystal Clock Input (XCLK). This signal provides timing for many portions of the TQUAD. Depending on the configuration of the TQUAD, XCLK is nominally a 37.056 MHz ± 32ppm or 12.352 MHz ± 50ppm, 50% duty cycle clock. When transmit clock generation or jitter attenuation is not required, XCLK may be driven with a 12.352 MHz clock. When transmit clock generation or jitter attenuation is required, XCLK must be driven with a 37.056 MHz clock. Vector Clock (VCLK). The VCLK signal is used during TQUAD production test to verify internal functionality.

Pin Name	Type	Pin No.	Function
INTB	Output	58	Active low open-drain Interrupt signal (INTB). This signal goes low when an unmasked interrupt event is detected on any of the internal interrupt sources, including the internal HDLC transceiver. Note that INTB will remain low until all active, unmasked interrupt sources are acknowledged at their source.
CSB	Input	44	Active low chip select (CSB). This signal must be low to enable TQUAD register accesses. CSB must go high at least once after a powerup to clear internal test modes. If CSB is not used, then it should be tied to an inverted version of RSTB, in which case, RDB and WRB determine register accesses.
D[0] D[1] D[2] D[3] D[4] D[5] D[6] D[7]	I/O	46 47 48 49 54 55 56 57	Bidirectional data bus (D[7:0]). This bus is used during TQUAD read and write accesses.
RDB	Input	43	Active low read enable (RDB). This signal is pulsed low to enable a TQUAD register read access. The TQUAD drives the D[7:0] bus with the contents of the addressed register while RDB and CSB are both low.
WRB	Input	42	Active low write strobe (WRB). This signal is pulsed low to enable a TQUAD register write access. The D[7:0] bus contents are clocked into the addressed normal mode register on the rising edge of WRB while CSB is low.
ALE	Input	41	Address latch enable (ALE). This signal latches the address bus contents, A[9:0], when low, allowing the TQUAD to be interfaced to a multiplexed address/data bus. When ALE is high, the address latches are transparent. ALE has an integral pull-up.
RSTB	Input	40	Active low reset (RSTB). This signal is set low to asynchronously reset the TQUAD. RSTB is a Schmitt-trigger input with integral pull-up.

Pin Name	Type	Pin No.	Function
A[0]	Input	30	Address bus (A[9:0]). This bus selects specific registers during TQUAD register accesses.
A[1]		31	
A[2]		32	
A[3]		33	
A[4]		34	
A[5]		35	
A[6]		36	
A[7]		37	
A[8]		38	
A[9]		39	
PHA[0]	Power	18	AC power pins (PHA[4:0]). These pins must be connected to a common, well decoupled +5V DC supply together with the DC power pins PHD[3:0] .
PHA[1]		52	
PHA[2]		89	
PHA[3]		105	
PHA[4]		121	
PHD[0]	Power	20	DC power pins (PHD[3:0]). These pins must be connected to a common, well decoupled +5V DC supply together with the AC power pins PHA[4:0].
PHD[1]		50	
PHD[2]		85	
PHD[3]		115	
PLA[0]	Ground	19	AC ground pins (PLA[5:0]). These pins must be connected to a common ground together with the DC ground pins PLD[3:0].
PLA[1]		53	
PLA[2]		90	
PLA[3]		106	
PLA[4]		122	
PLA[5]		1	
PLD[0]	Ground	21	DC ground pins (PLD[3:0]). These pins must be connected to a common ground together with the AC ground pins PLA[5:0].
PLD[1]		51	
PLD[2]		86	
PLD[3]		116	

Notes on Pin Description:

1. The PLA[5:0] and PLD[3:0] ground pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. The PHA[4:0] and PHD[3:0] power pins are not internally connected together. Failure to connect these pins externally may cause malfunction or damage the device. These power supply connections must all be utilized and must all connect to a common +5 V or ground rail, as appropriate.

2. Inputs MENB, RSTB and ALE have integral pull-up resistors.

3. All outputs have 2 mA drive capability except for MRD and the D[7:0] bidirectionals which have 4 mA drive capability

4. All inputs and bidirectionals present minimum capacitive loading and operate at TTL logic levels.

5. The TDLSIG/TDLINT[4:1] pins have integral pull-up resistors and default to being inputs after a reset.

6. When an internal RFDL is enabled, the RDLINT[x] output goes high:

    - when the number of bytes specified in the RFDL Interrupt Status/Control Register have been received on the data link,
    - immediately on detection of RFDL FIFO buffer overrun,
    - immediately on detection of end of message,
    - immediately on detection of an abort condition, or,
    - immediately on detection of the transition from receiving all ones to flags.

    The interrupt is cleared at the start of the next RFDL Data Register read that results in an empty FIFO buffer. This is independent of the FIFO buffer fill level for which the interrupt is programmed. If there is still data remaining in the buffer, RDLINT[x] will remain high. An interrupt due to a RFDL FIFO buffer overrun condition is not cleared on a RFDL Data Register read but on a RFDL Status Register read. The RDLINT[x] output can always be forced low by disabling the RFDL (setting the EN bit in the RFDL Configuration Register to logic 0, or by disabling the internal HDLC receiver in the TQUAD Receive

Data Link Configuration Register), or by forcing the RFDL to terminate reception (setting the TR bit in the RFDL Configuration Register to logic 1).

The RDLINT[x] output may be forced low by disabling the interrupts with the RFDL Interrupt Status/Control Register. However, the internal interrupt latch is not cleared, and the state of this latch can still be read through the RFDL Interrupt Status/Control Register.

7. The RDLEOM[x] output goes high:

    - immediately on detection of RFDL FIFO buffer overrun,
    - when the data byte written into the RFDL FIFO buffer due to an end of message condition is read,
    - when the data byte written into the RFDL FIFO buffer due to an abort condition is read, or,
    - when the data byte written into the RFDL FIFO buffer due to the transition from receiving all ones to flags is read.

    RDLEOM[x] is set low by reading the associated RFDL Status Register or by disabling the RFDL.

8. The TDLUDR[x] output goes high when the processor is unable to service the TDLINT[x] request for more data before a specific time-out period. This period is dependent upon the frequency of TDLCLK[x]:

9. for a TDLCLK[x] frequency of 4 kHz (ESF FDL at the full 4 kHz rate), the time-out is 1.0 ms;

    - for a TDLCLK[x] frequency of 2 kHz (half the ESF FDL), the time-out is 2.0ms;
    - for a TDLCLK[x] frequency of 8 kHz (T1DM R-bit insertion), the time-out is 500µs.

9 FUNCTIONAL DESCRIPTION

9.1 Digital DS-1 Receive Interface (DRIF)

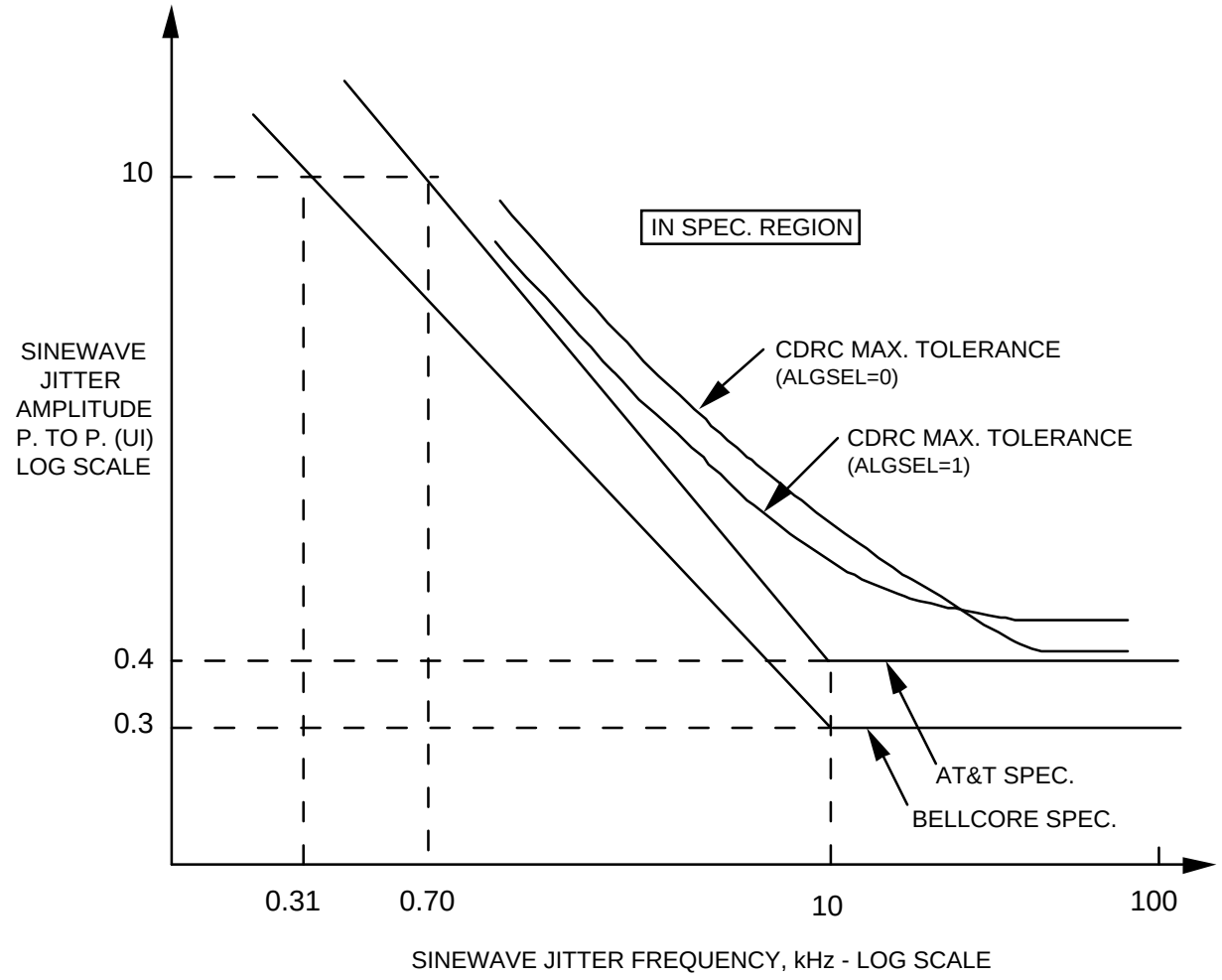
The Digital DS-1 Receive Interface provides control over the various input options available on the multifunctional digital receive pins RDP/RDD[x] and RDN/RLCV[x]. When configured for dual-rail input, the multifunctional pins become the RDP[x] and RDN[x] inputs. These inputs can be enabled to receive either return-to-zero (RZ) or non-return-to-zero (NRZ) signals; the NRZ input signals can be sampled on either the rising or falling edge of RCLKI[x]. When the interface is configured for single-rail input, the multifunctional pins become the RDD[x] and RLCV[x] inputs, which can be sampled on either the rising or falling RCLKI[x] edge.

9.2 Clock and Data Recovery (CDRC)

The Clock and Data Recovery function is provided by a Data and Clock Recovery (CDRC) block. The CDRC provides clock and PCM data recovery, B8ZS decoding, line code violation detection, and loss of signal detection. It recovers the clock from the incoming RZ data pulses using a digital phase-locked-loop and recovers the NRZ data. Loss of signal is indicated after 176 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs and is cleared after the occurrence of a single line pulse. An alternate loss of signal indication is provided which is cleared upon meeting an 1-in-8 pulse density criteria. If enabled, a microprocessor interrupt is generated when a loss of signal is detected and when the signal returns. A line code violation is defined as a bipolar violation (BPV) for AMI-coded signals and is defined as a BPV that is not part of a zero substitution code for B8ZS-coded signals.

The input jitter tolerance of CDRC complies with the Bellcore Document TA-TSY-000170 and with the AT&T specification TR62411. The tolerance is measured with a QRSS sequence (2^{20}-1 with 14 zero restriction). The CDRC block provides two algorithms for clock recovery that result in differing jitter tolerance characteristics. The first algorithm (when the ALGSEL register bit is logic 0) provides good low frequency jitter tolerance, but the high frequency tolerance is close to the TR62411 limit. The second algorithm (when ALGSEL is logic 1) provides much better high frequency jitter tolerance (approaching 0.5UIpp) at the expense of the low frequency tolerance; the low frequency tolerance of the second algorithm is approximately 80% of that of the first algorithm.

Figure 3 - CDRC Jitter Tolerance



9.3 Framer (FRMR)

The framing function is provided by the FRMR block. This block searches for the framing bit position in the incoming recovered PCM stream. It works in conjunction with the FRAM block and the Clock and Data Recovery (CDRC) block to search for the framing bit pattern in SF, ESF, T1DM, or SLC®96 framing formats. When searching for frame, the FRMR examines each of the 193 (SF, T1DM, SLC®96), or each of 4*193 (ESF) framing bit candidates. The FRAM block is addressed and controlled by the FRMR while frame synchronization is acquired.

The time required to find frame alignment to an error-free PCM stream containing randomly distributed channel data (i.e. each bit in the channel data has a 50% probability of being 1 or 0) is dependent upon the framing format. For standard superframe format (SF; also known as D4 format), the FRMR block will determine frame alignment within 4.4ms 99 times out of 100. For SLC®96 format, the FRMR will determine frame alignment within 9.9ms 99 times out of 100. For extended superframe format (ESF), the FRMR will determine frame alignment within 15ms 99 times out of 100. For T1DM format, the FRMR will determine frame alignment within 1.125ms 99 times out of 100.

Once the FRMR has found frame, the incoming PCM data is continuously monitored for framing bit errors, bit error events (a framing bit error in SF or SLC®96, a framing bit error or sync bit error in T1DM, or a CRC-6 error in ESF), and severe errored framing events. The FRMR also detects loss of frame, based on a selectable ratio of framing bit errors.

The FRMR extracts the yellow alarm signal bits from the incoming PCM data stream in SF and SLC®96 framing formats, and extracts the Y-bit from the T1DM sync word in T1DM framing format. The FRMR also extracts the SLC®96 data link in SLC®96 framing format, extracts the facility data link bits in ESF framing format, and extracts the R-bit from the T1DM sync word in T1DM framing format.

The FRMR can also be disabled to allow reception of unframed data. While the FRMR is disabled, control of the FRAM block is relinquished for use as the elastic store.

9.4 Framer/Slip Buffer RAM (FRAM)

The Framer/Slip Buffer RAM function is provided by the Framer RAM (FRAM) block. The FRAM is used to store up to 4 frames of PCM data while the FRMR is finding frame and up to 2 frames of PCM data during normal operation (i.e. when accessed by Elastic Store). The FRAM is shared between the Elastic Store (ELST) and the FRMR: when frame synchronization is lost, the FRMR takes control of the FRAM and uses it to find frame; when frame synchronization is determined, the FRMR relinquishes control of FRAM to ELST which buffers the incoming PCM data.

9.5 Inband Loopback Code Detector (IBCD)

The Inband Loopback Code Detection function is provided by the IBCD block. This block detects the presence of either of two programmable INBAND LOOPBACK ACTIVATE and DEACTIVATE code sequences in either framed or unframed data streams. The inband code sequences are expected to be

overwritten by the framing bit in framed data streams. Each INBAND LOOPBACK code sequence is defined as the repetition of the programmed code in the PCM stream for at least 5.1 seconds. The code sequence detection and timing is compatible with the specifications defined in T1.403-1989, TA-TSY-000312, and TR-TSY-000303. LOOPBACK ACTIVATE and DEACTIVATE code indication is provided through internal register bits. An interrupt is generated to indicate when either code status has changed.

9.6 Pulse Density Violation Detector (PDVD)

The Pulse Density Violation Detection function is provided by the PDVD block. The block detects pulse density violations of the requirement that there be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23). The PDVD also detects periods of 16 consecutive zeros in the incoming data. Pulse density violation detection is provided through an internal register bit. An interrupt is generated to signal a 16 consecutive zero event, and/or a change of state on the pulse density violation indication.

9.7 Performance Monitor Counters (PMON)

The Performance Monitor Counters function is provided by the PMON block. The block accumulates line code violations, CRC error events, Frame Synchronization bit error events, Line Code Violation events, and Loss Of Frame events, or optionally, Change of Frame Alignment (COFA) events with saturating counters over consecutive intervals as defined by the period of the supplied transfer clock signal (typically 1 second). When the transfer clock signal is applied, the PMON transfers the counter values into holding registers and resets the counters to begin accumulating events for the interval. The counters are reset in such a manner that error events occurring during the reset are not missed. If the holding registers are not read between successive transfer clocks, an OVERRUN register bit is asserted.

A line code violation is either a bipolar violation (only those not part of a zero substitution code for B8ZS-coded signals) or excessive zeros. Excessive zeros is a sequence of zeros greater than 15 bits log for an AMI-code signal and greater than 7 bits long for a B8ZS-coded signals. The inclusion of excessive zeros in the line code violation count can be disabled.

Generation of the transfer clock within the TQUAD chip is performed by writing to any counter register location. The holding register addresses are contiguous to facilitate polling operations.

9.8 Bit Oriented Code Detector (RBOC)

The Bit Oriented Code detection function is provided by the RBOC block. This block detects the presence of 63 of the possible 64 bit oriented codes transmitted in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1989 and in TR-TSY-000194. The 64th code (111111) is similar to the DL FLAG sequence and is used by the RBOC to indicate no valid code received.

Bit oriented codes are received on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated at least 10 times. The RBOC can be enabled to declare a received code valid if it has been observed for 8 out of 10 times or for 4 out of 5 times, as specified by the AVC bit in the control register.

Valid BOC are indicated through an internal status register. The BOC bits are set to all ones (111111) if no valid code has been detected. An interrupt is generated to signal when a detected code has been validated, or optionally, when a valid code goes away (i.e. the BOC bits go to all ones).

9.9 HDLC Receiver (RFDL)

The HDLC Receiver function is provided by the RFDL block. The RFDL is a microprocessor peripheral used to receive HDLC frames on the ESF facility data link (FDL).

The RFDL detects the change from flag characters to the first byte of data, removes stuffed zeros on the incoming data stream, receives frame data, and calculates the CRC-CCITT frame check sequence (FCS).

Received data is placed into a 4-level FIFO buffer. The Status Register contains bits which indicate overrun, end of message, flag detected, and buffered data available.

On end of message, the Status Register also indicates the FCS status and the number of valid bits in the final data byte. Interrupts are generated when one, two or three bytes (programmable via the RFDL configuration register) are stored in the FIFO buffer. Interrupts are also generated when the terminating flag sequence, abort sequence, or FIFO buffer overrun are detected.

When the internal HDLC receiver is disabled, the serial data extracted by the FRMR block is output on the RDLSIG[x] pin updated on the falling clock edge output on the RDLCLK[x] pin. Optionally, when the internal HDLC receiver is

used, a subset of channels (by default the D-channel of the Primary Rate interface) can be output on the RDLSIG[x] pin updated on the falling clock edge of RDLCLK[x].

9.10 Alarm Integrator (ALMI)

The Alarm Integration function is provided by the ALMI block. This block detects the presence of YELLOW, RED, and AIS Carrier Fail Alarms (CFA) in SF, T1DM, SLC®96, or ESF formats. The alarm detection and integration is compatible with the specifications defined in Bell Pub 43801, TA-TSY-000278, TR-TSY-000008, ANSI T1.403-1989, and TR-TSY-000191. Alarm detection and validation for SLC®96 is handled the same as SF framing format.

The ALMI block declares the presence of YELLOW alarm when the YELLOW pattern has been received for 425 ms (± 50 ms); the YELLOW alarm is removed when the YELLOW pattern has been absent for 425 ms (± 50 ms). The presence of RED alarm is declared when an out-of-frame condition has been present for 2.55 sec (± 40 ms); the RED alarm is removed when the out-of-frame condition has been absent for 16.6 sec (± 500 ms). In T1DM framing format the RED alarm declaration criteria can be selected to be either 400 ms (± 100 ms) or 2.55 sec (±40 ms); removal of the RED alarm in T1DM can be selected to be either 100 ms (±50 ms) or 16.6 sec (± 500 ms). The presence of AIS alarm is declared when an out-of-frame condition and all-ones in the PCM data stream have been present for 1.5 sec (±100 ms); the AIS alarm is removed when the AIS condition has been absent for 16.8 sec (±500 ms).

CFA alarm detection algorithms operate in the presence of a random 10^{-3} bit error rate.

The ALMI also indicates the presence or absence of the YELLOW, RED, and AIS alarm signal conditions over 40 ms, 40ms, and 60 ms intervals, respectively, allowing an external microprocessor to integrate the alarm conditions via software with any user-specific algorithms. Alarm indication is provided through internal register bits.

9.11 Elastic Store (ELST)

The Elastic Store (ELST) synchronizes incoming PCM frames to the local backplane clock, BRCLK. The frame data is buffered in a two frame circular data buffer. Input data is written to the buffer using a write pointer and output data is read from the buffer using a read pointer.

When the backplane timing is derived from the receive line data (i.e. the RCLKO[x] output is used), the elastic store can be bypassed to eliminate the 2 frame delay. In this configuration the elastic store can be used to measure frequency differences between the recovered line clock and another 1.544 MHz clock applied to the BRCLK input. A typical example might be to measure the difference in frequency between two received T1 streams (i.e. East-West frequency difference) by monitoring the number of SLIP occurrences of one direction with respect to the other. Alternately, the combination of the ELST and the digital phase locked loop may be used to attenuate jitter in the receive direction by locking the elastic store output clock to the recovered clock.

When the elastic store is being used, if the average frequency of the incoming data is greater than the average frequency of the backplane clock, the write pointer will catch up to the read pointer and the buffer will be filled. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The following frame of PCM data will be deleted.

If the average frequency of the incoming data is less than the average frequency of the backplane clock, the read pointer will catch up to the write pointer and the buffer will be empty. Under this condition a controlled slip will occur when the read pointer crosses the next frame boundary. The last frame which was read will be repeated.

A slip operation is always performed on a frame boundary.

To allow for the extraction of signaling information in the PCM data channels, superframe identification is also passed through the ELST.

For payload conditioning, the ELST inserts a programmable idle code into all channels when the FRMR is out of frame synchronization. This code is set to all 1's when the ELST is reset.

9.12 Signaling Extractor (SIGX)

The Signaling Extraction (SIGX) block provides signaling bit extraction from a PCM stream for ESF, SF, and SLC®96 framing formats, and serializes the bits into a 1.544 Mbit/s serial stream channel-aligned to the outgoing PCM data stream. The signaling data stream contains the A,B,C,D bits in the lower 4 channel bit locations (bits 5,6,7,8) in ESF framing format; in SF and SLC®96 formats the A and B bits are repeated in locations C and D (i.e. the signaling stream contains the bits ABAB for each channel). This signaling data stream is compatible with the Basic Transmitter XBAS block. The SIGX also provides user control over signaling freezing and provides control over channel data inversion, signaling bit fixing and signaling debounce on a per-channel basis. The block

contains three superframes worth of signal buffering to ensure that there is a greater than 95% probability that the signaling bits are frozen in the correct state for a 50% ones density out-of-frame condition, as specified in TR-TSY-000170 and BELL PUB 43801. With signaling debounce enabled, the per-channel signaling state must be in the same state for 2 superframes before appearing on the serial output stream.

The SIGX provides one superframe of signal freezing on the occurrence of slips. When a slip event occurs, the SIGX freezes the output signaling for the entire superframe in which the slip occurred; the signaling is unfrozen when the next slip-free superframe occurs.

9.13 Receive Per-channel Serial Controller (RPSC)

The Receive Per-channel Serial Controller (RPSC) function is provided by a second PCSC block.

The RPSC allows data and signaling trunk conditioning to be applied on the receive DS-1 stream on a per-channel basis. It also allows per-channel control of data inversion, idle code substitution, and digital milliwatt code substitution. The definition of the serial streams for the RPSC is analogous to those for TPSC.

9.14 Signaling Aligner (SIGA)

The Signaling Aligner can be positioned either after the signaling extractor or before the basic transmitter to provide superframe alignment between the backplane and either the received DS-1 stream or the transmit DS-1 stream. The purpose of the signaling alignment block is to maintain signaling bit integrity across superframe boundaries.

9.15 Backplane Receive Interface (BRIF)

The Backplane Receive Interface allows data to be presented to a backplane in either a 1.544Mbit/s, 2.048Mbit/s, 12.352Mbit/s or 16.384Mbit/s serial stream and allows BPV transparency by outputting dual-rail data at 1.544Mbit/s.

When configured to provide a 1.544Mbit/s data rate, the block generates the output data stream on the BRPCM[x] pin containing 24 channel bytes of data followed by a single bit containing the framing bit or parity over the 24 channels. The BRSIG[x] output pin contains 24 bytes of signaling nibble data located in the least significant nibble of each byte followed by a single bit position representing the "place holder" for the framing bit or parity over the 24 channels. The framing alignment indication on the BRFPO[x] pin indicates the first bit of the 193-bit

frame (or, optionally, the first bit of the first frame of the superframe, or every second superframe).

When configured to provide a 2.048Mbit/s data rate, the block internally gaps the 2.048MHz rate backplane clock to provide a serial PCM data on the BRPCM[x] pin containing three channel bytes of data followed by one byte of "filler" (can be logic "0" or logic "1"). The data stream on the BRSIG[x] pin is similar, containing three bytes of valid signaling nibbles (i.e. three channels' signaling contained in the least significant nibble of each of the three byte locations) followed by one byte of "filler". The frame alignment indication is provided on the BRFPO[x] pin, going to logic "1" for one BRCLK cycle during the first bit of the "filler" byte, indicating the next data byte is the first channel of the frame, or the first channel of the first frame of the superframe.

When configured for a multiplexed backplane, the four sets of PCM and signaling streams are bit interleaved into a 12.352Mbit/s or 16.384Mbit/s serial stream. The individual receivers must all be configured for either 1.544Mbit/s or 2.048Mbit/s. The MRFPI pin must go to logic "1" for one MRCLK cycle to indicate the alignment of the first PCM bit of the frame or superframe from receiver number one.

9.16 Basic Transmitter (XBAS)

The Basic Transmitter (XBAS) block generates the 1.544 Mbit/s T1 data stream according to SF, ESF, T1DM, or SLC®96 formats.

A serial PCM control stream provides per channel control of idle code substitution, data inversion (either all 8 bits, sign bit only, or magnitude only), digital milliwatt substitution, and zero code suppression. Three types of zero code suppression (GTE, Bell and DDS) are supported and selected on a per channel basis to provide minimum ones density control. A serial signaling control stream provides per channel control of robbed bit signaling and selection of the signaling source. All channels can be forced into a trunk conditioning state (idle code substitution and signaling conditioning) by use of the Master Trunk Conditioning bit in the Configuration Register.

A data link is provided for ESF, T1DM and SLC®96 modes. Serial data input and clock output allow a variety of data link sources including bit oriented codes and HDLC messages. Support is provided for the transmission of framed or unframed Inband Code sequences and transmission of AIS or Yellow alarm signals for all formats.

PCM output signals may be selected to conform to B8ZS or AMI line coding.

The transmitter can be disabled for framing via the disable bit in the Transmit Functions Enable register. When transmitting ESF formatted data, the framing bit, datalink bit, or the CRC-6 bit from the input PCM stream can be by-passed to the output PCM stream. Finally, the transmitter can be by-passed completely to provide BPV transparency.

9.17 Transmit Per-Channel Serial Controller (TPSC)

The Transmit Per-channel Serial Controller allows data and signaling trunk conditioning or idle code to be applied on the transmit DS-1 stream on a per-channel basis. It also allows per-channel control of zero code suppression, data inversion, and application of digital milliwatt.

The Transmit Per-channel Serial Controller function is provided by a Per-Channel Serial Controller (PCSC) block. The PCSC is a general purpose triple serializer. Data is sourced from 3 banks of 24 8-bit registers, each bank supporting a single serial output.

The TPSC interfaces directly to the XBAS block and provides serial streams for signaling control, idle code data and PCM data control.

The registers are accessible from the µP interface in an indirect address mode. The BUSY indication signal can be polled from an internal status register to check for completion of the current operation.

9.18 Inband Loopback Code Generator (XIBC)

The Inband Loopback Code Generator function is provided by the XIBC block. This block generates a stream of inband loopback codes (IBC) to be inserted into a T1 data stream. The IBC stream consists of continuous repetitions of a specific code and can be either framed or unframed. When the XIBC is enabled to generate framed IBC, the framing bit overwrites the inband code pattern. The contents of the code and its length are programmable from 3 to 8 bits. The XIBC interfaces directly to the XBAS Basic Transmitter block.

9.19 Bit Oriented Code Generator (XBOC)

The Bit Oriented Code Generator function is provided by the XBOC block. This block transmits 63 of the possible 64 bit oriented codes in the Facility Data Link channel in ESF framing format, as defined in ANSI T1.403-1989. The 64th code (111111) is similar to the HDLC Flag sequence and is used in the XBOC to disable transmission of any bit oriented codes.

Bit oriented codes are transmitted on the Facility Data Link channel as a 16-bit sequence consisting of 8 ones, a zero, 6 code bits, and a trailing zero (111111110xxxxxx0) which is repeated as long as the code is not 111111. The transmitted bit oriented codes have priority over any data transmitted on the FDL except for ESF YELLOW Alarm. The code to be transmitted is programmed by writing the code register.

9.20 HDLC Transmitter (XFDL)

The HDLC Transmitter function is provided by the XFDL block. This block is designed to provide a serial data link for the XBAS Basic Transmitter block. The XFDL is used under microprocessor or DMA control to transmit HDLC data frames in the ESF Facility Data Link when the TQUAD is enabled to use the internal HDLC transmitter. The XFDL performs all of the data serialization, CRC generation, zero-bit stuffing, as well as flag, idle, and abort sequence insertion. Data to be transmitted is provided on an interrupt-driven basis by writing to a double-buffered transmit data register. Upon completion of the frames, a CRC-CCITT frame check sequence is transmitted, followed by idle flag sequences. If the transmit data register underflows, an abort sequence is automatically transmitted.

When enabled for use (via the EN bit in the XFDL Configuration register), the XFDL continuously transmits the flag character (01111110). Data bytes to be transmitted are written into the Transmit Data Register. After the parallel-to-serial conversion of each data byte, an interrupt is generated to signal the controller to write the next byte into the Transmit Data Register. After the last data frame byte is transmitted, the CRC word (if CRC insertion has been enabled), or a flag (if CRC insertion has not been enabled) is transmitted. The XFDL then returns to the transmission of flag characters.

If there are more than five consecutive ones in the raw transmit data or in the CRC data, a zero is stuffed into the serial data output. This prevents the unintentional transmission of flag or abort characters.

Abort characters can be continuously transmitted at any time by setting a control bit. During transmission, an underrun situation can occur if data is not written to the Transmit Data Register before the previous byte has been depleted. In this case, an abort sequence is transmitted, and the controlling processor is notified via the TDLUDR[x] signal. Optionally, the interrupt and underrun signals can be independently enabled to also generate an interrupt on the INTB output, providing a means to notify the controlling processor of changes in the XFDL operating status.

When the internal HDLC transmitter is disabled, the serial data to be transmitted on the Facility Data Link can be input on the TDLSIG[x] pin timed to the clock rate output on the TDLCLK[x] pin.

9.21 Pulse Density Enforcer (XPDE)

The Pulse Density Enforcer function is provided by the XPDE block. Pulse density enforcement is enabled by a register bit within the XPDE.

This block monitors the digital output of the transmitter, detecting when the stream is about to violate the ANSI T1.403 12.5% pulse density rule over a moving 192-bit window. If a density violation is detected, the block can be enabled to insert a logic 1 into the digital stream to ensure the resultant output no longer violates the pulse density requirement. When the XPDE is disabled from inserting logic 1s, the digital stream from the transmitter is passed through unaltered.

9.22 Digital Jitter Attenuator (DJAT)

The Digital Jitter Attenuation function is provided by the DJAT block. This block receives jittery T1 data in NRZ format from XBAS. The incoming data streams are stored in a FIFO timed to the transmit clock (either BTCLK[x] or RCLKO[x]). The respective input data emerges from the FIFO timed to the jitter attenuated clock (TCLKO[x]) referenced to either TCLKI[x], BTCLK[x], or RCLKO[x].

The jitter attenuator generates the jitter-free 1.544 MHz TCLKO[x] output transmit clock by adaptively dividing the 37.056 MHz XCLK signal according to the phase difference between the generated TCLKO[x] and input data clock to DJAT (either BTCLK[x] or RCLKO[x]). Jitter fluctuations in the phase of the input data clock are attenuated by the phase-locked loop within DJAT so that the frequency of TCLKO[x] is equal to the average frequency of the input data clock. To best fit the jitter attenuation transfer function recommended by TR 62411, phase fluctuations with a jitter frequency above 6.6 Hz are attenuated by 6 dB per octave of jitter frequency. Wandering phase fluctuations with frequencies below 6.6 Hz are tracked by the generated TCLKO[x]. To provide a smooth flow of data out of DJAT[x], TCLKO[x] is used to read data out of the FIFO.

If the FIFO read pointer (timed to TCLKO[x]) comes within one bit of the write pointer (timed to the input data clock, BTCLK[x] or RCLKO[x]), DJAT will track the jitter of the input clock. This permits the phase jitter to pass through unattenuated, inhibiting the loss of data.

Jitter Characteristics

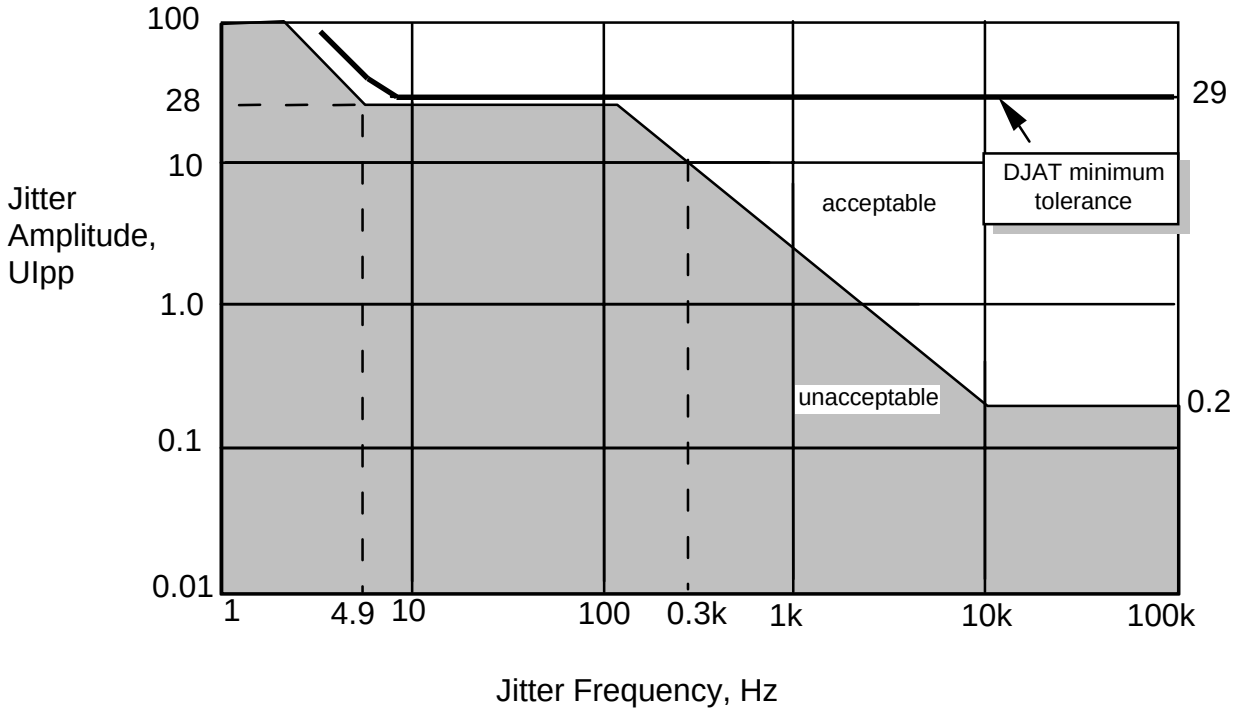
The DJAT Block provides excellent jitter tolerance and jitter attenuation while generating minimal residual jitter. It can accommodate up to 28 UIpp of input jitter at jitter frequencies above 6 Hz. For jitter frequencies below 6 Hz, more correctly called wander, the tolerance increases 20 dB per decade. In most applications the DJAT Block will limit jitter tolerance at lower jitter frequencies only. For high frequency jitter, above 10 kHz for example, other factors such as clock and data recovery circuitry may limit jitter tolerance and must be considered. For low frequency wander, below 10 Hz for example, other factors such as slip buffer hysteresis may limit wander tolerance and must be considered. The DJAT block meets the stringent low frequency jitter tolerance requirements of AT&T TR 62411 and thus allows compliance with this standard and the other less stringent jitter tolerance standards cited in the references.

DJAT exhibits negligible jitter gain for jitter frequencies below 6.6 Hz, and attenuates jitter at frequencies above 6.6 Hz by 20 dB per decade. In most applications the DJAT Block will determine jitter attenuation for higher jitter frequencies only. Wander, below 10 Hz for example, will essentially be passed unattenuated through DJAT. Jitter, above 10 Hz for example, will be attenuated as specified, however, outgoing jitter may be dominated by the generated residual jitter in cases where incoming jitter is insignificant. This generated residual jitter is directly related to the use of 24X (37.056 MHz) digital phase locked loop for transmit clock generation. DJAT meets the jitter attenuation requirements of AT&T TR 62411. The block allows the implied jitter attenuation requirements for a TE or NT1 given in ANSI Standard T1.408, and the implied jitter attenuation requirements for a type II customer interface given in ANSI T1.403 to be met.

Jitter Tolerance

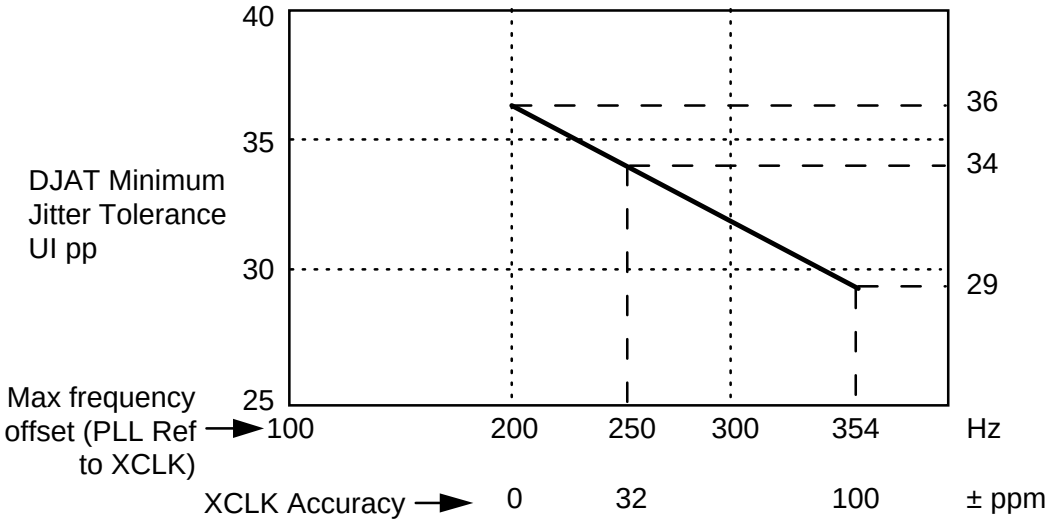
Jitter tolerance is the maximum input phase jitter at a given jitter frequency that a device can accept without exceeding its linear operating range, or corrupting data. For DJAT, the input jitter tolerance is 29 Unit Intervals peak-to-peak (UIpp) with a worst case frequency offset of 354 Hz. It is 48 UIpp with no frequency offset. The frequency offset is the difference between the frequency of XCLK divided by 24 and that of the input data clock.

Figure 4 - DJAT Jitter Tolerance



The accuracy of the XCLK frequency and that of the DJAT PLL reference input clock used to generate the jitter-free TCLKO[x] have an effect on the minimum jitter tolerance. Given that the DJAT PLL reference clock accuracy can be ±200 Hz from 1.544 MHz, and that the XCLK input accuracy can be ±100 ppm from 37.056 MHz, the minimum jitter tolerance for various differences between the frequency of PLL reference clock and XCLK ÷ 24 are shown in Figure 5.

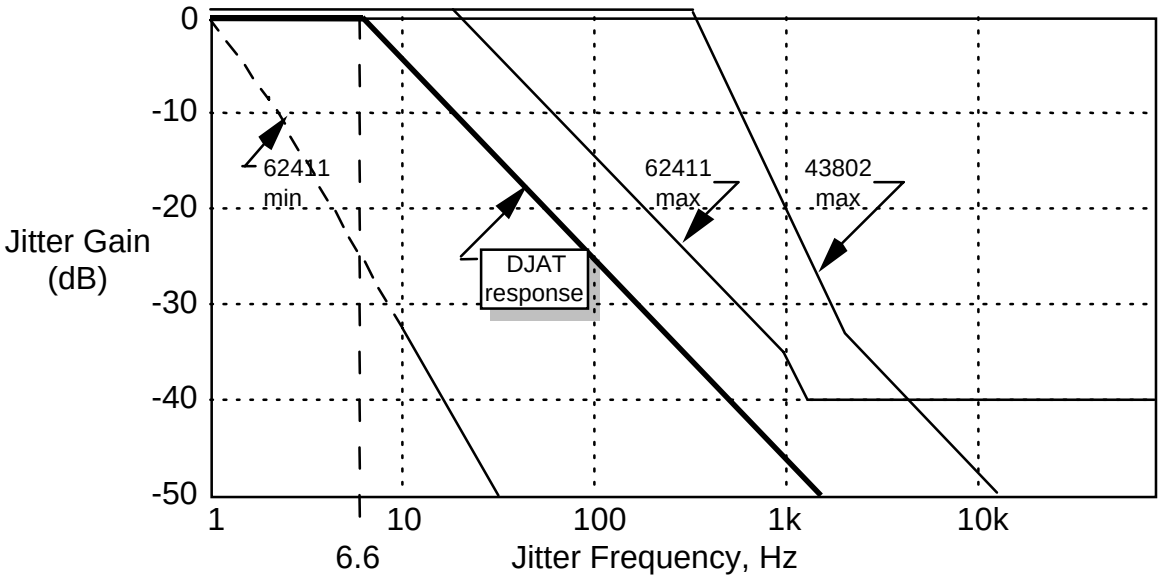
Figure 5 - DJAT Minimum Jitter Tolerance vs XCLK Accuracy



Jitter Transfer

The output jitter for jitter frequencies from 0 to 6.6 Hz is no more than 0.1 dB greater than the input jitter, excluding the 0.042 UI residual jitter. Jitter frequencies above 6.6 Hz are attenuated at a level of 6 dB per octave, as shown in Figure 6 below:

Figure 6 - DJAT Jitter Transfer



Frequency Range

In the non-attenuating mode, that is, when the FIFO is within one UI of overrunning or under running, the tracking range is 1.48 to 1.608 MHz. The guaranteed linear operating range for the jittered input clock is 1.544 MHz ± 200 Hz with worst case jitter (29 UIpp) and maximum XCLK frequency offset (± 100 ppm). The nominal range is 1.544 MHz ± 963 Hz with no jitter or XCLK frequency offset.

9.23 Timing Options (TOPS)

The Timing Options block provides a means of selecting the source of the internal input clock to the DJAT block, the reference signal for the digital PLL, and the clock source used to derive the output TCLKO[x] signal.

9.24 Digital DS-1 Transmit Interface (DTIF)

The Digital DS-1 Transmit Interface provides control over the various output options available on the multifunctional digital transmit pins TDP/TDD[x] and TDN/TFLG[x]. When configured for dual-rail output, the multifunctional pins become the TDP[x] and TDN[x] outputs. These outputs can be formatted as either return-to-zero (RZ) or non-return-to-zero (NRZ) signals and can be updated on either the rising or falling edge of TCLKO[x]. When the interface is configured for single-rail output, the multifunctional pins become the TDD[x] and TFLG[x] outputs, which can be enabled to be updated on either the rising or falling TCLKO[x] edge. Further, the TFLG[x] output can be enabled to indicate FIFO empty or FIFO full status.

The DTIF block also provides Alarm Indication Signaling (AIS) generation capability by generating alternating mark signals on the TDP/TDN[x] outputs, or all-ones on the TDD[x] output, when the TAISEN bit is set in the Transmit DS1 Interface Configuration register. This is useful when the internal loopback modes are used.

9.25 Backplane Transmit Interface (BTIF)

The Backplane Transmit Interface allows data to be taken from a backplane in either a 1.544Mbit/s, 2.048Mbit/s, 12.352Mbit/s or 16.384Mbit/s serial stream and allows BPV transparency by accepting dual-rail data input at 1.544Mbit/s.

When configured to receive a 1.544Mbit/s data rate stream, the block expects the input data stream on the BTPCM[x] pin to contain 24 channel bytes of data followed by a single bit location for the framing bit or optional parity over the

previous 24 channels. The BTSIG[x] input pin must contain 24 bytes of signaling nibble data located in the least significant nibble of each byte followed by a single bit position for the framing bit or optional parity over the previous frame. The framing alignment indication on the BTFP[x] pin indicates the framing bit position of the 193-bit frame (or, optionally, the framing bit position of the first frame of the superframe, or every second superframe).

When configured to receive a 2.048Mbit/s data rate stream, the block internally gaps the 2.048MHz rate backplane clock to convert the serial PCM data on the BTPCM[x] pin containing three channel bytes of data followed by one byte of "filler" (which can be logic "0" or logic "1") into an internal 1.544Mbit/s serial stream for transmission. The data stream on the BTSIG[x] pin, containing three bytes of valid signaling nibbles (i.e. three channels' signaling contained in the least significant nibble of each of the three byte locations) followed by one byte of "filler", is similarly converted to an internal 1.544Mbit/s rate. The frame alignment indication provided on the BTFP[x] pin must go to logic "1" for one BTCLK[x] cycle during the first bit of the "filler" byte, indicating the next data byte is the first channel of the frame, or the first channel of the first frame of the superframe.

When configured to interface to a 12.352Mbit/s or 16.384Mbit/s serial stream, the four sets of PCM and signaling streams are expected to be bit interleaved. The individual transmitters must all be configured for either 1.544Mbit/s or 2.048Mbit/s. The MTFP pin must go to logic "1" for one MTCLK cycle to mark the first PCM bit of the frame or superframe destined for transmitter number one.

9.26 Microprocessor Interface (MPIF)

The Microprocessor Interface allows the TQUAD to be configured, controlled and monitored via internal registers.

10 REGISTER DESCRIPTION

Table 1 - Normal Mode Register Memory Map

Address				Register
#1	# 2	# 3	# 4	
000H	080H	100H	180H	Receive Options
001H	081H	101H	181H	Receive Backplane Options
002H	082H	102H	182H	Datalink Options
003H	083H	103H	183H	Receive DS1 Interface Configuration
004H	084H	104H	184H	Transmit DS1 Interface Configuration
005H	085H	105H	185H	Transmit Backplane Options
006H	086H	106H	186H	Transmit Framing and Bypass Options
007H	087H	107H	187H	Transmit Timing Options
008H	088H	108H	188H	Interrupt Source #1
009H	089H	109H	189H	Interrupt Source #2
00AH	08AH	10AH	18AH	Diagnostics
00BH				Master Test
00CH				Revision/Chip ID/Global PMON Update
00DH	08DH	10DH	18DH	Framer Reset
00EH	08EH	10EH	18EH	Phase Status Word (LSB)
00FH	08FH	10FH	18FH	Phase Status Word (MSB)
010H	090H	110H	190H	CDRC Configuration
011H	091H	111H	191H	CDRC Interrupt Enable
012H	092H	112H	192H	CDRC Interrupt Status
013H	093H	113H	193H	Alternate Loss of Signal
014H-017H	094H-097H	114H-117H	194H-197H	Reserved
018H	098H	118H	198H	DJAT Interrupt Status

Address				Register
#1	# 2	# 3	# 4	
019H	099H	119H	199H	DJAT Reference Clock Divisor (N1) Control
01AH	09AH	11AH	19AH	DJAT Output Clock Divisor (N2) Control
01BH	09BH	11BH	19BH	DJAT Configuration
01CH	09CH	11CH	19CH	ELST Configuration
01DH	09DH	11DH	19DH	ELST Interrupt Enable/Status
01EH	09EH	11EH	19EH	ELST Trouble Code
01FH	09FH	11FH	19FH	ELST Reserved
020H	0A0H	120H	1A0H	FRMR Configuration
021H	0A1H	121H	1A1H	FRMR Interrupt Enable
022H	0A2H	122H	1A2H	FRMR Interrupt Status
023H	0A3H	123H	1A3H	FRMR Reserved
024H	0A4H	124H	1A4H	Channel Select (1 to 8)
025H	0A5H	125H	1A5H	Channel Select (9 to 16)
026H	0A6H	126H	1A6H	Channel Select (17 to 24)
027H	0A7H	127H	1A7H	Interrupt ID (reg 027H only)/Clock Monitor
028H	0A8H	128H	1A8H	Backplane Parity Configuration and Status
029H	0A9H	129H	1A9H	Reserved
02AH	0AAH	12AH	1AAH	RBOC Enable
02BH	0ABH	12BH	1ABH	RBOC Code Status
02CH	0ACH	12CH	1ACH	ALMI Configuration
02DH	0ADH	12DH	1ADH	ALMI Interrupt Enable
02EH	0AEH	12EH	1AEH	ALMI Interrupt Status
02FH	0AFH	12FH	1AFH	ALMI Alarm Detection Status
030H	0B0H	130H	1B0H	TPSC Configuration

Address				Register
#1	# 2	# 3	# 4	
031H	0B1H	131H	1B1H	TPSC µP Access Status
032H	0B2H	132H	1B2H	TPSC Channel Indirect Address/Control
033H	0B3H	133H	1B3H	TPSC Channel Indirect Data Buffer
034H	0B4H	134H	1B4H	XFDL Configuration
035H	0B5H	135H	1B5H	XFDL Interrupt Status
036H	0B6H	136H	1B6H	XFDL Transmit Data
037H	0B7H	137H	1B7H	XFDL Reserved
038H	0B8H	138H	1B8H	RFDL Configuration
039H	0B9H	139H	1B9H	RFDL Interrupt Control/Status
03AH	0BAH	13AH	1BAH	RFDL Status
03BH	0BBH	13BH	1BBH	RFDL Receive Data
03CH	0BCH	13CH	1BCH	IBCD Configuration
03DH	0BDH	13DH	1BDH	IBCD Interrupt Enable/Status
03EH	0BEH	13EH	1BEH	IBCD Activate Code
03FH	0BFH	13FH	1BFH	IBCD Deactivate Code
040H	0C0H	140H	1C0H	SIGX Configuration
041H	0C1H	141H	1C1H	SIGX µP Access Status
042H	0C2H	142H	1C2H	SIGX Channel Indirect Address/Control
043H	0C3H	143H	1C3H	SIGX Channel Indirect Data Buffer
044H	0C4H	144H	1C4H	XBAS Configuration
045H	0C5H	145H	1C5H	XBAS Alarm Transmit
046H	0C6H	146H	1C6H	XIBC Control
047H	0C7H	147H	1C7H	XIBC Loopback Code
048H	0C8H	148H	1C8H	PMON Reserved
049H	0C9H	149H	1C9H	PMON Interrupt Enable/status
04AH	0CAH	14AH	1CAH	PMON LCV Count (LSB)

Address				Register
#1	# 2	# 3	# 4	
04BH	0CBH	14BH	1CBH	PMON LCV Count (MSB)
04CH	0CCH	14CH	1CCH	PMON BEE Count (LSB)
04DH	0CDH	14DH	1CDH	PMON BEE Count (MSB)
04EH	0CEH	14EH	1CEH	PMON FER Count
04FH	0CFH	14FH	1CFH	PMON OOF/COFA Count
050H	0D0H	150H	1D0H	RPSC Configuration
051H	0D1H	151H	1D1H	RPSC µP Access Status
052H	0D2H	152H	1D2H	RPSC Channel Indirect Address/Control
053H	0D3H	153H	1D3H	RPSC Channel Indirect Data Buffer
054H	0D4H	154H	1D4H	PDVD Reserved
055H	0D5H	155H	1D5H	PDVD Interrupt Enable/Status
056H	0D6H	156H	1D6H	XBOC Reserved
057H	0D7H	157H	1D7H	XBOC Code
058H	0D8H	158H	1D8H	XPDE Reserved
059H	0D9H	159H	1D9H	XPDE Interrupt Enable/Status
05AH-07FH	0DAH-0FFH	15AH-17FH	1DAH-1FFH	Reserved
200H-3FFH				Reserved for Test

11 NORMAL MODE REGISTER DESCRIPTION

Normal mode registers are used to configure and monitor the operation of the TQUAD. Normal mode registers (as opposed to test mode registers) are selected when A[9] is low.

Notes on Normal Mode Register Bits:

1. Although the register bit descriptions for the four framers have been combined, each framer is completely independent of the others.

2. Writing values into unused register bits has no effect. Reading back unused bits can produce either a logic 1 or a logic 0; hence, unused register bits should be masked off by software when read.

3. All configuration bits that can be written into can also be read back. This allows the processor controlling the TQUAD to determine the programming state of the chip.

4. Writeable normal mode register bits are cleared to zero upon reset unless otherwise noted.

5. Writing into read-only normal mode register bit locations does not affect TQUAD operation unless otherwise noted.

Registers 000H, 080H, 100H and 180H: Receive Options

Bit	Type	Function	Default
Bit 7	R/W	Unused	X
Bit 6	R/W	UNF	0
Bit 5	R/W	ELSTBYP	0
Bit 4	R/W	TRSLIP	0
Bit 3	R/W	Unused	X
Bit 2	R/W	SRSFP	0
Bit 1	R/W	ALTRFP	0
Bit 0	R/W	CCOFA	0

These registers allow software to configure the receive functions of each framer.

UNF:

The UNF bit allows the framer to operate with unframed DS-1 data. When UNF is set to logic 1, the FRMR is disabled and the recovered data passes through the receiver section of the framer without frame or channel alignment. While UNF is held at logic 1, the Alarm Integrator continues to operate and detects and integrates AIS alarm. When UNF is set to logic 0, the framer operates normally, searching for frame alignment on the incoming data.

ELSTBYP:

The ELSTBYP bit allows the Elastic Store (ELST) to be bypassed, eliminating the one frame delay incurred through the ELST. When set to logic 1, the received data and clock inputs to ELST are internally routed directly to the ELST outputs.

TRSLIP:

The TRSLIP bit allows the ELST to be used to measure, through SLIP indications, the frequency difference between the recovered receive line clock and the transmit clock driving the XBAS when the ELST is bypassed. When TRSLIP is set to logic 1, the transmit clock input to XBAS is internally substituted for the BRCLK input to the system side of the ELST. When TRSLIP is set to logic 0, the BRCLK input is routed to the system side of the ELST. The TRSLIP bit is valid only when ELSTBYP is set to logic 1

SRSFP:

The SRSFP bit selects the output signal seen on the multifunction output RFP. When set to logic 1, the multifunction output becomes RSFP, the receive superframe pulse indication, which pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the FRMR). When SRSFP is set to logic 0, the multifunction output becomes RFP, which pulses high during each framing bit (i.e. every 193 bits).

ALTRFP:

The ALTRFP bit suppresses every second output pulse on the multifunction output RFP. When ALTRFP is set to logic 1, the output signal on RFP pulses every 386 bits, indicating every second framing bit (if the SRSFP bit is logic 0); or the output signal on RFP pulses every 24 or 48 frames (if the SRSFP bit is logic 1). When ALTRFP is set to logic 0, the output signal on RFP pulses in accordance to the SRSFP bit setting.

CCOFA

The CCOFA bit determines whether the PMON counts Change-Of-Frame Alignment (COFA) events or out-of-frame (OOF) events. When CCOFA is set to logic 1, COFA events are counted by PMON. When CCOFA is set to logic 0, OOF events are counted by PMON.

Upon reset of the TQUAD, these bits are cleared to zero.

Registers 001H, 081H, 101H and 181H: Receive Backplane Options

Bit	Type	Function	Default
Bit 7	R/W	RCLKOSEL	0
Bit 6	R/W	ALTFDL	0
Bit 5	R/W	RXDMAGAT	0
Bit 4	R/W	BRX2M	0
Bit 3	R/W	BRX2RAIL	0
Bit 2	R/W	BRXSFP	0
Bit 1	R/W	ALTBRFP	0
Bit 0	R/W	RXMTKC	0

These registers allow software to configure the Receive backplane interface format of each framer.

RCLKOSEL:

The RCLKOSEL bit selects the source of the RCLKO[x] output and the internal elastic store output clock. If RCLKOSEL is a logic zero, RCLKO[x] is the recovered clock derived from RDP[x] and RDN[x] or RCLKI[x] and the internal elastic store output clock is BRCLK. If RCLKOSEL is a logic one, RCLKO[x] and the internal elastic store output clock originate from the smooth 1.544 MHz clock generated by the DJAT phase locked loop. If the recovered clock is selected as the PLL reference, the configuration implements jitter attenuation in the receive direction. See the Operations Section for details on this application. TRSLIP must be set to logic 0.

ALTFDL:

The ALTFDL bit enables the framing bit position on the backplane PCM output to contain a copy of the FDL bit. When ALTFDL is set to logic 1, each M-bit value in the ESF-formatted stream is duplicated and replaces the subsequent CRC bit or F-bit in the output signal stream on BRPCM[x]. When ALTFDL is set to logic 0, the output BRPCM[x] stream contains the received M, CRC, or F bits in the framing bit position. Note that this function is only valid for ESF-formatted streams, ALTFDL should be set to logic 0 when other framing formats are being received.

RXDMAGAT:

The RXDMAGAT bit selects the gating of the RDLINT[x] output with the RDLEOM[x] output when the internal HDLC receiver is used with DMA. When RXDMAGAT is set to logic 1, the RDLINT[x] DMA output is gated with the RDLEOM output so that RDLINT is forced to logic 0 when RDLEOM is logic 1. When RXDMAGAT is set to logic 0, the RDLINT[x] and RDLEOM[x] outputs operate independently.

BRX2M:

The BRX2M bit selects the 2.048 MHz backplane data rate. When BRX2M is set to logic 1, the clock rate on the BRCLK input is expected to be 2.048MHz and the data stream on BRPCM[x] is output as 1 byte of "filler" followed by 3 bytes of channel data, repeated 8 times. When BRX2M is set to logic 0, the backplane data rate and format is identical to T1 (i.e. 1.544MHz rate with 24 contiguous channel bytes followed by 1 framing bit).

The BRX2M bit affects the data format when bit interleaved multiplexing is selected by asserting the MENB input low. When BRX2M for all four DS1s is set to logic 1, the clock rate on the MRCLK input is expected to be 16.384MHz. When BRX2M for all four DS1s is set to logic 0, the clock rate on the MRCLK input is expected to be 12.352MHz.

BRX2RAIL:

The BRX2RAIL bit selects whether the backplane receive data signal on the multifunction outputs BRPCM/BRDP[x] and BRSIG/BRDN[x] are in either dual rail or single rail format. When BRX2RAIL is set to logic 1, the multifunction pins become the BRDP[x] and BRDN[x] dual rail outputs, which contain the received positive and negative line pulses timed to the 1.544MHz receive line rate, RCLKO[x]. When BRX2RAIL is set to logic 0, the multifunction pins become the BRPCM[x] and BRSIG[x] digital outputs. For proper operation, RCLKOSEL must be set to a logic 0 if BRX2RAIL is set to a logic 1.

BRXSFP:

The BRXSFP bit selects the output signal seen on the backplane output BRFPO[x]. When set to logic 1, the BRFPO[x] output pulses high during the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the FRMR). When BRXSFP is set to logic 0, the BRFPO[x] output pulses high during each framing bit (i.e. every 193 bits).

ALTBRFP:

The ALTBRFP bit suppresses every second output pulse on the backplane output BRFPO[x]. When ALTBRFP is set to logic 1, the output signal on

BRFPO[x] pulses every 386 bits, indicating every second framing bit (if the BRXSFP bit is logic 0); or the output signal on BRFPO[x] pulses every 24 or 48 frames (if the BRXSFP bit is logic 1). This latter setting (i.e. both ALTBRFP and BRXSFP set to logic 1) is useful for converting SF formatted data to ESF formatted data between two TQUAD devices. When ALTBRFP is set to logic 0, the output signal on BRFPO[x] pulses in accordance to the BRXSFP bit setting.

RXMTKC:

The RXMTKC bit allows global trunk conditioning to be applied to the received data and signaling streams, BRPCM[x] and BRSIG[x]. When RXMKTC is set to logic 1, the data on BRPCM[x] for each channel is replaced with the data contained in the data trunk conditioning registers within RPSC; similarly, the signaling data on BRSIG[x] for each channel is replaced with the data contained in the signaling trunk conditioning registers. When RXMKTC is set to logic 0, the data and signaling signals are modified on a per-channel basis in accordance with the control bits contained in the per-channel control registers within the RPSC.

Upon reset of the TQUAD, these bits are cleared to zero.

Registers 002H, 082H, 102H and 182H: Datalink Options

Bit	Type	Function	Default
Bit 7	R/W	RXDMASIG	0
Bit 6	R/W	RXDCHAN	0
Bit 5	R/W	TXDMASIG	0
Bit 4	R/W	TXDCHAN	0
Bit 3	R/W	RDLINTE	0
Bit 2	R/W	RDLEOME	0
Bit 1	R/W	TDLINTE	0
Bit 0	R/W	TDLUDRE	0

These registers allow software to configure the datalink options of each framer.

RXDMASIG:

The RXDMASIG bit selects the internal HDLC receiver (RFDL) data-received interrupt (INT) and end-of-message (EOM) signals to be output on the RDLINT[x] and RDLEOM[x] pins when the RXDCHAN bit is logic 0. When RXDMASIG is set to logic 1, the RDLINT[x] and RDLEOM[x] output pins can be used by a DMA controller to process the datalink. When RXDMASIG is set to logic 0, the RFDL INT and EOM signals are no longer available to a DMA controller; the signals on RDLINT[x] and RDLEOM[x] become the extracted datalink data and clock, RDLSIG[x] and RDLCLK[x]. In this mode, the data stream available on the RDLSIG[x] output corresponds to the extracted facility datalink in ESF, the extracted R-bit value of the sync word in T1DM, or the extracted Fs framing bits in SLC®96. When RXDCHAN is set to logic 1, the RXDMASIG bit has no effect.

RXDCHAN:

The RXDCHAN bit selects whether a fractional T1 is extracted and made available on the RDLSIG[x] output, or whether the RDLINT/RDLSIG[x] and RDLEOM/RDLCLK[x] pins operate as defined by the RXDMASIG bit. When RXDCHAN is set to logic 1, the contents of the Channel Select registers determine which channels are output on RDLSIG[x] with an aligned burst clock output on RDLCLK[x]. By default, the Primary Rate D-Channel (channel 24 of every frame) is extracted. When RXDCHAN is set to logic 0, the RDLINT/RDLSIG[x] and RDLEOM/RDLCLK[x] pins contain the signals selected by the RXDMASIG bit.

TXDMASIG:

The TXDMASIG bit selects the internal HDLC transmitter (XFDL) request for service interrupt (INT) and data underrun (UDR) signals to be output on the TDLINT[x] and TDLUDR[x] pins when the TXDCHAN bit is logic 0. When TXDMASIG is set to logic 1, the TDLINT[x] and TDLUDR[x] output pins can be used by a DMA controller to service the datalink. When TXDMASIG is set to logic 0, the XFDL INT and UDR signals are no longer available to a DMA controller; the signals on TDLINT[x] and TDLUDR[x] become the serial datalink data input and clock, TDLSIG[x] and TDLCLK[x]. In this mode an external controller is responsible for formatting the data stream presented on the TDLSIG[x] input to correspond to the facility datalink in ESF, the R-bit value of the sync word in T1DM, or the Fs framing bits in SLC®96. When TXDCHAN is set to logic 1, the TXDMASIG bit has no effect.

TXDCHAN:

The TXDCHAN bit selects whether a fractional T1 is inserted into a subset of the channels of each frame via the TDLSIG input, or whether the TDLINT/TDLSIG[x] and TDLUDR/TDLCLK[x] pins operate as defined by the TXDMASIG bit. When TXDCHAN is set to logic 1, the channel data is expected on TDLSIG[x], sampled on the rising edge of a burst clock provided on TDLCLK. The channels inserted are determined by the Channel Select registers; all others are inserted through BTPCM[x]. By default, the Primary Rate D-Channel (channel 24) inserted through TDLSIG[x]. When TXDCHAN is set to logic 0, the TDLINT/TDLSIG[x] and TDLUDR/TDLCLK[x] pins contain the signals selected by the TXDMASIG bit.

RDLINTE:

The RDLINTE bit enables the RFDL received-data interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLINTE is set to logic 1, an event causing an interrupt in the RFDL (which is visible on the RDLINT[x] output pin when RXDMASIG is logic 1 and RXDCHAN is logic 0) also causes an interrupt to be generated on the INTB output. When RDLINTE is set to logic 0, an interrupt event in the RFDL does not cause an interrupt on INTB.

RDLEOME:

The RDLEOME bit enables the RFDL end-of-message interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the RFDL without needing to interface to the DMA control signals. When RDLEOME is set to logic 1, an end-of-message event causing an EOM interrupt in the RFDL (which is visible on the

RDLEOM[x] output pin when RXDMASIG is logic 1 and RXDCHAN is logic 0) also causes an interrupt to be generated on the INTB output. When RDLEOME is set to logic 0, an EOM interrupt event in the RFDL does not cause an interrupt on INTB. NOTE: within the RFDL, an end-of-message event causes an interrupt on both the EOM and INT RFDL interrupt outputs. See the Operation section for further details on using the RFDL.

TDLINTE:

The TDLINTE bit enables the XFDL request for service interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLINTE is set to logic 1, an request for service interrupt event in the XFDL (which is visible on the TDLINT[x] output pin when TXDMASIG is logic 1 and TXDCHAN is logic 0) also causes and interrupt to be generated on the INTB output. When TDLINTE is set to logic 0, an interrupt event in the XFDL does not cause an interrupt on INTB.

TDLUDRE:

The TDLUDRE bit enables the XFDL transmit data underrun interrupt to also generate an interrupt on the microprocessor interrupt, INTB. This allows a single microprocessor to service the XFDL without needing to interface to the DMA control signals. When TDLUDRE is set to logic 1, an underrun event causing an interrupt in the XFDL (which is visible on the TDLUDR[x] output pin when TXDMASIG is logic 1 and TXDCHAN is logic 0) also causes and interrupt to be generated on the INTB output. When TDLUDRE is set to logic 0, an underrun event in the XFDL does not cause an interrupt on INTB.

Upon reset of the TQUAD, these bits are cleared to zero.

Registers 003H, 083H, 103H and 183H: Receive DS1 Interface Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BPV	0
Bit 4	R/W	RDNINV	0
Bit 3	R/W	RDPINV	0
Bit 2	R/W	RUNI	0
Bit 1	R/W	RFALL	0
Bit 0	R/W	RRZ	0

These registers enable the Receive DS1 Interface to handle the various input waveform formats.

BPV:

The BPV bit enables only bipolar violations to indicate line code violations and be accumulated in the PMON LCV Count Registers. When BPV is set to logic 1, BPVs (which are not part of a valid B8ZS signature if B8ZS line coding is used) generate an LCV indication and increment the PMON LCV counter. When BPV is set to logic 0, both BPVs (which are not part of a valid B8ZS signature if B8ZS line coding is used) and excessive zeros (EXZ) generate an LCV indication and increment the PMON LCV counter. Excessive zeros is a sequence of zeros greater than 15 bits log for an AMI-code signal and greater than 7 bits long for a B8ZS-coded signals.

RDPINV,RDNINV:

The RDPINV and RDNINV bits enable the DS-1 Receive Interface to logically invert the signals received on pins RDP/RDD[x] and RDN/RLCV[x], respectively. When RDPINV is set to logic 1, the interface inverts the signal on the RDP/RDD[x] input. When RDPINV is set to logic 0, the interface passes the RDP/RDD[x] signal unaltered. When RDNINV is set to logic 1, the interface inverts the signal on the RDN/RLCV[x] input. When RDNINV is set to logic 0, the interface passes the RDN/RLCV[x] signal unaltered.

RUNI:

The RUNI bit enables the interface to receive uni-polar digital data and line code violation indications on the pins RDP/RDD[x] and RDN/RLCV[x]. When RUNI is set to logic 1, the RDP/RDD[x] and RDN/RLCV[x] multifunction pins become the data and line code violation inputs, RDD[x] and RLCV[x], sampled on the selected RCLKI[x] edge. When RUNI is set to logic 0, the RDP/RDD[x] and RDN/RLCV[x] multifunction pins become the positive and negative pulse inputs, RDP[x] and RDN[x], sampled on the selected RCLKI[x] edge.

RFALL:

The RFALL bit enables the DS-1 Receive Interface to sample the multifunction pins on the falling RCLKI[x] edge. When RFALL is set to logic 1, the interface is enabled to sample either the RDD[x] and RLCV[x] inputs, or the RDP[x] and RDN[x] inputs, on the falling RCLKI[x] edge. When RFALL is set to logic 0, the interface is enabled to sample the inputs on the rising RCLKI[x] edge.

RRZ:

The RRZ bit configures the interface to receive return-to-zero formatted waveforms. When RRZ is set to logic 1, the interface is configured to pass the signals on the RDP[x] and RDN[x] inputs unaltered directly into the CDRC. The RCLKI[x] input is ignored. When RRZ is set to logic 0, the interface is configured to sample either the RDD[x] input or the RDP[x] and RDN[x] inputs on the RCLKI[x] edge specified by the RFALL bit and generate an internal RZ representation of these inputs with duration equal to half the RCLKI[x] period. The internally-generated RZ signals are then passed on to CDRC. The RRZ bit is only valid when RUNI is set to logic 0.

When the system is reset, the contents of the register are set to logic 0 enabling reception of a bi-polar signal sampled on the rising edge of RCLKI[x].

Registers 004H, 084H, 104H and 184H: Transmit DS1 Interface Configuration

Bit	Type	Function	Default
Bit 7	R/W	FIFOBYP	0
Bit 6	R/W	TAISEN	0
Bit 5	R/W	TDNINV	0
Bit 4	R/W	TDPINV	0
Bit 3	R/W	TUNI	0
Bit 2	R/W	FIFOFULL	0
Bit 1	R/W	TRISE	0
Bit 0	R/W	TRZ	0

These registers enable the Transmit DS1 Interface to generate the required digital output waveform format.

FIFOBYP:

The FIFOBYP bit enables the transmit bi-polar input signals to DJAT to be bypassed around the FIFO to the bi-polar outputs. When jitter attenuation is not being used, the DJAT FIFO can be bypassed to reduce the delay through the transmitter section by typically 24 bits. When FIFOBYP is set to logic 1, the bi-polar inputs to DJAT are routed around the FIFO to the bi-polar outputs. When FIFOBYP is set to logic 0, the bi-polar transmit data passes through the DJAT FIFO.

TAISEN:

The TAISEN bit enables the interface to generate an unframed all-ones AIS alarm on the TDP/TDD[x] and TDN/TFLG[x] multifunction pins. When TAISEN is set to logic 1 and TUNI is set to logic 0, the bi-polar TDP[x] and TDN[x] outputs are forced to pulse alternately, creating an all-ones signal; when TAISEN and TUNI are both set to logic 1, the uni-polar TDD[x] output is forced to all-ones. When TAISEN is set to logic 0, the TDP/TDD[x] and TDN/TFLG[x] multifunction outputs operate normally. The transition to transmitting AIS on the TDP[x] and TDN[x] outputs is done in such a way as to not introduce any bi-polar violations.

TDPINV,TDNINV:

The TDPINV and TDNINV bits enable the DS-1 Transmit Interface to logically invert the signals output on the TDP/TDD[x] and TDN/TFLG[x] multifunction pins, respectively. When TDPINV is set to logic 1, the TDP/TDD[x] output is inverted. When TDPINV is set to logic 0, the TDP/TDD[x] output is not inverted. When TDNINV is set to logic 1, the TDN/TFLG[x] output is inverted. When TDNINV is set to logic 0, the TDN/TFLG[x] output is not inverted.

TUNI:

The TUNI bit enables the transmit interface to generate uni-polar digital outputs on the TDP/TDD[x] and TDN/TFLG[x] multifunction pins. When TUNI is set to logic 1, the TDP/TDD[x] and TDN/TFLG[x] multifunction pins become the unipolar outputs TDD[x] and TFLG[x], updated on the selected TCLKO edge. When TUNI is set to logic 0, the TDP/TDD[x] and TDN/TFLG[x] multifunction pins become the bipolar outputs TDP[x] and TDN[x], also updated on the selected TCLKO[x] edge.

FIFOFULL:

The FIFOFULL bit determines the indication given on the TFLG[x] output pin. When FIFOFULL is set to logic 1, the TFLG[x] output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming full. When FIFOFULL is set to logic 0, the TFLG[x] output indicates when the Digital Jitter Attenuator's FIFO is within 4 bit positions of becoming empty.

TRISE:

The TRISE bit configures the interface to update the multifunction outputs on the rising edge of TCLKO[x]. When TRISE is set to logic 1, the interface is enabled to update the TDP/TDD[x] and TDN/TFLG[x] output pins on the rising TCLKO[x] edge. When TRISE is set to logic 0, the interface is enabled to update the outputs on the falling TCLKO[x] edge.

TRZ:

The TRZ bit configures the interface to transmit bipolar return-to-zero formatted waveforms. When TRZ is set to logic 1, the interface is enabled to generate the TDP[x] and TDN[x] output signals as RZ waveforms with duration equal to half the TCLKO[x] period. When TRZ is set to logic 0, the interface is enabled to generate the TDP[x] and TDN[x] output signals as NRZ waveforms with duration equal to the TCLKO[x] period, updated on the selected edge of TCLKO[x]. The TRZ bit can only be used when TUNI and TRISE are set to logic 0.

When the system is reset, the contents of the register are set to logic 0, enabling the Transmit Interface to output NRZ formatted positive and negative pulse data on the TDP[x] and TDN[x] outputs, updated on the falling TCLKO[x] edge.

Registers 005H, 085H, 105H and 185H: Transmit Backplane Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ABXXEN	0
Bit 3	R/W	BTXCLK	0
Bit 2	R/W	BTX2M	0
Bit 1	R/W	BTX2RAIL	0
Bit 0	R/W	BTXSFP	0

These registers allow software to configure the Transmit backplane interface format of each framer.

ABXXEN:

The ABXXEN bit selects the format of the BTSIG[x] transmit signaling input signal. When ABXXEN is set to logic 1, BTSIG[x] is expected to contain only the A and B signaling bits in the upper two bit positions of the lower nibble of each channel (i.e. ABXX), with the lower two bit positions being "Don't Cares". When ABXXEN is set to logic 0, BTSIG[x] is expected to contain all four signaling bit in the lower nibble of each channel (i.e. ABCD), or it is expected to contain the A and B bits duplicated in the lower nibble (i.e. ABAB).

BTXCLK:

The BTXCLK bit selects the source of the XBAS transmit clock input signal. When BTXCLK is set to logic 1, the XBAS transmit clock is driven with the 1.544MHz recovered PCM output clock (RCLKO[x]) from the receiver section. When BTXCLK is set to logic 0, the XBAS transmit clock is driven with the 1.544MHz backplane transmit clock (BTCLK[x]), or the internal "gapped" clock derived from the 2.048MHz BTCLK[x].

BTX2M:

The BTX2M bit selects the 2.048 MHz data rate and format of the backplane transmit data and frame alignment signals. When BTX2M is set to logic 1, the clock rate on the BTCLK[x] input is expected to be 2.048 MHz and the data stream on BTPCM[x] and BTSIG[x] is expected to be formatted as 1 byte of

"filler" followed by 3 bytes of channel data, repeated 8 times. When BTX2M is set to logic 0, the backplane transmit data rate and format is identical to T1 (i.e. 1.544MHz rate with 24 contiguous channel bytes followed by 1 framing bit).

The BTX2M bit affects the data format when bit interleaved multiplexing is selected by asserting the MENB input low. When BTX2M for all four DS1s is set to logic 1, the clock rate on the MTCLK input is expected to be 16.384MHz. When BTX2M for all four DS1s is set to logic 0, the clock rate on the MTCLK input is expected to be 12.352MHz.

BTX2RAIL:

The BTX2RAIL bit selects whether the backplane transmit data signal presented to the transmitter on the multifunction inputs BTPCM/BTDP[x] and BTSIG/BTDN[x] are in either dual-rail or single-rail format. When BTX2RAIL is set to logic 1, the multifunction pins become the BTDP[x] and BTDN[x] dual-rail inputs, which bypass the XBAS and input directly into the jitter attenuator. It is expected that the framing bits be already inserted into the dual-rail streams before they are input on BTDP[x] and BTDN[x]. When BTX2RAIL is set to logic 0, the multifunction pins become the BTPCM[x] and BTSIG[x] digital inputs. The dual-rail mode works correctly only when the backplane data rate is set to 1.544 MHz.

BTXSFP:

The BTXSFP bit selects the type of backplane frame alignment signal presented to the transmitter BTFP[x] input. When BTXSFP is set to logic 1, a pulse on the BTFP[x] indicates the first framing bit of the 12 frame SF or the 24 frame ESF (depending on the framing format selected in the XBAS). BTFP[x] must toggle every superframe or extended superframe. When BTXSFP is set to logic 0, a pulse on the BTFP[x] indicates each framing bit. If the signaling aligner is used to ensure signaling bit integrity while XBAS generates an arbitrary superframe alignment between the backplane and the transmit DS-1 stream (i.e. SIGAEN is logic 1 and TXSIGA is logic 1 in register 06H), then BTXSFP must be set to logic 0. If the superframe alignment of the backplane is to be enforced on the transmit DS-1 stream, the BTXSFP bit must be set to logic 1. In this case the signaling aligner is unnecessary.

Upon reset of the TQUAD, these bits are cleared to zero.

Registers 006H, 086H, 106H and 186H: Transmit Framing and Bypass Options

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SIGAEN	0
Bit 4	R/W	TXSIGA	0
Bit 3	R/W	FDIS	0
Bit 2	R/W	FBITBYP	0
Bit 1	R/W	CRCBYP	0
Bit 0	R/W	FDLBYP	0

These registers allow software to configure the bypass options of the transmitter, the use and location of the Signaling Alignment block, and controls the global transmit framing disable.

SIGAEN:

The SIGAEN bit enables the operation of the signaling aligner (SIGA) to ensure superframe alignment between the backplane and either the receive or transmit DS-1 streams. When set to logic 1, the SIGA is inserted into the signaling bit data path either after the SIGX or before the XBAS , as selected by the TXSIGA register bit. When the signaling aligner is used, the backplane frame alignment indication must also be changed to indicate superframe alignment for either the receive or transmit backplane, based on the value of TXSIGA. When SIGAEN is set to logic 0, the SIGA is removed from the circuit and the TXSIGA bit is ignored.

TXSIGA:

The TXSIGA bit selects the location of the signaling aligner. When set to logic 1, the SIGA is inserted into the signaling bit data path before the XBAS. When set to logic 0, the SIGA is inserted into the data path after the SIGX.

FDIS:

The FDIS bit allows the framing generation through the XBAS to be disabled and the transmit data to pass through the XBAS unchanged. When FDIS is set to logic 1, XBAS is disabled from generating framing. When FDIS is set to

logic 0, XBAS is enabled to generate and insert the framing into the transmit data.

FBITBYP:

The FBITBYP bit allows the frame synchronization bit in the input data stream, BTPCM[x], to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FBITBYP is set to logic 1, the input frame synchronization bit is re-inserted into the output data stream. When FBITBYP is set to logic 0, the XBAS is allowed to generate the output frame synchronization bits.

CRCBYP:

The CRCBYP bit allows the framing bit corresponding to the CRC-6 bit position in the input data stream, BTPCM[x], to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When CRCBYP is set to logic 1, the input CRC-6 bit is re-inserted into the output data stream. When CRCBYP is set to logic 0, the XBAS is allowed to generate the output CRC-6 bits.

FDLBYP:

The FDLBYP bit allows the framing bit corresponding to the facility data link bit position in the input data stream, BTPCM[x], to bypass the generation through the XBAS and be re-inserted into the appropriate position in the digital output stream. When FDLBYP is set to logic 1, the input FDL bit is re-inserted into the output data stream. When FDLBYP is set to logic 0, the XBAS is allowed to generate the output FDL bit.

Upon reset of the TQUAD, these bits are cleared to zero.

Registers 007H, 087H, 107H and 187H: Transmit Timing Options

Bit	Type	Function	Default
Bit 7	R/W	HSBPSEL	0
Bit 6	R/W	XCLKSEL	0
Bit 5	R/W	OCLKSEL1	0
Bit 4	R/W	OCLKSEL0	0
Bit 3	R/W	PLLREF1	0
Bit 2	R/W	PLLREF0	0
Bit 1	R/W	TCLKISEL	0
Bit 0	R/W	SMCLKO	0

These registers allow software to configure the options of the transmit timing section.

HSBPSEL:

The HSBPSEL bit selects the source of the high-speed clock used in the ELST, SIGX, TPSC, and RPSC blocks. This allows the TQUAD to interface to higher rate backplanes (>2.048MHz, externally gapped, or 2.048MHz, internally gapped). Note, however, that the externally gapped instantaneous backplane clock frequency must not exceed 3.0MHz. When HSBPSEL is set to logic 1, the XCLK input signal is divided by 2 and used as the high-speed clock to these blocks. XCLK must be driven with 37.056MHz. When HSBPSEL is set to logic 0, the high-speed clock is driven with the internal 12.352MHz clock source selected by the XCLKSEL bit.

XCLKSEL:

The XCLKSEL bit selects the source of the high-speed clock used in the CDRC, FRMR, and PMON blocks. When XCLKSEL is set to logic 1, the XCLK input signal is used as the high-speed clock to these blocks. XCLK must be driven with 12.352MHz. When XCLKSEL is set to logic 0, the high-speed clock is driven with XCLK input signal is divided by 3. XCLK must be driven with 37.056MHz.

OCLKSEL1, OCLKSEL0:

The OCLKSEL[1:0] bits select the source of the Digital Jitter Attenuator FIFO output clock signal. When OCLKSEL1 is set to logic 1, the DJAT FIFO output

clock is driven with the input data clock driving the DJAT ICLK input. In this mode the jitter attenuation is disabled and the input clock must be jitter-free. When OCLKSEL1 is set to logic 0, the DJAT FIFO output clock is driven with either the TCLKI[x] input clock or an internal smooth 1.544MHz clock, as selected by the OCLKSEL0 bit. When OCLKSEL0 is set to logic 1, the DJAT FIFO output clock is driven with the TCLKI[x] input clock. When OCLKSEL0 is set to logic 0, the DJAT FIFO output clock is driven with the internal smooth 1.544MHz clock selected by the TCLKISEL and SMCLKO bits.

PLLREF1, PLLREF0:

The PLLREF[1:0] bits select the source of the Digital Jitter Attenuator phase locked loop reference signal as follows:

Table 2 -

PLLREF1	PLLREF0	Source of PLL Reference
0	0	Transmit clock used by XBAS (either the 1.544MHz BTCLK[x], the gapped clock derived from the 2.048MHz BTCLK[x], or the 1.544MHz RCLKO[x], as selected by BTXCLK and BTX2M)
0	1	BTCLK[x] input
1	0	RCLKO[x] output
1	1	TCLKI[x] input

TCLKISEL,SMCLKO:

The TCLKISEL and SMCLKO bits select the source of the internal smooth 1.544MHz and 12.352MHz output clock signals. When TCLKISEL and SMCLKO are set to logic 0, the internal 1.544MHz and 12.352MHz clock signals are driven by the smooth 1.544MHz and 12.352MHz clock sources generated by DJAT. When TCLKISEL is set to logic 0 and SMCLKO is set to logic 1, the internal 1.544MHz clock signal is driven by the TCLKI[x] input signal divided by 8, and the internal 12.352MHz clock signal is driven by the TCLKI[x] input signal. When TCLKISEL and SMCLKO are set to logic 1, the internal 1.544MHz clock signal is driven by the XCLK input signal divided by 8, and the internal 12.352MHz clock signal is driven by the XCLK input signal. The combination of TCLKISEL set to logic 1 and SMCLKO set to logic 0 should not be used.

The following table illustrates the required bit settings for these various clock sources to affect the transmitted data:

Table 3 -

Input Transmit Data	Bit Settings	XCLK Freq	Affect on Output Transmit Data
Backplane transmit data timed to 1.544 MHz BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =X TCLKISEL =0 SMCLKO =0 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	37.056MHz	Jitter attenuated. TCLKO[x] is a smooth 1.544MHz. TCLKO[x] referenced to BTCLK[x]. TCLKO[x] referenced to RCLKO[x]. TCLKO[x] referenced to TCLKI[x].

Input Transmit Data	Bit Settings	XCLK Freq	Affect on Output Transmit Data
Backplane transmit data timed to 2.048MHz BTCLK[x]. Internal transmit clock is "gapped".	HSBPSEL =1 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =0 TCLKISEL =0 SMCLKO =0 PLLREF1 =0 PLLREF0 =1 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	37.056MHz	Jitter attenuated. TCLKO[x] is a smooth 1.544MHz. TCLKO[x] referenced to internal "gapped" transmit clock. TCLKO[x] referenced to 2.048MHz BTCLK[x]. TCLKO[x] referenced to RCLKO[x]. TCLKO[x] referenced to TCLKI[x].

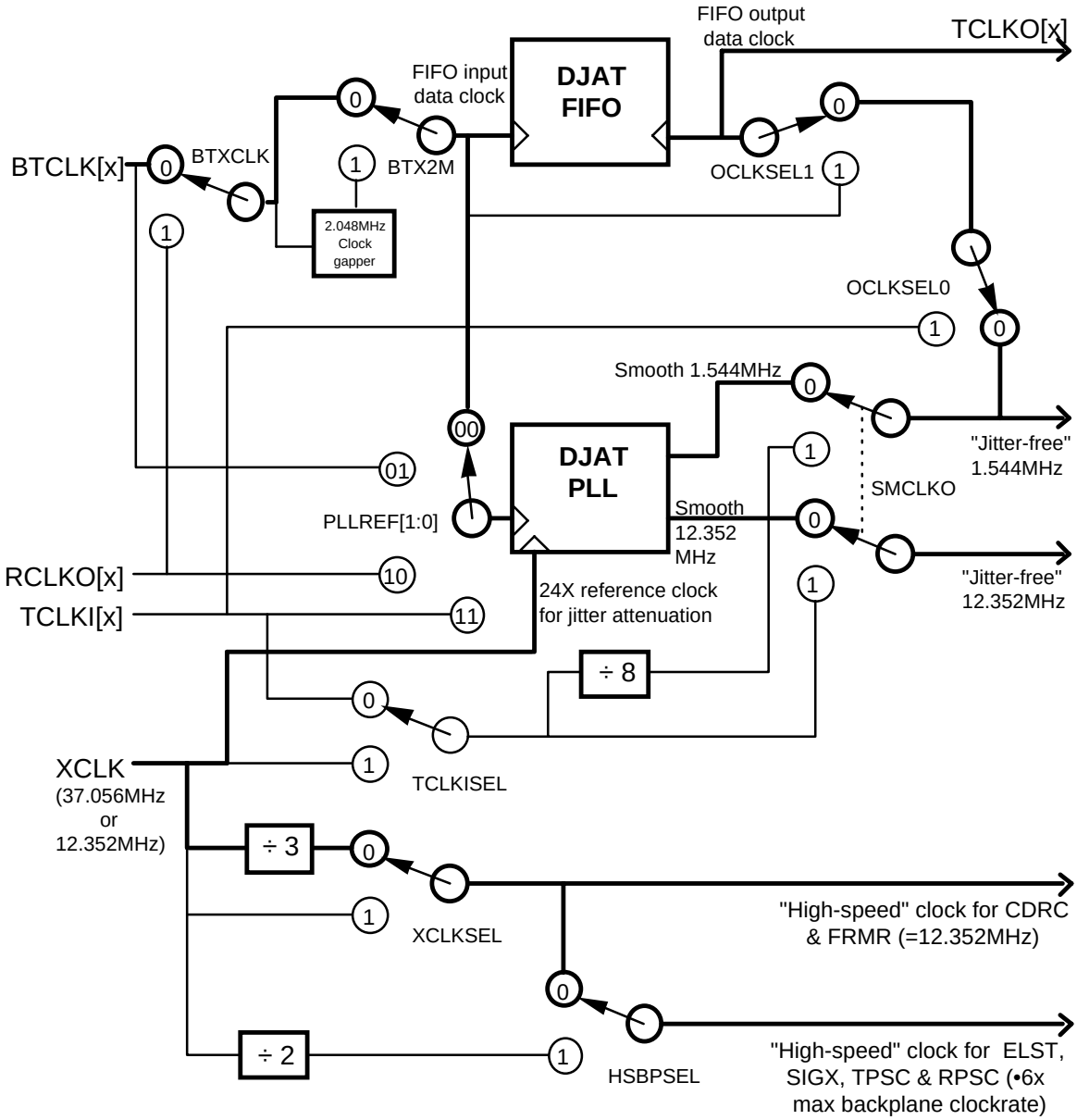
Input Transmit Data	Bit Settings	XCLK Freq	Affect on Output Transmit Data
Backplane transmit data timed to >2.048MHz backplane clock. BTCLK[x] is externally "gapped".	HSBPSEL =1 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =0 PLLREF0 =X TCLKISEL =0 SMCLKO =0 PLLREF1 =1 PLLREF0 =0 PLLREF1 =1 PLLREF0 =1	37.056MHz	Jitter attenuated. TCLKO[x] is a smooth 1.544MHz. TCLKO[x] referenced to externally "gapped" transmit clock. TCLKO[x] referenced to RCLKO[x]. TCLKO[x] referenced to TCLKI[x].
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =1 OCLKSEL0 =X PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =0 XCLKSEL =1 TCLKISEL =1 SMCLKO =1	37.056MHz 12.352MHz	No jitter attenuation. TCLKO[x] is equal to internal transmit clock, either BTCLK[x], gapped BTCLK[x], or RCLKO[x]. Same as above.

Input Transmit Data	Bit Settings	XCLK Freq	Affect on Output Transmit Data
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =1 PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =0 XCLKSEL =1 TCLKISEL =1 SMCLKO =1	37.056MHz 12.352MHz	No jitter attenuation. TCLKO[x] is equal to TCLKI[x] (useful for higher rate MUX applications). Same as above.
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =0 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =X PLLREF0 =X TCLKISEL =0 SMCLKO =1 XCLKSEL =1	37.056MHz 12.352MHz	TCLKI[x] is a jitter-free 12.352MHz clock. TCLKO[x] is equal to TCLKI[x]÷8.[1] Same as above.
Backplane transmit data timed to BTCLK[x].	HSBPSEL =0 XCLKSEL =1 OCLKSEL1 =0 OCLKSEL0 =0 PLLREF1 =X PLLREF0 =X TCLKISEL =1 SMCLKO =1	jitter-free 12.352MHz	XCLK is a jitter-free 12.352MHz clock. TCLKO[x] is equal to XCLK÷8.[1]

Upon reset of the TQUAD, these bits are cleared to zero, selecting digital jitter attenuation with TCLKO[x] referenced to the backplane transmit clock, BTCLK[x]. Figure 7 illustrates the various bit setting options, with the reset condition highlighted.

1. The register bits SYNC, CENT, and LIMIT in the DJAT Configuration Register must be set to logic 0 in these configurations.

Figure 7 - Transmit Timing Options



This diagram illustrates clock configurations for when the RCLKOSEL bit is set to logic 0. See the Operations - Receiver Jitter Attenuation section for DJAT clock configurations when RCLKOSEL is set to logic 1.

Registers 008H, 088H, 108H and 188H: Interrupt Source #1

Bit	Type	Function	Default
Bit 7	R	PMON	0
Bit 6	R	IBCD	0
Bit 5	R	FRMR	0
Bit 4	R	PDVD	0
Bit 3	R	ELST	0
Bit 2	R	RFDL	0
Bit 1	R	RBOC	0
Bit 0	R	ALMI	0

These registers allow software to determine the block which produced the interrupt on the INTB output pin.

Reading this register does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 009H, 089H, 109H and 189H: Interrupt Source #2

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R	PRTY	0
Bit 5	R	DJAT	0
Bit 4	R	XPDE	0
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	XFDL	0
Bit 0	R	CDRC	0

These registers allow software to determine the block which produced the interrupt on the INTB output pin.

The PRTY bit indicates a pending parity error indication needs servicing in the Backplane Parity Configuration and Status register.

Reading these registers does not remove the interrupt indication; the corresponding block's interrupt status register must be read to remove the interrupt indication.

Registers 00AH, 08AH, 10AH and 18AH: Master Diagnostics

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	PAYLB	0
Bit 4	R/W	LINELB	0
Bit 3		Unused	X
Bit 2	R/W	DDLB	0
Bit 1	R/W	TXMFP	0
Bit 0	R/W	TXDIS	0

These registers allow software to enable the diagnostic mode of each framer.

PAYLB:

The PAYLB bit selects the payload loopback mode, where the received data output from the ELST is internally connected to the transmit data input of the XBAS. The data read out of ELST is timed to the transmitter clock, and the transmit frame alignment is used to synchronize the output frame alignment of ELST. During payload loopback, the data output on BRPCM[x] is forced to logic 1. When PAYLB is set to logic 1, the payload loopback mode is enabled. When PAYLD is set to logic 0, the loopback mode is disabled.

LINELB:

The LINELB bit selects the line loopback mode, where the recovered positive and negative pulse outputs from the CDRC block are internally connected to the digital inputs of the DJAT. When LINELB is set to logic 1, the line loopback mode is enabled. When LINELB is set to logic 0, the line loopback mode is disabled. Note that when line loopback is enabled, the contents of the DJAT Reference Clock Divisor and Output Clock Divisor registers must be reprogrammed to decimal 47 to correctly attenuate the jitter on the 1.544 MHz receive clock and the Timing Options Register settings should be reviewed to ensure the options are such that data will pass error-free and "jitter"-free through DJAT (typically, the default setting, 00H, for register 7 will be appropriate for line loopback).

DDLB:

The DDLB bit selects the diagnostic digital loopback mode, where the digital positive and negative RZ pulse outputs from DJAT are internally connected to the receive positive and negative pulse inputs of CDRC (the RUNI and TUNI bits in the Receive DS1 Interface Configuration and the Transmit DS1 Interface Configuration registers respectively must be set to logic 0). When DDLB is set to logic 1, the diagnostic digital loopback mode is enabled. When DDLB is set to logic 0, the diagnostic digital loopback mode is disabled.

TXMFP:

The TXMFP bit introduces a mimic framing pattern in the digital output of the basic transmitter by forcing a copy of the current framing bit into bit location 1 of the frame, thereby creating a mimic pattern in the bit position immediately following the correct framing bit. When TXMFP is set to logic 1, the mimic framing pattern is generated. When TXMFP is set to logic 0, no mimic pattern is generated.

TXDIS:

The TXDIS bit provides a method of suppressing the output of the basic transmitter. When TXDIS is set to logic 1, the digital output of XBAS is disabled by forcing it to logic 0. When TXDIS is set to logic 0, the digital output of XBAS is not suppressed.

Upon reset of the TQUAD, these register bits are cleared to zero.

Register 00BH: TQUAD Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	A_TM[8]	X
Bit 5	R/W	A_TM[7]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select TQUAD test features. All bits, except for PMCTST and A_TM[8:7] are reset to zero by a hardware reset of the TQUAD; a software reset of the TQUAD does not affect the state of the bits in this register. Refer to the Test Features Description section for more information.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[7]:

The state of the A_TM[7] bit internally replaces the input address line A[7] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the TQUAD for PMC's manufacturing tests. When PMCTST is set to logic 1, the TQUAD microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output

enable for the data bus. While the DBCTRL bit is set, holding the CSB pin high causes the TQUAD to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the TQUAD for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in the "Test Features" section).

HIZIO,HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the TQUAD . While the HIZIO bit is a logic 1, all output pins of the TQUAD except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

Register 00CH: TQUAD Revision/Chip ID/Global PMON Update

Bit	Type	Function	Default
Bit 7	R	TYPE[2]	0
Bit 6	R	TYPE[1]	0
Bit 5	R	TYPE[0]	1
Bit 4	R	ID[4]	0
Bit 3	R	ID[3]	0
Bit 2	R	ID[2]	0
Bit 1	R	ID[1]	0
Bit 0	R	ID[0]	1

The version identification bits, ID[4:0], are set to a fixed value representing the version number of the TQUAD.

The chip identification bit, TYPE, is set to logic 1 representing the TQUAD.

Writing to this register causes all performance monitor counters to be updated simultaneously.

Registers 00DH, 08DH, 10DH and 18DH: Framer Reset

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R/W	RESET	0

The RESET bit implements a software reset. If the RESET bit is a logic 1, the individual framer is held in reset. This bit is not self-clearing; therefore, a logic 0 must be written to bring the framer out of reset. Holding the framer in a reset state effectively puts it into a low power, stand-by mode. A hardware reset clears the RESET bit, thus deasserting the software reset.

Registers 00EH, 08EH, 10EH and 18EH: Phase Status Word (LSB)

Bit	Type	Function	Default
Bit 7	R	PSB[7]	X
Bit 6	R	PSB[6]	X
Bit 5	R	PSB[5]	X
Bit 4	R	PSB[4]	X
Bit 3	R	PSB[3]	X
Bit 2	R	PSB[2]	X
Bit 1	R	PSB[1]	X
Bit 0	R	PSB[0]	X

These registers contain the least significant byte, PSB[7:0], of the 9-bit phase status word. The 9-bit phase status word indicates the relative phase difference between the received DS-1 line timing (available on RCLKO[x]) and a system timing which uses either a 2.048MHz backplane (input on BRCLK, with BRX2M=1) or a 1.544MHz backplane (input on BRCLK, with BRX2M=0). By utilizing the value of the phase status word, the system timing can be locked to the receive line timing via an external software controlled phase-locked-loop.

The least significant 8 bits contained in this register indicate a count value (either 0-255 for BRX2M=1 or 0-192 for BRX2M=0) of the number of system backplane clock cycles between successive 125µs frame pulses. The most significant 5 bits (PSB[7:3]) represent a channel number (0-31 for BRX2M=1 or 0-23 for BRX2M=0) and the least significant 3 bits (PSB[2:0]) represent the bit number within the channel (0-7). The count value corresponds to the location within the system frame where the receive line-timed frame pulse occurred. If the received line clock frequency is higher on average than the system clock frequency, the phase status word value will be seen to decrease during successive register reads. If the received line clock frequency is lower on average than the system clock frequency, the phase status word value will be seen to increase during successive register reads.

The 9th bit of the Phase Status Word indicates the "frame count" and will toggle when two successive 8-bit counter values straddle a frame boundary. The PSB[8] bit will toggle when the bit and channel count indicated by PSB[7:0] exceeds channel 31, bit 7 (when BRX2M=1; or channel 23, bit 7 when BRX2M=0) or the count goes below channel 0, bit 0. This is determined by comparing the PSB[7:5] bits of the current phase status word value to those of

the previous word value; PSB[8] is toggled only under the following conditions (all other bit value transitions leave PSB[8] unchanged):

Table 4 -

Previous PSB[7:5]	Current PSB[7:5]	Affect on PSB[8]
000	11X	toggle
000	1X1	toggle
11X	000	toggle
1X1	000	toggle

The contents of the Phase Status Word registers are internally updated on each receive line data frame pulse; a write to either Phase Status Word register address must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. write to either Phase Status Word register
2. read Phase Status Word MSB
3. read Phase Status Word LSB

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

Registers 00FH, 08FH, 10FH and 18FH: Phase Status Word (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	PSB[8]	X

These registers contain the most significant bit of the 9-bit phase status word.

The PSB[8] bit toggles when the bit and channel count (from the Phase Status Word LSB register) exceeds channel 31, bit 7 (channel 23, bit 7 when BRX2M=0) or goes below channel 0, bit 0.

The contents of the Phase Status Word registers are internally updated on each receive line data frame pulse; a write to either Phase Status Word register must be performed to freeze the contents before this register and the Phase Status Word (MSB) register can be read. The correct sequence for reading the contents of the Phase Status Word are:

1. write to either Phase Status Word register

2. read Phase Status Word MSB

3. read Phase Status Word LSB

This write-before-read is analogous to the latching of performance monitor counter values in PMON, and is required to ensure that the phase status word value remains valid during the µP read. It is important to read the MSB register before the LSB register because, once the Phase Status Word (LSB) register has been read, the phase status word counter is unfrozen and the contents may change immediately.

Registers 010H, 090H, 110H and 190H: CDRC Configuration

Bit	Type	Function	Default
Bit 7	R/W	AMI	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	ALGSEL	0
Bit 1		Unused	X
Bit 0		Unused	X

AMI:

The alternate mark inversion (AMI) bit specifies the line code of the incoming DS1 signal. A logic 1 selects AMI line code; a logic 0 selects B8ZS line code.

ALGSEL:

The Algorithm Select (ALGSEL) bit specifies the algorithm used by the DPLL for clock and data recovery. The choice of algorithm determines the high frequency input jitter tolerance of the CDRC. When ALGSEL is set to logic 1, the CDRC jitter tolerance is increased to approach 0.5UIpp for jitter frequencies above 20KHz. When ALGSEL is set to logic 0, the jitter tolerance is increased for frequencies below 20KHz (i.e. the tolerance is improved by 20% over that of ALGSEL=1 at these frequencies), but the tolerance approaches 0.4UIpp at the higher frequencies.

Registers 011H, 091H, 111H and 191H: CDRC Interrupt Enable

Bit	Type	Function	Default
Bit 7	R/W	LCVE	0
Bit 6	R/W	LOSE	0
Bit 5	R/W	B8ZSE	0
Bit 4	R/W	Z8DE	0
Bit 3	R/W	Z16DE	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The bit positions LCVE, LOSE, B8ZSE, Z8DE and Z16DE (bits 7 to 3) of this register are interrupt enables to select which of the status events (Line Code Violation , Loss Of Signal, B8ZS Pattern, 8 Zeros, or 16 Zeros), either singly or in combination, are enabled to generate an interrupt on the microprocessor INTB pin when they are detected. A logic 1 bit in the corresponding bit position enables the detection of these signals to generate an interrupt; a logic 0 bit in the corresponding bit position disables that signal from generating an interrupt.

When the TQUAD is reset, LCVE, LOSE, B8ZSE, Z8DE, and Z16DE are set to logic 0, disabling these events from generating an interrupt.

Registers 012H, 092H, 112H and 192H: CDRC Interrupt Status

Bit	Type	Function	Default
Bit 7	R	LCVI	0
Bit 6	R	LOSI	0
Bit 5	R	B8ZSI	0
Bit 4	R	Z8DI	0
Bit 3	R	Z16DI	0
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	LOS	0

The bit positions LCVI, LOSI, B8ZSI, Z8DI and Z16DI (bits 7 to 3) of this register indicate which of the status events generated an interrupt. A logic 1 in these bit positions indicate that the corresponding event was detected and generated an interrupt; a logic 0 in these bit positions indicate that no corresponding event has been detected. The bit positions LCVI, B8ZSI, Z8DI and Z16DI are set on the assertion of the corresponding event. LOSI is set on any change of state of the LOS alarm. Bits LCVI, LOSI, B8ZSI, Z8DI and Z16DI are cleared by reading this register. The current state of the LOS alarm can be determined by reading bit 0 of this register.

Registers 013H, 093H, 113H and 193H: Alternate Loss of Signal Status

Bit	Type	Function	Default
Bit 7	R/W	ALTLOSE	0
Bit 6	R	ALTLOSI	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	ALTLOS	X

The alternate loss of signal status provides a more stringent criteria for the deassertion of the alarm than the LOS indication in the CDRC Interrupt Status register.

ALTLOSE:

If the ALTLOSE bit is a logic 1, an interrupt is generated when the ALTLOS status bit changes state.

ALTLOSI:

The LOSI bit is set high when the ALTLOS status bit changes state. It is cleared when this register is read.

ALTLOS:

The ALTLOS bit is asserted after 176 consecutive bit periods of the absence of pulses on both the positive and negative line pulse inputs. The ALTLOS bit is deasserted only after pulse density requirements have been met. Specifically, there must be N ones in each and every time window of 8(N+1) data bits (where N can equal 1 through 23).

Registers 018H, 098H, 118H and 198H: DJAT Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	OVRI	0
Bit 0	R	UNDI	0

These registers contain the indication of the DJAT FIFO status.

OVRI:

The OVRI bit is asserted when an attempt is made to write data into the FIFO when the FIFO is already full. When UNDI is a logic 1, an overrun event has occurred.

UNDI:

The UNDI bit is asserted when an attempt is made to read data from the FIFO when the FIFO is already empty. When UNDI is a logic 1, an underrun event has occurred.

Registers 19H, 099H, 119H and 199H: DJAT Reference Clock Divisor (N1) Control

Bit	Type	Function	Default
Bit 7	R/W	N1[7]	0
Bit 6	R/W	N1[6]	0
Bit 5	R/W	N1[5]	1
Bit 4	R/W	N1[4]	0
Bit 3	R/W	N1[3]	1
Bit 2	R/W	N1[2]	1
Bit 1	R/W	N1[1]	1
Bit 0	R/W	N1[0]	1

These registers define an 8-bit binary number, N1, which is one less than the magnitude of the divisor used to scale down the DJAT PLL reference clock input. The REF divisor magnitude, (N1+1), is the ratio between the frequency of REF input and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit in the DJAT Configuration register is high, will also reset the FIFO.

Upon reset of the TQUAD, the default value of N1 is set to decimal 47 (2FH).

Registers 01AH, 09AH, 11AH and 19AH: DJAT Output Clock Divisor (N2) Control

Bit	Type	Function	Default
Bit 7	R/W	N2[7]	0
Bit 6	R/W	N2[6]	0
Bit 5	R/W	N2[5]	1
Bit 4	R/W	N2[4]	0
Bit 3	R/W	N2[3]	1
Bit 2	R/W	N2[2]	1
Bit 1	R/W	N2[1]	1
Bit 0	R/W	N2[0]	1

These registers define an 8-bit binary number, N2, which is one less than the magnitude of the divisor used to scale down the DJAT smooth output clock signal. The output clock divisor magnitude, (N2+1), is the ratio between the frequency of the smooth output clock and the frequency applied to the phase discriminator input.

Writing to this register will reset the PLL and, if the SYNC bit is high, will also reset the FIFO.

Upon reset of the TQUAD, the default value of N2 is set to decimal 47 (2FH).

Registers 01BH, 09BH, 11BH and 19BH: DJAT Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	Reserved	1
Bit 4	R/W	CENT	0
Bit 3	R/W	UNDE	0
Bit 2	R/W	OVRE	0
Bit 1	R/W	SYNC	1
Bit 0	R/W	LIMIT	1

These registers control the operation of the DJAT FIFO read and write pointers and controls the generation of interrupt by the FIFO status.

CENT:

The CENT bit allows the FIFO to self-center its read pointer, maintaining the pointer at least 4 UI away from the FIFO being empty or full. When CENT is set to logic 1, the FIFO is enabled to self-center for the next 384 transmit data bit period, and for the first 384 bit periods following an overrun or underrun event. If an EMPTY or FULL alarm occurs during this 384 UI period, then the period will be extended by the number of UI that the EMPTY or FULL alarm persists. During the EMPTY or FULL alarm conditions, data is lost. When CENT is set to logic 0, the self-centering function is disabled, allowing the data to pass through uncorrupted during EMPTY or FULL alarm conditions. The CENT bit can only be set to logic 1 if the SYNC bit is set to logic 0.

OVRE,UNDE:

The OVRE and UNDE bits control the generation of an interrupt on the microprocessor INTB pin when a FIFO error event occurs. When OVRE or UNDE is set to logic 1, an overrun event or underrun event, respectively, is allowed to generate an interrupt on the INTB pin. When OVRE or UNDE is set to logic 0, the FIFO error events are disabled from generating an interrupt.

SYNC:

The SYNC bit enables the PLL to synchronize the phase delay between the FIFO input and output data to the phase delay between reference clock input

and smooth output clock at the PLL. For example, if the PLL is operating so that the smooth output clock lags the reference clock by 24 UI, then the synchronization pulses that the PLL sends to the FIFO will force its output data to lag its input data by 24 UI. When using the 2Mbit/s transmit backplane option, the SYNC bit must be set to logic 0.

LIMIT:

The LIMIT bit enables the PLL to limit the jitter attenuation by enabling the FIFO to increase or decrease the frequency of the smooth output clock whenever the FIFO is within one unit interval (UI) of overflowing or underflowing. This limiting of jitter ensures that no data is lost during high phase shift conditions. When LIMIT is set to logic 1, the PLL jitter attenuation is limited. When LIMIT is set to logic 0, the PLL is allowed to operate normally.

Upon reset of the TQUAD, the LIMIT and SYNC bits are set to logic 1, and the OVRE, UNDE, and CENT bits are set to logic 0.

Registers 01CH, 09CH, 11CH and 19CH: ELST Configuration

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IR	0
Bit 0	R/W	OR	0

These registers control the format of the expected input frame to the ELST and the format of the generated output frame from the ELST.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

IR:

The IR bit selects the input frame format. The IR bit must be cleared to logic 0 to properly handle the T1 frame format being input into the ELST. SETTING IR TO LOGIC 1 IS A RESERVED SETTING AND SHOULD NOT BE USED.

OR:

The OR bit selects the output frame format. The OR bit must be cleared to properly generate the T1 frame format output from the ELST. SETTING OR TO LOGIC 1 IS A RESERVED SETTING AND SHOULD NOT BE USED.

Upon reset of the TQUAD, these bits are set to logic 0.

Registers 01DH, 09DH, 11DH and 19DH: ELST Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	SLIPE	0
Bit 1	R	SLIPD	0
Bit 0	R	SLIPI	0

SLIPE:

The SLIPE bit position enables generation of an interrupt on the microprocessor INTB pin when a slip event occurs.

SLIPI:

The SLIPI bit indicates whether a slip event has occurred since the last read of the Enable/Status register. SLIPI is a logic 1 if a slip has occurred; SLIPI is a logic 0 is no slip has occurred. The SLIPI bit is cleared after the register is read.

SLIPD:

The SLIPD bit indicates the direction of the last slip when SLIPI is a logic 1. If a slip has occurred and the SLIPD bit is a logic 1 then the slip was due to the frame buffer becoming full. If a slip has occurred and the SLIPD bit is a logic 0 then the slip was due to the frame buffer becoming empty.

Upon reset of the TQUAD, SLIPE is set to logic 0, disabling generation of an interrupt.

Registers 01EH, 09EH, 11EH and 19EH: ELST Trouble Code

Bit	Type	Function	Default
Bit 7	R/W	D7	1
Bit 6	R/W	D6	1
Bit 5	R/W	D5	1
Bit 4	R/W	D4	1
Bit 3	R/W	D3	1
Bit 2	R/W	D2	1
Bit 1	R/W	D1	1
Bit 0	R/W	D0	1

These registers allow the Trouble Code, transmitted in place of channel data when the framer is out of frame, to be programmed to any 8-bit value. A common requirement during a out of frame condition is to insert all ones in the channel data, therefore, the Trouble Code register is set to all ones when the TQUAD is reset. The code is transmitted from MSB (D7) to LSB (D0).

The writing of the trouble code pattern into the register is asynchronous with respect to the clocks within the framer. One channel of trouble code data will always be corrupted if the register is written while the receiver is out of frame.

Registers 020H, 0A0H, 120H and 1A0H: FRMR Configuration

Bit	Type	Function	Default
Bit 7	R/W	M2O[1]	0
Bit 6	R/W	M2O[0]	0
Bit 5	R/W	ESFFA	0
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1		Unused	X
Bit 0		Unused	X

These registers select the framing format and the frame loss criteria used by the FRMR.

M2O[1:0]:

The M2O[1:0] bits select the ratio of errored to total framing bits before declaring out of frame in SF, SLC®96, and ESF framing formats. A logic 00 selects 2 of 4 framing bits in error; a logic 01 selects 2 of 5 bits in error; a logic 10 selects 2 of 6 bits in error. In T1DM framing format, the ratio of errored to total framing bits before declaring out of frame is always 4 out of 12. A logic 11 in the M2O[1:0] bits is reserved and should not be used.

ESFFA:

The ESFFA bit selects one of two framing algorithms for ESF frame search in the presence of mimic framing patterns in the incoming data. A logic 0 selects the ESF algorithm where the FRMR does not declare inframe while more than one framing bit candidate is following the framing pattern in the incoming data. A logic 1 selects the ESF algorithm where a CRC-6 calculation is performed on each framing bit candidate, and is compared against the CRC bits associated with the framing bit candidate to determine the most likely framing bit position.

ESF:

The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either standard superframe, T1DM, or SLC®96

framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 or 11 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format. When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the facility data link data. A logic 00 in these bits enable the FRMR to receive FDL data at the full 4 kHz rate from every odd frame. A logic 01 in these bits enable the FRMR to receive FDL data at a 2 kHz rate from frames 3,7,11,15,19,23. A logic 10 in these bits enable the FRMR to receive FDL data at a 2 kHz rate from frames 1,5,9,13,17,21. Logic value 11 is reserved and should not be used.

The valid combinations of the ESFFA, ESF, FMS1, and FMS0 bits are summarized in the table below:

Table 5 -

ESF	FMS1	FMS0	Mode
0	0	0	Select SF framing format
0	0	1	Select T1DM framing format
0	1	0	Select SLC96 framing format
0	1	1	Select T1DM framing format
1	0	0	Select ESF framing format & 4 kHz FDL Data Rate
1	0	1	Select ESF framing format & 2 kHz FDL Data Rate using frames 3,7,11,15,19,23.
1	1	0	Select ESF framing format & 2 kHz FDL Data Rate using frames 1,5,9,13,17,21
1	1	1	RESERVED

Registers 021H, 0A1H, 121H and 1A1H: FRMR Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	ACCEL	0
Bit 5	R/W	COFAE	0
Bit 4	R/W	FERE	0
Bit 3	R/W	BEEE	0
Bit 2	R/W	SFEE	0
Bit 1	R/W	MFPE	0
Bit 0	R/W	INFRE	0

These registers select which of the MFP, COFA, FER, BEE, SFE, or INFR events generates an interrupt on the microprocessor INTB pin when their state changes or their event condition is detected.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

COFAE:

The COFAE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the new alignment differs from the previous alignment. When COFAE is set to logic 1, the declaration of a change of frame alignment is allowed to generate an interrupt. When COFAE is set to logic 0, a change in the frame alignment does not generate an interrupt.

FERE:

The FERE bit enables the generation of an interrupt when a framing bit error has been detected. When FERE is set to logic 1, the detection of a framing bit error is allowed to generate an interrupt. When FERE is set to logic 0, any error in the framing bits does not generate an interrupt.

BEEE:

The BEEE bit enables the generation of an interrupt when a bit error event has been detected. A bit error event is defined as framing bit errors for SF

formatted data, CRC-6 mismatch errors for ESF formatted data, Ft bit errors for SLC®96 formatted data, and either framing bit errors or sync word errors for T1DM formatted data. When BEEE is set to logic 1, the detection of a bit error event is allowed to generate an interrupt. When BEEE is set to logic 0, bit error events are disabled from generating an interrupt.

SFEE:

The SFEE bit enables the generation of an interrupt when a severely errored framing event has been detected. A severely errored framing event is defined as 2 or more framing bit errors during the current superframe for SF, ESF, or SLC®96 formatted data, and 2 or more framing bit errors or sync word errors during the current superframe for T1DM formatted data. When SFEE is set to logic 1, the detection of a severely errored framing event is allowed to generate an interrupt. When SFEE is set to logic 0, severely errored framing events are disabled from generating an interrupt.

MFPE:

The MFPE bit enables the generation of an interrupt when the frame find circuitry detects the presence of framing bit mimics. The occurrence of a mimic is defined as more than one framing bit candidate following the frame alignment pattern. When MFPE is set to logic 1, the assertion or deassertion of the detection of a mimic is allowed to generate an interrupt. When MFPE is set to logic 0, the detection of a mimic framing pattern is disabled from generating an interrupt.

INFRE:

The INFRE bit enables the generation of an interrupt when the frame find circuitry determines that frame alignment has been achieved and that the framer is now "inframe". When INFRE is set to logic 1, the assertion or deassertion of the "inframe" state is allowed to generate an interrupt. When INFRE is set to logic 0, a change in the "inframe" state is disabled from generating an interrupt.

Upon reset of the TQUAD, these bits are set to logic 0, disabling the generation of interrupts.

Registers 022H, 0A2H, 122H and 1A2H: FRMR Interrupt Status

Bit	Type	Function	Default
Bit 7	R	COFAI	0
Bit 6	R	FERI	0
Bit 5	R	BEEI	0
Bit 4	R	SFEI	0
Bit 3	R	MFPI	0
Bit 2	R	INFRI	0
Bit 1	R	MFP	0
Bit 0	R	INFR	0

These registers indicate whether a change of frame alignment, a framing bit error, a bit error event, or a severely errored framing event generated an interrupt. These registers also indicate whether a mimic framing pattern was detected or whether there was a change in the "inframe" state of the frame circuitry.

COFAI,FERI,BEEI,SFEI:

A logic 1 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the occurrence of the corresponding event generated an interrupt; a logic 0 in the status bit positions COFAI, FERI, BEEI, and SFEI indicate that the corresponding event did not generate an interrupt.

MFPI:

A logic 1 in the MFPI status bit position indicates that the assertion or deassertion of the mimic detection indication has generated an interrupt; a logic 0 in the MFPI bit position indicates that no change in the state of the mimic detection indication occurred.

INFRI:

A logic 1 in the INFRI status bit position indicates that a change in the "inframe" state of the frame alignment circuitry generated an interrupt; a logic 0 in the INFRI status bit position indicates that no state change occurred.

MFP,INFR:

The bit position MFP and INFR indicate the current state of the mimic detection and of the frame alignment circuitry.

The interrupt and the status bit positions (COFAI, FERI, BEEI, SFEI, MFPI, and INFRI) are cleared to logic 0 when this register is read.

Registers 024H, 0A4H, 124H and 1A4H: Channel Select (1 to 8)

Bit	Type	Function	Default
Bit 7	R/W	CH[8]	0
Bit 6	R/W	CH[7]	0
Bit 5	R/W	CH[6]	0
Bit 4	R/W	CH[5]	0
Bit 3	R/W	CH[4]	0
Bit 2	R/W	CH[3]	0
Bit 1	R/W	CH[2]	0
Bit 0	R/W	CH[1]	0

Registers 025H, 0A5H, 125H and 1A5H: Channel Select (9 to 16)

Bit	Type	Function	Default
Bit 7	R/W	CH[16]	0
Bit 6	R/W	CH[15]	0
Bit 5	R/W	CH[14]	0
Bit 4	R/W	CH[13]	0
Bit 3	R/W	CH[12]	0
Bit 2	R/W	CH[11]	0
Bit 1	R/W	CH[10]	0
Bit 0	R/W	CH[9]	0

Registers 026H, 0A6H, 126H and 1A6H: Channel Select (17 to 24)

Bit	Type	Function	Default
Bit 7	R/W	CH[24]	1
Bit 6	R/W	CH[23]	0
Bit 5	R/W	CH[22]	0
Bit 4	R/W	CH[21]	0
Bit 3	R/W	CH[20]	0
Bit 2	R/W	CH[19]	0
Bit 1	R/W	CH[18]	0
Bit 0	R/W	CH[17]	0

These registers determine which channels are presented on RDLSIG[x] or inserted from TDLSIG[x] when the RXDCHAN or TXDCHAN register bit is set to logic 1 respectively.

If the RXDCHAN register bit is a logic 1, each DS0 for which the associated CH bit is set will be presented on the RDLSIG[x] output. The RDLCLK[x] output will generate a pulse for each extracted bit. When RXDCHAN is a logic 1, the Primary Rate D-Channel is presented by default.

If the TXDCHAN register bit is a logic 1, the serial stream input on TDLSIG[x] will replace the DS0 on BTPCM[x] for which the associated CH bit is set The TDLCLK[x] output will generate a pulse to clock in each defined bit. When TXDCHAN is a logic 1, the Primary Rate D-Channel is inserted by default.

Registers 027H, 0A7H, 127H and 1A7H: Interrupt ID/Clock Monitor

Bit	Type	Function	Default
Bit 7	R	INT4	0
Bit 6	R	INT3	0
Bit 5	R	INT2	0
Bit 4	R	INT1	0
Bit 3	R	BTCLKA	0
Bit 2	R	TCLKIA	0
Bit 1	R	BRCLKA	0
Bit 0	R	RCLKIA	0

These registers provide interrupt identification and activity monitoring on TQUAD clocks. The T1 framer which caused the INTB output to transition low can be identified by reading register 027H - the INTx bits in register 0A7H, 127H, and 1A7H are invalid. The INTx bit in register 027H will be high if the xth T1 framer block caused the interrupt. When a monitored clock signal makes a low to high transition, the corresponding register bit is set high. The bit will remain high until this register is read, at which point, all the bits in this register are cleared. A lack of transitions is indicated by the corresponding register bit reading low. These registers should be read at periodic intervals to detect clock failures.

INT4, INT3, INT2, INT1:

The INTx bit will be high if the xth T1 framer (the T1 framer corresponding to the input pin BTCLK[x]) causes the INTB pin to transition low.

BTCLKA:

The BTCLK active (BTCLKA) bit monitors for low to high transitions on the BTCLK[x] input. BTCLKA is set high on a rising edge of BTCLK[x], and is set low when this register is read.

TCLKIA:

The TCLKI active (TCLKIA) bit monitors for low to high transitions on the TCLKI[x] input. TCLKIA is set high on a rising edge of TCLKI[x], and is set low when this register is read.

BRCLKA:

The BRCLK active (BRCLKA) bit monitors for low to high transitions on the BRCLK input. BRCLKA is set high on a rising edge of BRCLK, and is set low when this register is read.

RCLKIA:

The RCLKI active (RCLKA) bit monitors for low to high transitions on the RCLKI[x] input. RCLKIA is set high on a rising edge of RCLKI[x], and is set low when this register is read.

Registers 028H, 0A8H, 128H and 1A8H: Backplane Parity Configuration and Status

Bit	Type	Function	Default
Bit 7	R/W	BTPTYP	0
Bit 6	R/W	BTPRTYE	0
Bit 5	R	BTPCMPI	X
Bit 4	R	BTSIGPI	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	BRPTYP	0
Bit 0	R/W	BRPRTYE	0

These registers provide control and status reporting of data intregrity checking on the backplane buses. A single parity bit in the F-bit position represents parity over the previous frame (excluding the F-bit and the undefined bit postions). If a 2.048 Mbit/s backplane rate is selected, the parity calculation is performed over the defined bit positions. Signaling parity is calculated over the defined 'A', 'B', 'C', and 'D' bit positions only. BRX2RAIL must be set to logic 0.

BTPTYP:

The transmit backplane parity type (BTPTYP) bit sets even or odd parity in the transmit streams. If BTPTYP is a logic zero, then the expected parity value in the F-bit position of BTPCM[x] and BTSIG[x] is even, thus it is a one if the number of ones in the previous frame (excluding the F-bit and the undefined bits) is odd. If BTPTYP is a logic one, then the expected parity value in the F-bit position of BTPCM[x] and BTSIG[x] is odd, thus it is a one if the number of ones in the previous frame (excluding the F-bit and the undefined bits) is even.

BTPRTYE:

The BTPRTYE bit enables transmit parity interrupts. When set a logic one, parity errors on inputs BTPCM[x] and BTSIG[x] are indicated by the BTPCMI and BTSIGI bits, respectively, and by the INTB output. When set to logic zero, parity errors are indicated by the BTPCMI and BTSIGI status bits but are not indicated on the INTB output. The TXDCHAN bit must be set to logic 0.

BTPCMI:

The BTPCMI bit indicates if a parity error has been detected on the BTPCM[x] input. This bit is cleared when this register is read. Odd or even parity is selected by the BTPTYP bit.

BTSIGI:

The BTSIGI bit indicates if a parity error has been detected on the BTSIG[x] input. This bit is cleared when this register is read. Odd or even parity is selected by the BTPTYP bit.

BRPTYP:

The receive backplane parity type (BRPTYP) bit sets even or odd parity in the receive streams. If BRPTYP is a logic zero, then the parity value in the F-bit position of BRPCM[x] and BRSIG[x] is even, thus it is a one if the number of ones in the previous frame (excluding the F-bit and the undefined bits) is odd. If BRPTYP is a logic one, then the parity value in the F-bit position of BRPCM[x] and BRSIG[x] is odd, thus it is a one if the number of ones in the previous frame (excluding the F-bit and the undefined bits) is even. BRPTYP only has effect if BRPRTYE is a logic one.

BRPRTYE:

The BRPRTYE bit enables receive parity insertion. When set a logic one, parity is inserted into the F-bit position of the BRPCM[x] and BRSIG[x] streams. When set to logic zero, the F-bit passes through transparently.

Registers 02AH, 0AAH, 12AH and 1AAH: RBOC Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	IDLE	0
Bit 1	R/W	AVC	0
Bit 0	R/W	BOCE	0

These registers select the validation criteria to be used in determining a valid bit oriented code (BOC) and enables generation of an interrupt on a change in code status.

IDLE:

The IDLE bit position enables or disables the generation of an interrupt when there is a transition from a validated BOC to idle code. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

AVC:

The AVC bit position selects the validation criteria used in determining a valid BOC. A logic 1 in the AVC bit position selects the "alternate" validation criterion of 4 out of 5 matching BOCs; a logic 0 selects the 8 out of 10 matching BOC criterion.

BOCE:

The BOCE bit position enables or disables the generation of an interrupt on the microprocessor INTB pin when a valid BOC is detected. A logic 1 in this bit position enables generation of an interrupt; a logic 0 in this bit position disables interrupt generation.

Registers 02BH, 0ABH, 12BH and 1ABH: RBOC Code Status

Bit	Type	Function	Default
Bit 7	R	IDLEI	0
Bit 6	R	BOCI	0
Bit 5	R	BOC[5]	1
Bit 4	R	BOC[4]	1
Bit 3	R	BOC[3]	1
Bit 2	R	BOC[2]	1
Bit 1	R	BOC[1]	1
Bit 0	R	BOC[0]	1

These registers indicate the current state value of the BOC[5:0] bits and indicates whether an interrupt was generated by a change in the code value.

IDLEI:

The IDLEI bit position indicates whether an interrupt was generated by the detection of the transition from a valid BOC to idle code. A logic 1 in the IDLEI bit position indicates that a transition from a valid BOC to idle code has generated an interrupt; a logic 0 in the IDLEI bit position indicates that no transition from a valid BOC to idle code has been detected. IDLEI is cleared to logic 0 when the register is read.

BOCI:

The BOCI bit position indicates whether an interrupt was generated by the detection of a valid BOC. A logic 1 in the BOCI bit position indicates that a validated BOC code has generated an interrupt; a logic 0 in the BOCI bit position indicates that no BOC has been detected. BOCI is cleared to logic 0 when the register is read.

When the TQUAD is reset, the BOC[5:0] bits are set to logic 1, and the BOCI and IDLEI bits are set to logic 0.

Registers 02CH, 0ACH, 12CH and 1ACH: ALMI Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1		Unused	X
Bit 0		Unused	X

These registers allow selection of the framing format and the data rate of the Facility Data Link in ESF to allow operation of the CFA detection algorithms.

ESF:

The ESF bit selects either extended superframe format or enables the frame mode select bits to select either regular superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF, T1DM, "alternate" T1DM, or SLC®96.

FMS1,FMS0:

The FMS1 and FMS0 bits select standard superframe, T1DM, "alternate" T1DM, or SLC®96 framing formats. A logic 00 in these bits enable the SF framing format; a logic 01 in these bit positions enable the T1DM framing format; a logic 10 in these bit positions enable the SLC®96 framing format; and a logic 11 in these bit positions enable the "alternate" T1DM framing format. The "alternate" T1DM framing format configures the ALMI to process the RED ALARM as if the SF, SLC®96, or ESF framing format were selected; the YELLOW ALARM is still processed as T1DM.

When ESF is selected (ESF bit set to logic 1), the FMS1 and FMS0 bits select the data rate and the source channel for the Facility Data Link (FDL) data. A logic 00 in these bits enables the ALMI to receive FDL data and validate the YELLOW alarm at the full 4 kbit rate. A logic 01 or 10 in these bits enables the ALMI to receive FDL data and validate the YELLOW alarm at a 2 kbit rate.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

Table 6 -

ESF	FMS1	FMS0	Mode
0	0	0	Select Superframe framing format
0	0	1	Select T1DM framing format
0	1	0	Select SLC-96 framing format
0	1	1	Select "alternate" T1DM mode
1	0	0	Select ESF framing format & 4 kbit FDL Data Rate
1	0	1	Select ESF framing format & 2 kbit FDL Data Rate
1	1	0	Select ESF framing format & 2 kbit FDL Data Rate.
1	1	1	RESERVED

Registers 02DH, 0ADH, 12DH and 1ADH: ALMI Interrupt Enable

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	FASTD	0
Bit 3	R/W	ACCEL	0
Bit 2	R/W	YELE	0
Bit 1	R/W	REDE	0
Bit 0	R/W	AISE	0

These registers select which of the three CFA's can generate an interrupt when their logic state changes and enables the "fast" deassertion mode of operation.

FASTD:

The FASTD bit enables the "fast" deassertion of RED and AIS alarms. When FASTD is set to a logic 1, deassertion of RED alarm occurs within 120 ms of going in frame. Deassertion of AIS alarm occurs within 180 ms of either detecting a 60 ms interval containing 127 or more zeros, or going in frame. When FASTD is set to a logic 0, RED and AIS alarm deassertion times remain as defined in the ALMI description.

ACCEL:

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

YELE,REDE,AISE:

A logic 1 in the enable bit positions (YELE, REDE, AISE) enables a state change in the corresponding CFA to generate an interrupt; a logic 0 in the enable bit positions disables any state changes to generate an interrupt. The enable bits are independent; any combination of YELLOW, RED, and AIS CFA's can be enabled to generate an interrupt.

Upon reset of the TQUAD, these bits are cleared to logic 0.

Registers 02EH, 0AEH, 12EH and 1AEH: ALMI Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R	YELI	0
Bit 4	R	REDI	0
Bit 3	R	AISI	0
Bit 2	R	YEL	0
Bit 1	R	RED	0
Bit 0	R	AIS	0

These registers indicate which of the three CFA's generated an interrupt when their logic state changed in bit positions 5 through 3; and indicate the current state of each CFA in bit positions 2 through 0. A logic 1 in the status positions (YELI, REDI, AISI) indicate that a state change in the corresponding CFA has generated an interrupt; a logic 0 in the status positions indicates that no state change has occurred. Both the status bit positions (bits 5 through 3) and the interrupt generated because of the change in CFA state are cleared to logic 0 when the register containing then is read.

Registers 02FH, 0AFH, 12FH and 1AFH: ALMI Alarm Detection Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	REDD	X
Bit 1	R	YELD	X
Bit 0	R	AISD	X

These registers indicate the presence or absence of one or more OOF occurrences within the last 40ms; the presence or absence of the YELLOW ALARM signal over the last 40ms; and indicate the presence or absence of the AIS ALARM signal over the last 60ms.

REDD:

When REDD is a logic 1, one or more out of frame events have occurred during the last 40ms interval. When REDD is a logic 0, no out of frame events have occurred within the last 40ms interval.

YELD:

When YELD is logic 1, a valid YELLOW signal was present during the last 40ms interval. When YELD is logic 0, the YELLOW signal was absent during the last 40ms interval. For each framing format, a valid YELLOW signal is deemed to be present if:

- bit 2 of each channel is not logic 0 for 16 or fewer times during the 40 ms interval for SF and SLC®96 framing formats;
- the Y-bit is not logic 0 for 4 or fewer times during the 40 ms interval for T1DM framing format;
- the 16-bit YELLOW bit oriented code is received error-free 8 or more times during the interval for ESF framing format with a 4 kHz data link;

- the 16-bit YELLOW bit oriented code is received error-free 4 or more times during the interval for ESF framing format with a 2 kHz data link.

AISD:

When AISD is logic 1, a valid AIS signal was present during the last 60ms interval. When AISD is logic 0, the AIS signal was absent during the last 60ms interval. A valid AIS signal is deemed to be present during a 60 ms interval if the out of frame condition has persisted for the entire interval and the received PCM data stream is not logic 0 for 126 or fewer times.

Registers 030H, 0B0H, 130H and 1B0H: TPSC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

These registers allow selection of the microprocessor read access type and output enable control for the Transmit Per-channel Serial Controller.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TQUAD is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, each channel's PCM Control byte, IDLE Code byte, and SIGNALING Control byte are passed on to the XBAS. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

Registers 031H, 0B1H, 131H and 1B1H: TPSC µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 032H, 0B2H, 132H and 1B2H: TPSC Channel Indirect Address / Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

These registers allow the µP to access the internal TPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal TPSC register is requested; when R/WB is set to a logic 0, an write to the internal TPSC register is requested.

Registers 033H, 0B3H, 133H and 1B3H: TPSC Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

These registers contain either the data to be written into the internal TPSC registers when a write request is initiated or the data read from the internal TPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal TPSC registers control the per-channel functions on the Transmit PCM data, provide the per-channel Transmit IDLE Code, and provide the per-channel Transmit signaling control and the alternate signaling bits. The functions are allocated within the registers as follows:

Table 7 -

01H	PCM Data Control byte for Channel 1
02H	PCM Data Control byte for Channel 2
•	•
•	•
17H	PCM Data Control byte for Channel 23
18H	PCM Data Control byte for Channel 24
19H	IDLE Code byte for Channel 1

1AH	IDLE Code byte for Channel 2
•	•
•	•
2FH	IDLE Code byte for Channel 23
30H	IDLE Code byte for Channel 24
31H	SIGNALING Control byte for Channel 1
32H	SIGNALING Control byte for Channel 2
•	•
•	•
47H	SIGNALING Control byte for Channel 23
48H	SIGNALING Control byte for Channel 24

The bits within each control byte are allocated as follows:

TPSC Internal Registers 01-18H: PCM Data Control byte

Bit	Type	Function
Bit 7	R/W	INVERT
Bit 6	R/W	IDLC
Bit 5	R/W	DMW
Bit 4	R/W	SIGNINV
Bit 3		Unused
Bit 2	R/W	ZCS2
Bit 1	R/W	ZCS0
Bit 0	R/W	ZCS1

INVERT:

When the INVERT bit is set to a logic 1, data from the BTPCM input is inverted for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit from the BTPCM input is inverted for that channel.

The INVERT and SIGNINV can be used to produce the following types of inversions:

Table 8 -

INVERT	SIGNINV	Effect on PCM Channel Data
0	0	PCM Channel data is unchanged
1	0	All 8 bits of the PCM channel data are inverted
0	1	Only the MSB of the PCM channel data is inverted (SIGN bit inversion)
1	1	All bits EXCEPT the MSB of the PCM channel data is inverted (Magnitude inversion)

IDLC:

When the IDLC bit is set to a logic 1, data from the IDLE Code Byte replaces the BTPCM input data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the BTPCM input data for the duration of that channel.

Data inversion, idle and digital milliwatt insertion are performed independent of the transmit framing format selected. Digital milliwatt insertion takes precedence over idle code insertion which, in turn, takes precedence over the various data inversions.

ZCS2, ZCS1,ZCS0:

The ZCS[2:0] bits select the zero code suppression used as follows:

Table 9 -

ZCS2	ZCS1	ZCS0	Description
0	0	0	No Zero Code Suppression
0	0	1	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.)
0	1	0	DDS Zero Code Suppression (All zero data byte replaced with "10011000")
0	1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)
1	0	0	"Jammed bit 8" - Every bit 8 is forced to a one. This may be used for 56kbit/s data service.
1	0	1	Reserved - Do not use.
1	1	0	Reserved - Do not use.
1	1	1	Reserved - Do not use.

TPSC Internal Registers 19-30H: IDLE Code byte

Bit	Type	Function
Bit 7	R/W	IDLE7
Bit 6	R/W	IDLE6
Bit 5	R/W	IDLE5
Bit 4	R/W	IDLE4
Bit 3	R/W	IDLE3
Bit 2	R/W	IDLE2
Bit 1	R/W	IDLE1
Bit 0	R/W	IDLE0

The contents of the IDLE Code byte register is substituted for the channel data on BTPCM[x] when the IDLC bit in the PCM Control Byte is set to a logic 1. The IDLE Code is transmitted from MSB (IDLE7) to LSB (IDLE0).

TPSC Internal Registers 31-48H: SIGNALING Control byte

Bit	Type	Function	Default
Bit 7	R/W	SIGC0	
Bit 6	R/W	SIGC1	
Bit 5		Unused	
Bit 4		Unused	
Bit 3	R/W	A'	
Bit 2	R/W	B'	
Bit 1	R/W	C'	
Bit 0	R/W	D'	

Signaling insertion is controlled by the SIGC[1:0] bits. The source of the signaling bits is determined by SIGC0: when SIGC0 is set to a logic 1, signaling data is taken from the A', B', C', and D' bits; when SIGC0 is set to logic 0, signaling data is taken from the A,B,C, and D bit locations on the BTSIG[x] input. Signaling insertion is controlled by SIGC1: when SIGC1 is set to a logic 1 and ESF, SF, or SLC®96 transmit format is selected, insertion of signaling bits is enabled; when SIGC1 is set to logic 0, the insertion of signaling bits is disabled. For SF and SLC®96 formats, the C' and D' or C and D bits from Signaling Control byte or BTSIG[x], respectively, are inserted into the A and B signaling bit positions of every second superframe that is transmitted. It is assumed that C=A and D=B.

Registers 034H, 0B4H, 134H and 1B4H: XFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	EOM	0
Bit 3	R/W	INTE	0
Bit 2	R/W	ABT	0
Bit 1	R/W	CRC	0
Bit 0	R/W	EN	0

EN:

The enable bit (EN) controls the overall operation of the XFDL. When the EN bit is set to a logic 1, the XDFL is enabled and flag sequences are sent until data is written into the Transmit Data register. When the EN bit is set to logic 0, the XFDL is disabled.

CRC:

The CRC enable bit controls the generation of the CCITT-CRC frame check sequence (FCS). Setting the CRC bit to logic 1 enables the CCITT-CRC generator and the appends the 16 bit FCS to the end of each message. When the CRC bit is set to logic 0, the FCS is not appended to the end of the message. The CRC type used is the CCITT-CRC with generator polynomial = $x^{16} + x^{12} + x^5 + 1$. The high order bit of the FCS word is transmitted first.

ABT:

The Abort (ABT) bit controls the sending of the 7 consecutive ones HDLC abort code. Setting the ABT bit to a logic 1 causes the 11111110 code to be transmitted after the last byte from the Transmit Data Register is transmitted. Aborts are continuously sent until this bit is reset to a logic 0.

INTE:

The INTE bit enables the generation of an interrupt via the TDLINT[x] output. Setting the INTE bit to logic 1 enables the generation of an interrupt; setting INTE to logic 0 disables the generation of an interrupt. If the TDLINTE bit is

also set to logic 1 in the Datalink Options register, the interrupt generated on the TDLINT[x] output is also generated on the microprocessor INTB pin.

EOM:

The EOM bit indicates that the last byte of data written in the Transmit Data register is the end of the present data packet. If the CRC bit is set then the 16-bit FCS word is appended to the last data byte transmitted and a continuous stream of flags is generated. The EOM bit is automatically cleared before transmission of the next data packet begins.

Registers 035H, 0B5H, 135H and 1B5H: XFDL Interrupt Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R	INT	1
Bit 0	R/W	UDR	0

INT:

The INT bit indicates when the XFDL is ready to accept a new data byte for transmission. The INT bit is set to a logic 1 when the previous byte in the Transmit Data register has been loaded into the parallel to serial converter and a new byte can be written into the Transmit Data register. The INT bit is set to a logic 0 while new data is in the Transmit Data register. The INT bit is not disabled by the INTE bit in the configuration register.

UDR:

The UDR bit indicates when the XFDL has underrun the data in the Transmit Data register. The UDR bit is set to a logic 1 if the parallel to serial conversion of the last byte in the Transmit Data register has completed before the new byte was written into the Transmit Data register. Once an underrun has occurred, the XFDL transmits an ABORT, followed by a flag, and waits to transmit the next valid data byte. If the UDR bit is still set after the transmission of the flag the XFDL will continuously transmit the all-ones idle pattern. The UDR bit can only be cleared by writing a logic 0 to the UDR bit position in this register.

Registers 036H, 0B6H, 136H and 1B6H: XFDL Transmit Data

Bit	Type	Function	Default
Bit 7	R/W	TD7	X
Bit 6	R/W	TD6	X
Bit 5	R/W	TD5	X
Bit 4	R/W	TD4	X
Bit 3	R/W	TD3	X
Bit 2	R/W	TD2	X
Bit 1	R/W	TD1	X
Bit 0	R/W	TD0	X

Data written to this register is serialized and transmitted on the facility data link least significant bit first. The XFDL signals when the next data byte is required by setting the TDLINT[x] output high (if enabled) and by setting the INT bit in the XFDL Interrupt Status register high. When INT and/or TDLINT[x] is set, the Transmit Data register must be written with the new data within 4 data bit periods to prevent the occurrence of an underrun. At a 4 kbit/sec FDL data rate this period corresponds to 1.00 ms.

Registers 038H, 0B8H, 138H and 1B8H: RFDL Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	TR	0
Bit 0	R/W	EN	0

TR:

Setting the terminate reception bit (TR) forces the RFDL to immediately terminate the reception of the current HDLC frame, empty the FIFO, clear the interrupts, and begin searching for a new flag sequence. The RFDL handles the TR input in the same manner as if the EN bit had been cleared and then set. The TR bit in this register will reset itself after a rising and falling edge have occurred on the CLK input to the RFDL once the write to this register has completed and WEB goes inactive. If this register is read after this time, the TR bit value returned will be zero.

EN:

The enable bit (EN) controls the overall operation of the RFDL. When set, the RDFL is enabled; when reset the RFDL is disabled. When the block is disabled, the FIFO and interrupts are all cleared, however, the programming of the RFDL Interrupt Control/Status Register is not affected. When the block is enabled, it will immediately begin looking for flags.

The RFDL handles the TR input in the same manner as clearing and setting the EN bit, therefore, the RFDL state machine will begin searching for flags and an interrupt will be generated when the first flag is detected.

Registers 039H, 0B9H, 139H and 1B9H: RFDL Interrupt Control/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTC1	0
Bit 1	R/W	INTC0	0
Bit 0	R	INT	0

INTC1,INTC0:

The INTC1 and INTC0 bits control when an interrupt is asserted based on the number of received data bytes in the FIFO as follows:

Table 10 -

INTC1	INTC0	Description
0	0	Disable interrupts (All sources)
0	1	Enable interrupt when FIFO receives data
1	0	Enable interrupt when FIFO has 2 bytes of data
1	1	Enable interrupt when FIFO has 3 bytes of data

INT:

The INT bit reflects the status of the external RDLINT[x] interrupt unless the INTC1 and INTC0 bits are set to disable interrupts. In that case, the RDLINT[x] output is forced to 0 and the INT bit of this register will reflect the state of the internal interrupt latch.

In addition to the FIFO fill status, interrupts are also generated for EOM (end of message), OVR (FIFO overrun), detection of the abort sequence while not receiving all ones and on detection of the first flag while receiving all ones. The interrupt is reset by a RFDL Receive Data Register read that empties the FIFO, unless the cause of the interrupt was due to a FIFO overrun. The interrupt due to

a FIFO overrun is cleared on a RFDL Status register read, by disabling the block, or by setting TR high.

The contents of this register should only be changed when the RFDL is disabled to prevent any erroneous interrupt generation.

Registers 03AH, 0BAH, 13AH and 1BAH: RFDL Status

Bit	Type	Function	Default
Bit 7	R	FE	1
Bit 6	R	OVR	0
Bit 5	R	FLG	0
Bit 4	R	EOM	0
Bit 3	R	CRC	0
Bit 2	R	NVB[2]	1
Bit 1	R	NVB[1]	1
Bit 0	R	NVB[0]	1

The FLG and EOM bits in this register contain values which correspond to the last byte read from the RFDL Data Register.

FE:

The FIFO Empty bit (FE) is high when the last FIFO entry is read and goes low when the FIFO is loaded with new data.

OVR:

The Receiver Overrun bit (OVR) is set when data is written over unread data in the FIFO. This bit is not reset until after the Status register is read. While OVR is high, the RFDL and FIFO are held in the reset state, causing the FLG and EOM bits in the status register to be reset also.

FLG:

The flag bit (FLG) is set if the RFDL has detected the presence of the HDLC flag sequence (01111110) in the data. FLG is reset only when the HDLC abort sequence (01111111) is detected in the data or when the RFDL is disabled. This bit is passed through the FIFO with the Data so that the status of this bit will correspond to the data just read from the RFDL Data Register. The reception of bit-oriented codes over the data link will also force an abort due to its eight ones pattern.

EOM:

The End of Message bit (EOM) follows the RDLEOM[x] output. It is set when:

- The last byte in the HDLC frame (EOM) is being read from the Receive Data Register,
- An abort sequence is detected while not in the receiving all-ones state and the byte, written to the FIFO due to the detection of the abort sequence, is being read from the FIFO,
- The first flag has been detected and the dummy byte, written into the FIFO when the RFDL changes from the receiving all-ones state to the receiving flags state, is being read from the FIFO,
- Immediately on detection of FIFO overrun.

The EOM bit is passed through the FIFO with the Data so that the status of this bit will correspond to the data just read from the RFDL Data Register.

CRC:

The CRC bit is set if a CRC error was detected in the last received HDLC frame. The CRC bit is only valid when EOM is logic 1 and FLG is a logic 1 and OVR is a logic 0.

NVB[2:0]:

The NVB[2:0] bit positions indicate the number of valid bits in the RFDL Receive Data Register byte. It is possible that not all of the bits in the RFDL Receive Data Register are valid when the last data byte is read since the data frame can be any number of bits in length and not necessarily an integral number of bytes. The RFDL Receive Data Register is filled starting from the MSB bit position (RD7) and the data bits are shifted to lower bit positions as more bits are received, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0]. An NVB[2:0] value of 000 binary indicates that only the FE bit in this register is valid. An NVB[2:0] value of 011 indicates that RD[7:4] contain valid data bits where RD4 is the data bit that was received first. NVB[2:0] is only valid when the EOM bit is a logic 1 and the FLG bit is a logic 1 and the OVR bit is a logic 0.

On an interrupt generated from the detection of first flag, reading the RFDL Status register will return invalid NVB[2:0] and CRC bits, even though the EOM bit is logic 1 and the FLG bit is logic 1.

If the Receive Data register is read while there is no valid data, then a FIFO underrun condition occurs. The underrun condition is reflected in the Status register by forcing all bits to logic zero on the first Status register read

immediately following the Received Data register read which caused the underrun condition.

Registers 03BH, 0BBH, 13BH and 1BBH: RFDL Receive Data

Bit	Type	Function	Default
Bit 7	R	RD7	X
Bit 6	R	RD6	X
Bit 5	R	RD5	X
Bit 4	R	RD4	X
Bit 3	R	RD3	X
Bit 2	R	RD2	X
Bit 1	R	RD1	X
Bit 0	R	RD0	X

The RFDL Receive Data Register is filled starting from the MSB bit position (RD7) and the data bits are shifted to lower bit positions as more bits are received, with one to eight data bits being valid. The number of valid bits is equal to 1 plus the value of NVB[2:0] from the RFDL Status Register. An NVB[2:0] value of 111 indicates that RD[7:0] contain valid data bits where RD0 corresponds to the first bit of the serial byte received by the RFDL.

These registers are actually 4 level FIFOs. If data is available, the FE bit in the Status register is low. If INTC[1:0] (in the RFDL Interrupt Control/Status register) is set to 01, this register must be read within 31 data bit periods to prevent an overrun. If INTC[1:0] is set to 11, this register must be read within 15 data bit periods.

When an overrun is detected, an interrupt is generated and the FIFO is held cleared until the Status register is read. When the HDLC abort sequence (01111111) is detected in the data an ABORT interrupt is generated and the data that has been shifted into the serial to parallel converter is written into the FIFO.

A read of this register increments the FIFO pointer at the end of the read. If this register read causes a FIFO underrun, then the pointer is inhibited from incrementing. The underrun condition will be signalled in the next RFDL Status register read by returning all zeros.

Registers 03CH, 0BCH, 13CH and 1BCH: IBCD Configuration

Bit	Type	Function	Default
Bit 7	R/W	ACCEL	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	DSEL1	0
Bit 2	R/W	DSEL0	0
Bit 1	R/W	ASEL1	0
Bit 0	R/W	ASEL0	0

These registers provide the selection of the Activate and De-activate loopback code lengths (from 3 bits to 8 bits) as follows:

Table 11 -

DEACTIVATE CODE		ACTIVATE CODE		CODE LENGTH
DSEL1	DSEL0	ASEL1	ASEL0	
0	0	0	0	5 bits
0	1	0	1	6 (or 3*) bits
1	0	1	0	7 bits
1	1	1	1	8 (or 4*) bits

*Note: 3 and 4 bit code sequences can be accommodated by configuring the IBCD for 6 or 8 bits and by programming two repetitions of the code sequence.

The ACCEL bit is used for production test purposes only. THE ACCEL BIT MUST BE PROGRAMMED TO LOGIC 0 FOR NORMAL OPERATION.

Registers 03DH, 0BDH, 13DH and 1BDH: IBCD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R	LBACP	0
Bit 6	R	LBDCP	0
Bit 5	R/W	LBAE	0
Bit 4	R/W	LBDE	0
Bit 3	R	LBAI	0
Bit 2	R	LBDI	0
Bit 1	R	LBA	0
Bit 0	R	LBD	0

LBACP,LBDCP:

The LBACP and LBDCP bits indicate when the corresponding loopback code is present during a 39.8 ms interval.

LBAE:

The LBAE bit enables the assertion or deassertion of the inband Loopback Activate (LBA) detect indication to generate an interrupt on the microprocessor INTB pin. When LBAE is set to logic 1, any change in the state of the LBA detect indication generates an interrupt. When LBAE is set to logic 0, no interrupt is generated by changes in the LBA detect state.

LBDE:

The LBDE bit enables the assertion or deassertion of the inband Loopback Deactivate (LBD) detect indication to generate an interrupt on the microprocessor INTB pin. When LBDE is set to logic 1, any change in the state of the LBD detect indication generates an interrupt. When LBDE is set to logic 0, no interrupt is generated by changes in the LBD detect state.

LBAI,LBDI:

The LBAI and LBDI bits indicate which of the two expected loopback codes generated the interrupt when their state changed. A logic 1 in these bit positions indicate that a state change in that code has generated an interrupt; a logic 0 in these bit positions indicate that no state change has occurred.

LBA,LBD:

The LBA and LBD bits indicate the current state of the corresponding loopback code detect indication. A logic 1 in these bit positions indicate the presence of that code has been detected; a logic 0 in these bit positions indicate the absence of that code.

Registers 03EH, 0BEH, 13EH and 1BEH: IBCD Activate Code

Bit	Type	Function	Default
Bit 7	R/W	ACT7	0
Bit 6	R/W	ACT6	0
Bit 5	R/W	ACT5	0
Bit 4	R/W	ACT4	0
Bit 3	R/W	ACT3	0
Bit 2	R/W	ACT2	0
Bit 1	R/W	ACT1	0
Bit 0	R/W	ACT0	0

This 8 bit register selects the Activate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 00001, then the first 8 bits of two repetitions (0000100001) is programmed into the register, i.e.00001000. Note that bit ACT7 corresponds to the first code bit received.

Upon reset of the TQUAD, the register contents are set to logic 0.

Registers 03FH, 0BFH, 13FH and 1BFH: IBCD Deactivate Code

Bit	Type	Function	Default
Bit 7	R/W	DACT7	0
Bit 6	R/W	DACT6	0
Bit 5	R/W	DACT5	0
Bit 4	R/W	DACT4	0
Bit 3	R/W	DACT3	0
Bit 2	R/W	DACT2	0
Bit 1	R/W	DACT1	0
Bit 0	R/W	DACT0	0

This 8 bit register selects the Deactivate code sequence that is to be detected. If the code sequence length is less than 8 bits, the first 8 bits of several repetitions of the code sequence must be used to fill the 8 bit register. For example, if code sequence is a repeating 001, then the first 8 bits of three repetitions (001001001) is programmed into the register, i.e.00100100. Note that bit DACT7 corresponds to the first code bit received.

Upon reset of the TQUAD, the register contents are set to logic 0.

Registers 040H, 0C0H, 140H and 1C0H: SIGX Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

These registers allow selection of the framing format, the microprocessor access type, and allows enabling of the per-channel configuration registers.

ESF:

The framing format is controlled by the ESF, FMS1, and FMS0 bits. The ESF bit selects either extended superframe format or enables the Frame Mode Select bits to select either regular superframe or SLC®96 framing formats. A logic 1 in the ESF bit position selects ESF; a logic 0 bit enables FMS1 and FMS0 to select SF or SLC®96.

FMS1,FMS0:

The FMS1 bit selects standard Superframe or SLC®96 framing formats. A logic 0 in the FMS1 bit enables the SF framing format; a logic 1 in the FMS1 bit position enables the SLC®96 framing format. The FMS0 bit disables the signaling extraction and bit fixing. A logic 0 in the FMS0 bit position enables the SIGX to provide an extracted signaling bit stream and to provide bit fixing on the processed PCM stream; a logic 1 in the FMS0 bit position disables the signaling extraction, forcing the signaling output stream to logic 0 and disables bit fixing on the PCM stream.

When ESF is selected (ESF bit set to logic 1), the extended superframe format is selected and the FMS1 and FMS0 bits are ignored.

The valid combinations of the ESF, FMS1, and FMS0 bits are summarized in the table below:

Table 12 -

ESF	FMS1	FMS0	Mode
0	0	0	Select Superframe framing format
0	1	0	Select SLC®96 framing format
0	X	1	Disable signaling extraction
1	X	X	Select ESF framing format

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TQUAD is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, data inversion, bit fixing, and signaling debouncing are performed on a per-channel basis. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

Upon reset of the TQUAD, the ESF, FMS[1:0], IND, and PCCE bits are all set to logic 0, selecting the Superframe framing format, disabling µP indirect access, and disabling per-channel functions.

Registers 041H, 0C1H, 141H and 1C1H: SIGX µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 042H, 0C2H, 142H and 1C2H: SIGX Channel Indirect Address / Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6		Unused	X
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

These registers allow the µP to access to internal SIGX registers addressed by the A[5:0] bits and perform the operation specified by the R/WB bit. Writing to one of these registers with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal SIGX register is requested, when R/WB is set to a logic 0, an write to the internal SIGX register is requested.

Registers 043H, 0C3H, 143H and 1C3H: SIGX Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

These registers contain either the data to be written into the internal SIGX registers when a write request is initiated or the data read from the internal SIGX registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the nibble to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data bits.

The internal registers of the SIGX control the per-channel functions on the Receive PCM data and allow the µP to read the channel's current signaling data. The address bit A5 selects whether a channel's configuration data register is to be accessed (A5=1) or whether a channel's signaling data register is to be accessed. The channel registers are allocated within the SIGX as follows:

Table 13 -

01H	Channel 1 Signaling Data
02H	Channel 2 Signaling Data
• •	• •
17H	Channel 23 Signaling Data
18H	Channel 24 Signaling Data

19-1FH	Ignored
20H	SIGX Configuration
21H	Channel 1 Per-channel Configuration Data
22H	Channel 2 Per-channel Configuration Data
• •	• •
37H	Channel 23 Per-channel Configuration Data

The bits within each channel register byte are allocated as follows:

SIGX Internal Registers 01-18H: Signaling Data

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R	A
Bit 2	R	B
Bit 1	R	C
Bit 0	R	D

When the Signaling Data registers are read, the byte returned contains the 4 signaling bits in the 4 least significant bit positions. If SF or SLC®96 framing format is selected then C=A and D=B. The bits read correspond to the signaling state extracted from the third to last superframe received.

When reading the extracted signaling data for a channel with signaling state debounce enabled, the signaling data returned is the debounced version, meaning that the signaling state value for that channel must have been the same for two consecutive superframes before it was allowed to propagate through the signaling buffers and be visible in the signaling data registers. If the state was not the same, the current state (accessible via these registers) is not changed.

SIGX Internal Registers 21-38H: Per-Channel Configuration Data

Bit	Type	Function
Bit 7		Unused
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R/W	INV
Bit 2	R/W	FIX
Bit 1	R/W	POL
Bit 0	R/W	DEB

INV:

The INV bit controls data inversion for the selected channel: a logic 1 in the INV bit position enables data inversion; a logic 0 disables data inversion. Inversion only affects the channel data, F-bits are passed unchanged.

FIX:

The FIX bit controls whether the signaling bit (the least significant bit of the channel byte) is fixed to the polarity specified by the POL bit. A logic 1 in the FIX position enables bit fixing; a logic 0 in the FIX position disables bit fixing.

POL:

The POL bit selects the logic level the signaling bit is fixed to when bit fixing is enabled. NOTE: when data inversion is selected for the channel and bit fixing is enabled, then the sense of POL is also inverted (i.e. if inversion is enabled and POL=1, then the bit will be fixed to logic 0).

DEB:

The DEB bit controls whether a channel's signaling bits are to be debounced. Debouncing requires that the signaling bits be in the same state for two successive superframes before the signaling bits are changed to that state.

Registers 044H, 0C4H, 144H and 1C4H: XBAS Configuration

Bit	Type	Function	Default
Bit 7	R/W	MTRK	0
Bit 6	R/W	Reserved	0
Bit 5	R/W	B8ZS	0
Bit 4	R/W	ESF	0
Bit 3	R/W	FMS1	0
Bit 2	R/W	FMS0	0
Bit 1	R/W	ZCS1	0
Bit 0	R/W	ZCS0	0

Bit 6 of the configuration register is reserved and must be set to logic 0 for proper operation.

ZCS[1:0]:

The ZCS[1:0] bits select the Zero Code Suppression format to be used. These bits are logically ORed with the ZCS[1:0] bits in the TPSC per-channel PCM Control byte. The bits are encoded as follows:

Table 14 -

ZCS1	ZCS0	Zero Code Suppression Format
0	0	None
0	1	GTE Zero Code Suppression (Bit 8 of an all zero channel byte is replaced by a one, except in signaling frames where bit 7 is forced to a one.)
1	0	DDS Zero Code Suppression (All zero data byte replaced with "10011000")
1	1	Bell Zero Code Suppression (Bit 7 of an all zero channel byte is replaced by a one.)

B8ZS:

The B8ZS bit enables B8ZS line coding when it is a logic 1.

ESF, FMS1, FMS0:

The ESF bit selects either Extended Superframe format or enables the Frame Mode Select bits (FMS) to select either regular superframe, T1DM or SLC®96 framing formats. The mode is encoded as follows:

Table 15 -

ESF	FMS1	FMS0	MODE
0	0	0	SF framing format
0	0	1	T1DM framing format (R bit unaffected)
0	1	0	SLC®96
0	1	1	T1DM framing format (FDL data replaces R bit)
1	0	0	ESF framing format - 4 kbit/s data link
1	0	1	ESF framing format - 2 kbit/s data link (frames 3,7,11,15,19,23)
1	1	0	ESF framing format - 2 kbit/s data link (frames 1,5,9,13,17,21)
1	1	1	ESF framing format - 4 kbit/s data link

MTRK:

The MTRK bit forces trunk conditioning, idle code substitution and signaling conditioning, on all channels when MTRK is a logic 1. This has the same effect as setting the IDLC bit in the PCM Control byte and the SIG0 bit in the SIGNALING Control byte for all channels.

Registers 045H, 0C5H, 145H and 1C5H: XBAS Alarm Transmit

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	XYEL	0
Bit 0	R/W	XAIS	0

These registers control the transmission of YELLOW or AIS alarm.

XYEL:

The XYEL bit enables the XBAS to generate a YELLOW alarm in the appropriate framing format. When XYEL is set to logic 1, XBAS is enabled to set bit 2 of each channel to logic 0 for SF and SLC®96 formats, the Y-bit to logic 0 for T1DM format, and XBAS is enabled to transmit repetitions of 1111111100000000 (the YELLOW Alarm BOC) on the FDL for ESF format. When XYEL is set to logic 0, XBAS is disabled from generating the YELLOW alarm.

XAIS:

The XAIS bit enables the XBAS to generate an unframed all-ones AIS alarm. When XAIS is set to logic 1, the XBAS bi-polar outputs are forced to pulse alternately, creating an all-ones signal. When XAIS is set to logic 0, the XBAS bi-polar outputs operate normally.

Registers 046H, 0C6H, 146H and 1C6H: XIBC Control

Bit	Type	Function	Default
Bit 7	R/W	EN	0
Bit 6	R/W	UF	0
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	CL1	0
Bit 0	R/W	CL0	0

EN:

The EN bit controls whether the Inband Code is transmitted or not. A logic 1 in the EN bit position enables transmission of inband codes; a logic 0 in the EN bit position disables inband code transmission.

UF:

The UF bit controls whether the code is transmitted framed or unframed. A logic 1 in the UF bit position selects unframed inband code transmission; a logic 0 in the UF bit position selects framed inband code transmission. Note: the UF register bit controls the XBAS directly and is not qualified by the EN bit. When UF is set to logic 1, the XBAS is disabled and no framing is inserted regardless of the setting of EN. The UF bit should only be written to logic 1 when the EN bit is set, and should be cleared to logic 0 when the EN bit is cleared.

CL1, CL0:

The bit positions CL[1:0] (bits 1 & 0) of this register indicate the length of the inband loopback code sequence, as follows:

Table 16 -

CL1	CL0	Code Length
0	0	5
0	1	6
1	0	7
1	1	8

Codes of 3 or 4 bits in length may be accommodated by treating them as half of a double-sized code (i.e. a 3-bit code would use the 6-bit code length setting).

Registers 047H, 0C7H, 147H and 1C7H: XIBC Loopback Code

Bit	Type	Function	Default
Bit 7	R/W	IBC7	X
Bit 6	R/W	IBC6	X
Bit 5	R/W	IBC5	X
Bit 4	R/W	IBC4	X
Bit 3	R/W	IBC3	X
Bit 2	R/W	IBC2	X
Bit 1	R/W	IBC1	X
Bit 0	R/W	IBC0	X

These registers contain the inband loopback code pattern to be transmitted. The code is transmitted most significant bit (IBC7) first, followed by IBC6 and so on. The code, regardless of the length, must be aligned with the MSB always in the IBC7 position (e.g., a 5-bit code would occupy the IBC7 through IBC2 bit positions). To transmit a 3-bit or a 4-bit code pattern, the pattern must be paired to form a double-sized code (i.e., the 3-bit code '011' would be written as the 6-bit code '011011').

When the TQUAD is reset, the contents of this register are not affected.

Registers 049H, 0C9H, 149H and 1C9H: PMON Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R/W	INTE	0
Bit 1	R	XFER	0
Bit 0	R	OVR	0

These registers contain status information indicating when counter data has been transferred into the holding registers and indicating whether the holding registers have been overrun.

INTE:

The INTE bit controls the generation of a microprocessor interrupt when the transfer clock has caused the counter values to be stored in the holding registers. A logic 1 bit in the INTE position enables the generation of an interrupt ; a logic 0 bit in the INTE position disables the generation of an interrupt.

XFER:

The XFER bit indicates that a transfer of counter data has occurred. A logic 1 in this bit position indicates that a latch request, initiated by writing to one of the counter register locations, was received and a transfer of the counter values has occurred. A logic 0 indicates that no transfer has occurred. The XFER bit is cleared (acknowledged) by reading this register.

OVR:

The OVR bit is the overrun status of the holding registers. A logic 1 in this bit position indicates that a previous transfer (indicated by XFER being logic 1) has not been acknowledged before the next transfer clock has been issued and that the contents of the holding registers have been overwritten. A logic 0 indicates that no overrun has occurred. The OVR bit is cleared by reading this register.

Registers 04A-04FH, 0CA-0CFH, 14A-14FH and 1CA-1CFH: Latching Performance Data

The Performance Data registers for a single framer are updated as a group by writing to any of the PMON count registers (addresses x4AH-x4FH). A write to one (and only one) of these locations loads performance data located in the PMON into the internal holding registers. Alternately, the Performance Data registers for all four framers are updated by writing to the Revision/Chip ID/Global PMON Update register (address 00CH). The data contained in the holding registers can then be subsequently read by microprocessor accesses into the PMON count register address space. The latching of count data, and subsequent resetting of the counters, is synchronized to the internal event timing so that no events are missed.

The PMON is loaded with new performance data within 3.5 recovered clock, RCLKO[x], periods of the latch performance data register write. With nominal line rates, the PMON registers should not be polled until 2.3 µsec have elapsed from the "latch performance data" register write.

When the TQUAD is reset, the contents of the PMON count registers are unknown until the first latching of performance data is performed.

Registers 04AH, 0CAH, 14AH and 1CAH: PMON LCV Count (LSB)

Bit	Type	Function	Default
Bit 7	R	LCV7	X
Bit 6	R	LCV6	X
Bit 5	R	LCV5	X
Bit 4	R	LCV4	X
Bit 3	R	LCV3	X
Bit 2	R	LCV2	X
Bit 1	R	LCV1	X
Bit 0	R	LCV0	X

These registers contain the lower eight bits of the 12 bit Line Code Violation event counter. A Line Code Violation event is defined as the occurrence of a Bipolar Violation or Excessive Zeros. The counting of Excessive Zeros can be disabled by the BPV bit of the Receive DS1 Interface Configuration register.

Registers 04BH, 0CBH, 14BH and 1CBH: PMON LCV Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R	LCV11	X
Bit 2	R	LCV10	X
Bit 1	R	LCV9	X
Bit 0	R	LCV8	X

These registers contain the upper four bits of the 12 bit Line Code Violation event counter.

Registers 04CH, 0CCH, 14CH and 1CCH: PMON BEE Count (LSB)

Bit	Type	Function	Default
Bit 7	R	BEE7	X
Bit 6	R	BEE6	X
Bit 5	R	BEE5	X
Bit 4	R	BEE4	X
Bit 3	R	BEE3	X
Bit 2	R	BEE2	X
Bit 1	R	BEE1	X
Bit 0	R	BEE0	X

These registers contain the lower eight bits of the 9-bit Bit Error event counter. A Bit Error event is defined as a CRC-6 error in ESF, a framing bit error in SF, an F_T-bit error in SLC®96, and an F-bit or sync bit error (there can be up to 7 bits in error per frame) in T1DM.

Registers 04DH, 0CDH, 14DH and 1CDH: PMON BEE Count (MSB)

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0	R	BEE8	X

These registers contain the upper bit of the 9-bit Bit Error event counter.

Registers 04EH, 0CEH, 14EH and 1CEH: PMON FER Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	FER4	X
Bit 3	R	FER3	X
Bit 2	R	FER2	X
Bit 1	R	FER1	X
Bit 0	R	FER0	X

These registers contain the value of the 5 bit Framing Bit Error event counter.

Registers 04FH, 0CFH, 14FH and 1CFH: PMON OOF/COFA Count

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2	R	OOF2/COFA2	X
Bit 1	R	OOF1/COFA1	X
Bit 0	R	OOF0/COFA0	X

These registers contain the value of the 3 bit counter accumulating Out Of Frame or Change Of Frame Alignment events.

Registers 050H, 0D0H, 150H and 1D0H: RPSC Configuration

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1	R/W	IND	0
Bit 0	R/W	PCCE	0

These registers allow selection of the microprocessor read access type and output enable control for the Receive Per-channel Serial Controller.

IND:

The IND bit controls the microprocessor access type: either indirect or direct. The IND bit must be set to logic 1 for proper operation. When the TQUAD is reset, the IND bit is set low, disabling the indirect access mode.

PCCE:

The PCCE bit enables the per-channel functions. When the PCCE bit is set to a logic 1, the Data Trunk Conditioning Code byte and Signaling Trunk Conditioning Code byte are enabled to modify the received data and extracted signaling data streams (visible on BRPCM[x] and BRSIG[x], if selected) under direction of each channel's PCM Control byte. When the PCCE bit is set to logic 0, the per-channel functions are disabled.

Registers 051H, 0D1H, 151H and 1D1H: RPSC µP Access Status

Bit	Type	Function	Default
Bit 7	R	BUSY	0
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3		Unused	X
Bit 2		Unused	X
Bit 1		Unused	X
Bit 0		Unused	X

The BUSY bit in the Status register is high while a µP access request is in progress. The BUSY bit goes low timed to an internal high-speed clock rising edge after the access has been completed. During normal operation, the Status Register should be polled until the BUSY bit goes low before another µP access request is initiated. A µP access request is typically completed within 640 ns.

Registers 052H, 0D2H, 152H and 1D2H: RPSC Channel Indirect Address / Control

Bit	Type	Function	Default
Bit 7	R/W	R/WB	0
Bit 6	R/W	A6	0
Bit 5	R/W	A5	0
Bit 4	R/W	A4	0
Bit 3	R/W	A3	0
Bit 2	R/W	A2	0
Bit 1	R/W	A1	0
Bit 0	R/W	A0	0

These registers allow the µP to access the internal RPSC registers addressed by the A[6:0] bits and perform the operation specified by the R/WB bit. Writing to this register with a valid address and R/WB bit initiates an internal µP access request cycle. The R/WB bit selects the operation to be performed on the addressed register: when R/WB is set to a logic 1, a read from the internal RPSC register is requested; when R/WB is set to a logic 0, an write to the internal RPSC register is requested.

Registers 053H, 0D3H, 153H and 1D3H: RPSC Channel Indirect Data Buffer

Bit	Type	Function	Default
Bit 7	R/W	D7	0
Bit 6	R/W	D6	0
Bit 5	R/W	D5	0
Bit 4	R/W	D4	0
Bit 3	R/W	D3	0
Bit 2	R/W	D2	0
Bit 1	R/W	D1	0
Bit 0	R/W	D0	0

These registers contain either the data to be written into the internal RPSC registers when a write request is initiated or the data read from the internal RPSC registers when a read request has completed. During normal operation, if data is to be written to the internal registers, the byte to be written must be written into this Data register before the target register's address and R/WB=0 is written into the Address/Control register, initiating the access. If data is to be read from the internal registers, only the target register's address and R/WB=1 is written into the Address/Control register, initiating the request. After 640 ns, this register will contain the requested data byte.

The internal RPSC registers control the per-channel functions on the Receive PCM data, provide the per-channel Data Trunk Conditioning Code, and provide the per-channel Signaling Trunk Conditioning Code. The functions are allocated within the registers as follows:

Table 17 -

01H	PCM Data Control byte for Channel 1
02H	PCM Data Control byte for Channel 2
•	•
•	•
17H	PCM Data Control byte for Channel 23
18H	PCM Data Control byte for Channel 24
19H	Data Trunk Conditioning byte for Channel 1

1AH	Data Trunk Conditioning byte for Channel 2
•	•
•	•
2FH	Data Trunk Conditioning byte for Channel 23
30H	Data Trunk Conditioning byte for Channel 24
31H	Signaling Trunk Conditioning byte for Channel 1
32H	Signaling Trunk Conditioning byte for Channel 2
•	•
•	•
47H	Signaling Trunk Conditioning byte for Channel 23
48H	Signaling Trunk Conditioning byte for Channel 24

The bits within each control byte are allocated as follows:

RPSC Internal Registers 01-18H: PCM Data Control byte

Bit	Type	Function
Bit 7	R/W	INVERT
Bit 6	R/W	DTRKC
Bit 5	R/W	DMW
Bit 4	R/W	SIGNINV
Bit 3		Unused
Bit 2		Unused
Bit 1		Unused
Bit 0		Unused

INVERT:

When the INVERT bit is set to a logic 1, data output on the BRPCM[x] pin is the bit inverse of the received data for the duration of that channel.

SIGNINV:

When the SIGNINV bit is set to a logic 1, the most significant bit of the data output on the BRPCM[x] pin is inverse of the received data most significant bit for that channel.

The INVERT and SIGNINV can be used to produce the following types of inversions:

Table 18 -

INVERT	SIGNINV	Effect on PCM Channel Data
0	0	PCM Channel data is unchanged
1	0	All 8 bits of the received PCM channel data are inverted
0	1	Only the MSB of the received PCM channel data is inverted (SIGN bit inversion)
1	1	All bits EXCEPT the MSB of the received PCM channel data is inverted (Magnitude inversion)

DTRKC:

When the DTRKC bit is set to a logic 1, data from the Data Trunk Conditioning Code Byte replaces the BRPCM[x] output data for the duration of that channel.

DMW:

When the DMW bit is set to a logic 1, the digital milliwatt pattern replaces the BRPCM[x] output data for the duration of that channel.

Data inversion, data trunk conditioning, and digital milliwatt insertion are performed independent of the received framing format. Digital milliwatt insertion takes precedence over data trunk conditioning which, in turn, takes precedence over the various data inversions.

RPSC Internal Registers 19-30H: Data Trunk Conditioning Code byte

Bit	Type	Function
Bit 7	R/W	DTRK7
Bit 6	R/W	DTRK6
Bit 5	R/W	DTRK5
Bit 4	R/W	DTRK4
Bit 3	R/W	DTRK3
Bit 2	R/W	DTRK2
Bit 1	R/W	DTRK1
Bit 0	R/W	DTRK0

The contents of the Data Trunk Conditioning Code byte register is substituted for the channel data on BRPCM[x] when the DTRKC bit in the PCM Control Byte is set to a logic 1. The Data Trunk Conditioning Code is transmitted from MSB (DTRK7) to LSB (DTRK0).

RPSC Internal Registers 31-48H: Signaling Trunk Conditioning byte

Bit	Type	Function
Bit 7	R/W	STRKC
Bit 6		Unused
Bit 5		Unused
Bit 4		Unused
Bit 3	R/W	A'
Bit 2	R/W	B'
Bit 1	R/W	C'
Bit 0	R/W	D'

The contents of the Signaling Trunk Conditioning Code byte register is substituted for the channel signaling data on BRSIG[x] when the STRKC bit is set to a logic 1. The Signaling Trunk Conditioning Code is placed in least significant nibble of the channel byte.

Registers 055H, 0D5H, 155H and 1D5H: PDVD Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4	R	PDV	0
Bit 3	R	Z16DI	0
Bit 2	R	PDVI	0
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist. When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether interrupts are enabled or disabled.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the

PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

Registers 057H, 0D7H, 157H and 1D7H: XBOC Code

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	BC[5]	1
Bit 4	R/W	BC[4]	1
Bit 3	R/W	BC[3]	1
Bit 2	R/W	BC[2]	1
Bit 1	R/W	BC[1]	1
Bit 0	R/W	BC[0]	1

These registers enables the XBOC to generate a bit oriented code and selects the 6-bit code to be transmitted.

When this register is written with any 6-bit code other than 111111, that code will be transmitted repeatedly in the ESF Facility Data Link with the format 111111110[BC0][BC1][BC2][BC3][BC4][BC5]0, overwriting any HDLC packets currently being transmitted. When the register is written with 111111, the XBOC is disabled.

Registers 059H, 0D9H, 159H and 1D9H: XPDE Interrupt Enable/Status

Bit	Type	Function	Default
Bit 7	R/W	STUFE	0
Bit 6	R/W	STUFF	0
Bit 5	R	STUFI	0
Bit 4	R	PDV	0
Bit 3	R	Z16DI	0
Bit 2	R	PDVI	0
Bit 1	R/W	Z16DE	0
Bit 0	R/W	PDVE	0

STUFE:

The STUFE bit enables the occurrence of pulse stuffing to generate an interrupt on INTB. When STUFE is set to logic 1, an interrupt is generated on the occurrence of a bit stuff. When STUFE is a logic 0, bit stuffing occurrences do not generate an interrupt on INTB.

STUFF:

The STUFF bit enables pulse stuffing to occur upon detection of a violation of the pulse density rule. Bit stuffing is performed in such a way that the resulting data stream no longer violates the pulse density rule. When STUFF is set to logic 1, bit stuffing is enabled and the STUFI bit indicates the occurrence of bit stuffs. When STUFF is a logic 0, bit stuffing is disabled and the PDVI bit indicates occurrences of pulse density violation. Also, when STUFF is a logic 0, PCM data passes through XPDE unaltered.

STUFI:

The STUFI bit is valid when pulse stuffing is active. This bit indicates when a bit stuff occurred to eliminate a pulse density violation and that an interrupt was generated due to the bit stuff (if STUFE is logic 1). When pulse stuffing is active, PDVI remains logic 0, indicating that the stuffing has removed the density violation. The STUFI bit is reset to logic 0 once this register is read. If the STUFE bit is also logic 1, the interrupt is also cleared once this register is read.

PDV:

The PDV bit indicates the current state of the pulse density violation indication. When PDV is a logic 1, a violation of the pulse density rule exists. When PDV is a logic 0, no violation of the pulse density rule exists. Note: the PDV indication persists for the duration of the pulse density violation. At its minimum, PDV may be asserted for only 1 bit time, therefore, reading this bit may not return a logic 1 even though a pulse density violation has occurred. When the XPDE is enabled for pulse stuffing, PDV remains logic 0.

PDVI, Z16DI:

The PDVI and Z16DI bits identify the source of a generated interrupt. PDVI is a logic 1 whenever a change in the pulse density violation indication generated an interrupt. PDVI is cleared to 0 when this register is read. Z16DI is a logic 1 whenever 16 consecutive zeros are detected. Z16DI is cleared to 0 when this register is read. Note that the PDVI and Z16DI interrupt indications operate regardless of whether the corresponding interrupt enables are enabled or disabled. When STUFF is set to logic 1, the PDVI and Z16DI bits are forced to logic 0.

Z16DE:

The Z16DE bit enables an interrupt to be generated on the microprocessor INTB pin when 16 consecutive zeros are detected. When Z16DE is set to logic 1, interrupt is generation is enabled. When Z16DE is set to logic 0, interrupt generation is disabled.

PDVE:

The PDVE bit enables an interrupt to be generated on the microprocessor INTB pin when a change in the pulse density is detected. When PDVE is set to logic 1, an interrupt is generated whenever a pulse density violation occurs or when the pulse density ceases to exist (if STUFE is logic 0). When PDVE is set to logic 0, interrupt generation by pulse density violations is disabled.

12 TEST FEATURES DESCRIPTION

Simultaneously asserting the CSB, RDB and WRB inputs causes all output pins and the data bus to be held in a high-impedance state. This test feature may be used for board testing.

Test mode registers are used to apply test vectors during production testing of the TQUAD. Test mode registers (as opposed to normal mode registers) are mapped into addresses 200H-3FFH.

Test mode registers may also be used for board testing. When all of the constituent Telecom System Blocks within the TQUAD are placed in test mode 0, device inputs may be read and device outputs may be forced via the microprocessor interface (refer to the section "Test Mode 0" for details).

Notes on Test Mode Register Bits:

1. Writing values into unused register bits has no effect. Reading unused bits can produce either a logic 1 or a logic 0; hence unused register bits should be masked off by software when read.

2. Writeable test mode register bits are not initialized upon reset unless otherwise noted.

Register 00BH: TQUAD Master Test

Bit	Type	Function	Default
Bit 7		Unused	X
Bit 6	R/W	A_TM[8]	X
Bit 5	R/W	A_TM[7]	X
Bit 4	W	PMCTST	X
Bit 3	W	DBCTRL	0
Bit 2	R/W	IOTST	0
Bit 1	W	HIZDATA	0
Bit 0	R/W	HIZIO	0

This register is used to select TQUAD test features. All bits, except for PMCTST and A_TM[8:7] are reset to zero by a hardware reset of the TQUAD; a software reset of the TQUAD does not affect the state of the bits in this register.

A_TM[8]:

The state of the A_TM[8] bit internally replaces the input address line A[8] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

A_TM[7]:

The state of the A_TM[7] bit internally replaces the input address line A[7] when PMCTST is set. This allows for more efficient use of the PMC manufacturing test vectors.

PMCTST:

The PMCTST bit is used to configure the TQUAD for PMC's manufacturing tests. When PMCTST is set to logic 1, the TQUAD microprocessor port becomes the test access port used to run the PMC manufacturing test vectors. The PMCTST bit is logically "ORed" with the IOTST bit, and is cleared by setting CSB to logic 1.

DBCTRL:

The DBCTRL bit is used to pass control of the data bus drivers to the CSB pin. When the DBCTRL bit is set to logic 1, the CSB pin controls the output enable for the data bus. While the DBCTRL bit is set, holding the CSB pin

high causes the TQUAD to drive the data bus and holding the CSB pin low tri-states the data bus. The DBCTRL bit overrides the HIZDATA bit. The DBCTRL bit is used to measure the drive capability of the data bus driver pads.

IOTST:

The IOTST bit is used to allow normal microprocessor access to the test registers and control the test mode in each block in the TQUAD for board level testing. When IOTST is a logic 1, all blocks are held in test mode and the microprocessor may write to a block's test mode 0 registers to manipulate the outputs of the block and consequently the device outputs (refer to the "Test Mode 0 Details" in this section).

HIZIO, HIZDATA:

The HIZIO and HIZDATA bits control the tri-state modes of the TQUAD . While the HIZIO bit is a logic 1, all output pins of the TQUAD except the data bus are held in a high-impedance state. The microprocessor interface is still active. While the HIZDATA bit is a logic 1, the data bus is also held in a high-impedance state which inhibits microprocessor read cycles.

12.1 Test Mode 0

In test mode 0, the TQUAD allows the logic levels on the device inputs to be read through the microprocessor interface, and allows the device outputs to be forced to either logic level through the microprocessor interface.

To enable test mode 0, the IOTST bit in the Master Test Register is set to logic 1 and the following addresses must be written with 00H: 211H, 219H, 21DH, 221H, 22AH, 22BH, 22CH, 22DH, 235H, 239H, 23CH, 23DH, 241H, 245H, 248H, 249H, 254H, 255H, 258H, 259H, 291H, 299H, 29DH, 2A1H, 2AAH, 2ABH, 2ACH, 2ADH, 2B5H, 2B9H, 2BCH, 2BDH, 2C1H, 2C5H, 2C8H, 2C9H, 2D4H, 2D5H, 2D8H, 2D9H, 311H, 319H, 31DH, 321H, 32AH, 32BH, 32CH, 32DH, 335H, 339H, 33CH, 33DH, 341H, 345H, 348H, 349H, 354H, 355H, 358H, 359H, 391H, 399H, 39DH, 3A1H, 3AAH, 3ABH, 3ACH, 3ADH, 3B5H, 3B9H, 3BCH, 3BDH, 3C1H, 3C5H, 3C8H, 3C9H, 3D4H, 3D5H, 3D8H, and 3D9H. Also, to enable input and output signals to propagate through the Interface blocks, the value 00H must be written to addresses 001H, 081H, 101H, and 181H, the value 01H must be written to addresses 003H, 083H, 103H, and 183H, the value 00H must be written to addresses 004H, 084H, 104H, and 184H, and the value 0CH must be written to addresses 007H, 087H, 107H, and 187H.

Reading the following address locations returns the values for the indicated inputs :

Table 19 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
210H						RCLKI[1]	RDN[1]	RDP[1]
218H					XCLK	TCLKI[1]		
21CH	BRFPI	BRCLK						
234H							TDLSIG[1]	
244H	BTCLK[1]		BTFP[1]		BTSIG[1]			BTPCM[1]
290H						RCLKI[2]	RDN[2]	RDP[2]
298H						TCLKI[2]		
29CH	BRFPI	BRCLK						
2B4H							TDLSIG[2]	
2C4H	BTCLK[2]		BTFP[2]		BTSIG[2]			BTPCM[2]
310H						RCLKI[3]	RDN[3]	RDP[3]
318H					XCLK	TCLKI[3]		
31CH	BRFPI	BRCLK						
334H							TDLSIG[3]	
344H	BTCLK[3]		BTFP[3]		BTSIG[3]			BTPCM[3]
390H						RCLKI[4]	RDN[4]	RDP[4]
398H						TCLKI[4]		
39CH	BRFPI	BRCLK						
3B4H							TDLSIG[4]	
3C4H	BTCLK[4]		BTFP[4]		BTSIG[4]			BTPCM[4]

Table 20 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
210H						RCLKI[1]	RDN[1]	RDP[1]
218H					XCLK	TCLKI[1]		
21CH	BRFPI	BRCLK						
234H							TDLSIG[1]	
244H	BTCLK[1]		BTFP[1]		BTSIG[1]			BTPCM[1]
290H						RCLKI[2]	RDN[2]	RDP[2]
298H						TCLKI[2]		
29CH	BRFPI	BRCLK						
2B4H							TDLSIG[2]	

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
2C4H	BTCLK[2]		BTFP[2]		BTSIG[2]			BTPCM[2]
310H						RCLKI[3]	RDN[3]	RDP[3]
318H					XCLK	TCLKI[3]		
31CH	BRFPI	BRCLK						
334H							TDLSIG[3]	
344H	BTCLK[3]		BTFP[3]		BTSIG[3]			BTPCM[3]
390H						RCLKI[4]	RDN[4]	RDP[4]
398H						TCLKI[4]		
39CH	BRFPI	BRCLK						
3B4H							TDLSIG[4]	
3C4H	BTCLK[4]		BTFP[4]		BTSIG[4]			BTPCM[4]

Writing the following address locations forces the outputs to the value in the corresponding bit position:

Table 21 -

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
210H		INTB[1]						RCLKO[1]
218H						TCLKO[1][2]	TDN[1]	TDP[1]
21CH		INTB[1]					BRFPO[1]	
220H					RFP[1]			
222H		INTB[1]	RDLSIG[1]	RDLCLK[1]				
240H						BRPCM[1]	BRSIG[1]	
						MRD		
244H	TDLCLK[1]							
290H		INTB[1]						RCLKO[2]
298H						TCLKO[2][2]	TDN[2]	TDP[2]
29CH		INTB[1]					BRFPO[2]	
2A0H					RFP[2]			
2A2H		INTB[1]	RDLSIG[2]	RDLCLK[2]				
2C0H						BRPCM[2]	BRSIG[2]	
2C4H	TDLCLK[2]							
310H		INTB[1]						RCLKO[3]
318H						TCLKO[3][2]	TDN[3]	TDP[3]

Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
31CH		INTB[1]					BRFPO[3]	
320H					RFP[3]			
322H		INTB[1]	RDLSIG[3]	RDLCLK[3]				
340H						BRPCM[3]	BRSIG[3]	
344H	TDLCLK[3]							
390H		INTB[1]						RCLKO[4]
398H						TCLKO[4][2]	TDN[4]	TDP[4]
39CH		INTB[1]					BRFPO[4]	
3A0H					RFP[4]			
3A2H		INTB[1]	RDLSIG[4]	RDLCLK[4]				
3C0H						BRPCM[4]	BRSIG[4]	
3C4H	TDLCLK[4]							

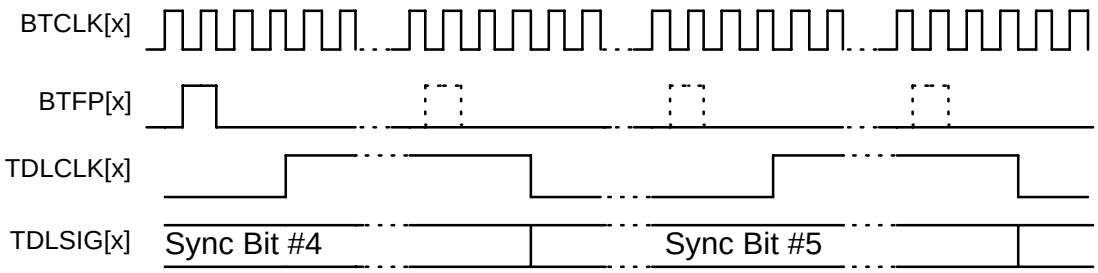
Notes:

1. Writing a logic 1 to any of the block interrupt signals asserts the INTB output low.

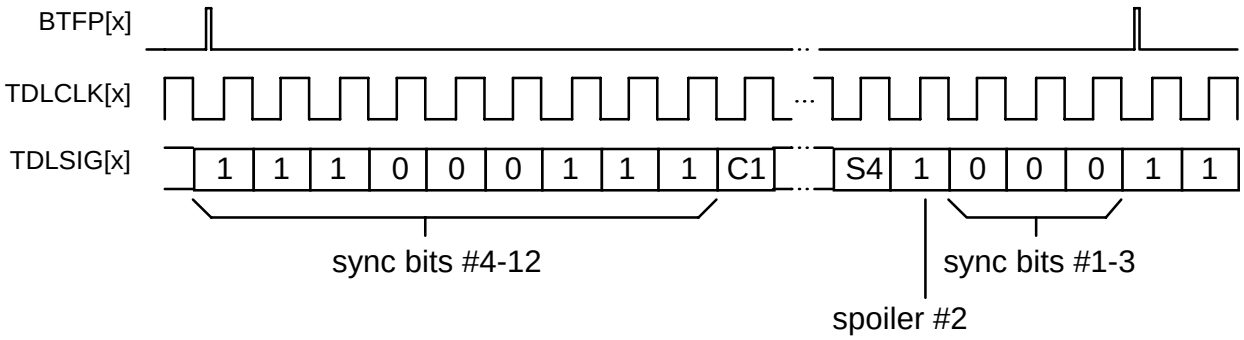
2. To set TCLKO[x], the shown register bit must be set to the desired TCLKO[x] state, then register 21AH, 29AH, 31AH, or 39AH (depending on the quadrant being tested) must be written with 04H and then again with 00H for TCLKO[x] to change state.

13 FUNCTIONAL TIMING DIAGRAMS

Figure 8 - SLC®96 Transmit Datalink Interface

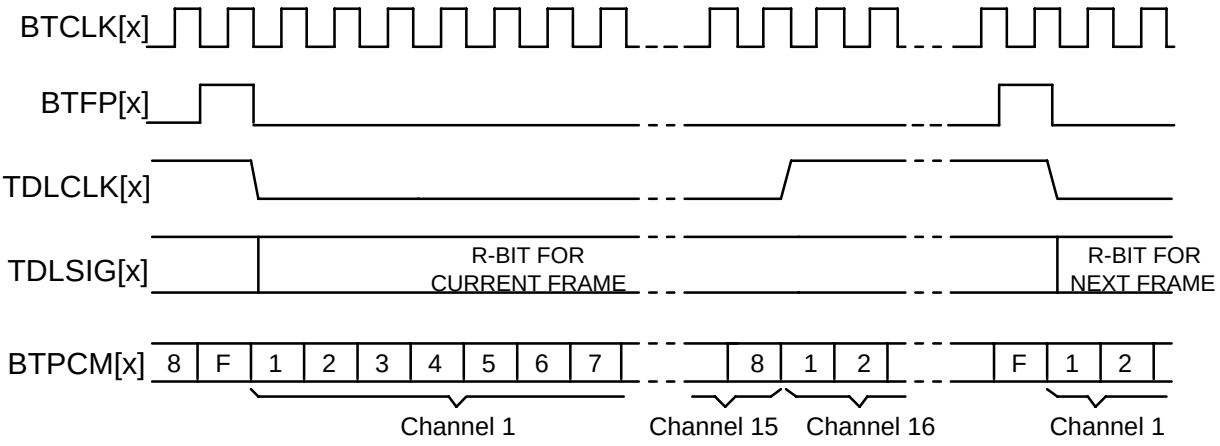


BTFP[x] is the SLC®96 superframe pulse, occurring once every 9 ms. It indicates the presence of the fourth Synchronization pattern bit on the TDLSIG input. The TDLSIG pattern should be aligned to the BTFP[x] superframe pulse as follows so that robbed bit signalling can be inserted in the correct signalling frames:



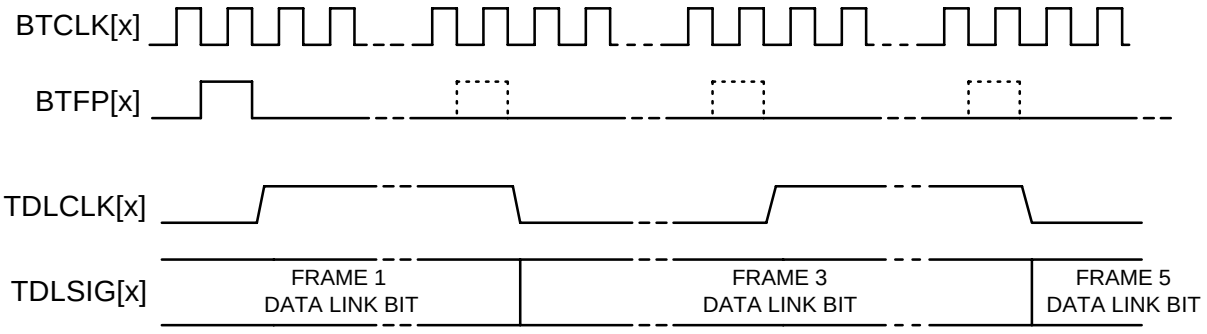
The XBAS is configured to generate SLC®96 formatted data. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the superframe alignment (BTXSFP=1). The dotted frame pulses are shown for reference, indicating the subsequent frame boundaries of the superframe.

Figure 9 - T1DM Transmit Datalink Interface



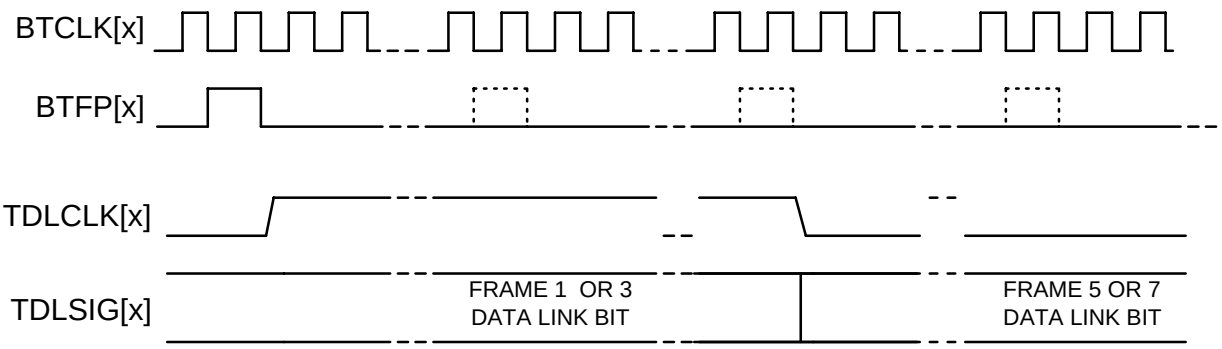
The XBAS is configured to generate T1DM formatted data. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the frame alignment (BTXSFP=0).

Figure 10 - ESF 4Kbit/s Transmit Datalink Interface



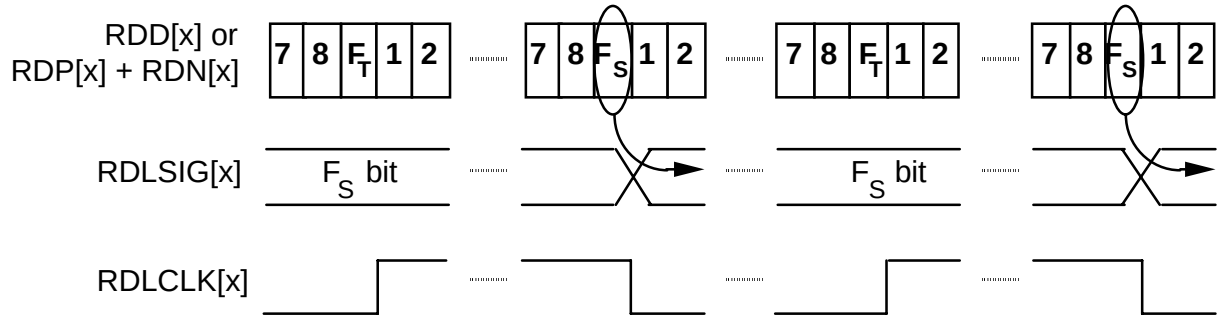
The XBAS is configured to generate ESF formatted data with a 4 kbit/s data link. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the superframe alignment (BTXSFP=1). The dotted frame pulses are shown for reference, indicating the subsequent frame boundaries of the superframe.

Figure 11 - ESF 2Kbit/s Transmit Datalink Interface



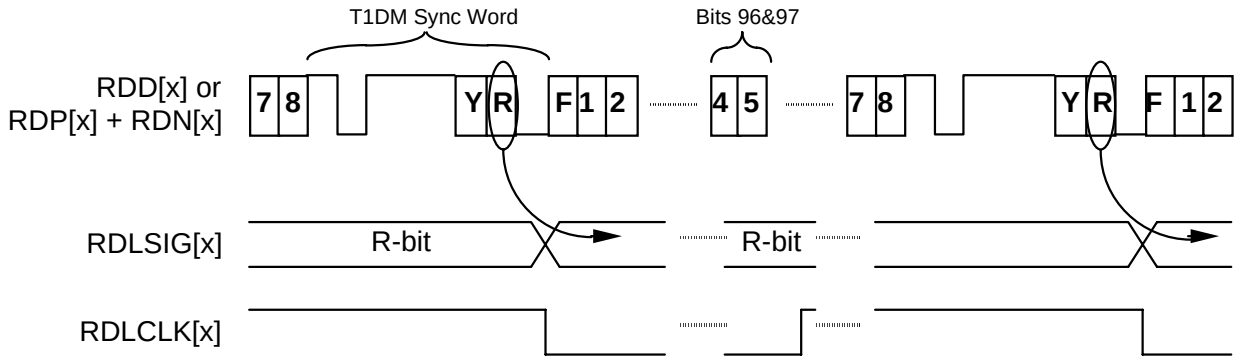
The XBAS is configured to generate ESF formatted data with a 2 kbit/s data link. The data sampled on the TDLSIG[x] input is inserted into the framing bit position of frames 1,5,9,13,17,21 when the "lower" 2 kbit/s channel is selected; the data is inserted into frames 3,7,11,15,19,23 when the "upper" 2 kbit/s channel is selected. The Data Link Options register is programmed to provide access to the data link (TXDMASIG=0). The Transmit Backplane Options is programmed for 1.544MHz data rate, single-rail, with the frame alignment indication representing the superframe alignment (BTXSFP=1). The dotted frame pulses are shown for reference, indicating the subsequent frame boundaries of the superframe.

Figure 12 - SLC®96 Receive Datalink Interface



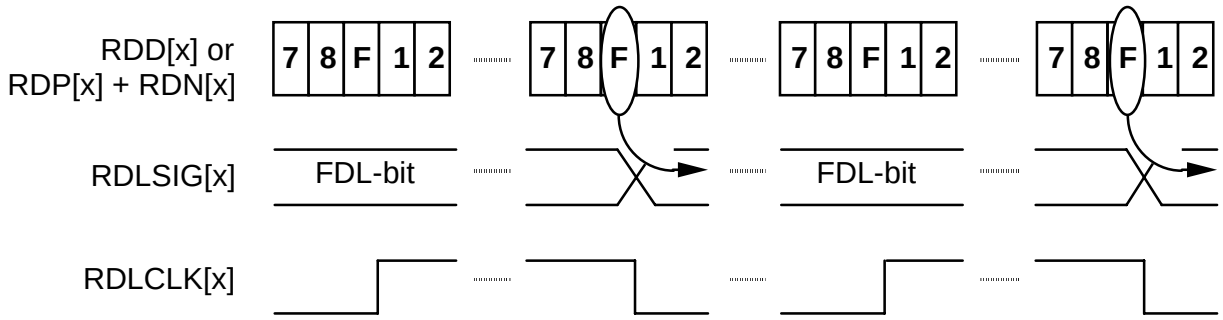
The FRMR is configured to receive SLC®96 formatted data. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

Figure 13 - T1DM Receive Datalink Interface



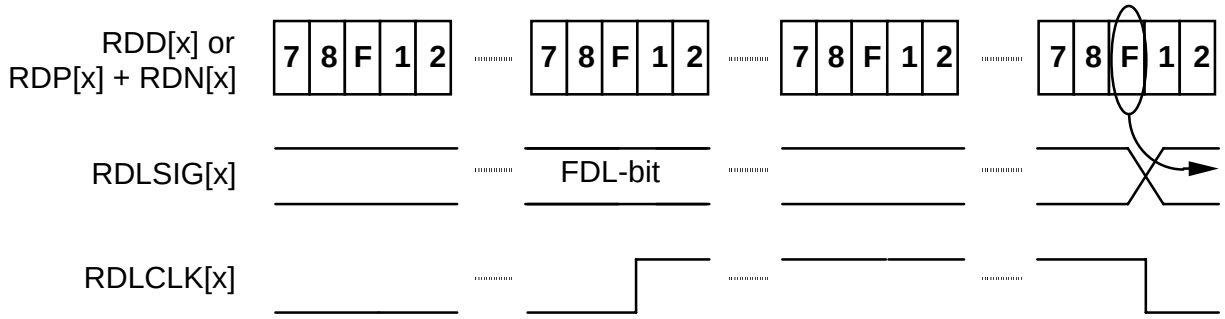
The FRMR is configured to receive T1DM formatted data. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

Figure 14 - ESF 4Kbit/s Receive Datalink Interface



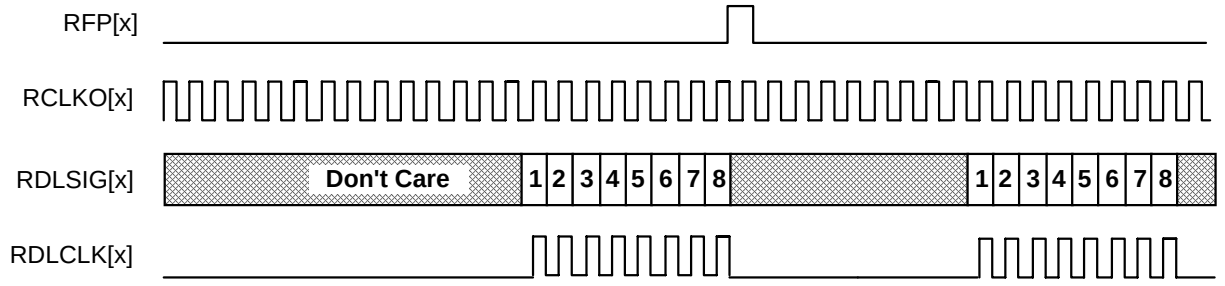
The FRMR is configured to receive ESF formatted data with a 4 kbit/s data link. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

Figure 15 - ESF 2Kbit/s Receive Datalink Interface



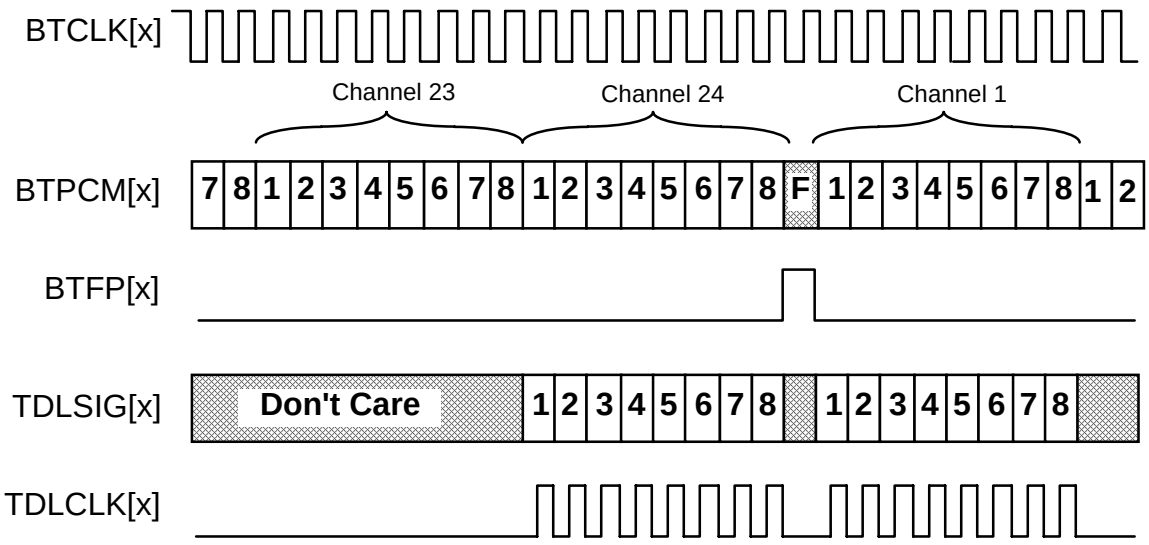
The FRMR is configured to receive ESF formatted data with a 2 kbit/s data link. The data output on the RDLSIG pin is extracted from the framing bit position of frames 1,5,9,13,17,21 when the "lower" 2 kbit/s channel is selected; the data is extracted from frames 3,7,11,15,19,23 when the "upper" 2 kbit/s channel is selected. The Data Link Options register is programmed to provide access to the extracted data link (RXDMASIG=0).

Figure 16 - ReceiveChannel Interface



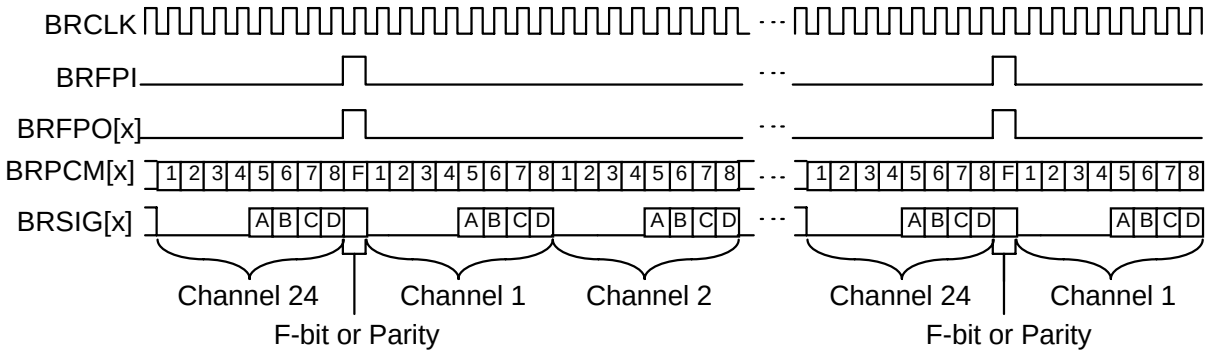
The Data Link Options register is programmed to provide access to the receive DS0 channels (RXDMASIG=X, RXDCHAN=1). In this example, the CH[2] and CH[24] bits in the Channel Select registers are set. The RDLCLK[x] output clock is gapped so that it is only active for channels with the associated CH bit set. If either SRSFP or ALTRFP is set, then RFP[x] will pulse only during the appropriate frames.

Figure 17 - Transmit Channel Interface



The Data Link Options register is programmed to provide access to the transmit DS0 channels (TXDMASIG=X, TXDCHAN=1). In this example, the CH[1] and CH[24] bits in the Channel Select registers are set. The TDLCLK output clock is gapped so that it is only active for channels with the associated CH bit set.

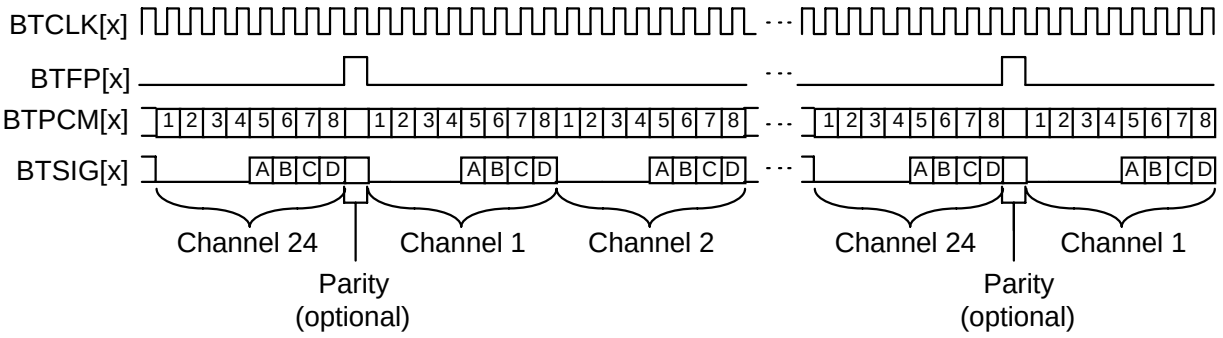
Figure 18 - 1.544MHz Receive Backplane Interface



The Receive Backplane is configured to generate 1.544MHz, single-rail formatted data with frame alignment indication. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=0. (If BRXSFP=1, the BRFPO output only pulses on the frame boundary indication the start of the superframe alignment; if ALTBRFP=1, the BRFPO[x] output pulses on every second indication of either the frame or the superframe boundary). The first bit

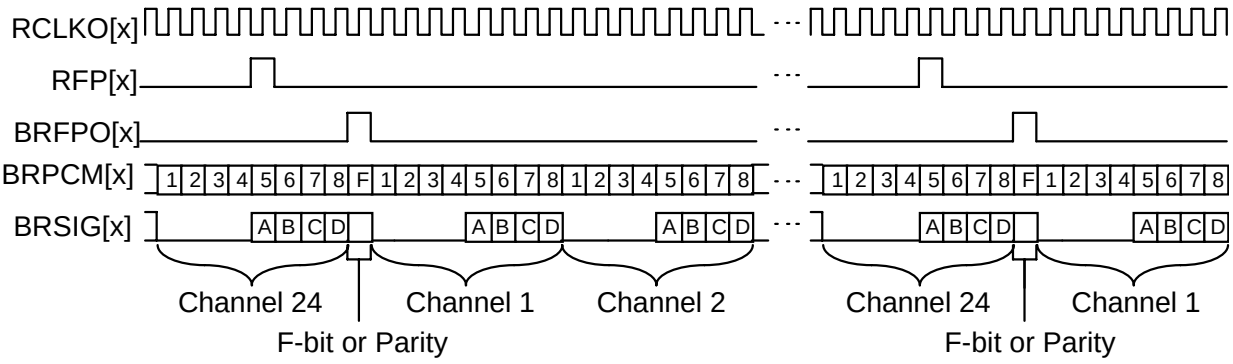
position of the frame may be configured to carry the F-bit value or the parity value of the previous 192 bit positions.

Figure 19 - 1.544MHz Transmit Backplane Interface



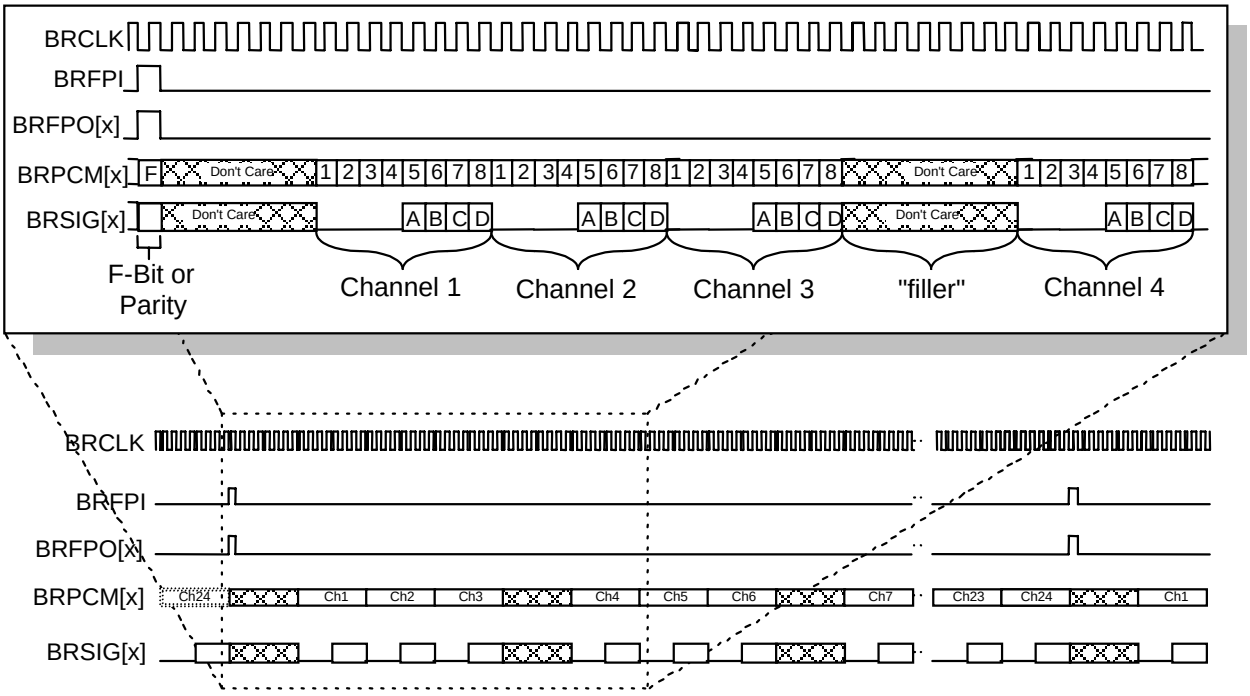
The Transmit Backplane is configured to receive 1.544MHz, single-rail formatted data with frame alignment indication. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=0. (If BTXSFP=1, the BTFP[x] input should only pulse on the frame boundary indicating the start of the superframe alignment. The first bit position of the frame may be used to provide parity protection over the previous 192 bit positions. Parity errors are indicated by the BTPCMPI and BTSIGPI bits of the Backplane Parity Configuration and Status register and by a maskable interrupt.

Figure 20 - 1.544MHz Receive Backplane Interface with ELSTBYP=1



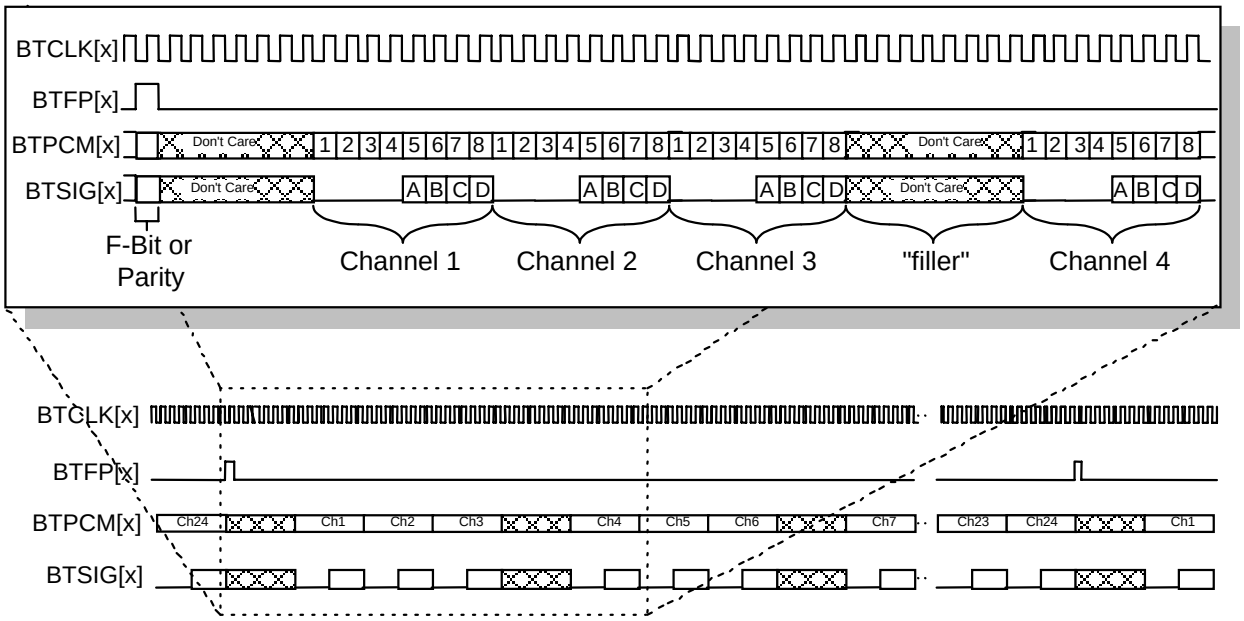
The Receive Backplane is configured to generate 1.544MHz, single-rail formatted data with frame alignment indication and with the ELST bypassed (ELSTBYP=1). The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=0, and RCLKOSEL=0. The first bit position of the frame may be configured to carry the F-bit value or the parity value of the previous 192 bit positions. The backplane output signals are now timed off of the output clock RCLKO[x] instead of the input clock BRCLK.

Figure 21 - - 2.048MHz Receive Backplane Interface



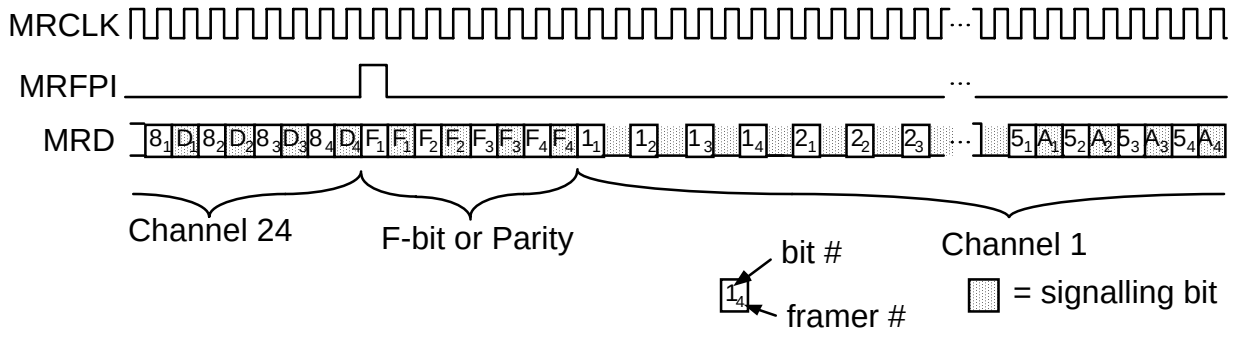
The Receive Backplane is configured to generate 2.048MHz, single-rail formatted data with frame alignment indication. The Receive Backplane Options register is programmed to BRX2M=1, BRX2RAIL=0, BRXSFP=0. (If BRXSFP=1, the BRFPO output only pulses on the frame boundary indication the start of the superframe alignment; if ALTBRFP=1, the BRFPO[x] output pulses on every second indication of either the frame or the superframe boundary). The first bit position of the frame may be configured to carry the F-bit value or to be the parity over the defined bits in the previous frame.

Figure 22 - 2.048MHz Transmit Backplane Interface



The Transmit Backplane is configured to receive 2.048MHz, single-rail formatted data with frame alignment indication. The Transmit Backplane Options register is programmed to BTX2M=1, BTX2RAIL=0, BTXSFP=0. (If BTXSFP=1, the BTFP[x] input should only pulse on the frame boundary indicating the start of the superframe alignment.) If desired, the contents of the F-bit placeholder bit positions can be bypassed around the XBAS and be inserted into the outgoing stream via the FBITBYP, CRCBYP, or FDLBYP bits of register 6, the Transmit Framing and Bypass Options register. Alternatively, the first bit position of the frame may be used to provide parity protection over the defined bits in the previous frame. Parity errors are indicated by the BTPCMPI and BTSIGPI bits of the Backplane Parity Configuration and Status register and by a maskable interrupt.

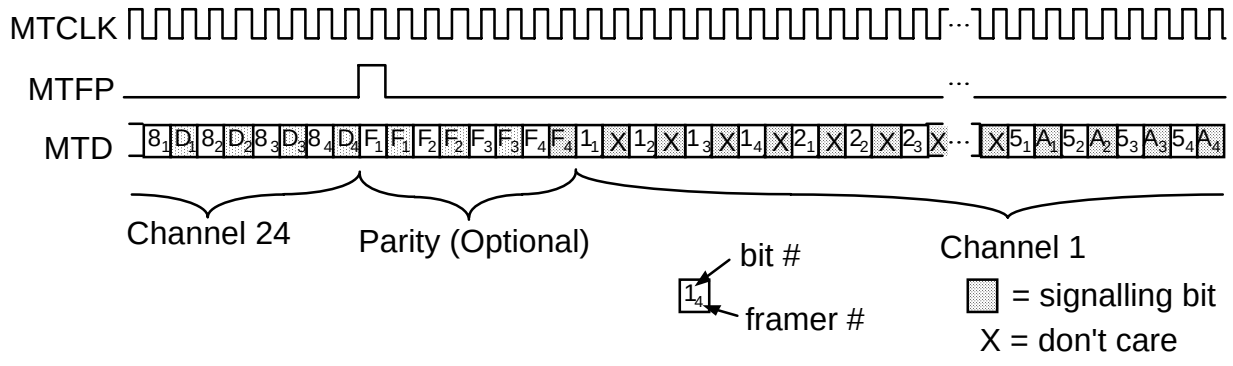
Figure 23 - Multiplexed Receive Backplane Interface



The Receive Backplane is configured to generate bit interleaved 12.352MHz data. PCM and signaling for all four receivers are presented on a single pin, MRD. The subscripts represent the index of the particular DS1 stream. The Receive Backplane Options register for each receiver is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=0 and the MENB input is low. The eight bit positions of the frame may be configured to carry the F-bit value or to be the parity over the previous 192 bit positions for each DS1 stream.

When BRX2M=1, the data is presented as a 16.384MHz bit interleaved data stream. The individual bit streams are multiplexed in the same order as the 12.352MHz case, but the format of each stream is consistent with the 2.048MHz Receive Backplane Interface illustrated above. The first bit position of the frame for each PCM and signaling stream may be configured to carry the F-bit value or to be the parity over the defined bits in the previous frame.

Figure 24 - Multiplexed Transmit Backplane Interface

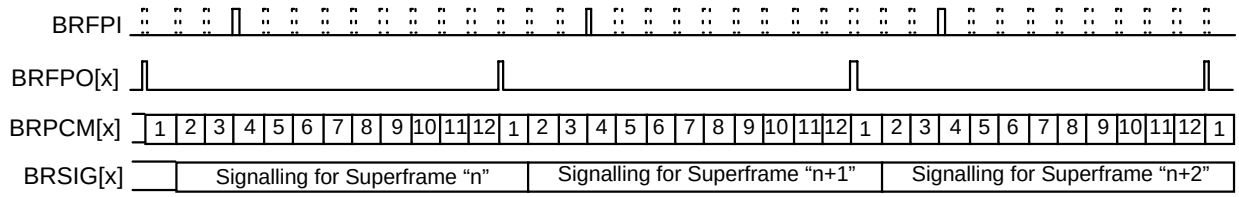


The Transmit Backplane is configured to expect bit interleaved 12.352MHz data. PCM and signaling for all four receivers are presented on a single pin, MTD. The

subscripts represent the index of the particular DS1 stream. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=0 and the MENB input is low. (If BTXSFP=1, the MTFP input should only pulse on the frame boundary indicating the start of the superframe alignment.) The first eight bit positions of the frame may be used to provide parity protection over the previous 192 bit positions for each DS1 stream. Parity errors are indicated by the BTPCMPI and BTSIGPI bits of each Backplane Parity Configuration and Status register and by a maskable interrupt.

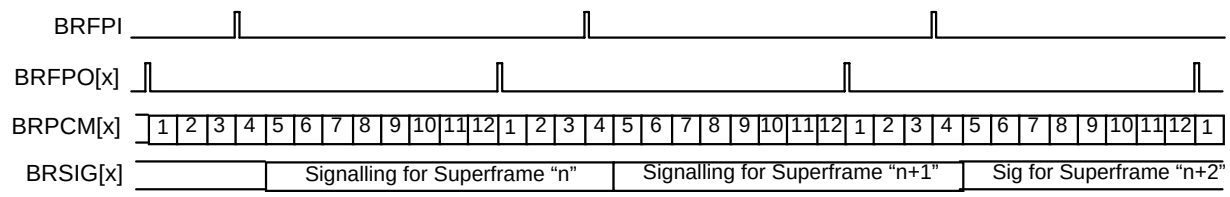
When BTX2M=1, the data is expected to be 16.384MHz bit interleaved data stream. The individual bit streams are multiplexed in the same order as the 12.352MHz case, but the format of each stream is consistent with the 2.048MHz Transmit Backplane Interface illustrated above.

Figure 25 - 1.544MHz Receive Backplane Interface - without signaling alignment



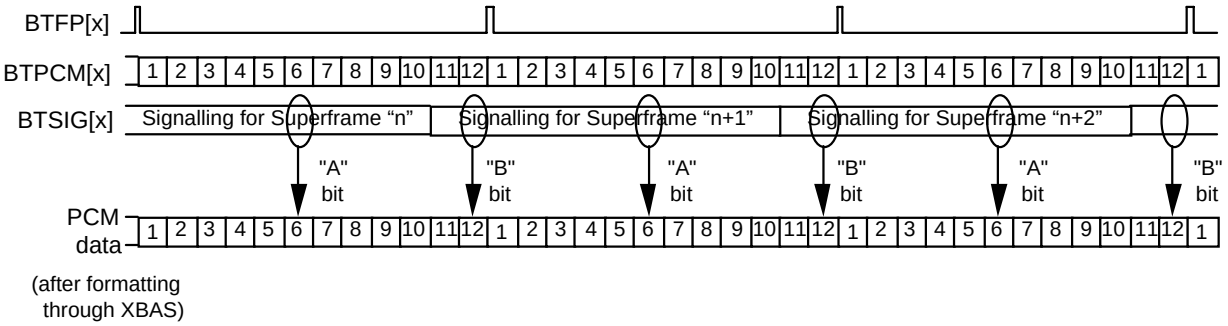
The FRMR is configured to receive SF formatted data and the Receive Backplane is configured to output 1.544MHz, single-rail formatted data with superframe alignment indication, and no signaling alignment. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=1; the TQUAD Receive Options register is programmed to SIGAEN=0, TXSIGA=X, or SIGAEN=1 and TXSIGA=1. The pulse applied on BRFPI can repeat every frame (dotted pulses) or every superframe, and forces only frame alignment of the PCM data and extracted signaling to the location of the input BRFPI. The superframe boundary of the signaling data lags the output superframe pulse on BRFPO[x] by one frame.

Figure 26 - 1.544MHz Receive Backplane Interface - with signaling alignment



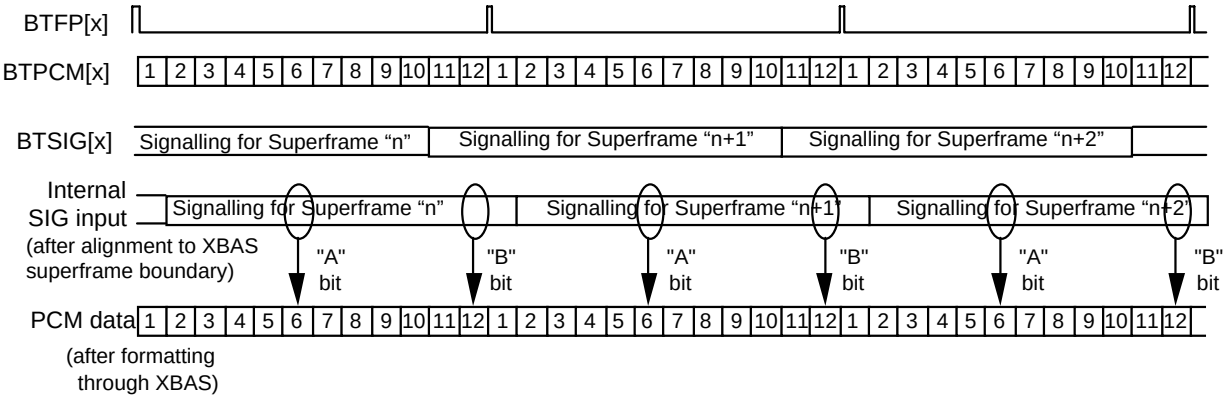
The FRMR is configured to receive SF formatted data and the Receive Backplane is configured to output 1.544MHz, single-rail formatted data with superframe alignment indication, and signaling alignment. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=1; the TQUAD Receive Options register is programmed to SIGAEN=1 and TXSIGA=0. The pulse applied on BRFPI is expected to repeat every superframe, and forces both frame alignment of the PCM data and superframe alignment of the extracted signaling to the location of the input BRFPI. The superframe boundary of the PCM data is indicated by the output superframe pulse on BRFPO[x], which is separated by an integral number of frames from the BRFPI pulse. The superframe boundary of the signaling data lags the input superframe pulse on BRFPI by one frame.

Figure 27 - 1.544MHz Transmit Backplane Interface - without signaling alignment



The XBAS is configured to transmit SF formatted data and the Transmit Backplane is configured to accept 1.544MHz, single-rail formatted data with superframe alignment indication, and no signaling alignment. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=1; the TQUAD Receive Options register is programmed to SIGAEN=0, TXSIGA=X, or SIGAEN=1 and TXSIGA=0. The pulse applied on BTFP[x] is expected to repeat every superframe, and forces superframe alignment of the transmitted PCM data. A potential problem arises when the signaling data on BTSIG[x] is allowed to change midway through a transmit superframe boundary defined by the BTFP[x] pulse. Under this condition the transmitted signaling bits are taken from two separate sets of signaling bits (i.e. the "A" bit is taken from superframe "n" and the "B" bit is taken from superframe "n+1"), which can generate non-existent signaling states. This same situation can exist if XBAS is allowed to generate its own superframe alignment and BTFP[x] pulses every frame (i.e. BTXSFP=0). Under this condition the signaling bits may also be taken from two separate superframes.

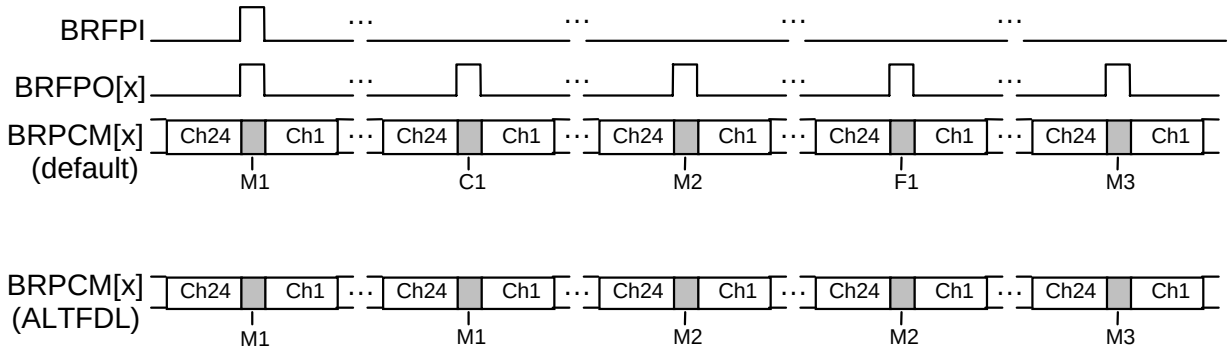
Figure 28 - 1.544MHz Transmit Backplane Interface - with signaling alignment



The XBAS is configured to transmit SF formatted data and the Transmit Backplane is configured to accept 1.544MHz, single-rail formatted data with superframe alignment indication, and signaling alignment. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=1; the TQUAD Receive Options register is programmed to SIGAEN=1 and TXSIGA=1. The pulse applied on BTFP[x] is expected to repeat every superframe, and forces superframe alignment of the transmitted PCM data. Internally, the signaling data on BTSIG[x] is aligned to the internal superframe pulse generated by XBAS, thereby ensuring the signaling data does not change midway through the superframe. This internally-aligned stream is passed on to the XBAS for insertion into the transmit PCM. The "A" and "B" signaling bits now are taken from the same superframe set of bits, eliminating the potential transmission of non-existent signaling states.

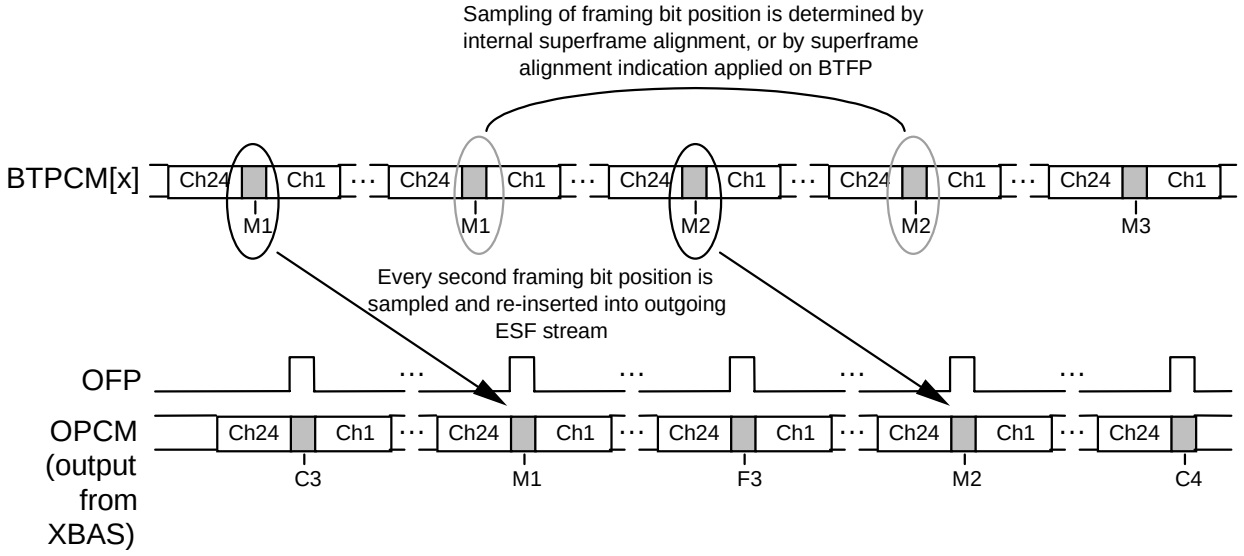
In a system that ensures that the transmit signaling changes only on the indicated superframe boundary on BTFP[x], the signaling aligner in the transmit direction is unnecessary.

Figure 29 - 1.544MHz Receive Backplane Interface with ALTFDL



The FRMR is configured to receive ESF formatted data and the Receive Backplane is configured to output 1.544MHz, single-rail formatted data with frame alignment indication, and signaling alignment. The Receive Backplane Options register is programmed to BRX2M=0, BRX2RAIL=0, BRXSFP=0; the TQUAD Receive Options register is programmed to SIGAEN=1 and TXSIGA=0. When ALTFDL=0 is programmed in the Receive Backplane Options register, the PCM data on BRPCM[x] contains all the overhead bits (M-bits, CRC6 bits, and F-bits) in the framing bit positions. When ALTFDL=1 is programmed in the Receive Backplane Options register, the PCM data on BRPCM[x] contains only the data link bits in the framing bit position, with each M-bit duplicated and occupying the subsequent framing bit location (overwriting the CRC-6 or F-bit).

Figure 30 - 1.544MHz Transmit Backplane Interface-with ALTFDL



The XBAS is configured to transmit ESF formatted data and the Transmit Backplane is configured to accept 1.544MHz, single-rail formatted data. The Transmit Backplane Options register is programmed to BTX2M=0, BTX2RAIL=0, BTXSFP=0; the TQUAD Receive Options register is programmed to SIGAEN=0 and TXSIGA=X. The data link, with each bit duplicated, is carried in the framing bit position on the BTPCM[x] stream. To transmit this data link in the correct position in the ESF-formatted stream, the FDL bypass function must be used by programming the FDLBYP=1 in the Transmit Framing and Bypass Options register.

14 OPERATIONS

14.1 Configuring the TQUAD from Reset

After a system reset (either via the RSTB pin or via the RESET register bit), the TQUAD will default to the following settings:

Table 22 - Default Settings

Setting	Receiver Section	Transmitter Section
Framing Format	SF	SF
Line Code	B8ZS	AMI
DS1 interface	• Pins RDP/RDD[x] and RDN/RLCV[x] active as digital inputs RDP[x] and RDN[x] and used for clock and data recovery	• TDP[x], TDN[x] outputs NRZ data updated on falling TCLKO[x] edge
System Backplane	• 1.544MHz data rate • BRPCM[x], BRSIG[x] active • BRFPO[x] indicates frame pulses	• 1.544MHz data rate • BTPCM[x] active • BTSIG[x] inactive • BTFP[x] indicates frame alignment
Data Link	• internal RFDL disabled • RDLSIG[x] and RDLCLK[x] outputs held low	• internal XFDL disabled • TDLCLK[x] output held low, TDLSIG[x] input ignored
Options	• ELST not bypassed • RFP held low • PMON accumulates OOFs (not COFAs)	• Signaling alignment disabled • F, CRC, FDL bit bypass disabled
Timing Options	Not applicable	• Digital jitter attenuation enabled, with TCLKO[x] referenced to BTCLK[x]
Diagnostics	• All diagnostic modes disabled	• All diagnostic modes disabled

In the following tables the "Addr Offset" is the address relative to 000H, 080H, 100H or 180H, depending on which framer is being configured.

To configure the TQUAD for ESF framing format, after a reset, the following registers should be written with the indicated values:

Table 23 - ESF Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	00H	Select B8ZS line code for receiver
Write XBAS Configuration Register	44H	3XH	Select B8ZS, enable for ESF in transmitter (bits defined by 'X' determine the FDL data rate & Zero Code suppression algorithm used)
Write FRMR Configuration Register	20H	1XH or 5XH or 9XH	Select ESF, 2 of 4 OOF threshold Select ESF, 2 of 5 OOF threshold Select ESF, 2 of 6 OOF threshold (bits defined by 'X' determine the FDL data rate, should be same as those written to XBAS)
Write RBOC Enable Register	2AH	00H or 02H	Enable 8 out of 10 validation Enable 4 out of 5 validation
Write ALMI Configuration Register	2CH	1XH	Select ESF (bits defined by 'X' determine the ESF YELLOW data rate, should be same as those written to FRMR)

Action	Addr Offset	Data	Effect
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	1XH	Select ESF (bits defined by 'X' should be same as those written to FRMR)

To configure the TQUAD for SLC®96 framing format, after a reset, the following registers should be written with the indicated values:

Table 24 - SLC®96 Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	80H	Select AMI line code for receiver
Write XBAS Configuration Register	44H	08H	Select AMI, enable for SLC®96 in transmitter
Write FRMR Configuration Register	20H	08H or 48H or 88H	Select SLC®96, 2 of 4 OOF threshold Select SLC®96, 2 of 5 OOF threshold Select SLC®96, 2 of 6 OOF threshold
Write ALMI Configuration Register	2CH	08H	Select SLC®96
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern

Action	Addr Offset	Data	Effect
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	08H	Select SLC®96

To configure the TQUAD for SF framing format, after a reset, the following registers should be written with the indicated values:

Table 25 - SF Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	80H	Select AMI line code for receiver
Write XBAS Configuration Register	44H	00H	Select AMI, enable for SF in transmitter
Write FRMR Configuration Register	20H	00H or 40H or 80H	Select SF, 2 of 4 OOF threshold Select SF, 2 of 5 OOF threshold Select SF, 2 of 6 OOF threshold
Write ALMI Configuration Register	2CH	00H	Select SF
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	00H	Select SF

To configure the TQUAD for T1DM framing format, after a reset, the following registers should be written with the indicated values:

Table 26 - T1DM Frame Format

Action	Addr Offset	Data	Effect
Write CDRC Configuration Register	10H	80H	Select AMI line code for receiver
Write XBAS Configuration Register	44H	04H or 0CH	Select AMI, enable for T1DM in transmitter
Write FRMR Configuration Register	20H	04H or 44H or 84H	Select T1DM, 2 of 4 OOF threshold Select T1DM, 2 of 5 OOF threshold Select T1DM, 2 of 6 OOF threshold
Write ALMI Configuration Register	2CH	04H or 0CH	Select T1DM with standard RED integration Select T1DM with alternate RED integration
Write IBCD Configuration Register	3CH	00H	Enable Inband Code detection
Write IBCD Activate Code Register	3EH	08H	Program Loopback Activate Code pattern
Write IBCD Deactivate Code Register	3FH	44H	Program Loopback Deactivate Code pattern
Write SIGX Configuration Register	40H	04H	Disable robbed bit signaling extraction

To access the Performance Monitor Registers, the following polling sequence should be used:

Table 27 - PMON Polling Sequence

Action	Addr Offset	Data	Effect
Write PMON LCV Count (LSB) Register (To transfer the PMON registers for all four framers, write the Revision/Chip ID/Global PMON Update register.)	4AH	00H	Latch performance data into PMON registers
Read LCV Count (LSB) Register	4AH		Read least significant byte of line code violation count
Read LCV Count (MSB) Register	4BH		Read most significant byte of line code violation count
Read BEE Count (LSB) Register	4CH		Read least significant byte of bit error event count
Read BEE Count (MSB) Register	4DH		Read most significant byte of bit error event count
Read FER Count Register	4EH		Read Framing bit error count
Read OOF/COFA Count Register	4FH		Read out-of-frame event count (or change of frame alignment event count if CCOFA bit in TQUAD Receive Options Register is set)

To configure the TQUAD to utilize the internal HDLC transmitter and receiver, the following registers should be written with the indicated values:

Table 28 - ESF FDL Processing

Action	Addr Offset	Data	Effect
Write TQUAD Datalink Options Register	02H	A0H	Enable RFDL & XFDL to process the ESF Facility Datalink (XBAS and FRMR must be configured for ESF framing format). The DMA signals are available on RDLINT[x], RDLEOM[x], TDLINT[x], TDLUDR[x] outputs.

14.2 Using the Internal FDL Transmitter

Upon reset of the TQUAD, the XFDL should be disabled by setting the EN bit in the XFDL Configuration Register to logic 0. If data is not ready to be transmitted, the TDLINT[x] output should also be masked by setting the INTE bit to logic 0.

If the internal HDLC controller is to be used, the XFDL Configuration Register should be initialized for transmission: if the FCS is desired, the CRC bit should be set to logic 1; if the block is to be used in interrupt driven mode, interrupts should be enabled by setting the INTE bit to logic 1. Finally, the XFDL can be enabled by setting the EN bit to logic 1.

The XFDL can be used in a polled, interrupt driven, or DMA-controlled mode for the transfer of frame data. In the polled mode, the TDLINT[x] and TDLUDR[x] outputs of the XFDL are not used, and the processor controlling the XFDL must periodically read the XFDL Status Register to determine when to write to the XFDL Transmit Data Register. In the interrupt driven mode, the processor controlling the XFDL uses either the TDLINT[x] output, or the main processor INTB output and the interrupt source registers, to determine when to write to the XFDL Transmit Data Register. In the DMA controlled mode, the TDLINT[x] output of the XFDL is used as a DMA request input to the DMA controller, and the TDLUDR[x] output is used as an interrupt to the processor to allow handling of exceptions. The TDLUDR[x] output can also be enabled to generate a processor interrupt through the common INTB output via the TDLUDRE bit in the Datalink Options register.

14.2.1 Polled Mode

If the XFDL data transfer is operating in the polled mode (TXDMASIG, TXDCHAN, TDLINTE, and TDLUDRE bits in the Datalink Options Register are set to logic 0), then a timer periodically starts up a service routine, which should process data as follows:

1. Read the XFDL Interrupt Status Register and poll the UDR and INT bits.

2. If UDR=1, then clear the UDR bit in the XFDL Interrupt Status Register to logic 0, and restart the current frame. Go to step 1.

3. If INT=1, then:

   a) If there is still data to send, then write the next data byte to the XFDL Transmit Data Register;

   b) If all bytes in the frame have been sent, then set the EOM bit in the XFDL Configuration Register to logic 1.

4. If EOM bit was set to logic 1 in step 3b, then:

   a) Read the XFDL Interrupt Status Register and check the UDR bit.

   b) If UDR=1 then reset the UDR bit in the XFDL Interrupt Status Register

   and the EOM bit in the XFDL Configuration Register to logic 0, and retransmit the last frame.

5. Go to step 1.

14.2.2 Interrupt Mode

In the case of interrupt driven data transfer, the TDLINT[x] output is connected to the interrupt input of the processor, and the interrupt service routine should process the data exactly as described above for the polled mode. The INTE bit in the XFDL Configuration Register must be set to logic 1. Alternately, the INTB output can be connected to the interrupt input of the processor if the TDLINTE bit of the Datalink Options Register is set to logic 1. If this mode is used, additional polling of the Interrupt ID/Clock Monitor and Master Interrupt Source registers must be performed to identify the cause of the interrupt before the initiating the interrupt service routine.

14.2.3 DMA-Controlled Mode

The XFDL can also be used with a DMA controller to process the frame data. In this case, the TDLUDR[x] output is connected to the processor interrupt input. The TDLINT[x] output of the XFDL is connected to the DMA request input of the DMA controller. The INTE bit in the XFDL Configuration Register must be set to logic 1 before enabling the XFDL. The DMA controller writes a data byte to the XFDL whenever the TDLINT[x] output is high. If there is a problem during transmission and an underrun condition occurs, then the TDLUDR[x] output goes high and the processor is interrupted. The processor can then halt the DMA controller, reset the UDR bit in the XFDL Interrupt Status Register, reset the frame data pointers, and restart the DMA controller to resend the data frame. After the message transmission is completed, the DMA controller must initiate a write to set the EOM bit in the XFDL Configuration Register and then verify that TDLUDR[x] is not set prior to setting EOM.

14.3 Using the Internal FDL Receiver

On power up of the TQUAD, the RFDL should be disabled by setting the EN bit in the Configuration Register to logic 0. The RFDL Interrupt Control/Status Register should then be initialized to select the FIFO buffer fill level at which an interrupt will be generated.

After the Interrupt Control/Status Register has been written to, the RFDL can be enabled at any time by setting the EN bit in the Configuration Register to logic 1. When the RFDL is enabled, it will assume that the link status is idle (all ones) and immediately begin searching for flags. When the first flag is found, an interrupt will be generated (if enabled), and the byte received before the first flag was detected will be written into the FIFO buffer. Because the FLG and EOM bits are passed through the buffer, this dummy write allows the RFDL Status Register to accurately reflect the current state of the data link. A RFDL Status Register read after a RFDL Data Register read of the dummy byte will return EOM as logic 1 and FLG as logic 1. The first interrupt and data byte read after the RFDL is enabled (or TR bit set to logic 1) is an indication of the link status, and the data byte should therefore be discarded. It is up to the controlling processor to keep track of the link state as idle (all ones or bit-oriented messages active) or active (flags received).

The RFDL can be used in a polled, interrupt driven, or DMA controlled mode for the transfer of frame data.

14.3.1 Polled Mode

In the polled mode, the RDLINT[x] and RDLEOM[x] outputs of the RFDL are not used, and the processor controlling the RFDL must periodically read the RFDL Interrupt/Status to determine when to read the Data Register. If the RFDL data transfer is operating in the polled mode, entry to the service routine is from a timer. The processor service routine should process the data in the following order:

1. Poll the INT bit in the RFDL Interrupt/Status Register until it is set to logic 1. Once INT is set to logic 1, then proceed to step 2.

2. Read the RFDL Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

   c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

   ELSE

   d) Save the last data byte read.

   e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

   f) If FE=0, then go to step 2, else go to step 1.

The link state is typically a local software variable. The link state is inactive if the RFDL is receiving all ones or receiving bit-oriented codes which contain a sequence of eight ones. The link state is active if the RFDL is receiving flags or data.

14.3.2 Interrupt Mode

In the interrupt driven mode, the processor controlling the RFDL uses either the RDLINT[x] output, or the main processor INTB output (RDLINTE bit of the

Datalink Options Register is set to logic 1), the Interrupt ID/Clock Monitor, and the Interrupt Source Registers, to determine when to read the Data Register. The RXDMASIG bit in the Datalink Options Register should be set to logic 1. RDLINTE of the same register should be set to logic 1 if the INTB output is used as the interrupt source. The processor interrupt service routine should process the data in the following order:

1. Wait for an interrupt originating from the RFDL. Once the interrupt is set, then proceed to step 2.

2. Read the RFDL Data Register.

3. Read the RFDL Status Register to check for the following:

   a) If OVR=1, then discard the current frame and go to step 1.

   ELSE

   b) If FLG=0 (i.e. an abort has been received) and the link state was active, then set the link state to inactive, discard the current frame, and go to step 1.

   c) If FLG=1 and the link state was inactive, then set the link state to active, discard the last data byte, and go to step 1.

   ELSE

   d) Save the last data byte read.

   e) If EOM=1, then read the CRC and NVB[2:0] bits of the RFDL Status Register to process the frame properly.

   f) If FE=0, then go to step 2, else go to step 1.

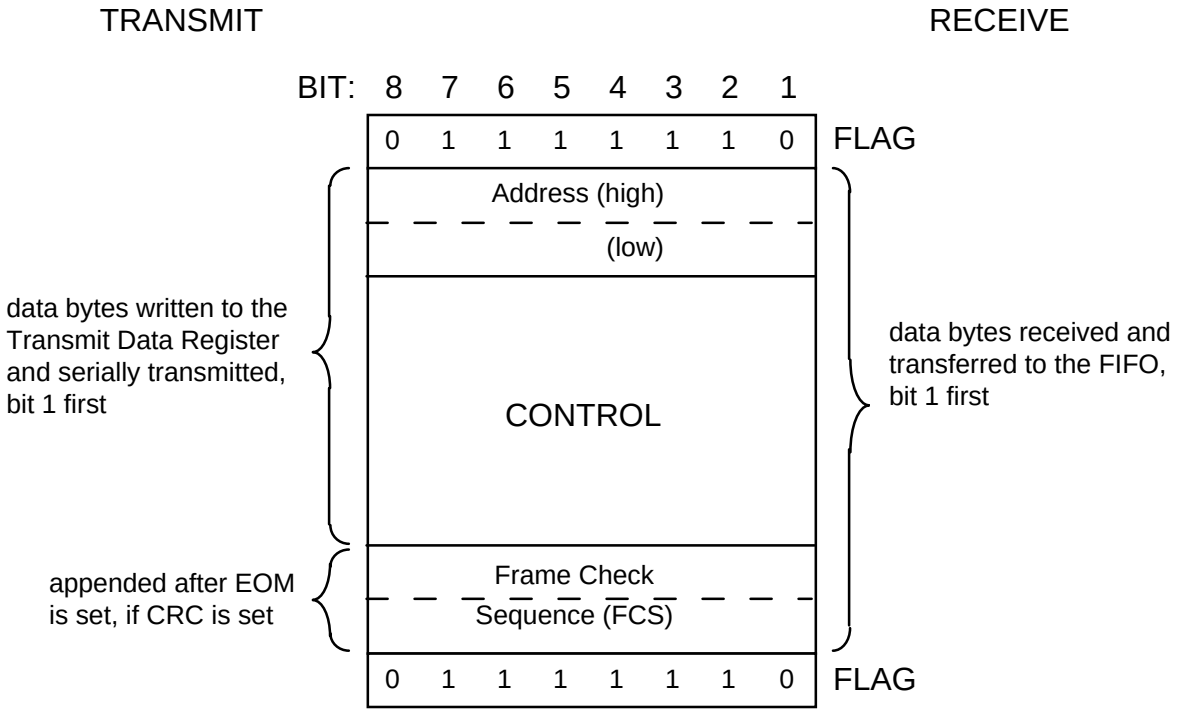
14.3.3 DMA-Controlled Mode

The RFDL can also be used with a DMA controller to process the frame data. In the DMA controlled mode, the RDLINT[x] output of the RFDL is used as a DMA request input to the DMA controller, and the RDLEOM[x] output is used as an interrupt to the processor to allow handling of exceptions and as an indication of when to process a frame. The RXDMASIG bit of the Datalink Options Register should be set to logic 1.

The RDLINT[x] output of the RFDL is connected through a gate to the DMA request input of the DMA controller to optionally inhibit the DMA request if the RDLEOM[x] output is high. The DMA controller reads the data bytes from the

RFDL whenever the RDLINT[x] output is high. When the current byte read from the Data Register is the last byte in a frame (due to an end-of-message or an abort), or an overrun condition occurs, then the RDLEOM[x] output goes high. The DMA controller is inhibited from reading any more bytes, and the processor is interrupted. The processor can then halt the DMA controller, read the Status Register, process the frame, and finally reset the DMA controller to process the data for the next frame. The RDLEOM[x] output can optionally be enabled to generate a processor interrupt through the common INTB output via the RDLEOME bit in the Datalink Options register, rather than tying the RDLEOM[x] output directly to the microprocessor. This allows a central microprocessor controlling the TQUAD operation to also respond to conditions affecting the DMA servicing of RFDL. When using the INTB output, the central processor must poll the Interrupt ID/Clock Monitor, and the Interrupt Source Registers to identify the source of the interrupt before beginning any interrupt service routine.

Figure 31 - Typical Data Frame



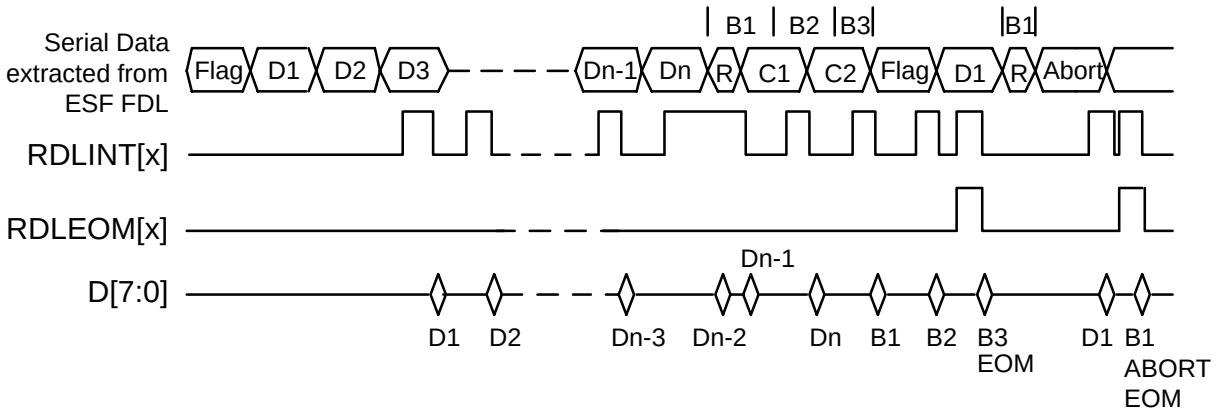
Bit 1 is the first serial bit to be transmitted or received.

Both the address and control bytes must be supplied by an external processor and are shown for reference purposes only.

14.3.4 Key used on subsequent diagrams

Flag	- flag sequence (01111110)
Abort	- abort sequence (01111111)
D1 - Dn	- n frame data bytes
R	- remainder bits (less than 8)
C1, C2	- CRC-CCITT information
B1, B2, B3	- groupings of 8 bits

Figure 32 - RFDL Normal Data and Abort Sequence



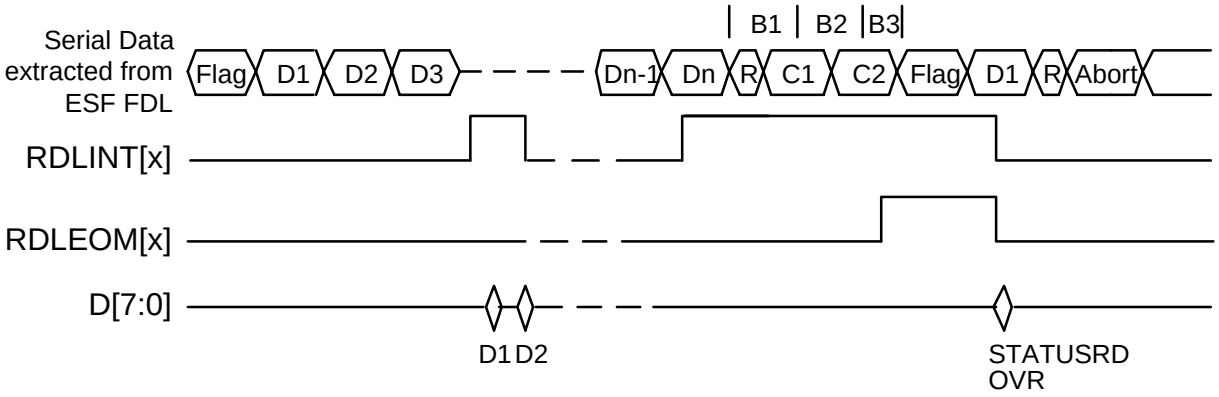
This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when one byte is present in the FIFO buffer. The RFDL is assumed to be operating in the interrupt driven mode. Each read shown is composed of two register reads: first a read of the RFDL Data Register, followed by a read of the RFDL Status Register. A read of the RFDL Data Register sets the RDLINT[x] output to low if no more data exists in the FIFO buffer. The status of the FE bit returned in the RFDL Status Register read will indicate the FIFO buffer fill status as well. The RFDL Data Register read Dn-2 is shown to occur after two bytes have been written into the buffer. The RDLINT[x] output does not go low after the first RFDL Data Register read because a data byte still remains to be read. The RDLINT[x] output goes low after RFDL Data Register read Dn-1. The FE bit will be logic 0 in RFDL Status Register read Dn-2 and logic 1 in RFDL Status Register read Dn-1.

The RDLEOM[x] output goes high as soon as the last byte in the frame is read from the RFDL Data Register. The RDLINT[x] output will go low if the FIFO buffer is empty. The next RFDL Status Register read will return a value of logic 1 for the EOM and FLG bits, and cause the RDLEOM[x] output of the RFDL to return low.

In the next frame, the first data byte is received, and after a delay of ten bit periods, it is written to the FIFO buffer, and read by the processor after the interrupt. When the abort sequence is detected, the data received up to the abort is written to the FIFO buffer and an interrupt generated. The processor then reads the partial byte from the RFDL Data Register and the RDLEOM[x] output is set high. The processor then reads the RFDL Status Register which will return a value of logic 1 for the EOM and FLG bits, and set the RDLEOM[x] output low. The FIFO buffer is not cleared when an abort is detected. All bytes received up to the abort are available to be read.

After an abort, the RFDL state machine will be in the receiving all ones state, and the data link status will be idle. When the first flag is detected, a new interrupt will be generated, with a dummy data byte loaded into the FIFO buffer, to indicate that the data link is now active.

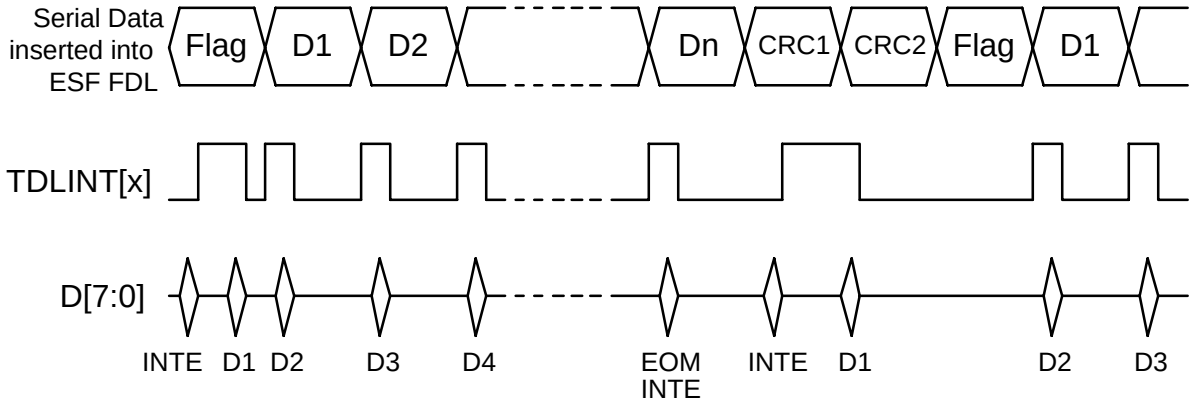
Figure 33 - RFDL FIFO Overrun



This diagram shows the relationship between RFDL inputs and outputs for the case where interrupts are programmed to occur when two data bytes are present in the FIFO buffer. Each read is composed of two register reads, as described above. In this example, data is not read by the end of B2. An overrun occurs since unread data (Dn-3) has been overwritten by B1. This sets the RDLEOM[x] output high, and resets both the RFDL and the FIFO buffer. The RFDL is held disabled until the RFDL Status Register is read. The start flag sequence is not detected since the RFDL is still held disabled when it occurs. Consequently, the

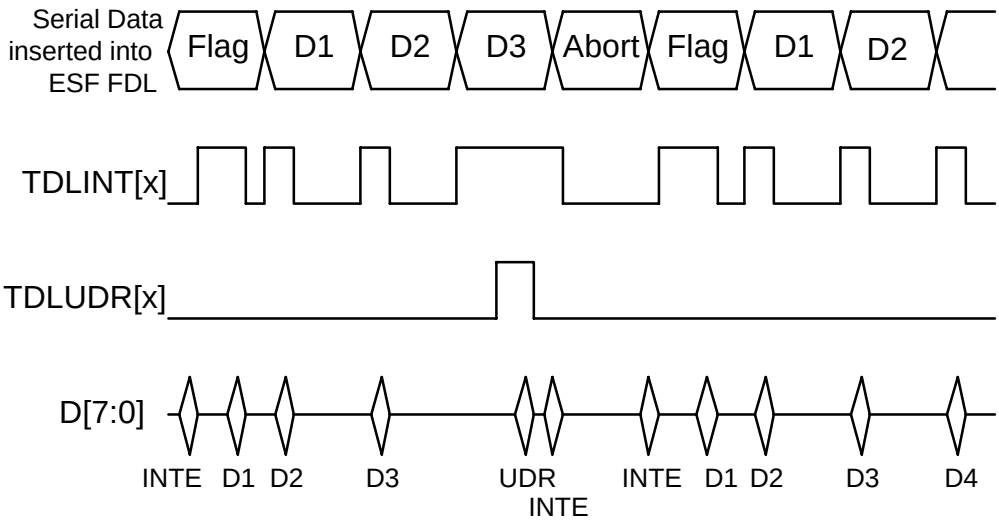
RFDL will ignore the entire frame including the abort sequence (since it has not occurred in a valid frame or during flag reception, according to the RFDL).

Figure 34 - XFDL Normal Data Sequence



This diagram shows the relationship between XFDL inputs and outputs for the case where interrupts and CRC are enabled for regular data transmission. The process is started by setting the INTE bit in the XFDL Configuration Register to logic 1, thus enabling the TDLINT[x] signal. When TDLINT[x] goes high, the interrupt service routine is started, which writes the first byte (D1) of the data frame to the XFDL Transmit Data Register. When this byte begins to be shifted out on the data link, TDLINT[x] goes high. This restarts the interrupt service routine, and the next data byte (D2) is written to the XFDL Transmit Data Register. When D2 begins to be shifted out on the data link, TDLINT[x] goes high again. This cycle continues until the last data byte (Dn) of the frame is written to the XFDL Transmit Data Register. When Dn begins to be shifted out on the data link, TDLINT[x] again goes high. Since all the data has been sent, the interrupt service routine sets the EOM bit in the XFDL Configuration Register to logic 1. The TDLINT[x] interrupt should also be disabled at this time by setting the INTE bit in the XFDL Configuration Register to logic 0. The XFDL will then shift out the two-byte CRC word and closing flag, which ends the frame. Whenever new data is ready, the TDLINT[x] signal can be re-enabled by setting the INTE bit in the XFDL Configuration Register to logic 1, and the cycle starts again.

Figure 35 - XFDL Underrun Sequence



This diagram shows the relationship between XFDL inputs and outputs in the case of an underrun error. An underrun error occurs if the XFDL finishes transmitting the current message byte before the processor writes the next byte into the XFDL Transmit Data Register; that is, the processor fails to write data to the XFDL in time. In this example, data is not written to the XFDL within the time-out period after TDLINT[x] goes high at the beginning of the transmission of byte D3. The TDLUDR[x] interrupt becomes active at this point, and an abort, followed by a flag, is sent out on the data link. Meanwhile, the processor must clear the TDLUDR[x] interrupt by setting the UDR bit in the XFDL Interrupt Status Register to logic 0. The TDLINT[x] interrupt should also be disabled at this time by setting the INTE bit in the XFDL Configuration Register to logic 0. The data frame can then be restarted as usual, by setting the INTE bit logic to 1. Transmission of the frame then proceeds normally.

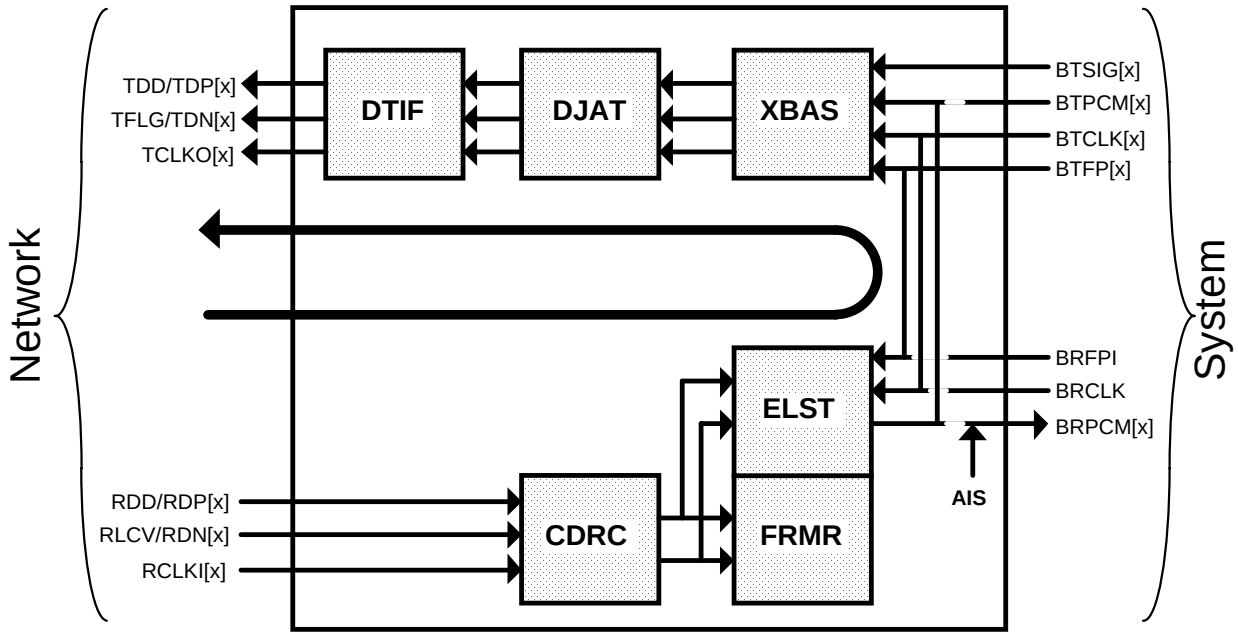
14.4 Using the Loopback Modes

The TQUAD provides three loopback modes to aid in network and system diagnostics. The network loopbacks (Payload and Line) can be initiated at any time via the µP interface, but are usually initiated once an inband loopback activate code is detected. The system Diagnostic Digital loopback can be initiated at any time by the system via the µP interface to check the path of system data through the framer.

14.4.1 Payload Loopback

When PAYLOAD loopback (PAYLB) is initiated by writing 20H to the Master Diagnostics Register (00AH, 08AH, 10AH, or 18AH) and disabling the TPSC by clearing the PCCE bit in the TPSC Configuration Register (030H, 0B0H, 130H, or 1B0H) to 0, the appropriate T1 framer in the TQUAD is configured to internally connect the output of its ELST to the PCM input of its XBAS. Payload loopback will only function if there is a valid BTCLK input signal and a valid BTFP signal (alternatively, BTFP can be tied either high or low). BTFP cannot, though, be derived from the BRFPO output of the loopbacked channel. The data is read out of ELST timed to the transmitter clock, and the transmit frame alignment indication is used to synchronize the output frame alignment of ELST. Conceptually, the data flow through a single T1 framer in this loopback condition can be shown as follows:

Figure 36 - Payload Loopback

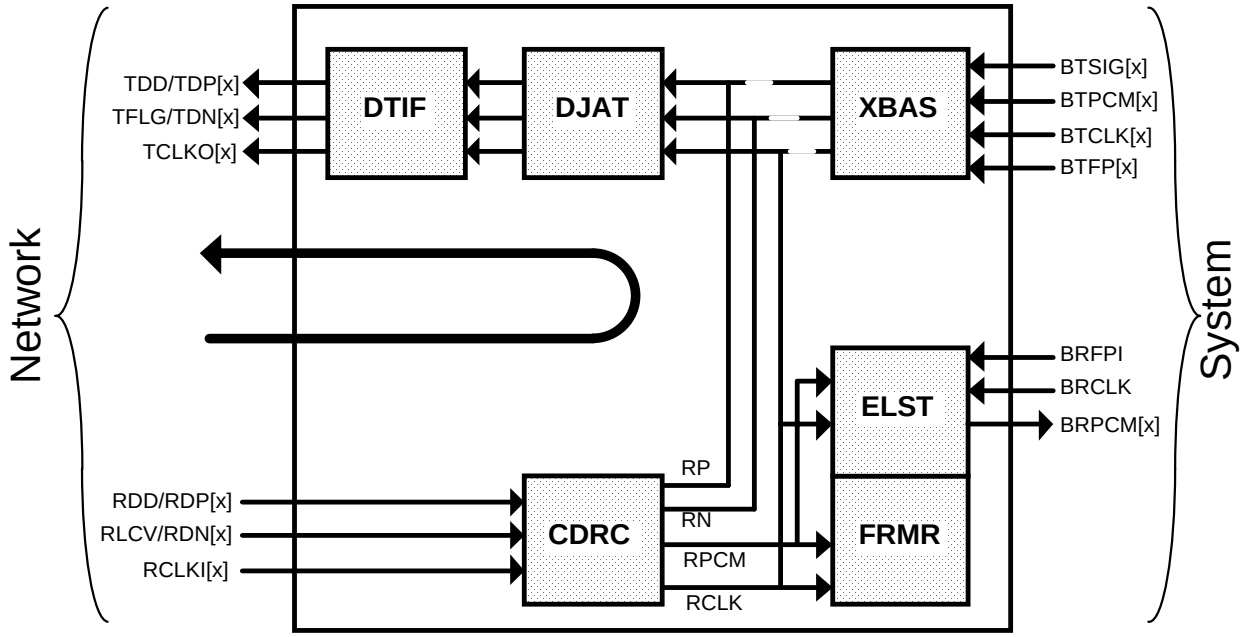


14.4.2 Line Loopback

When LINE loopback (LINELB) is initiated by writing 10H to the Master Diagnostics Register (00AH, 08AH, 10AH, or 18AH), the appropriate T1 framer in the TQUAD is configured to internally connect its dual-rail positive and negative line data output pulses from its CDRC to the dual-rail inputs of its DJAT. The jitter in the line data is attenuated through DJAT, therefore the DJAT Divisor registers

(019H and 01AH, 099H and 09AH, 119H and 11AH, or 199H and 19AH) must be programmed to the value 2FH. Conceptually, the data flow through a single T1 framer in this loopback condition can be shown as follows:

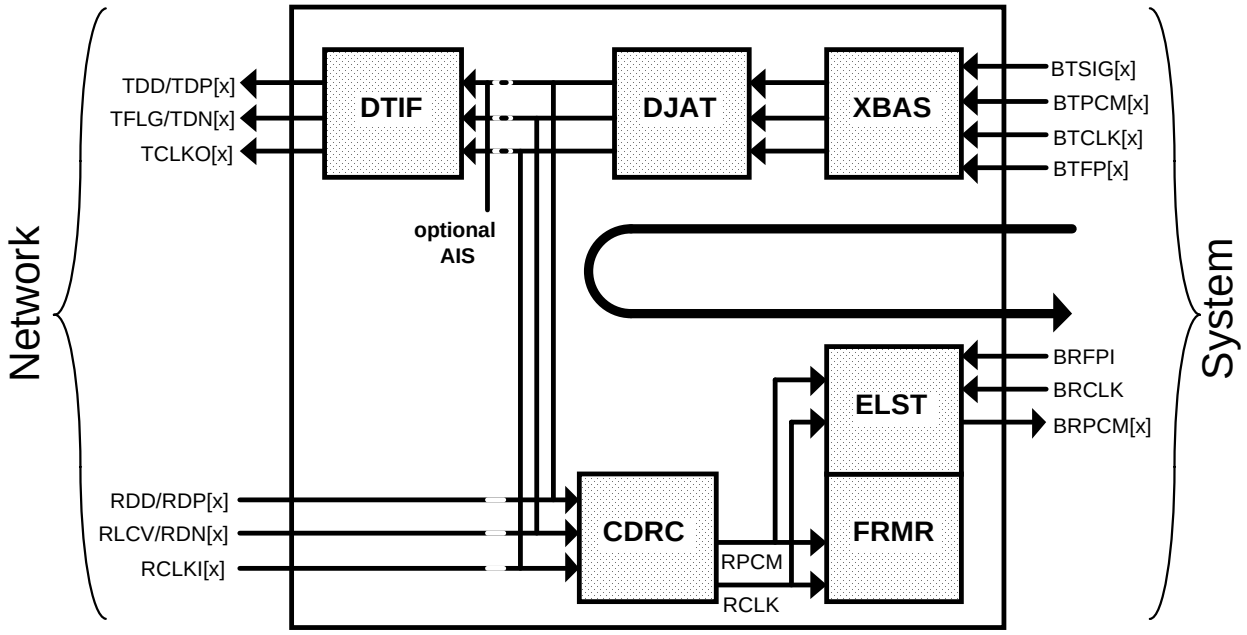
Figure 37 - Line Loopback



14.4.3 Diagnostic Digital Loopback

When Diagnostic Digital loopback (DDLB) is initiated by writing 04H to the Master Diagnostics Register (00AH, 08AH, 10AH, or 18AH), the appropriate T1 framer in the TQUAD is configured to internally connect its dual-rail positive and negative data pulses output from its DJAT to the dual-rail inputs of its CDRC (RUNI and TUNI bits in the Receive DS1 Interface Configuration and the Transmit DS1 Interface Configuration registers respectively must be set to logic 0). Conceptually, the data flow through a single T1 framer in this loopback condition can be shown as follows:

Figure 38 - Diagnostic Digital Loopback



14.5 Using the Per-Channel Serial Controllers

14.5.1 Initialization

Before the TPSC (RPSC) block can be used, a proper initialization of the internal registers must be performed to eliminate erroneous control data from being produced on the block outputs. The output control streams should be disabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 0. Then, all 72 locations of the TPSC (RPSC) must be filled with valid data. Finally, the output streams can be enabled by setting the PCCE bit in the TPSC (RPSC) Configuration Register to logic 1.

14.5.2 Direct Access Mode

Direct access mode to the TPSC or RPSC is not used in the TQUAD. However, direct access mode is selected by default whenever the TQUAD is reset. The IND bit within the TPSC and RPSC Configuration Registers must be set to logic 1 after a reset is applied.

14.5.3 Indirect Access Mode

Indirect access mode is selected by setting the IND bit in the TPSC or RPSC Configuration Register to logic 1. When using the indirect access mode, the status of the BUSY indication bit should be polled to determine the status of the microprocessor access: when the BUSY bit is logic 1, the TPSC or RPSC is processing an access request; when the BUSY bit is logic 0, the TPSC or RPSC has completed the request.

The indirect write programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write the channel data to the TPSC (RPSC) Channel Indirect Data Buffer register.

3. Write RWB=0 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

4. Poll the BUSY bit until it goes to logic 0. The BUSY bit will go to logic 1 immediately after step 3 and remain at logic 1 until the request is complete.

5. If there is more data to be written, go back to step 1.

The indirect read programming sequence for the TPSC (RPSC) is as follows:

1. Check that the BUSY bit in the TPSC (RPSC) µP Access Status Register is logic 0.

2. Write RWB=1 and the channel address to the TPSC (RPSC) Channel Indirect Address/Control Register.

3. Poll the BUSY bit, waiting until it goes to a logic 0. The BUSY bit will go to logic 1 immediately after step 2 and remain at logic 1 until the request is complete.

4. Read the requested channel data from the TPSC (RPSC) Channel Indirect Data Buffer register.

5. If there is more data to be read, go back to step 1.

14.6 Reset Procedure

In the SIGX block that there is a small state machine which will not clear itself out if it happens to get in an all-ones state. The result is that the SIGX remains frozen after a reset. The probability that this state will occur is very small, about 1 in 3600 or about 0.028 percent probability of occurrence.

14.6.1 Hardware Application for the SIGX Function

This hardware solution is to simply hold the BRCLK and the BTCLK[4:1] signals low for at least 85 ns (greater than one cycle of an 8x clock) after a hardware or software reset. The SIGX will then not remain frozen after this reset. If ELSTBYP is to be set, it should not be done so within 85 ns of a hardware or software reset.

14.6.2 Software Application for the SIGX Function

For applications which use the SIGX function, another solution is to perform a self-test after every reset. This self-test routine would use the TPSC functional block to source known signaling data which would be looped back to the SIGX. If the SIGX can detect changes in the signaling data, then the SIGX block is okay; if it cannot detect changes in the signaling data, then a reset must be performed and the self-test repeated (until the SIGX is okay).

Here are the suggested steps to be taken after every reset (software or hardware reset) of a TQUAD in which the SIGX functional block is being used. Note that this setup configures the TQUAD in default SF framing mode.

1) Perform the reset (software or hardware).

   A software reset is performed by setting then clearing the RESET bit in Registers 00DH, 08DH, 10DH, and 18DH; a hardware reset is performed by asserting the RSTB pin low then deserting high.
   The reset will make all the TQUAD's normal mode registers revert to their default state as described in the TQUAD data book section entitled "Internal Registers." This default state enables the TQUAD to operate as described in the TQUAD data book section entitled "Configuring the TQUAD from Reset." Note that indirect registers contained in the SIGX, TPSC, and RPSC are not affected by a reset.

2) Configure and enable the TPSC functional block for the self-test.

   The method of accessing the indirect registers within the TPSC functional block is explained in the TQUAD data book section entitled "Using the Per-Channel Serial Controllers."

The TPSC should be configured as follows:

a) Set the IND bit in Registers 030H, 0B0H, 130H, and 1B0H to a logic one. This will enable accesses to the TPSC indirect registers.
b) Program the TPSC indirect registers such that, for all channels, the PCM Data Control Bytes in TPSC Internal Registers 01-18H are equal to 20H, and the SIGNALING Control Bytes in TPSC Internal Registers 31-48H are equal to C5H. The IDLE Code Bytes can be left (they are don't-cares). This will configure the TPSC to insert Digital Milliwatt patterns into all channels, and to insert a signaling state of AB=01.
c) Set the PCCE bit in Registers 030H, 0B0H, 130H, and 1B0H to a logic one. This will enable the TPSC to perform the functions configured in Step (b) above.

3) Configure the SIGX functional block for the self-test.

The method of accessing the indirect registers within the SIGX functional block is the same as that explained in the TQUAD data book section entitled "Using the Per-Channel Serial Controllers."

The SIGX should be configured as follows:

a) Set the IND bit in Registers 040H, 0C0H, 140H, and 1C0H to a logic one. This will enable accesses to the SIGX indirect registers.
b) Program the SIGX indirect registers such that, for all channels, the PER-CHANNEL Configuration Data in SIGX Internal Registers 21-38H is equal to 01H. This will configure the SIGX to debounce the received signaling states as explained in the DEB bit description.
c) Set the PCCE bit in Registers 040H, 0C0H, 140H, and 1C0H to a logic one. This will enable the SIGX to perform the functions configured in Step (b) above.

4) Configure for Diagnostic (Digital) Loopback. To accomplish this:

- Program Registers 00AH, 08AH, 10AH, and 18AH to 04H. This will enable the Diagnostic Digital Loopback mode of the TQUAD which internally loops back the transmit data to the receive circuitry. This mode is sometimes called a "local" loopback.
- Program Registers 010H, 090H, 110H, and 190H to 80H. This will enable the receiver to accept the AMI-encoded signal sourced by the transmitter.

5) Disable Elastic Store.

This can be done by bypassing elastic store. To do this, program Register 00H (080H, 100H, 180H) to a value of 20H.

6) Wait until the FRMR functional block is solidly in-frame.

   This can be determined by polling the INFR and INFRI bits in Registers 022H, 0A2H, 122H, and 1A2H. When the INFR bit is high (logic one) for two consecutive polls, and the INFRI bit is low (logic zero) on the second consecutive poll, then you can assume that the FRMR functional block of the TQUAD has found a stable frame alignment pattern.

7) Further wait until at least five signaling multiframes have been received (> 7.5 ms) to give SIGX time to unfreeze and debounce the signaling data.

8) Verify that the SIGX signaling data registers contain the expected value (that is transmitted by the TPSC functional block). If not, return to Step (1).
   This is accomplished by reading the SIGX SIGNALING Data registers in SIGX Internal Registers 01-18H for all channels. The values returned should contain 5H in the lower nybble — if not, return to Step (1).

9) Change the signaling data transmitted by the TPSC for all channels.
   A value of C0H should be written to the TPSC SIGNALING Control Bytes in TPSC Internal Registers 31-48H are of all the channels. This will configure the TPSC to insert a signaling state of AB=00.

10) Wait until at least two signaling multiframes have been received (> 3 ms) to give SIGX time to extract and debounce the new signaling data.

11) Verify that the SIGX signaling data registers contain the new values. If not, return to Step (1).

    This is accomplished by reading the SIGX SIGNALING Data registers for all channels. The values returned should contain 0H in the lower nibble — if not, return to Step (1).

12) The self-test passed — the TQUAD is ready for operation.

    The TQUAD can now be configured for the desired application. It is allowable to reconfigure the TPSC and SIGX functional blocks.
    Every time a reset (software or hardware reset) occurs, the above procedure, Steps (1) to (12), should be performed.

14.7 Using the Digital Jitter Attenuator

The key to using DJAT lies in selecting the appropriate divisors for the phase comparison between the selected reference clock and the generated smooth TCLKO[x[.

14.7.1 Default Application

Upon reset, the TQUAD default condition provides jitter attenuation with TCLKO[x] referenced to the transmit clock, BTCLK[x]. The DJAT SYNC bit is also logic 1 by default. DJAT is configured to divide its input clock rate, BTCLK[x], and its output clock rate, TCLKO[x], both by 48, which is the maximum length of the FIFO. These divided down clock rates are then used by the phase comparator to update the DJAT DPLL. The phase delay between BTCLK[x] and TCLKO[x] is synchronized to the physical data delay through the FIFO. For example, if the phase delay between BTCLK[x] and TCLKO[x] is 12UI, the FIFO will be forced to lag its output data 12 bits from its input data.

The default mode works well with the transmit backplane running at 1.544MHz.

14.7.2 Data Burst Application

In applications where the 2.048MHz transmit backplane rate (or a higher backplane rate with external gapping) is used, a few factors must be considered to adequately filter the resultant TCLKO[x] into a smooth 1.544MHz clock. The magnitude of the phase shifts in the incoming bursty data are too large to be properly attenuated by the PLL alone. However, the magnitudes, and the frequency components of these phase shifts are known, and are most often multiples of 8 kHz.

When using the 2.048MHz transmit backplane rate, the input clock to DJAT is a gapped version of the 2.048MHz BTCLK[x]. The phase shifts of the input clock with respect to the generated TCLKO[x] in this case are large, but when viewed over a longer period, such as a frame, there is little net phase shift. Therefore, by choosing the divisors appropriately, the large phase shifts can be filtered out, leaving a stable reference for the DPLL to lock onto. In this application, the N1 and N2 divisors should be changed to C0H (i.e. divisors of 193). Consequently, the frequency of the clock inputs to the phase discriminator in the PLL is 8 kHz. The DJAT SYNC option must be disabled, since the divisor magnitude of 193 is not an integer multiple of the FIFO length, 48.

The self-centering circuitry of the FIFO should be enabled by setting the CENT register bit. This sets up the FIFO read pointer to be at least 4 UI away from the end of the FIFO registers, and then disengages. Should variations in the frequency of input clock or the output clock cause the read pointer to drift to within one unit interval of FIFO overflow or underflow, the pointer will be incrementally pushed away by the LIMIT control without any loss of data.

With SYNC disabled, CENT and LIMIT enabled, the maximum tolerable phase difference between the bursty input clock and the smooth TCLKO[x] is 40UI. Phase wander between the two clock signals is compensated for by the LIMIT control.

14.7.3 Elastic Store Application

In multiplex applications where the jitter attenuation is not required, the DJAT FIFO can be used to provide an elastic store function. For example, in a M12 application, the data is written into the FIFO at 1.544MHz and the data is read out of the FIFO with a gapped DS2 rate clock applied on TCLKI. In this configuration, the Timing Options OCLKSEL[1:0] bits should be programmed to 01, the TCLKISEL bit should be programmed to 1, and the SMCLKO bit should be programmed to 1. Also, the DJAT SYNC and LIMIT bits should be disabled and the CENT bit enabled. This provides the maximum phase difference between the input clock and the gapped output clock of 40UI. The maximum jitter and wander between the two clocks is 8UIp-p.

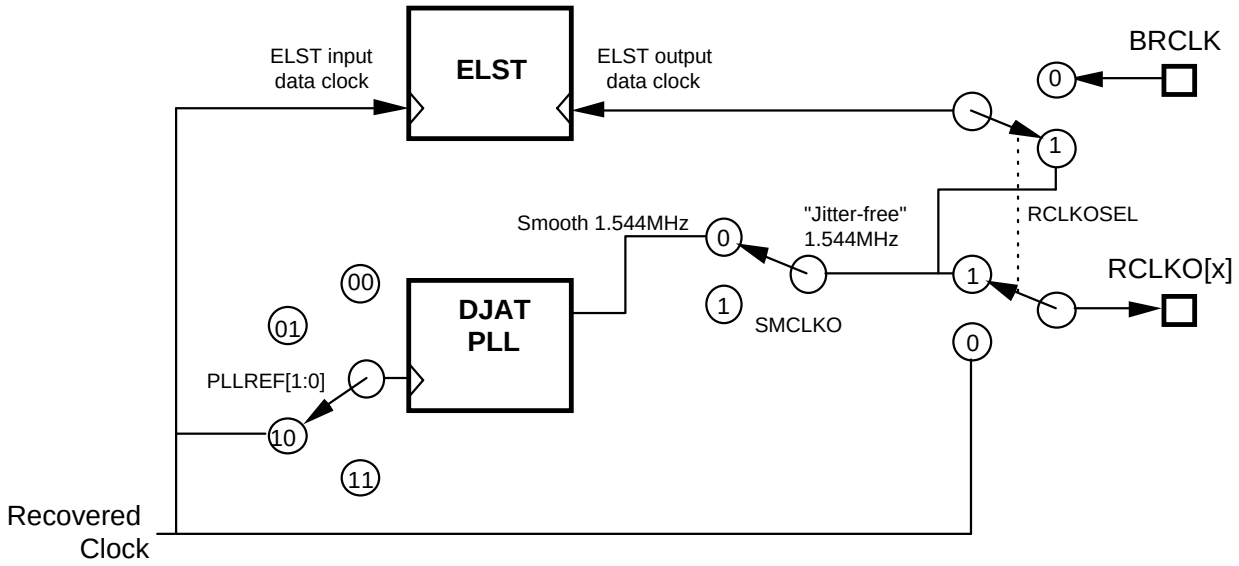
14.7.4 Alternate TCLKO Reference Application

In applications where TCLKO[x] is referenced to an Nx8 kHz clock source applied on TCLKI[x], DJAT can be configured by programming the output clock divisor, N2, to C0H and the input clock divisor, N1, to the value (N-1). The resultant input clocks to the phase comparator are both 8kHz. The DJAT SYNC and LIMIT bits should be disabled in this configuration.

14.7.5 Receiver Jitter Attenuation

The combination of the receive elastic store and the digital phase locked loop may be used to attenuate jitter in the receive direction by locking the elastic store output clock to the recovered clock. The following diagram illustrates the concept.

Figure 39 - Timing Options for Receive Jitter Attenuation

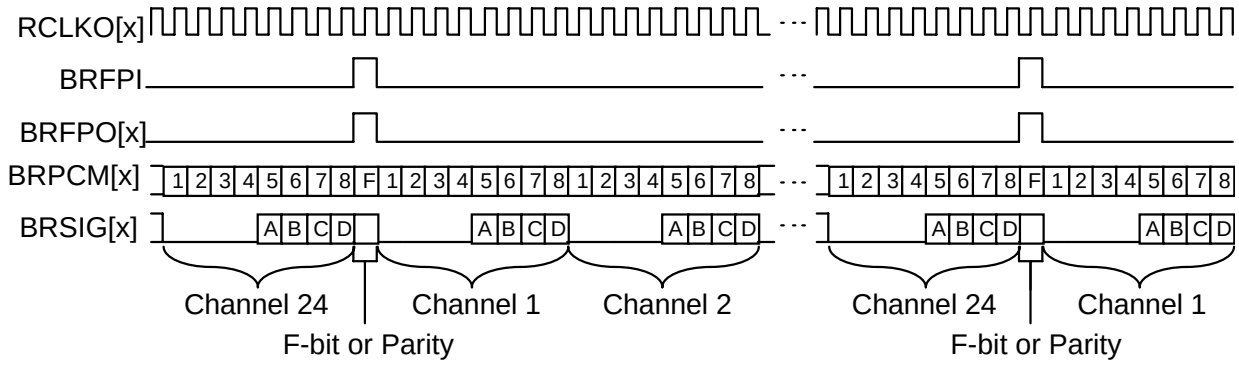


The jitter on the recovered clock is absorbed by the two frame slip buffer in the elastic store. BRPCM[x], BRSIG[x], and BRFPO[x] are updated on the falling edge of RCLKO[x].

The framing alignment on BRPCM[x] and BRSIG[x] is still set by the BRFPI input. However, BRFPI must now be timed with respect to the individual output clock RCLKO[x] instead of BRCLK for each quadrant of the TQUAD in which RCLKOSEL is set to logic 1. A possible configuration would have RCLKOSEL set to logic 1 in only one quadrant and BRFPI timed to that quadrant's RCLKO. The same RCLKO can then be connected to BRCLK which will be used as the timing reference for all the other quadrants which will have RCLKOSEL set to logic 0. Otherwise, if backplane frame alignment is not necessary, RCLKOSEL can be set to logic 1 in every quadrant and BRFPI should be tied low.

Figure 40 shows the functional waveforms for a configuration where RCLKOSEL is set to logic 1 in quadrant x. BRFPI and all the backplane outputs are timed to RCLKO [x].

Figure 40 - 1. 544MHz Receive Backplane Interface with RCLKOSEL = 1



It should also be noted that RFP[x] can no longer be sampled by RCLKO[x] since RCLKO[x] is a smoothed version of the recovered clock, and RFP[x] is timed by the unsmoothed recovered clock.

Register bits ELSTBYP, TRSLIP, BRX2M, and BRX2RAIL must be cleared for proper operation. The DJAT Configuration register should be cleared to all zeros to disable the LIMIT and SYNC bits. Note that the DJAT PLL is no longer in the transmit path. Therefore, the FIFOBYP bit of the Transmit DS1 Interface Configuration register must be set.

14.8 Using the Performance Monitor Counter Values

All PMON event counters are of sufficient length so that the probability of counter saturation over a one second interval at a 10^{-3} BER is less than 0.001%. The odds of any one of the counters saturating during a one second sampling interval go up as the BER increases. At some point, the probability of counter saturation reaches 50%. This point varies, depending upon the framing format and the type of event being counted. The BER at which the probability of counter saturation reaches 50% is shown below for various counters:

Table 29 -

Counter	Format	BER
LCV	all	2.75×10^{-3}
FER	SF	4.0×10^{-3}
	T1DM	4.0×10^{-3}
	SLC®96	8.0×10^{-3}
	ESF	1.58×10^{-2}
BEE	SF	6.4×10^{-2}
	T1DM	9.2×10^{-3}
	SLC®96	1.35×10^{-1}
	ESF	cannot saturate

Below these 50% points, the relationship between the BER and the counter event count (averaged over many one second samples) is essentially linear. Above the 50% point, the relationship between BER and the average counter event count is highly non-linear due to the likelihood of counter saturation. Figures 39-46 show this relationship for various counters and framing formats. These graphs can be used to determine the BER, given the average event count. In general, if the BER is above 10^{-3}, the average counter event count cannot be used to determine the BER without considering the statistical effect of occasional counter saturation.

Figure 41 - LCV Count vs. BER

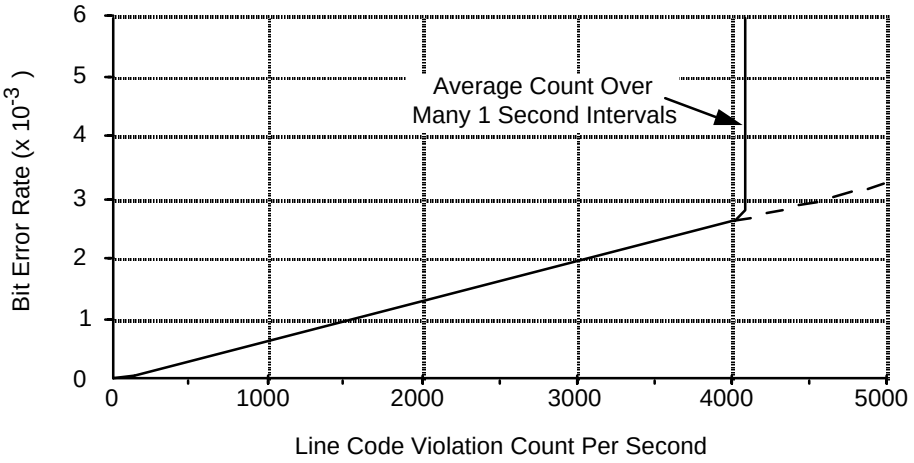


Figure 42 - FER Count vs. BER for SF and T1DM Framing Formats

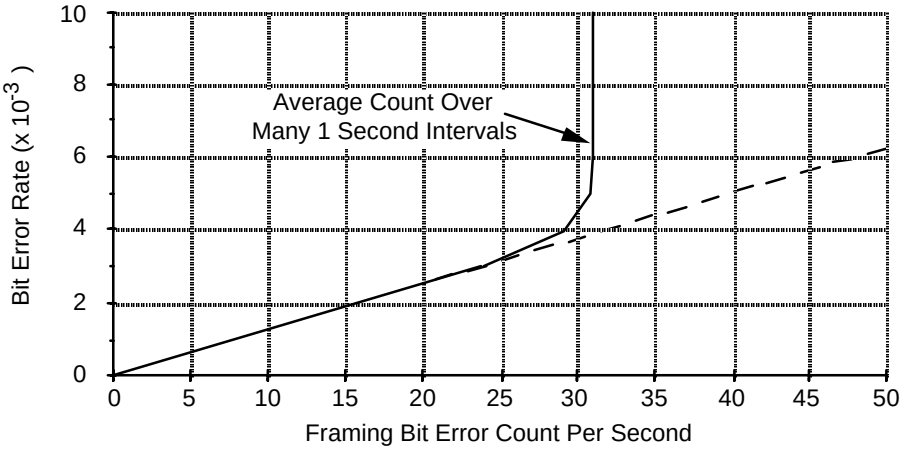


Figure 43 - FER Count vs. BER for SLC®96 Framing Format

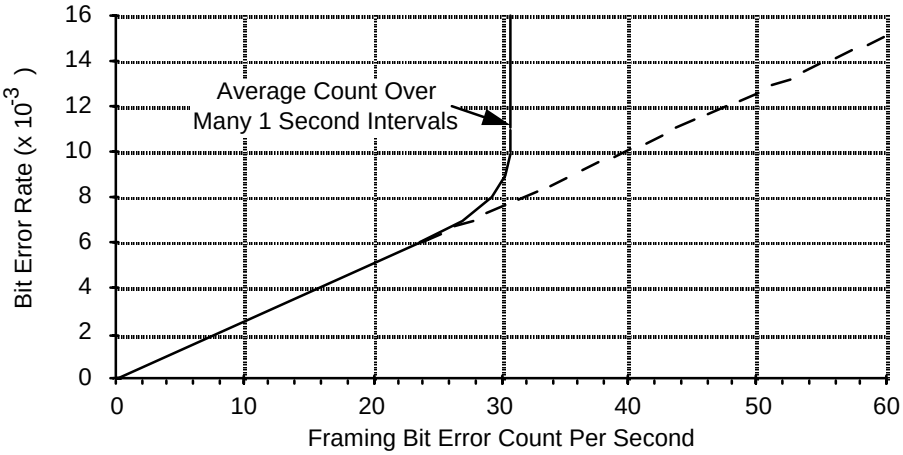


Figure 44 - FER Count vs. BER for ESF Framing Format

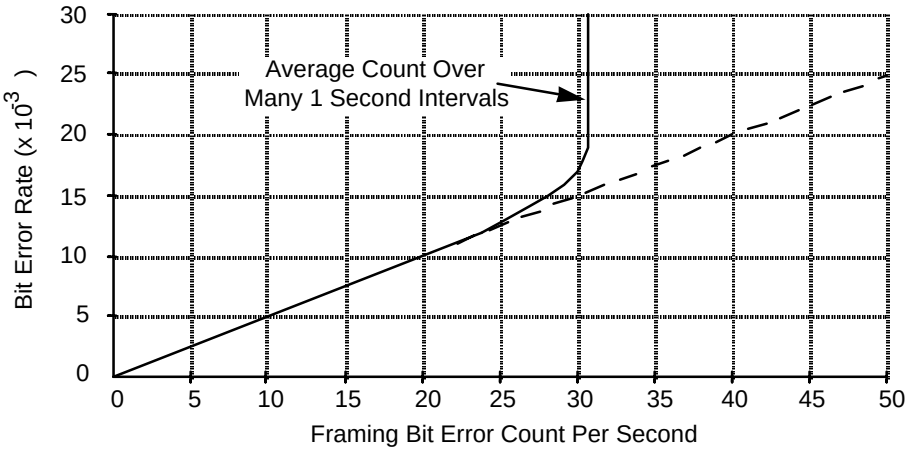
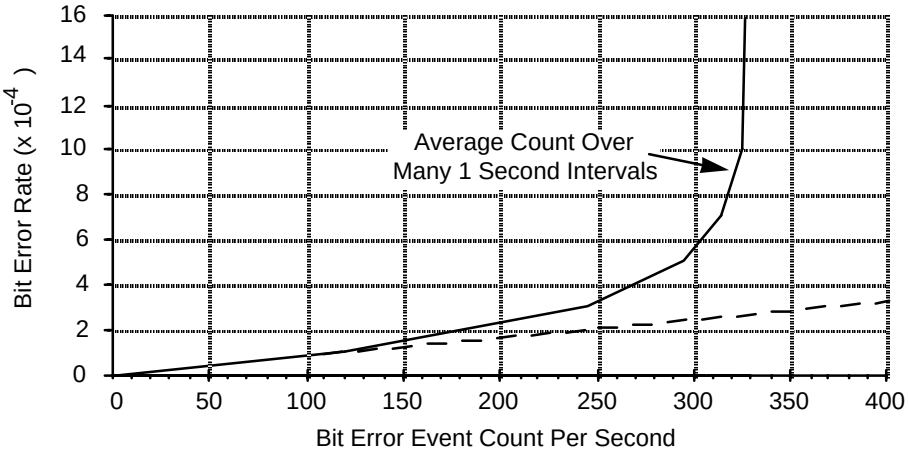


Figure 45 - BEE Count vs. BER for ESF Framing Format



Since the maximum number of ESF superframes that can occur in one second is 333, the 9-bit BEE counter cannot saturate in one second in ESF framing format. Despite this, there is not a linear relationship between BER and BEE count, due to the nature of the CRC-6 calculation. At BERs below 10^{-4}, there tends to be no more than one bit error per superframe, so the number of CRC-6 errors is generally equal to the number of bit errors, which is directly related to the BER. However, at BERs above 10^{-4}, each CRC-6 error is often due to more than one bit error. Thus, the relationship between BER and BEE count becomes non-linear above a 10^{-4} BER. This must be taken into account when using ESF CRC-6 counts to determine the BER.

Figure 46 - BEE Count vs. BER for SF Framing Format

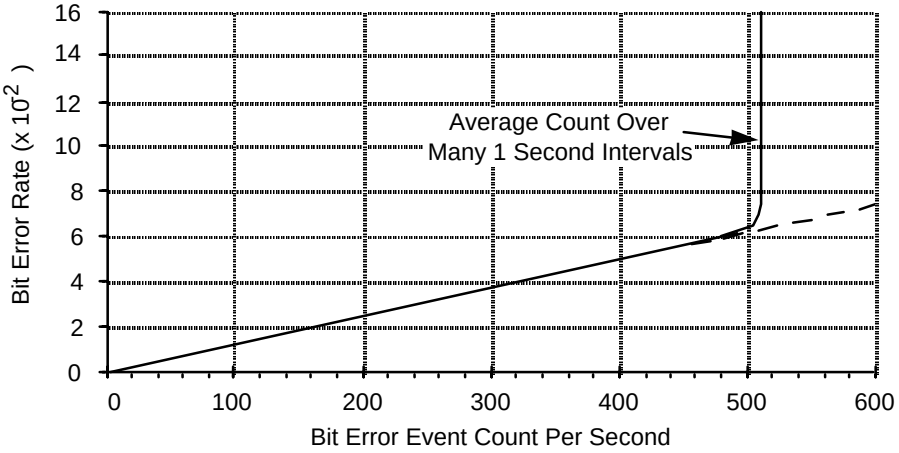


Figure 47 - BEE Count vs. BER for SLC®96 Framing Format

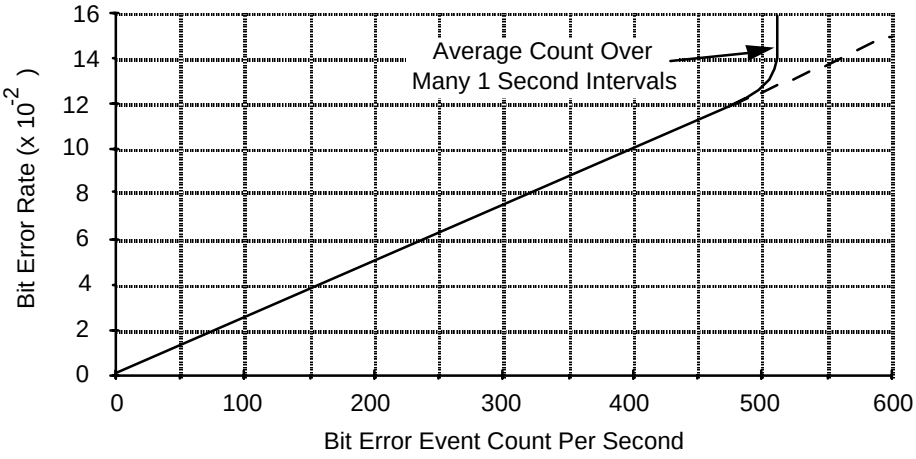
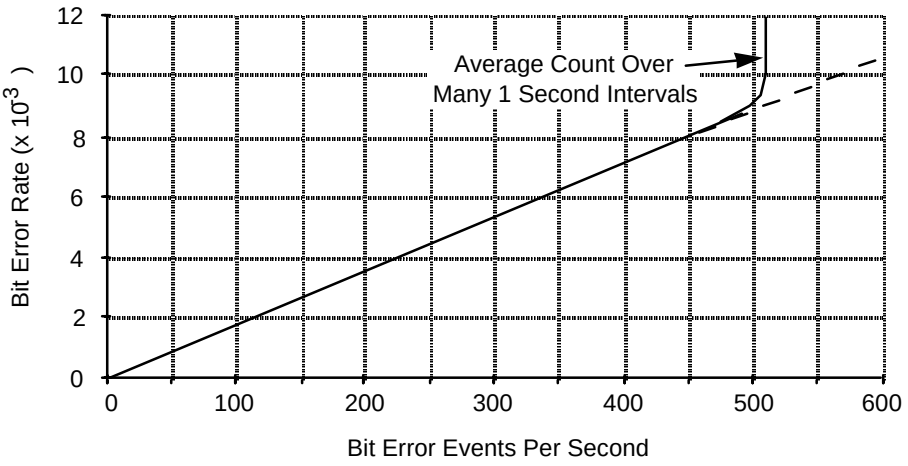


Figure 48 - BEE Count vs. BER for T1DM Framing Format



15 ABSOLUTE MAXIMUM RATINGS

Table 30 -

Ambient Temperature under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on VDD with Respect to GND	-0.5V to +7.0V
Voltage on Any Pin	VSS-0.5V to VDD+0.5V
Static Discharge Voltage	±1000 V
Latch-Up Current (T_A = -40°C to +85°C)	100 mA

16 CAPACITANCE

Table 31 -

Symbol	Parameter	Typical	Units	Conditions
Cin	Input Capacitance	5	pF	T_A = 25°C, f = 1 MHz
Cout	Output Capacitance	5	pF	T_A = 25°C, f = 1 MHz
Cbidir	Bidirectional Capacitance	5	pF	T_A = 25°C, f = 1 MHz

17 D.C. CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 32 -

Symbol	Parameter	Min	Typ	Max	Units	Conditions
PHA, PHD	Power Supply	4.5	5	5.5	Volts	
V_{IL}	Input Low Voltage	-0.5		0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}	Input High Voltage	2.0		V_{DD}+0.5	Volts	Guaranteed Input HIGH Voltage
V_{OL}	Output or Bidirectional Low Voltage		0.1	0.4	Volts	V_{DD} = min, I_{OL} = -4 mA for D[7:0] and MRD and -2 mA for others[3]
V_{OH}	Output or Bidirectional High Voltage	V_{DD}-1.0			Volts	V_{DD} = min, I_{OL} = 4 mA for D[7:0] and MRD and 2 mA for others[3]
V_{T+}	Reset Input High Voltage	3.5			Volts	
V_{T-}	Reset Input Low Voltage			0.6	Volts	
V_{TH}	Reset Input Hysteresis Voltage		1.45		Volts	
I_{ILPU}	Input Low Current[1,3]	+100	+350	+525	µA	V_{IL} = GND
I_{IHPU}	Input High Current[1,3]	-10	0	+10	µA	V_{IH} = V_{DD}

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{IL}	Input Low Current[2,3]	-10	0	+10	µA	V_{IL} = GND
I_{IH}	Input High Current[2,3]	-10	0	+10	µA	$V_{IH} = V_{DD}$
I_{DDOP}	Operating Current		38	80	mA	V_{DD} = 5.5 V, Outputs Unloaded, XCLK = 37.056 MHz BTCLK[4:1] = 1.544MHz

Notes on D.C. Characteristics:

1. Input pin or bidirectional pin with internal pull-up resistors.
2. Input pin or bidirectional pin without internal pull-up resistors
3. Negative currents flow into the device (sinking), positive currents flow out of the device (sourcing).

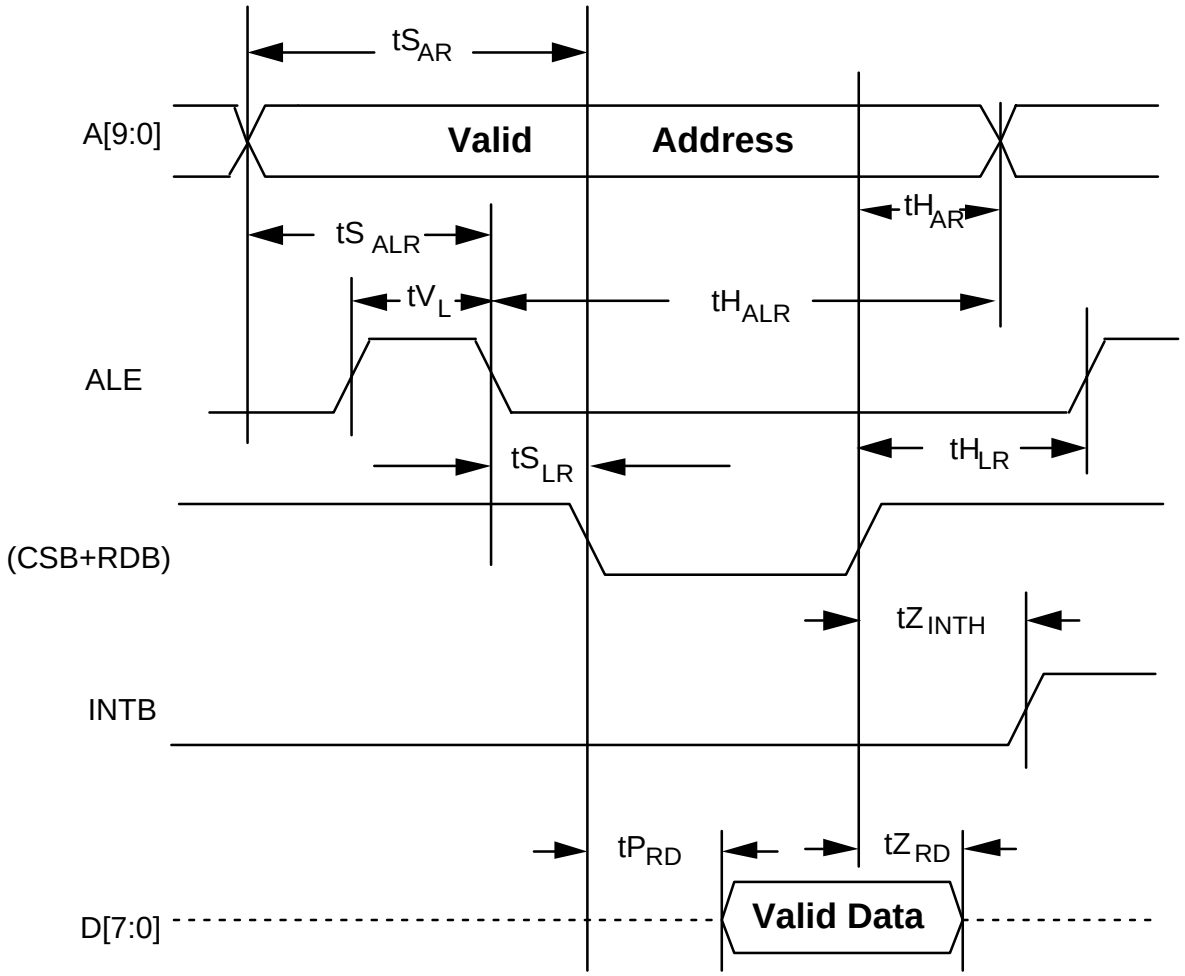
18 MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 33 - Microprocessor Read Access (Figure 49)

Symbol	Parameter	Min	Max	Units
tS_{AR}	Address to Valid Read Set-up Time	10		ns
tH_{AR}	Address to Valid Read Hold Time	5		ns
tS_{ALR}	Address to Latch Set-up Time	10		ns
tH_{ALR}	Address to Latch Hold Time	10		ns
tV_{L}	Valid Latch Pulse Width	20		ns
tS_{LR}	Latch to Read Set-up	0		ns
tH_{LR}	Latch to Read Hold	5		ns
tP_{RD}	Valid Read to Valid Data Propagation Delay		80	ns
tZ_{RD}	Valid Read Negated to Output Tri-state		20	ns
tZ_{INTH}	Valid Read Negated to INTB high		50	ns

Figure 49 - Microprocessor Read Access Timing



Notes on Microprocessor Read Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
2. Maximum output propagation delays are measured with a 50 pF load on the Microprocessor Interface data bus, (D[7:0]).
3. A valid read cycle is defined as a logical OR of the CSB and the RDB signals.
4. Microprocessor Interface timing applies to normal mode register accesses only.

5. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

6. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

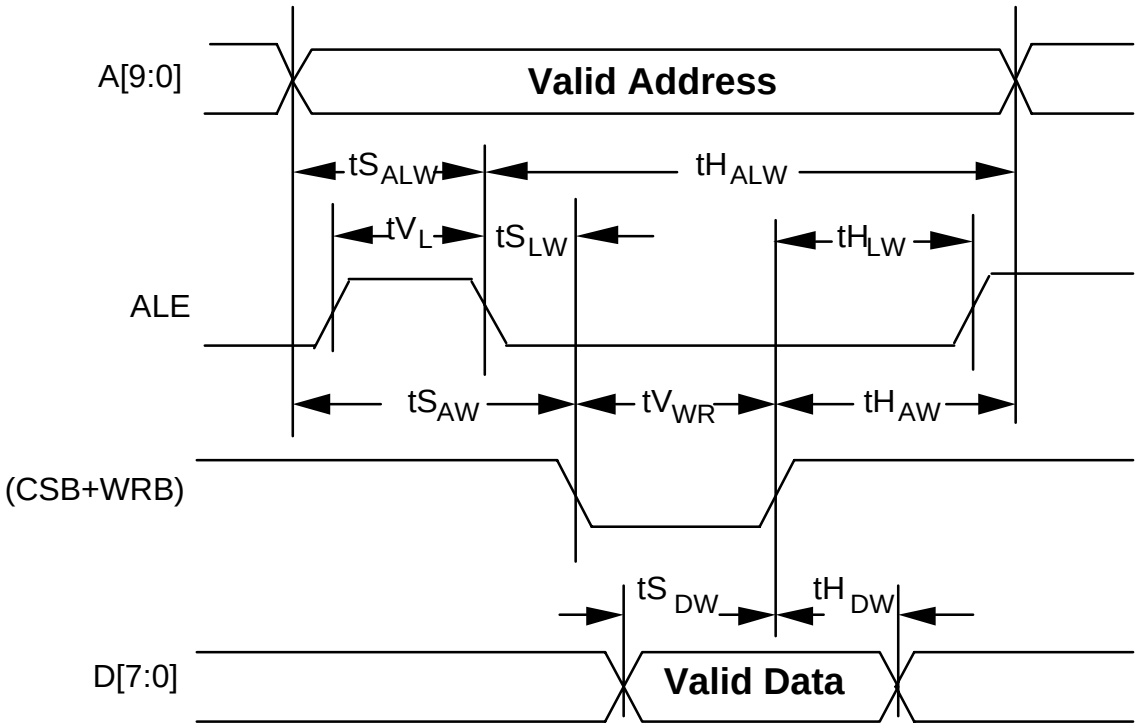
7. In non-multiplexed address/data bus architectures ALE can be held high; parameters tS_{ALR}, tH_{ALR}, tV_L, and tS_{LR}, tH_{LR} are not applicable.

8. Parameter tH_{AR} is not applicable when address latching is used.

Table 34 - Microprocessor Write Access (Figure 50)

Symbol	Parameter	Min	Max	Units
tS_{AW}	Address to Valid Write Set-up Time	10		ns
tS_{DW}	Data to Valid Write Set-up Time	20		ns
tS_{ALW}	Address to Latch Set-up Time	10		ns
tH_{ALW}	Address to Latch Hold Time	10		ns
tV_L	Valid Latch Pulse Width	20		ns
tS_{LW}	Latch to Write Set-up	0		ns
tH_{LW}	Latch to Write Hold	5		ns
tH_{DW}	Data to Valid Write Hold Time	5		ns
tH_{AW}	Address to Valid Write Hold Time	5		ns
tV_{WR}	Valid Write Pulse Width	40		ns

Figure 50 - Microprocessor Write Access Timing



Notes on Microprocessor Interface Write Timing:

1. A valid write cycle is defined as a logical OR of the CSB and the WRB signals.
2. Microprocessor Interface timing applies to normal mode register accesses only.
3. In non-multiplexed address/data bus architectures, ALE can be held high, parameters tS_{ALW}, tH_{ALW}, tV_L, and tS_{LW}, tH_{LW} are not applicable.
4. Parameters tH_{AW} and tS_{AW} are not applicable if address latching is used.
5. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.
6. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

7. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

19 TQUAD I/O TIMING CHARACTERISTICS

TA= -40° to +85°C, VDD=5V ±10%

Table 35 - Backplane Transmit Input Timing, MENB Input High (Figure 51)

Symbol	Description	Min	Max	Units
	Backplane Transmit Clock Frequency[1,2](Typically 1.544 MHz ± 130 ppm or2.048 MHz ± 130 ppm)	1.5	2.1	MHz
	Backplane Transmit Clock Duty Cycle[4]	30	70	%
tS_{TCLK}	BTCLK[x] to Backplane Input Set-up Time[7]	20		ns
tH_{TCLK}	BTCLK[x] to Backplane Input Hold Time[8]	20		ns

Figure 51 - Backplane Transmit Input Timing Diagram

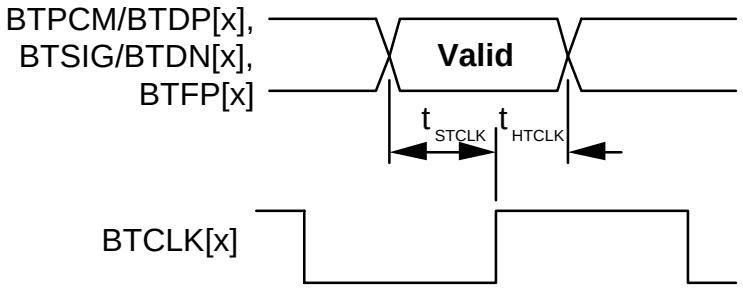


Table 36 - Backplane Transmit Input Timing, MENB Input Low (Figure 52)

Symbol	Description	Min	Max	Units
	Backplane Transmit Clock Frequency[2,3] (Typically 12.352 MHz ± 130 ppm or 16.384 MHz ± 130 ppm)	12.0	16.8	MHz

Symbol	Description	Min	Max	Units
	Backplane Transmit Clock Duty Cycle[4]	40	60	%
tS_{MTCLK}	MTCLK to Backplane Input Set-up Time[7]	10		ns
tH_{MTCLK}	MTCLK to Backplane Input Hold Time[8]	3		ns

Figure 52 - Backplane Transmit Input Timing Diagram

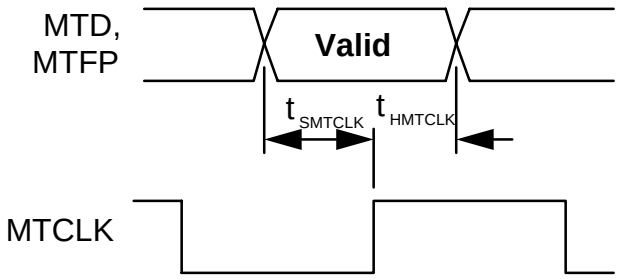


Table 37 - XCLK=37.056 MHz Input (Figure 53)

Symbol	Description	Min	Max	Units
tL_{XCLK}	XCLK Low Pulse Width[4]	10		ns
tH_{XCLK}	XCLK High Pulse Width[4]	10		ns
t_{XCLK}	XCLK Period (typically 1/37.056 MHz)[5]	20		ns

Figure 53 - XCLK=37.056 MHz Input Timing

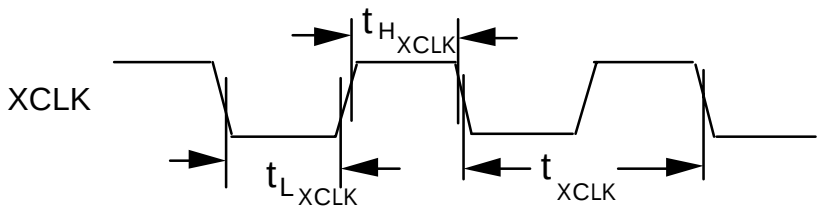


Table 38 - TCLKI Input (Figure 54)

Symbol	Description	Min	Max	Units
	TCLKI[x] Frequency (when used for DJAT REF or for mux operation), typically 1.544 MHz ± 130 ppm[2,6]		1.545	MHz
	TCLKI[x] Frequency (when DJAT PLL not used), typically 12.352 MHz		12.8	MHz
t_{HTCLKI}	TCLKI[x] High Duration[4]	160		ns
t_{LTCLKI}	TCLKI[x] Low Duration[4]	160		ns

Figure 54 - TCLKI Input Timing

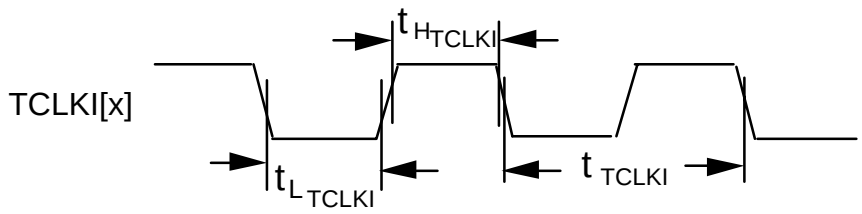
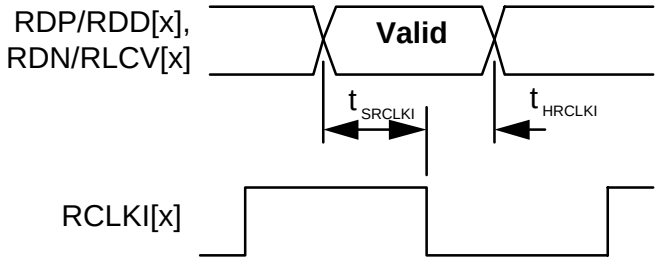


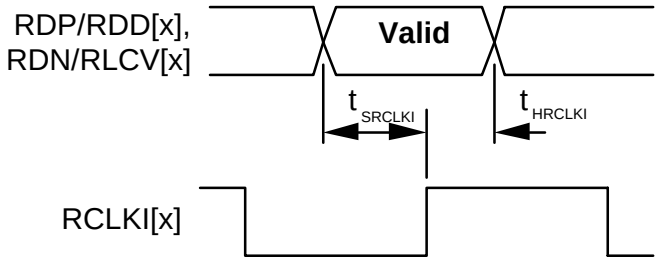
Table 39 - Digital Receive Interface Input Timing (Figure 55)

Symbol	Description	Min	Max	Units
	Digital Receive Clock RCLKI[x] Frequency (nominally 1.544 MHz ± 130 ppm)[2]		1.6	MHz
tHI_{RCLKI}	Digital Receive Clock High Duration[4]	250		ns
tLO_{RCLKI}	Digital Receive Clock Low Duration[4]	250		ns
tS_{RCLKI}	RCLKI[x] to NRZ Receive Input Set-up Time[7]	20		ns
tH_{RCLKI}	RCLKI[x] to NRZ Receive Input Hold Time[8]	20		ns
tW_{RDPN}	RZ Receive Input Pulse Width[2,4]	250	400	ns

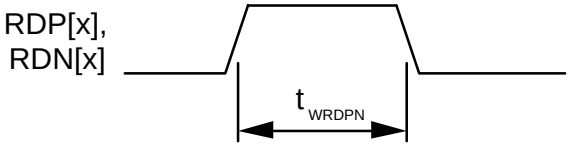
Figure 55 - Digital Receive Interface Input Timing Diagram



With RFALL bit =1, RRZ=0



With RFALL bit =0, RRZ=0



With RRZ=1

Table 40 - Transmit Data Link Input Timing (Figure 56)

Symbol	Description	Min	Max	Units
tS_{DIN}	TDLCLK[x] to TDLSIG[x] Input Set-up Time[7]	80		ns
tH_{DIN}	TDLCLK[x] to TDLSIG[x] Input Hold Time[8]	20		ns

Figure 56 - Transmit Data Link Input Timing Diagram

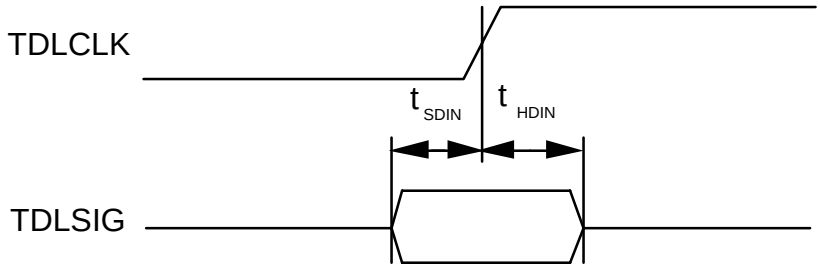


Table 41 - Backplane Receive Timing, MENB Input High (Figure 57)

Symbol	Description	Min	Max	Units
t_{SBRFPI}	BRCLK to BRFPI Input Set-up Time[7]	20		ns
t_{HBRFPI}	BRCLK to BRFPI Input Hold Time[8]	20		ns
t_{PBRCLK}	BRCLK to Backplane Output Signals Propagation Delay[10,11]		50	ns

Figure 57 - Backplane Receive Timing Diagram

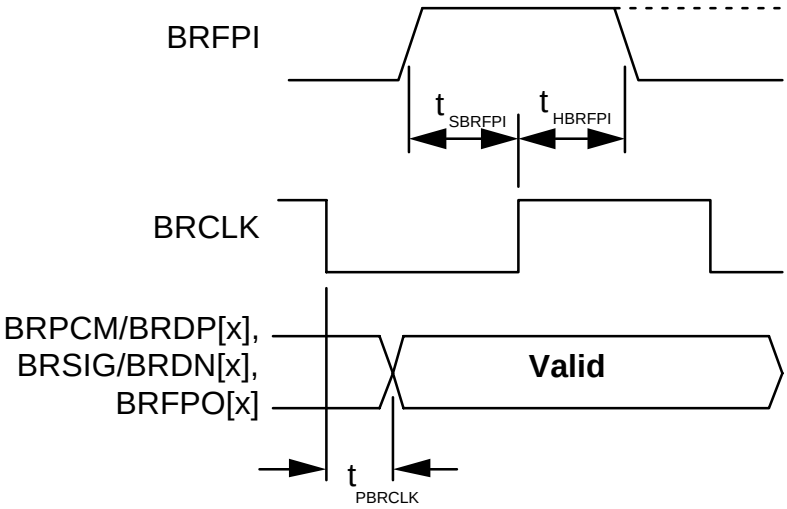


Table 42 - Backplane Receive Timing, MENB Input High, RCLKOSEL = 1 (Figure 58)

Symbol	Description	Min	Max	Units
$t_{SBRFPIO}$	RCLKO to BRFPI Input Set-up Time[7]	25		ns
$t_{HBRFPIO}$	RCLKO to BRFPI Input Hold Time[8]	20		ns
$t_{PBRCLKO}$	RCLKO to Backplane Output Signals Propagation Delay[10,11]		50	ns

Figure 58 - Backplane Receive Timing (RCLKOSEL = 1) Diagram

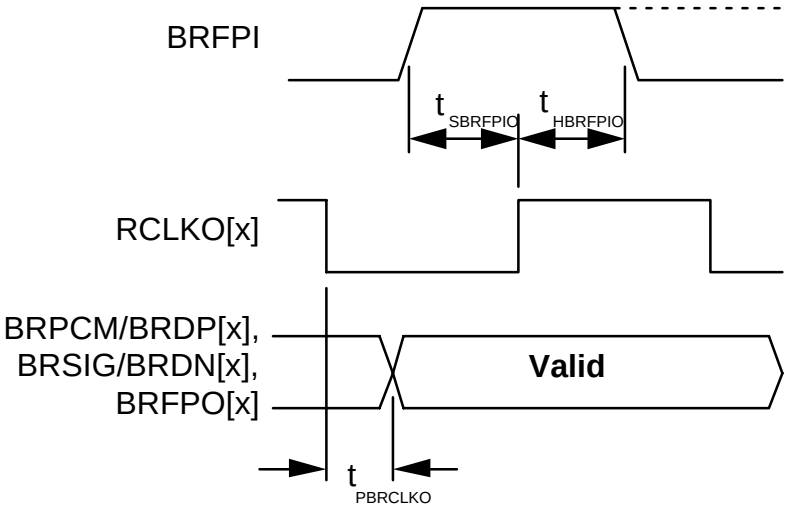


Table 43 - Multiplexed Backplane Receive Timing, MENB Input Low (Figure 59)

Symbol	Description	Min	Max	Units
t_{SMFPI}	MRCLK to MRFPI Input Set-up Time[7]	10		ns
t_{HMRFPI}	MRCLK to MRFPI Input Hold Time[8]	2		ns
t_{PMRD}	BRCLK to MRD Propagation Delay[10,11]		25	ns

Figure 59 - Multiplexed Backplane Receive Timing Diagram

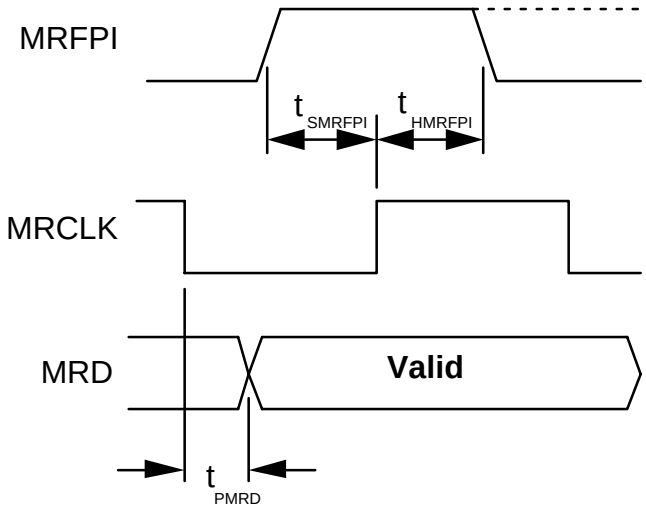


Table 44 - Receive Data Link Output Timing (Figure 60)

Symbol	Description	Min	Max	Units
$t_{PRDLCLK}$	RDLCLK[x] to RDLSIG[x] Propagation Delay[10,11]		50	Ns

Figure 60 - Receive Data Link Output Timing Diagram

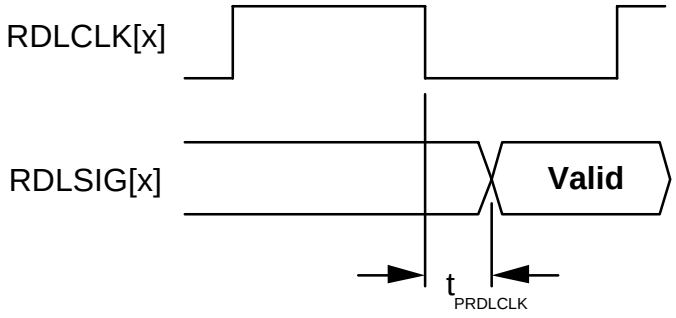


Table 45 - Recovered Frame Pulse Output Timing (Figure 61)

Symbol	Description	Min	Max	Units
t_{PRFP}	RCLKO[x] to Recovered Frame Pulse (RFP[x]) Propagation Delay[9,10,11]		50	ns

Figure 61 - Recovered Frame Output Timing Diagram

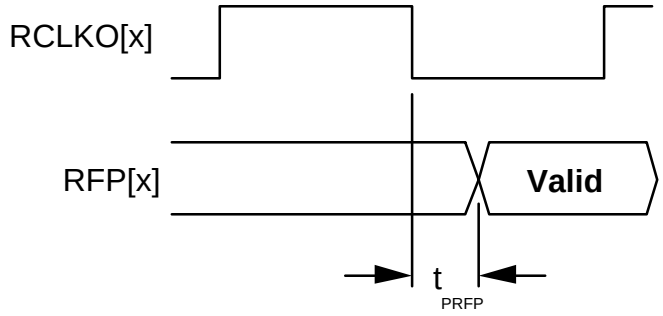
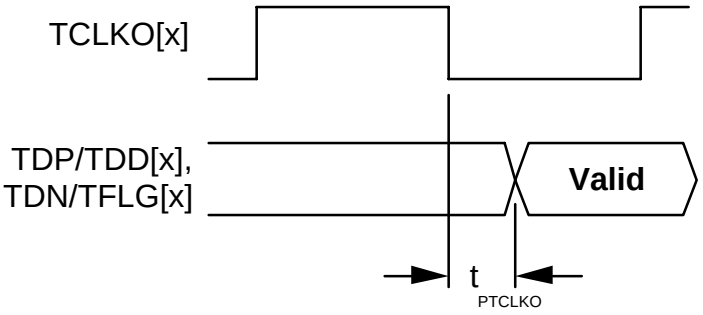


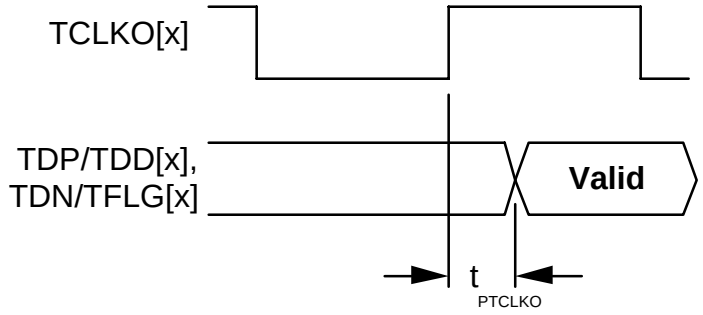
Table 46 - Transmit Interface Output Timing (Figure 62)

Symbol	Description	Min	Max	Units
t_{PTCLKO}	TCLKO[x] to Digital Transmit Data Output Signals Propagation Delay[10,11]		50	ns

Figure 62 - Transmit Interface Output Timing Diagram



With TRISE bit=0



With TRISE bit= 1

Table 47 - Transmit Data Link DMA Interface Output Timing (Figure 63)

Symbol	Description	Min	Max	Units
tPTINT	Transmit Data Register Serviced (WRB low) to TDLINT[x] Low Propagation Delay[10,11]		50	ns
tPTUDR	Transmit Data Register Serviced (WRB high) to TDLUDR[x] Low Propagation Delay[10,11]		50	ns

Figure 63 - Transmit Data Link DMA Interface Output Timing Diagram

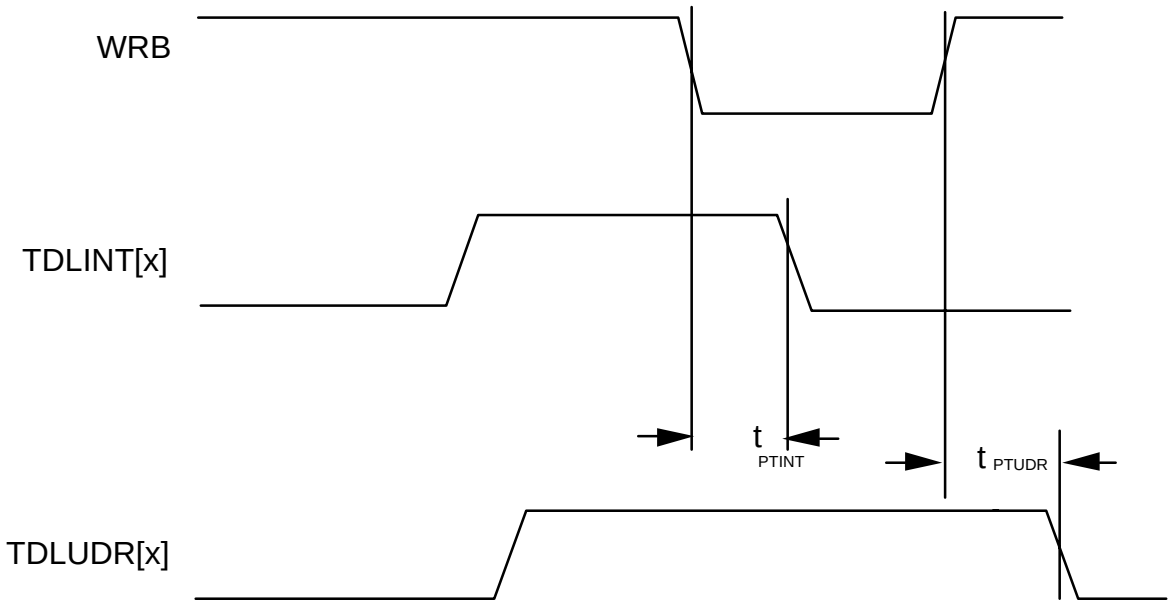
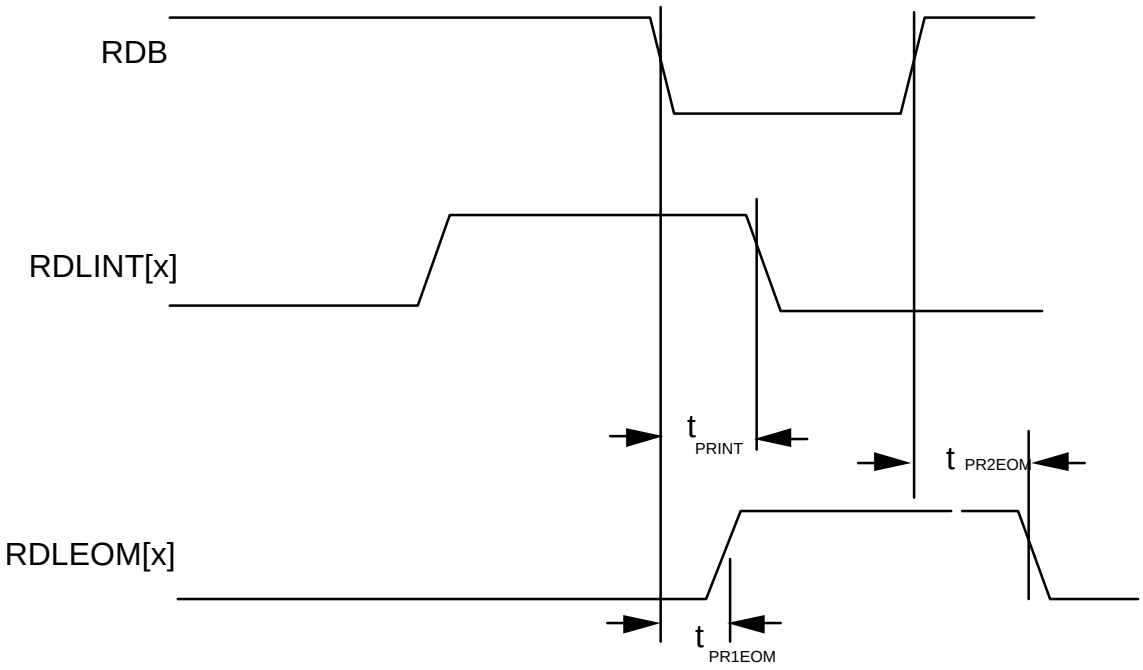


Table 48 - Receive Data Link DMA Interface Output Timing (Figure 64)

Symbol	Description	Min	Max	Units
tPRINT	Receive Data Register Serviced (RDB low) to RDLINT[x] Low Propagation Delay[10,11]		70	ns
tPR1EOM	Receive Data Register Serviced (RDB low) to RDLEOM[x] High Propagation Delay[10,11]		80	ns
tPR2EOM	Receive Status Register Serviced (RDB high) to RDLEOM[x] Low Propagation Delay[10,11]		50	ns

Figure 64 - Receive Data Link DMA Interface Output Timing Diagram



Notes on Input Timing:

1. BTCLK can be a jittered clock signal subject to the minimum and maximum instantaneous frequencies and duty cycles shown.

2. Guaranteed by design for nominal XCLK input frequencies (37.056 MHz ±100 ppm or 12.352 MHz ± 100 ppm).

3. MTCLK can be a jittered clock signal subject to the minimum and maximum instantaneous frequencies and duty cycles shown. These specifications correspond to nominal XCLK input frequencies.

4. High pulse width is measured from the 1.4 Volt points of the rise and fall ramps. Low pulse width is measured from the 1.4 Volt points of the fall and rise ramps.

5. XCLK accuracy is ± 100 ppm.

6. TCLKI[x] can be a jittered clock signal subject to the minimum high and low durations tH_{TCLKI}, tL_{TCLKI}. These durations correspond to nominal XCLK input frequencies.

7. When a set-up time is specified between an input and a clock, the set-up time is the time in nanoseconds from the 1.4 Volt point of the input to the 1.4 Volt point of the clock.

8. When a hold time is specified between an input and a clock, the hold time is the time in nanoseconds from the 1.4 Volt point of the clock to the 1.4 Volt point of the input.

9. tP_{RFP} does not apply if the RCLKOSEL register bit from the Receive Backplane Options register is set to logic 1.

Notes on Output Timing:

1. Output propagation delay time is the time in nanoseconds from the 1.4 Volt point of the reference signal to the 1.4 Volt point of the output.

2. Maximum output propagation delays are measured with a 50 pF load on the outputs.

20 ORDERING AND THERMAL INFORMATION

Table 49 -

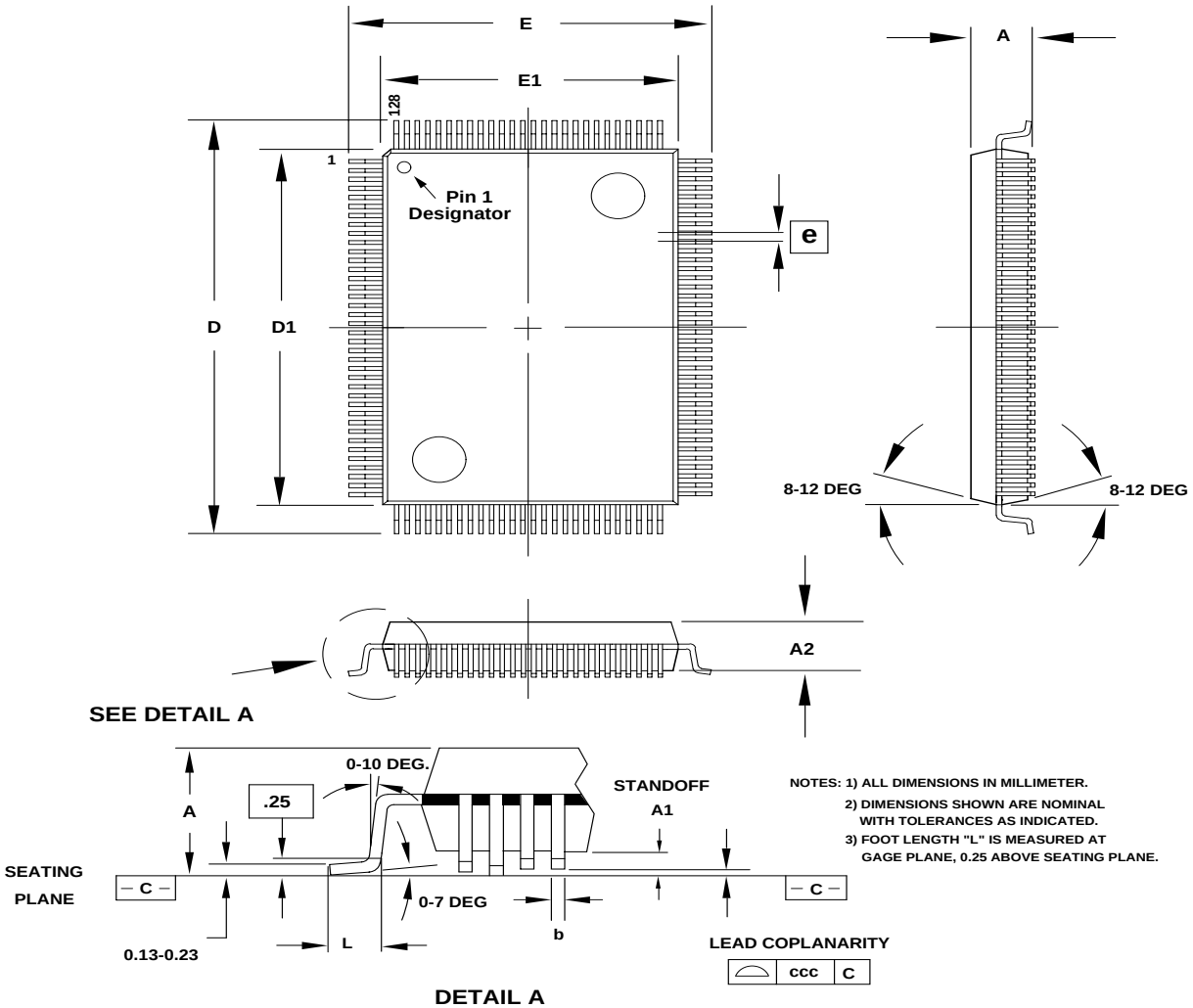
PART NO.	DESCRIPTION
PM4344-RI	128 Plastic Quad Flat Pack (PQFP)

Table 50 -

PART NO.	AMBIENT TEMPERATURE	Theta Ja	Theta Jc
PM4344-RI	-40°C to 85°C	47 °C/W	14 °C/W

21 MECHANICAL INFORMATION

Figure 65 - 128 Pin Copper Leadframe Plastic Quad Flat Pack (R Suffix):



PACKAGE TYPE: 128 PIN METRIC RECTANGULAR PLASTIC QUAD FLATPACK-MQFP											
BODY SIZE: 14 x 20 x 2.7 MM											
Dim.	A	A1	A2	D	D1	E	E1	L	e	b	ccc
Min.	2.82	0.25	2.57	22.95	19.90	16.95	13.90	0.73		0.17	
Nom.			2.70	23.20	20.00	17.20	14.00	0.88	0.50	0.22	
Max.	3.40	0.53	2.87	23.45	20.10	17.45	14.10	1.03		0.27	0.10

NOTES

NOTES

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