WM8581

Multichannel CODEC with S/PDIF Transceiver

DESCRIPTION

The WM8581 is a multi-channel audio CODEC with S/PDIF transceiver. The WM8581 is ideal for DVD and surround sound processing applications for home hi-fi, automotive and other audiovisual equipment.

Integrated into the device is a stereo 24-bit multi-bit sigma delta ADC with support for digital audio output word lengths from 16-bit to 32-bit, and sampling rates from 8kHz to 192kHz.

Also included are four stereo 24-bit multi-bit sigma delta DACs, each with a dedicated oversampling digital interpolation filter. Digital audio input word lengths from 16-bits to 32-bits and sampling rates from 8kHz to 192kHz are supported. Each DAC channel has independent digital volume and mute control.

Two independent audio data interfaces support I^2S, Left Justified, Right Justified and DSP digital audio formats. Each audio interface can operate in either Master Mode or Slave Mode.

The S/PDIF transceiver is IEC-60958-3 compatible and supports frame rates from 32k/s to 192k/s. It has four multiplexed inputs and one output. Status and error monitoring is built-in and results can reported over the serial interface or via GPO pins. S/PDIF Channel Block configuration is also supported.

The device has two PLLs that can be configured independently to generate two system clocks for internal or external use.

Device control and setup is via a 2-wire or 3-wire (SPI compatible) serial interface. The serial interface provides access to all features including channel selection, volume controls, mutes, de-emphasis, S/PDIF control/status, and power management facilities. Alternatively, the device has a Hardware Control Mode where device features can be enabled/disabled using selected pins.

The device is available in a 48-lead TQFP package.

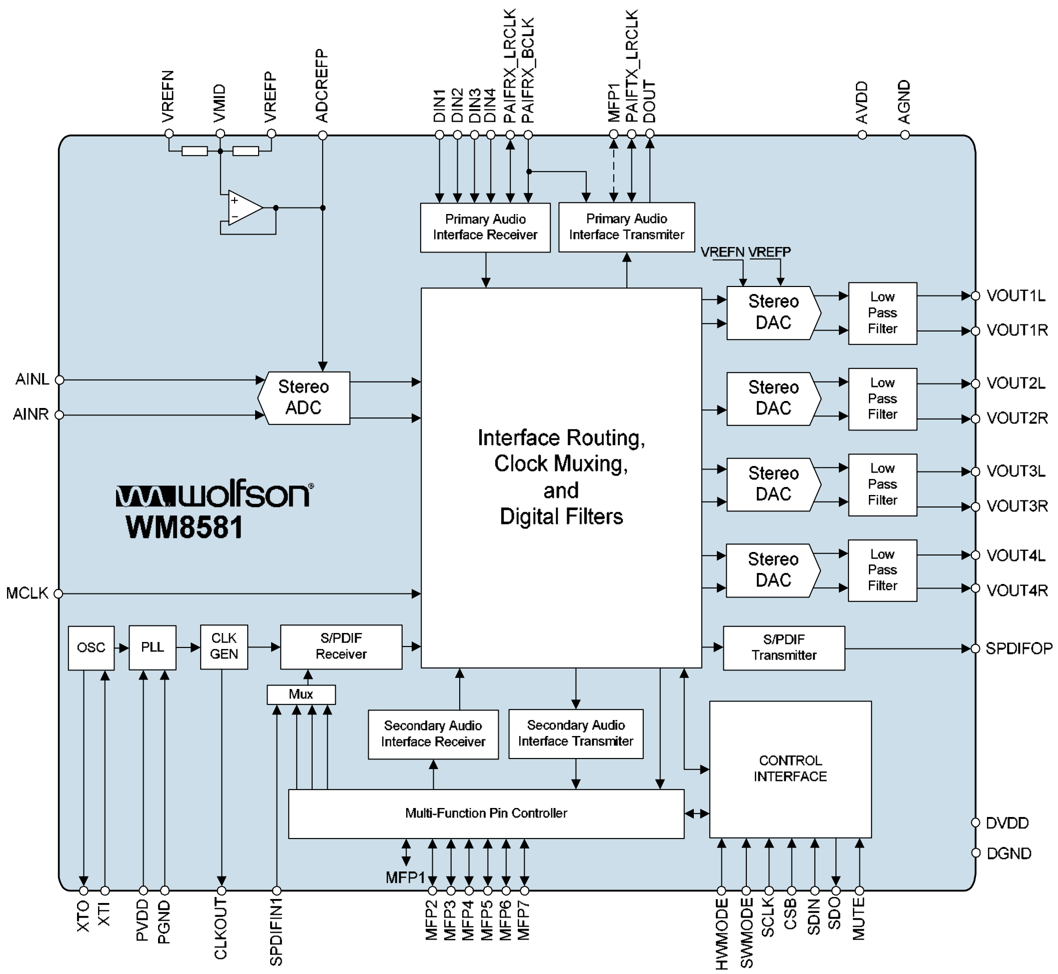
FEATURES

- Mutli-channel CODEC with 4 Stereo DACs and 1 Stereo ADC
- Integrated S/PDIF / IEC-60958-3 transceiver
- Audio Performance
  - 103dB SNR (‘A’ weighted @ 48kHz) DAC
  - -90dB THD (48kHz) DAC
  - 100dB SNR (‘A’ weighted @ 48kHz) ADC
  - -90dB THD (48kHz) ADC
- DAC Sampling Frequency: 8kHz – 192kHz
- ADC Sampling Frequency: 8kHz – 192kHz
- Independent ADC and DAC Sample Rates
- 2 and 3-Wire Serial Control Interface with readback, or Hardware Control Interface
- GPO pins allow visibility of user selected status flags
- Programmable Audio Data Interface Modes
  - I^2S, Left, Right Justified or DSP
  - 16/20/24/32 bit Word Lengths
- Four independent stereo DAC outputs with independent digital volume controls
- Two Independent Master or Slave Audio Data Interfaces
- Flexible Digital Interface Routing with Clock Selection Control
- 2.7V to 5.5V Analogue, 2.7V to 3.6V Digital Supply Operation
- 48-lead TQFP Package

APPLICATIONS

- Digital TV
- DVD Players and Receivers
- Surround Sound AV Processors and Hi-Fi systems
- Automotive Audio

BLOCK DIAGRAM



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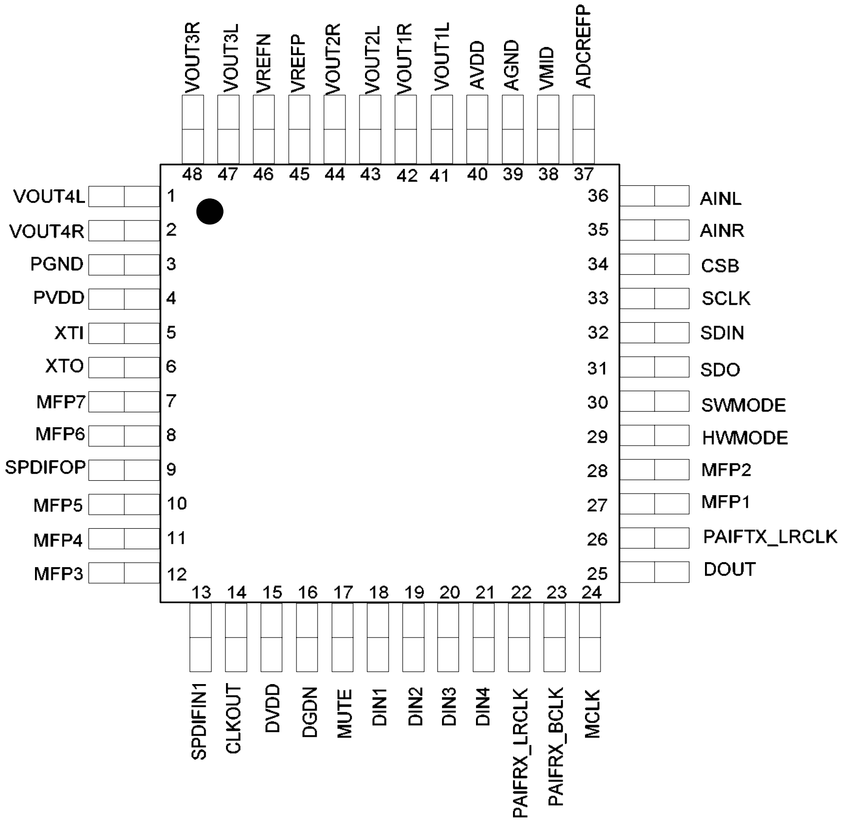
PIN CONFIGURATION



ORDERING INFORMATION

DEVICE	TEMPERATURE RANGE	PACKAGE	MOISTURE SENSITIVITY LEVEL	PEAK SOLDERING TEMPERATURE
WM8581SEFT/V	-25 to +85°C	48-lead TQFP (Pb-free)	MSL1	260°C
WM8581SEFT/RV	-25 to +85°C	48-lead TQFP (Pb-free, tape and reel)	MSL1	260°C

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	VOUT4L	Analogue Output	DAC channel 4 left output
2	VOUT4R	Analogue Output	DAC channel 4 right output
3	PGND	Supply	PLL ground
4	PVDD	Supply	PLL positive supply
5	XTI	Digital Input	Crystal or CMOS clock input
6	XTO	Digital Output	Crystal output
7	MFP7	Digital Input/Output	Multi-Function Pin (MFP) 7. See Table 1 for details of all MFP pins.
8	MFP6	Digital Input/Output	Multi-Function Pin (MFP) 6. See Table 1 for details of all MFP pins.
9	SPDIFOP	Digital Output	S/PDIF transmitter output
10	MFP5	Digital Input/Output	Multi-Function Pin (MFP) 5. See Table 1 for details of all MFP pins.
11	MFP4	Digital Input/Output	Multi-Function Pin (MFP) 4. See Table 1 for details of all MFP pins.
12	MFP3	Digital Input/Output	Multi-Function Pin (MFP) 3. See Table 1 for details of all MFP pins.
13	SPDIFIN1	Digital Input	S/PDIF Receiver Input 1
14	CLKOUT	Digital Output	PLL or crystal oscillator clock output
15	DVDD	Supply	Digital positive supply
16	DGND	Supply	Digital ground
17	MUTE	Digital Input/Output	DAC mute-all input/ All-DAC Infinite Zero Detect (IZD) flag output
18	DIN1	Digital Input	Primary Audio Interface (PAIF) receiver data input 1
19	DIN2	Digital Input	Primary Audio Interface (PAIF) receiver data input 2
20	DIN3	Digital Input	Primary Audio Interface (PAIF) receiver data input 3
21	DIN4	Digital Input	Primary Audio Interface (PAIF) receiver data input 4
22	PAIFRX_LRCLK	Digital Input/Output	Primary Audio Interface (PAIF) receiver left/right word clock
23	PAIFRX_BCLK	Digital Input/Output	Primary Audio Interface (PAIF) receiver bit clock
24	MCLK	Digital Input/Output	System Master clock; 256, 384, 512, 768, 1024 or 1152 fs
25	DOUT	Digital Output	Primary Audio Interface (PAIF) transmitter data output
26	PAIFTX_LRCLK	Digital Input/Output	Primary audio interface transmitter left/right word clock
27	MFP1	Digital Input/Output	Multi-Function Pin (MFP) 1. See Table 1 for details of all MFP pins.
28	MFP2	Digital Input/Output	Multi-Function Pin (MFP) 2. See Table 1 for details of all MFP pins.
29	HWMODE	Digital Input	Configures control to be either Software Mode or Hardware Mode
30	SWMODE	Digital Input/Output	Configures software interface to be either 2-wire or 3-wire. See note 2.
31	SDO	Digital Output	3-wire control interface data output. See note 3.
32	SDIN	Digital Input/Output	Control interface data input (and output under 2-wire control)
33	SCLK	Digital Input	Control interface clock
34	CSB	Digital Input	3-wire control interface latch signal / device address selection
35	AINR	Analogue Input	ADC Right Channel Input
36	AINL	Analogue Input	ADC Left Channel Input
37	ADCREFP	Analogue Output	ADC reference buffer decoupling pin; 10uF external decoupling
38	VMID	Analogue Output	Midrail divider decoupling pin; 10uF external decoupling
39	AGND	Supply	Analogue ground
40	AVDD	Supply	Analogue positive supply
41	VOUT1L	Analogue Output	DAC channel 1 left output
42	VOUT1R	Analogue Output	DAC channel 1 right output
43	VOUT2L	Analogue Output	DAC channel 2 left output
44	VOUT2R	Analogue Output	DAC channel 2 right output
45	VREFP	Analogue Input	DAC and ADC positive reference
46	VREFN	Analogue Input	DAC and ADC ground reference

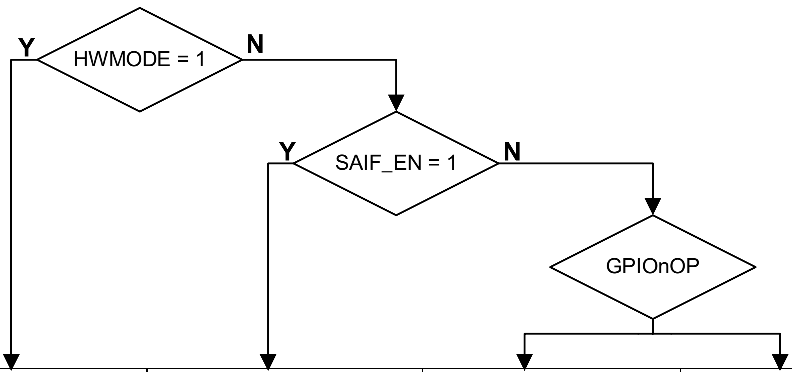
PIN	NAME	TYPE	DESCRIPTION
47	VOUT3L	Analogue Output	DAC channel 3 left output
48	VOUT3R	Analogue Output	DAC channel 3 right output

Notes :

1. Digital input pins have Schmitt trigger input buffers. Pins 32, 33, 34 are 5V tolerant.
2. In hardware control mode, pin 30 is used for UNLOCK flag output.
3. In hardware control mode, pin 31 is used for NON_AUDIO flag output.

MULTI-FUNCTION PINS

The WM8581 has 7 Multi-Function Input/Output pins (MFP1 etc.). The function and direction (input/output) of these pins reconfigured using the HWMODE input pin and software register control as shown below. If HWMODE is set, the MFPs have the function shown in column 1 of Table 1. If HWMODE is not set, and the register SAIF_EN is set, the MFPs have the function shown in column 2. Otherwise, the GPOnOP registers determine the MFP function as shown in columns 3 and 4.



PIN NAME	HARDWARE CONTROL MODE FUNCTION 1	SECONDARY AUDIO INTERFACE FUNCTION 2	S/PDIF INPUT & INDEPENDENT CLOCKING 3	GENERAL PURPOSE OUTPUT FUNCTION 4
MFP1	PAIFTX_BCLK	n/a[1]	PAIFTX_BCLK[2]	GPO1
MFP2	ADCMCLK	n/a[1]	ADCMCLK[3]	GPO2
MFP3	DR1	n/a[1]	SPDIFIN2	GPO3
MFP4	DR2	SAIF_DIN	SPDIFIN3	GPO4
MFP5	DR3	SAIF_DOUT	SPDIFIN4	GPO5
MFP6	DR4	SAIF_BCLK	GPO6	GPO6
MFP7	ALLPD	SAIF_LRCLK	GPO7	GPO7

Table 1 Multi-Function Pin Configuration

Notes:

1. These pins are not used as part of the Secondary Audio Interface, so their function is that of either Column 3 or Column 4.
2. MFP1 can by GPO1 only if ADC_CLKSEL and PAIFTXMST_CLKSEL (if in master mode) source MCLK.
3. MFP2 can be GPO2 if neither ADC_CLKSEL, TX_CLKSEL or SAIFMST_CLKSEL (if in master mode) source ADCMCLK.

PIN FUNCTION	TYPE	DESCRIPTION
PAIFTX_BCLK	Digital Input/Output	Primary Audio Interface Transmitter (PAIFTX) Bit Clock
ADCMCLK	Digital Input	Master ADC clock; 256fs, 384fs, 512fs ,786fs, 1024fs or 1152fs
SAIF_DIN	Digital Input	Secondary Audio Interface (SAIF) Receiver data input
SAIF_DOUT	Digital Output	Secondary Audio Interface (SAIF) Transmitter data output
SAIF_BCLK	Digital Input/Output	Secondary Audio Interface (SAIF) Bit Clock
SAIF_LRCLK	Digital Input/Output	Secondary Audio Interface (SAIF) Left/Right Word Clock
SPDIFIN2/3/4	Digital Input	S/PDIF Receiver Input
GPO1 - GPO7	Digital Output	General Purpose Output
DR1/2/3/4	Digital Input	Internal Digital Routing Configuration in Hardware Mode
ALLPD	Digital Input	Chip Powerdown in Hardware Mode
C	Digital Output	Recovered channel-bit for current S/PDIF sub-frame
SFRM_CLK	Digital Output	Indicates current S/PDIF sub-frame: 1 = Sub-frame A 0 = Sub-frame B
192BCLK	Digital Output	Indicates start of S/PDIF 192-frame block. High for duration of frame 0.

Table 2 Multi-Function Pin Description

ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are stress ratings only. Permanent damage to the device may be caused by continuously operating at or beyond these limits. Device functional operating limits and guaranteed performance specifications are given under Electrical Characteristics at the test conditions specified.

ESD Sensitive Device. This device is manufactured on a CMOS process. It is therefore generically susceptible to damage from excessive static voltages. Proper ESD precautions must be taken during handling and storage of this device.

The WM8581 has been classified as MSL1, which has an unlimited floor life at <30°C / 85% Relative Humidity and therefore will not be supplied in moisture barrier bags.

CONDITION	MIN	MAX
Digital supply voltage	-0.3V	+3.63V
Analogue supply voltage	-0.3V	+7V
PLL supply voltage	-0.3V	+5V
Voltage range digital inputs (SCLK, CSB & SDIN only)	DGND -0.3V	+7V
Voltage range digital inputs	DGND -0.3V	DVDD + 0.3V
Voltage range analogue inputs [1]	AGND -0.3V PGND -0.3V	AVDD +0.3V PVDD +0.3V
Master Clock Frequency		37MHz
Operating temperature range, T_A	-25°C	+85°C
Storage temperature prior to soldering	30°C max / 85% RH max	
Storage temperature after soldering	-65°C	+150°C
Pb Free Package body temperature (soldering 10 seconds)		+260°C
Package body temperature (soldering 2 minutes)		+183°C

Notes: 1. Analogue and digital grounds must always be within 0.3V of each other.

Table 3 Absolute Maximum Ratings

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital supply range	DVDD		2.7		3.6	V
Analogue supply range	AVDD, PVDD		2.7		5.5	V
Ground	AGND, VREFN, DGND. PGND			0		V
Difference DGND to AGND/PGND			-0.3	0	+0.3	V

Note: Digital supply DVDD must never be more than 0.3V greater than AVDD.

Table 4 Recommended Operating Conditions

ELECTRICAL CHARACTERISTICS

Test Conditions

AVDD, PVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, PGND, DGND = 0V, T_A = +25°C, 1kHz Signal, fs = 48kHz, 24-Bit Data, Slave Mode, MCLK, ADCMCLK = 256fs, $1V_{rms}$ Input Signal Level unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC Performance (Load = 10kΩ, 50pF)						
0dBFs Full scale output voltage				1.0 x VREFP/5		V_{rms}
Signal to Noise Ratio (Note 1,2,4)	SNR	A-weighted, @ fs = 48kHz		103		dB
		Unweighted, @ fs = 48kHz		100		dB
		A-weighted, @ fs = 48kHz, AVDD = 3.3V		99		dB
		A-weighted, @ fs = 96kHz		101		dB
		Unweighted, @ fs = 96kHz		98		dB
		A-weighted, @ fs = 96kHz, AVDD = 3.3V		99		dB
		A-weighted, @ fs = 192kHz		101		dB
		Unweighted, @ fs = 192kHz		98		dB
		A-weighted, @ fs = 192kHz, AVDD = 3.3V		99		dB
Dynamic Range (Note 2,4)	DNR	A-weighted, -60dB full scale input		103		dB
Total Harmonic Distortion	THD	1kHz, 0dB Full Scale @ fs = 48kHz		-90		dB
		1kHz, 0dB Full Scale @ fs = 96kHz		-87		dB
		1kHz, 0dB Full Scale @ fs = 192kHz		-84		dB
DAC Channel separation				100		dB
Mute Attenuation		1kHz Input, 0dB gain		100		dB
Output Offset Error				2		mV

Test Conditions

AVDD, PVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, PGND, DGND = 0V, T_A = +25°C, 1kHz Signal, fs = 48kHz, 24-Bit Data, Slave Mode, MCLK, ADCMCLK = 256fs, $1V_{rms}$ Input Signal Level unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply Rejection Ratio	PSRR	1kHz $100mV_{p-p}$		50		dB
		20Hz to 20kHz $100mV_{p-p}$		45		dB
ADC Performance						
Full Scale Input Signal Level (for ADC 0dB Input)				1.0 x VREFP/5		V_{rms}
Input resistance				20		kΩ
Input capacitance				10		pF
Signal to Noise Ratio (Note 1,2,4)	SNR	A-weighted, @ fs = 48kHz		100		dB
		Unweighted, @ fs = 48kHz		97		dB
		A-weighted, @ fs = 48kHz, AVDD = 3.3V		97		dB
		A-weighted, @ fs = 96kHz		97		dB
		Unweighted, @ fs = 96kHz		94		dB
		A-weighted, @ fs = 96kHz, AVDD = 3.3V		94		dB
		A-weighted, @ fs = 192kHz		97		dB
		Unweighted, @ fs = 192kHz		94		dB
		A-weighted, @ fs = 192kHz, AVDD = 3.3V		94		dB
Total Harmonic Distortion	THD	1kHz, -1dB Full Scale @ fs = 48kHz		-90		dB
		1kHz, -1dB Full Scale @ fs = 96kHz		-88		dB
		1kHz, -1dB Full Scale @ fs = 192kHz		-85		dB
Dynamic Range	DNR	-60dB FS		100		
ADC Channel Separation		1kHz Input		100		dB
Channel Level Matching (Note 4)		1KHz Signal		0.1		dB
Channel Phase Deviation		1kHz Signal		0.0001		Degree
Offset Error		HPF On		0		LSB
		HPF Off		100		LSB
Power Supply Rejection Ratio	PSRR	1kHz 100mVpp		50		dB
		20Hz to 20kHz 100mVpp		45		dB
Digital Logic Levels (CMOS Levels)						
Input LOW level	V_{IL}				0.3 x DVDD	V
Input HIGH level	V_{IH}		0.7 x DVDD			V
Input leakage current			-1	±0.2	+1	µA
Input capacitance				5		pF
Output LOW	V_{OL}	I_{OL}=1mA			0.1 x DVDD	V
Output HIGH	V_{OH}	I_{OH}= -1mA	0.9 x DVDD			V

Test Conditions

AVDD, PVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, PGND, DGND = 0V, T_A = +25°C, 1kHz Signal, fs = 48kHz, 24-Bit Data, Slave Mode, MCLK, ADCMCLK = 256fs, $1V_{rms}$ Input Signal Level unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analogue Reference Levels						
Reference voltage	V_{VMID}		VREFP/2 – 50mV	VREFP/2	VREFP/2 + 50mV	V
Potential divider resistance	R_{VMID}	VREFP to VMID and VMID to VREFN		2050		kΩ
S/PDIF Transceiver Performance						
Jitter on recovered clock				50		ps
S/PDIF Input Levels CMOS MODE						
Input LOW level	V_{IL}				0.3 X DVDD	V
Input HIGH level	V_{IH}		0.7 X DVDD			V
Input capacitance				1.25		pF
Input Frequency					36	MHz
S/PDIF Input Levels Comparator MODE						
Input capacitance				1.31		pF
Input resistance				18		Ω
Input frequency					25	MHz
Input Amplitude			200		0.5 X DVDD	mV
PLL						
Period Jitter				80		ps(rms)
XTAL						
Input XTI LOW level	VX_{IL}		0		557	mV
Input XTI HIGH level	VX_{IH}		853			mV
Input XTI capacitance	C_{XJ}		3.32		4.491	pF
Input XTI leakage	IX_{leak}		28.92		38.96	mA
Output XTO LOW	VX_{OL}	15pF load capacitors	86		278	mV
Output XTO HIGH	VX_{OH}	15pF load capacitors	1.458		1.942	V
Supply Current						
Analogue supply current		AVDD, VREFP = 5V		45		mA
Analogue supply current		AVDD, VREFP = 3.3V		30		mA
Digital supply current		DVDD = 3.3V		16		mA
Power Down				10		µA

Table 5 Electrical Characteristics

Notes:

1. Ratio of output level with 1kHz full scale input, to the output level with all zeros into the digital input, measured ‘A’ weighted.
2. All performance measurements done with 20kHz low pass filter, and where noted an A-weight filter. Failure to use such a filter will result in higher THD+N and lower SNR and Dynamic Range readings than are found in the Electrical Characteristics. The low pass filter removes out of band noise; although it is not audible it may affect dynamic specification values.
3. VMID decoupled with 10uF and 0.1uF capacitors (smaller values may result in reduced performance).

TERMINOLOGY

1. Signal-to-noise ratio (dB) - SNR is a measure of the difference in level between the full scale output and the output with no signal applied. (No Auto-zero or Automute function is employed in achieving these results).
2. Dynamic range (dB) - DNR is a measure of the difference between the highest and lowest portions of a signal. Normally a THD+N measurement at 60dB below full scale. The measured signal is then corrected by adding the 60dB to it. (e.g. THD+N @ -60dB= -32dB, DR= 92dB).
3. THD (dB) - THD is a ratio, of the rms values, of Distortion/Signal.
4. Stop band attenuation (dB) - Is the degree to which the frequency spectrum is attenuated (outside audio band).
5. Channel Separation (dB) - Also known as Cross-Talk. This is a measure of the amount one channel is isolated from the other. Normally measured by sending a full scale signal down one channel and measuring the other.
6. Pass-Band Ripple - Any variation of the frequency response in the pass-band region.

MASTER CLOCK TIMING

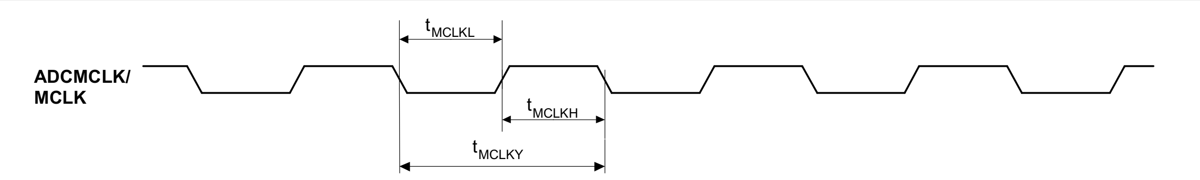


Figure 1 Master Clock Timing Requirements

Test Conditions

AVDD, PVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN = 0V, PGND, DGND = 0V, T_A = +25°C

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
System Clock Timing Information						
ADCMCLK and MCLK System clock pulse width high	t_{MCLKH}		11			ns
ADCMCLK and MCLK System clock pulse width low	t_{MCLKL}		11			ns
ADCMCLK and MCLK System clock cycle time	t_{MCLKY}		28			ns
ADCMCLK and MCLK Duty cycle			40:60		60:40	

Table 3 Master Clock Timing Requirements

DIGITAL AUDIO INTERFACE – MASTER MODE

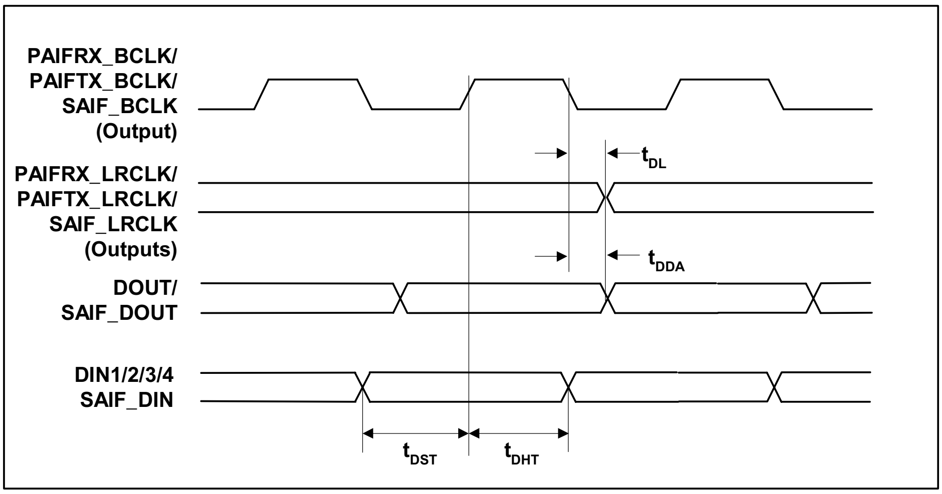


Figure 2 Digital Audio Data Timing – Master Mode

Test Conditions

AVDD, PVDD, VREFP = 5V, DVDD = 3.3V, AGND, VREFN, PGND, DGND = 0V, T_A = +25°C, Master Mode, fs = 48kHz, MCLK and ADCMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
PAIFTX_LRCLK/ PAIFRX_LRCLK/ SAIF_LRCLK propagation delay from PAIFTX_BCLK/ PAIFRX_BCLK/ SAIF_BCLK falling edge	t_{DL}		0		10	ns
DOUT/SAIF_DOUT propagation delay from PAIFTX_BCLK/ SAIF_BCLK falling edge	t_{DDA}		0		10	ns
DIN1/2/3/4/SAIF_DIN setup time to PAIFRX_BCLK/SAIF_BCLK rising edge	t_{DST}		10			ns
DIN1/2/3/4/SAIF_DIN hold time from PAIFRX_BCLK/SAIF_BCLK rising edge	t_{DHT}		10			ns

Table 4 Digital Audio Data Timing – Master Mode

DIGITAL AUDIO INTERFACE – SLAVE MODE

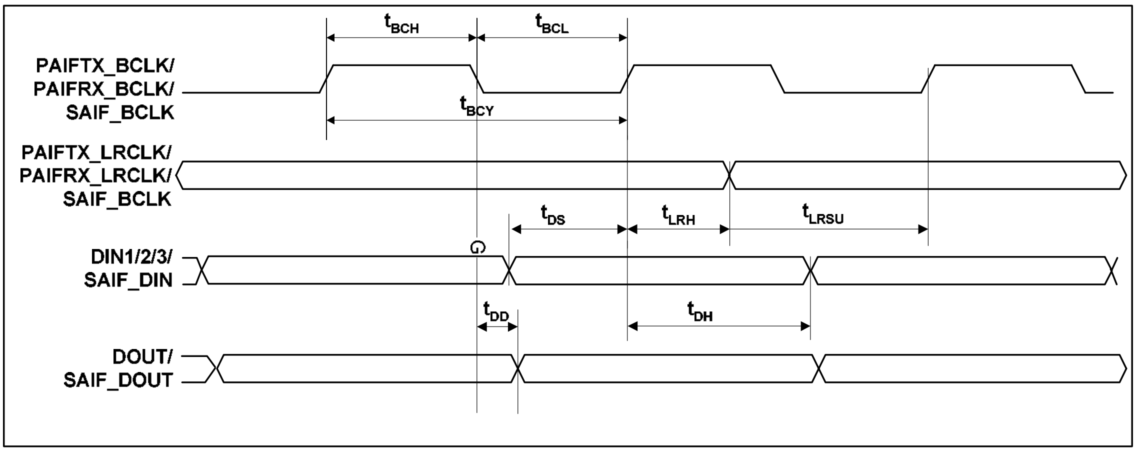


Figure 3 Digital Audio Data Timing – Slave Mode

Test Conditions

AVDD, PVDD = 5V, DVDD = 3.3V, AGND = 0V, PGND,DGND = 0V, T_A = +25°C, Slave Mode, fs = 48kHz, MCLK and ADCMCLK = 256fs unless otherwise stated.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Audio Data Input Timing Information						
PAIFTX_BCLK/ PAIFRX_BCLK/SAIF_BCLK cycle time	t_{BCY}		50			ns
PAIFTX_BCLK/ PAIFRX_BCLK/SAIF_BCLK pulse width high	t_{BCH}		20			ns
PAIFTX_BCLK/ PAIFRX_BCLK/SAIF_BCLK pulse width low	t_{BCL}		20			ns
PAIFTX_LRCLK/ PAIFRX_LRCLK/SAIF_BCLK set-up time to PAIFTX_BCLK/ PAIFRX_BCLK/SAIF_BCLK rising edge	t_{LRSU}		10			ns
PAIFTX_LRCLK/ PAIFRX_LRCLK/ SAIF_LRCLK hold time from PAIFTX_BCLK/ PAIFRX_BCLK/SAIF_BCLK rising edge	t_{LRH}		10			ns
DIN1/2/3/4/SAIF_DIN set-up time to PAIFRX_BCLK/ SAIF_BCLK rising edge	t_{DS}		10			ns
DIN1/2/3/4/SAIF_DIN hold time from PAIFRX_BCLK/SAIF_BCLK rising edge	t_{DH}		10			ns
DOUT/SAIF_DOUT propagation delay from PAIFTX_BCLK/SAIF_BCLK falling edge	t_{DD}		0		10	ns

Table 5 Digital Audio Data Timing – Slave Mode

CONTROL INTERFACE TIMING – 3-WIRE MODE

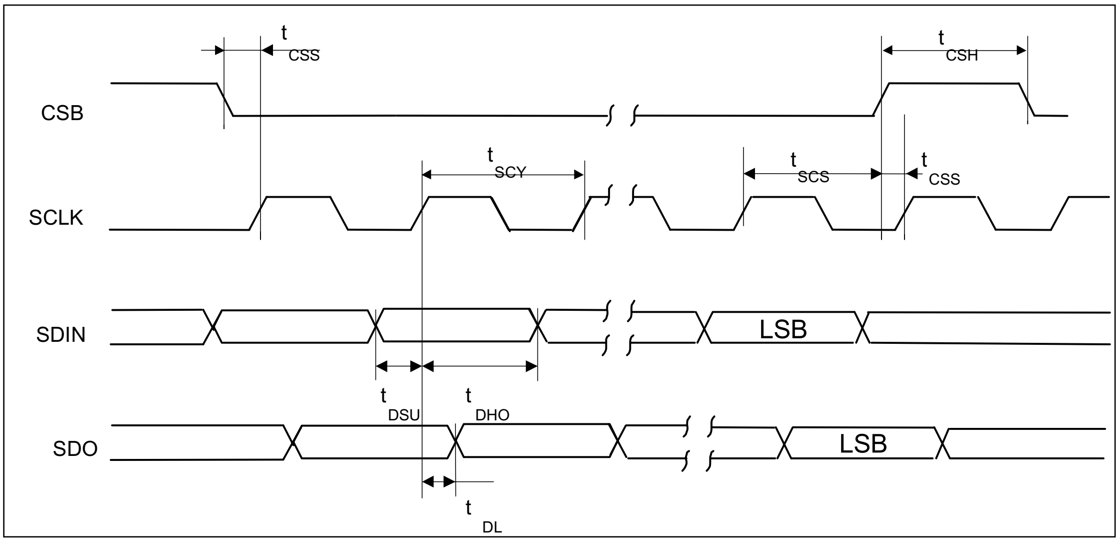


Figure 4 SPI Compatible Control Interface Input Timing

Test Conditions

AVDD, PVDD = 5V,DVDD = 3.3V, AGND, PGND,DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK and ADCMCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
SCLK rising edge to CSB rising edge	t_{SCS}	60			ns
SCLK pulse cycle time	t_{SCY}	80			ns
SCLK duty cycle		40/60		60/40	ns
SDIN to SCLK set-up time	t_{DSU}	20			ns
SDIN hold time from SCLK rising edge	t_{DHO}	20			ns
SDO propagation delay from SCLK rising edge	t_{DL}			5	ns
CSB pulse width high	t_{CSH}	20			ns
CSB rising/falling to SCLK rising	t_{CSS}	20			ns
Pulse width of spikes that will be suppressed	t_{ps}	2		8	ns

Table 6 3-wire SPI Compatible Control Interface Input Timing Information

CONTROL INTERFACE TIMING – 2-WIRE MODE

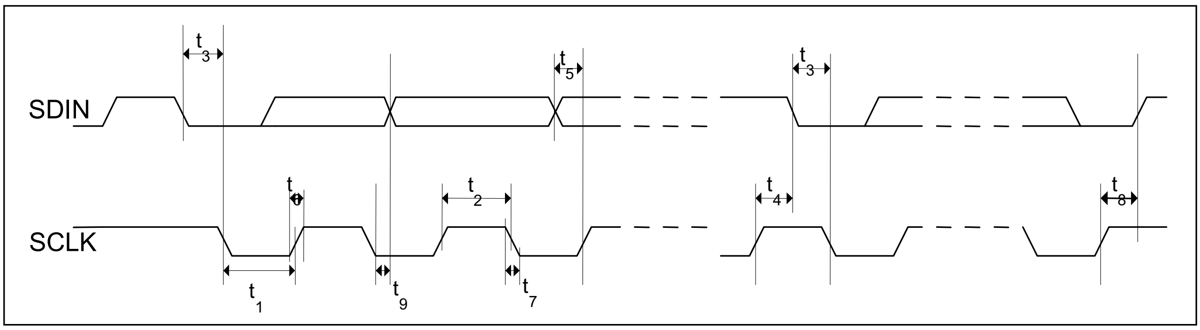


Figure 5 Control Interface Timing – 2-Wire Serial Control Mode

Test Conditions

AVDD, PVDD = 5V,DVDD = 3.3V, AGND, PGND,DGND = 0V, T_A = +25°C, fs = 48kHz, MCLK and ADCMCLK = 256fs unless otherwise stated

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Program Register Input Information					
SCLK Frequency		0		526	kHz
SCLK Low Pulse-Width	t_1	1.3			us
SCLK High Pulse-Width	t_2	600			ns
Hold Time (Start Condition)	t_3	600			ns
Setup Time (Start Condition)	t_4	600			ns
Data Setup Time	t_5	100			ns
SDIN, SCLK Rise Time	t_6			300	ns
SDIN, SCLK Fall Time	t_7			300	ns
Setup Time (Stop Condition)	t_8	600			ns
Data Hold Time	t_9			900	ns
Pulse width of spikes that will be suppressed	t_{ps}	0		5	ns

Table 7 2-Wire Control Interface Timing Information

DEVICE DESCRIPTION

INTRODUCTION

WM8581 is a complete mutli-channel CODEC with integrated S/PDIF transceiver. The device comprises four separate stereo DACs and a stereo ADC, in a single package, and controlled by either software or hardware interfaces.

The four stereo DAC outputs are ideal to implement a complete 7.1 channel surround system. Each DAC has its own digital volume control (adjustable in 0.5dB steps) with zero cross detection. With zero cross enabled, volume updates occur as a signal transitions through its zero point. This minimises audible clicks and 'zipper' noise as the gain values change.

Each stereo DAC has its own data input (DIN1/2/3/4) and shared word clock (PAIFRX_LRCLK), bit clock (PAIFRX_BCLK) and master clock (MCLK). The stereo ADC has data output (DOUT), word clock (PAIFTX_LRCLK), and bit clock (PAIFTX_BCLK). This allows the ADC to operate at a different sample rate to the DACs. In addition, a separate ADC master clock (ADCMCLK) can be used instead of MCLK for further flexibility.

There are two independent Digital Audio Interfaces, which may be configured to operate in either master or slave mode. In Slave mode, the LRCLKs and BCLKs are inputs. In Master mode, the LRCLKs and BCLKs are outputs.

The Audio Interfaces support Right Justified, Left Justified, I^2S and DSP formats. Word lengths of 16, 20, 24 and 32 bits are available (with the exception of 32 bit Right Justified).

Operation using system clocks of 128fs, 192fs, 256fs, 384fs, 512fs, 768fs or 1152fs is provided. In Slave mode, selection between clock rates is automatically controlled. In master mode, the master clock to sample rate ratio is set by register control. Sample rates (fs) from less than 8ks/s up to 192ks/s are permitted providing the appropriate system clock is input.

The S/PDIF Transceiver is IEC-60958-3 compatible with 32k frames/s to 192k frames/s support. S/PDIF data can be input on one of four pins, and routed internally to the Audio Interfaces, DAC1, and S/PDIF transmitter. Error flags and status information can be read back over the serial interface, or output on GPO pins. The S/PDIF Transmitter can source data from the ADC, S/PDIF Receiver or Audio Interfaces. The Transceiver supports Consumer Mode Channel information, and transmitted Channel bits can be configured via register control.

The Digital Routing paths between all the interfaces can be configured by the user, as can the corresponding interface clocking schemes.

There are two PLLs, which can be independently configured to generate two system clocks for internal or external use.

The serial control interface is controlled by pins CSB, SCLK, and SDIN, which are 5V tolerant with TTL input thresholds, allowing the WM8581 to be used with DVDD = 3.3V and be controlled by a controller with 5V output.

The WM8581 may also be controlled in hardware mode, selected by the HWMODE pin. In hardware mode, limited control of internal functionality is available via the Multi-Function Pins (MFPs) and CSB, SCLK, SDIN and MUTE pins.

CONTROL INTERFACE OPERATION

Control of the WM8581 is implemented either in Hardware Control Mode or Software Control Mode. The method of control is determined by the state of the HWMODE pin. If the HWMODE pin is low, Software Control Mode is selected. If the HWMODE pin is high, Hardware Control Mode is selected. The Software Control Interface is described below and Hardware Control Mode is described on page 70.

Software control is implemented with a 3-wire (3-wire write, 4-wire read, SPI compatible) or 2-wire (2-wire write, 2-wire read) serial interface.

The interface configuration is determined by the state of the SWMODE pin. If the SWMODE pin is low, the 2-wire configuration is selected. If SWMODE is high the 3-wire SPI compatible configuration is selected.

HWMODE		SWMODE	
0	1	0	1
Software Control	Hardware Control	2-wire control	3-wire control

Table 8 Hardware/Software Mode Setup

The control interface is 5V tolerant, meaning that the control interface input signals CSB, SCLK and SDIN may have an input high level of 5V while DVDD is 3V. Input thresholds are determined by DVDD.

3-WIRE (SPI COMPATIBLE) SERIAL CONTROL MODE WITH READ-BACK

SDIN is used to program data, SCLK is used to clock in the program data and CSB is used to latch the program data. SDIN is sampled on the rising edge of SCLK. The 3-wire interface write protocol is shown in Figure 6.

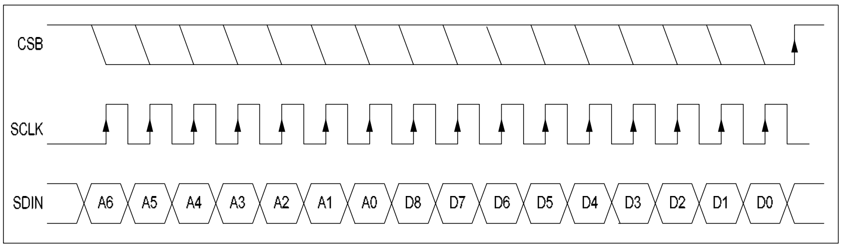


Figure 6 3-Wire SPI Compatible Interface.

1. A[6:0] are Control Address Bits
2. D[8:0] are Control Data Bits
3. CSB is edge sensitive – the data is latched on the rising edge of CSB.

REGISTER READ-BACK

The read-only status registers can be read back via the SDO pin. To enable readback the READEN control register bit must be set. The status registers can then be read using one of two methods, selected by the CONTREAD register bit.

With CONTREAD set, a single register can be read back simply by writing to any other register or a dummy register. The register to be readback is determined by the READMUX[2:0] bits. When a write to the device is done, the device will respond with the status byte set by the READMUX register bits in the last 8 bits of the write.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R52 READBACK 34h	2:0	READMUX [2:0]	000	Determines which status register is to be read back: 000 = Error Register 001 = Channel Status Register 1 010 = Channel Status Register 2 011 = Channel Status Register 3 100 = Channel Status Register 4 101 = Channel Status Register 5 110 = S/PDIF Status Register
	3	CONTREAD	0	Continuous Read Enable. 0 = Continuous read-back mode disabled 1 = Continuous read-back mode enabled
	4	READEN	0	Read-back mode enable. 0 = read-back mode disabled 1 = read-back mode enabled

Table 9 Read-back Control Register

The 3-wire interface readback protocol is shown below. Note that the SDO pin is tri-state unless CSB is held low; therefore CSB must be held low for the duration of the read.

READEN=1 & CONTREAD=1

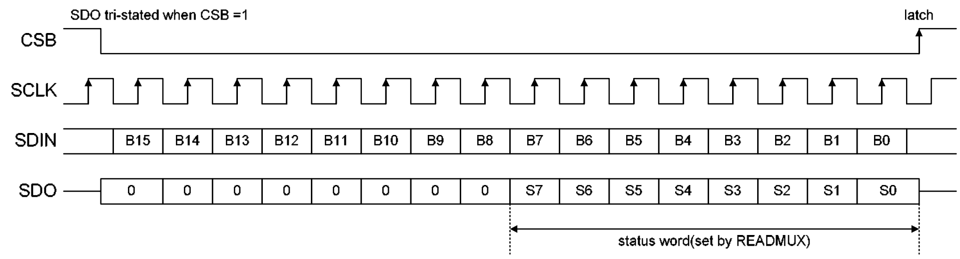


Figure 7 3-Wire SPI Compatible Interface Continuous Readback

If CONTREAD is set to zero, the user can read back directly from the register by writing to the register address, to which the device will respond with data. The protocol for this system is shown in Figure 8 below.

READEN=1 & CONTREAD=0

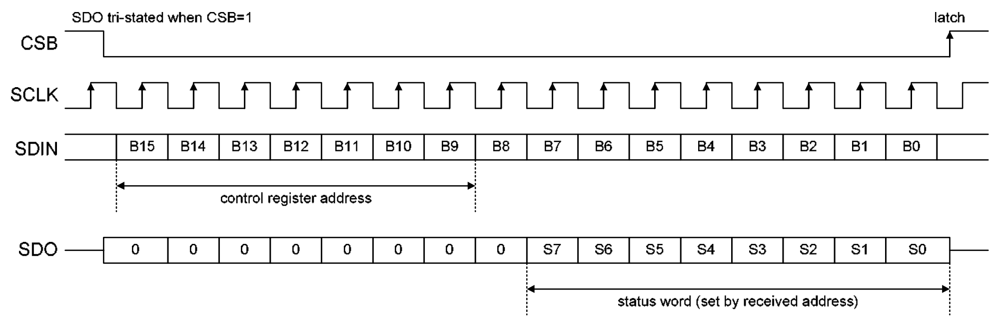


Figure 8 3-Wire SPI Compatible Control Interface Non-Continuous Readback

2-WIRE SERIAL CONTROL MODE WITH READ-BACK

The WM8581 supports software control via a 2-wire (2-wire write, 3-wire read) serial bus. Many devices can be controlled by the same bus, and each device has a unique 7-bit address (see Table 10).

The controller indicates the start of data transfer with a high to low transition on SDIN while SCLK remains high. This indicates that a device address and data will follow. All devices on the 2-wire bus respond to the start condition and shift in the next eight bits on SDIN (7-bit address + Read/Write bit, MSB first). If the device address received matches the address of the WM8581, the WM8581 responds by pulling SDIN low on the next clock pulse (ACK). If the address is not recognised, the WM8581 returns to the idle condition and wait for a new start condition and valid address.

Once the WM8581 has acknowledged a correct address, the controller sends the first byte of control data (B15 to B8, i.e. the WM8581 register address plus the first bit of register data). The WM8581 then acknowledges the first data byte by pulling SDIN low for one clock pulse. The controller then sends the second byte of control data (B7 to B0, i.e. the remaining 8 bits of register data), and the WM8581 acknowledges again by pulling SDIN low.

The transfer of data is complete when there is a low to high transition on SDIN while SCLK is high. After receiving a complete address and data sequence the WM8581 returns to the idle state and waits for another start condition. If a start or stop condition is detected out of sequence at any point during data transfer (i.e. SDIN changes while SCLK is high), the device jumps to the idle condition.

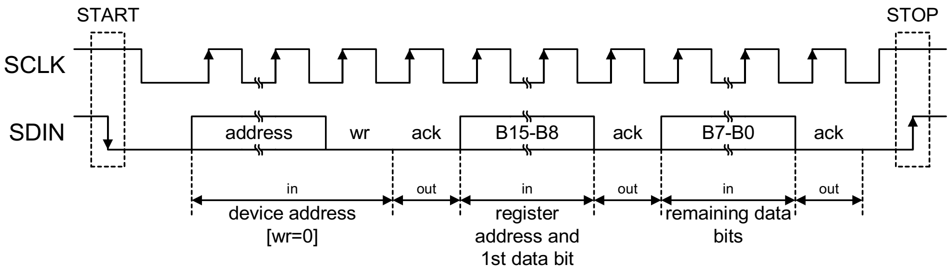


Figure 9 2-Wire Serial Control Interface

The WM8581 has two possible device addresses, which can be selected using the CSB pin.

CSB STATE	DEVICE ADDRESS IN 2-WIRE MODE
Low or Unconnected	0011010
High	0011011

Table 10 2-Wire MPU Interface Address Selection

REGISTER READBACK

The WM8581 allows readback of certain registers in 2-wire mode. As in 3-wire mode, there are two methods of reading back data: continuous and non-continuous readback. Continuous readback is set by writing to the Readback Control register (see Table 9) to set READEN and CONTREAD to 1, and to set the READMUX bits to select the register to be read back. The status of this register can then be readback using the protocol shown in Figure 10.

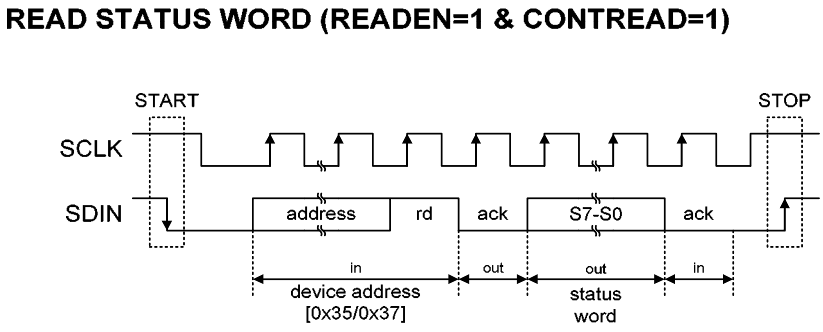


Figure 10 2-Wire Continuous Readback

If CONTREAD is set to zero, the user can read back directly from the register by writing to the register address, to which the device will respond with data. The protocol for this system is shown in Figure 11.

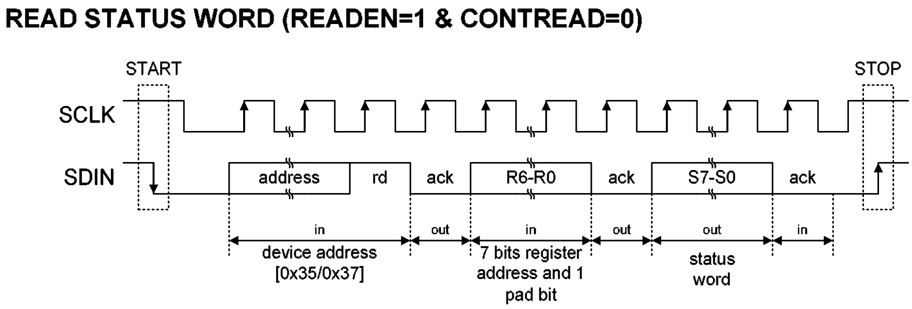


Figure 11 2-Wire Non-Continuous Readback

SOFTWARE REGISTER RESET

Writing to register R53 will cause a register reset, resetting all register bits to their default values. Note that the WM8581 is powered down by default so writing to this register will power down the device.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R53 RESET 35h	8:0	RESET	n/a	Writing any data value to this register will apply a reset to the device registers.

Table 11 Software Reset

DIGITAL AUDIO INTERFACES

Audio data is transferred to and from the WM8581 via the Digital Audio Interfaces. There are two Receive Audio Interfaces and two Transmit Audio Interfaces. The Digital Routing options for these interfaces are described on page 24. Control of the audio interfaces is described below.

MASTER AND SLAVE MODES

The Audio Interfaces require both a left-right-clock (LRCLK) and a bit-clock (BCLK). These can be supplied externally (slave mode) or they can be generated internally (master mode). When in master mode, the BCLKs and LRCLKs for an interface are output on the corresponding BCLK and LRCLK pins. By default, all interfaces operate in slave mode, but can operate in master mode by setting the PAIFTXMS, PAIFRXMS, SAIFMS register bits. In Hardware Control Mode, the PAIF Transmitter can operate in master mode by setting the SDI pin.

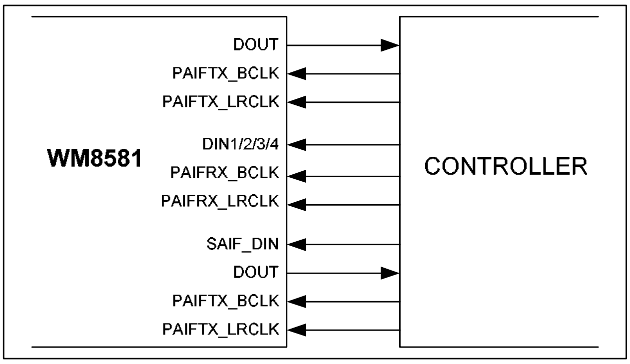


Figure 12 Slave Mode

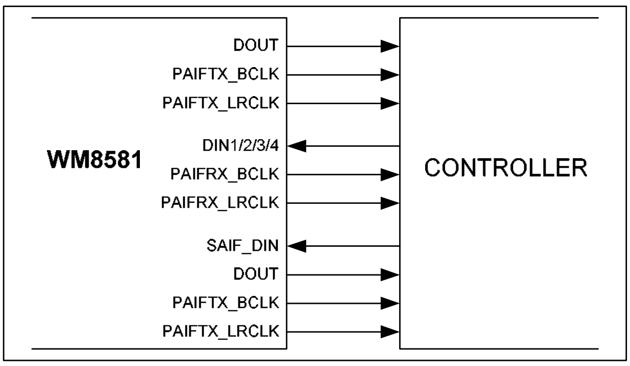


Figure 13 Master Mode

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9	5	PAIFRX MS	0	PAIF Rx Master/Slave Mode Select: 0 = Slave Mode 1 = Master Mode
R10	5	PAIFTX MS	0	PAIF Tx Master/Slave Mode Select: 0 = Slave Mode 1 = Master Mode
R11	5	SAIFMS	0	SAIF Master/Slave Mode Select: 0 = Slave Mode 1 = Master Mode

Table 26 Master Mode Registers

The frequency of a master mode LRCLK is dependant on system clock and the RATE register control bits. Table 27 shows the settings for common sample rates and system clock frequencies.

SAMPLING RATE (LRCLK)	MCLK CLOCK FREQUENCY (MHZ)						
	128fs	**192fs**	**256fs**	**384fs**	**512fs**	**768fs**	**1152fs**
	RATE =000	RATE =001	RATE =010	RATE =011	RATE =100	RATE =101	RATE =110
32kHz	4.096	6.144	8.192	12.288	16.384	24.576	36.864
44.1kHz	5.6448	8.467	11.2896	16.9340	22.5792	33.8688	Unavailable
48kHz	6.144	9.216	12.288	18.432	24.576	36.864	Unavailable
96kHz	12.288	18.432	24.576	36.864	Unavailable	Unavailable	Unavailable
192kHz	24.576	36.864	Unavailable	Unavailable	Unavailable	Unavailable	Unavailable

Table 12 Master Mode MCLK / LRCLK Frequency Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 PAIF 1 09h	2:0	PAIFRX_RATE [2:0]	010	Master Mode MCLK/LRCLK Ratio: 000 = 128fs 001 = 192fs 010 = 256fs 011 = 384fs 100 = 512fs 101 = 768fs 110 = 1152fs
R10 PAIF 2 0Ah	2:0	PAIFTX_RATE [2:0]	010	
R11 SAIF 1 0Bh	2:0	SAIF_RATE [2:0]	010	

Table 13 Master Mode RATE Registers

In master mode, the BCLKSEL register controls the number of BCLKs per LRCLK. If the MCLK:LRCLK ratio is 128fs or 192fs and BCLKSEL = 10, BCLKSEL is overwritten to be 128 BCLKs/LRCLK. Also, if BCLKSEL = 00, and LRCLK is 192fs or 1152fs, the generated BCLK has a mark-space ratio of 1:2.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9 PAIF 1 09h	4:3	PAIFRX_BCLKSEL [1:0]	00	Master Mode BCLK Rate: 00 = 64 BCLKs/LRCLK 01 = 128 BCLKs/LRCLK 10 = 256 BCLKs/LRCLK 11 = BCLK = System Clock.
R10 PAIF 2 0Ah	4:3	PAIFTX_BCLKSEL [1:0]	00	
R11 SAIF 1 0Bh	4:3	SAIF_BCLKSEL [1:0]	00	

Table 14 Master Mode BCLK Control

AUDIO DATA FORMATS

Five popular interface formats are supported:

- Left Justified mode
- Right Justified mode
- I^2S mode
- DSP Mode A
- DSP Mode B

All five formats send the MSB first and support word lengths of 16, 20, 24 and 32 bits, with the exception of 32 bit right justified mode, which is not supported.

Audio Data for each stereo channel is time multiplexed with the interface's Left-Right-Clock (LRCLK), indicating whether the left or right channel is present. The LRCLK is also used as a timing reference to indicate the beginning or end of the data words.

In Left Justified, Right Justified and I^2S modes, the minimum number of BCLKs per LRCLK period is 2 times the selected word length. LRCLK must be high for a minimum of BCLK periods equivalent to the audio word length, and low for minimum of the same number of BCLK periods. Any mark to space ratio on LRCLK is acceptable provided these requirements are met.

In DSP modes A and B, left and right channels must be time multiplexed and input on the input data line on the Audio Interface. For the PAIF Receiver, all four left/right DAC channels are multiplexed on DIN1 (assuming DAC_SEL = 00). LRCLK is used as a frame synchronisation signal to identify the MSB of the first word. The minimum number of BCLKs per LRCLK period is eight times the selected word length. Any mark to space ratio is acceptable on LRCLK provided the rising edge is correctly positioned.

LEFT JUSTIFIED MODE

In Left Justified mode, the MSB of the input data is sampled by the WM8581 on the first rising edge of BCLK following a LRCLK transition. The MSB of the output data changes on the same falling edge of BCLK as LRCLK and may be sampled on the next rising edge of BCLK. LRCLK is high during the left samples and low during the right samples.

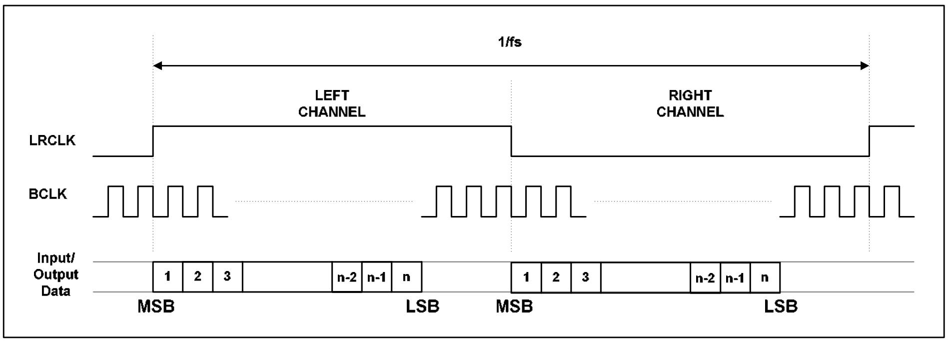


Figure 14 Left Justified Mode Timing Diagram

RIGHT JUSTIFIED MODE

In Right Justified mode, the LSB of input data is sampled on the rising edge of BCLK preceding a LRCLK transition. The LSB of the output data changes on the falling edge of BCLK preceding a LRCLK transition, and may be sampled on the next rising edge of BCLK. LRCLKs are high during the left samples and low during the right samples.

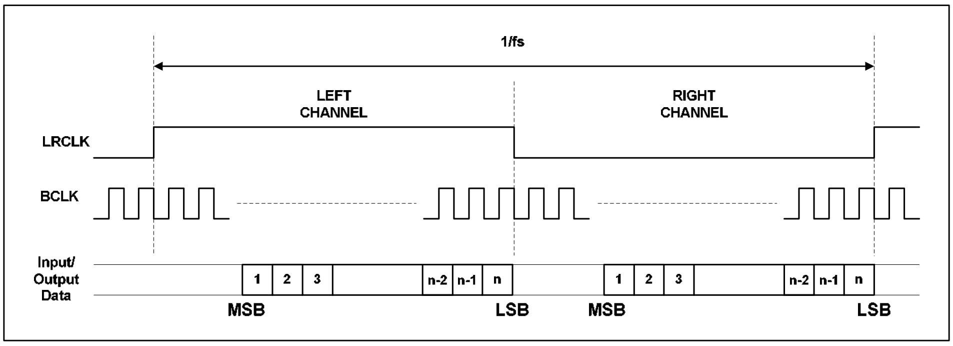


Figure 15 Right Justified Mode Timing Diagram

I^{2}S MODE

In I^{2}S mode, the MSB of DIN1/2/3/4 is sampled on the second rising edge of BCLK following a LRCLK transition. The MSB of the output data changes on the first falling edge of BCLK following an LRCLK transition, and may be sampled on the next rising edge of BCLK. LRCLKs are low during the left samples and high during the right samples.

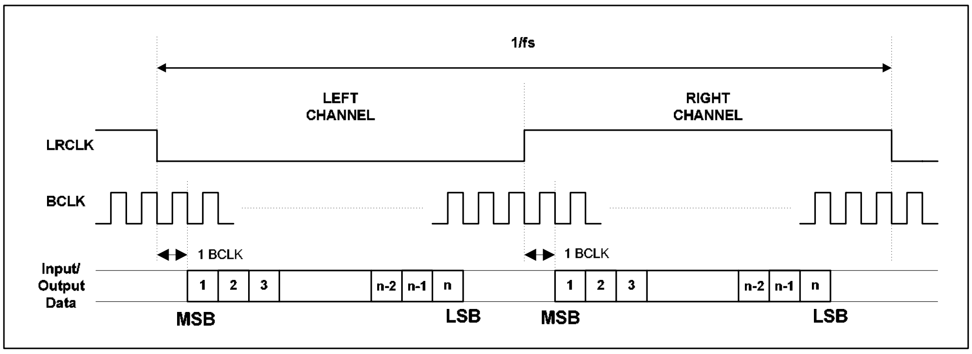


Figure 16 I^{2}S Mode Timing Diagram

DSP MODE A

In DSP Mode A, the MSB of Channel 1 left data is sampled on the second rising edge of BCLK following a LRCLK rising edge. Channel 1 right data then follows. For the PAIF Receiver, Channels 2 , 3 and 4 follow as shown in Figure 17.

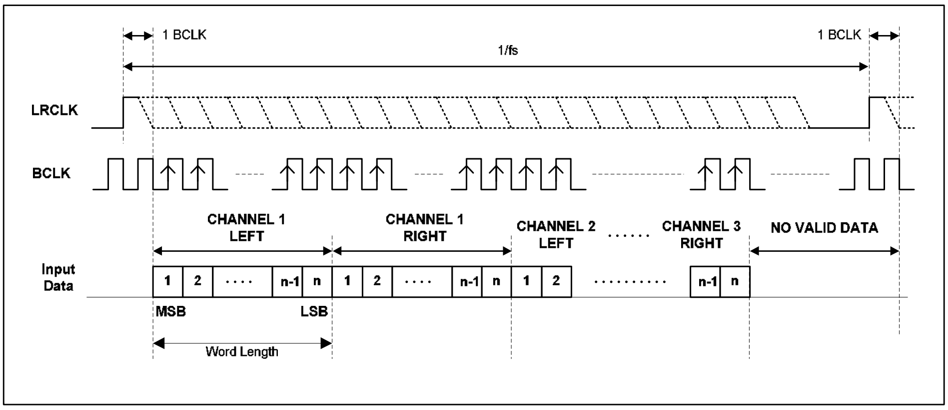


Figure 17 DSP Mode A Timing Diagram – PAIF Receiver Input Data

For the SAIF receiver, only stereo information is processed.

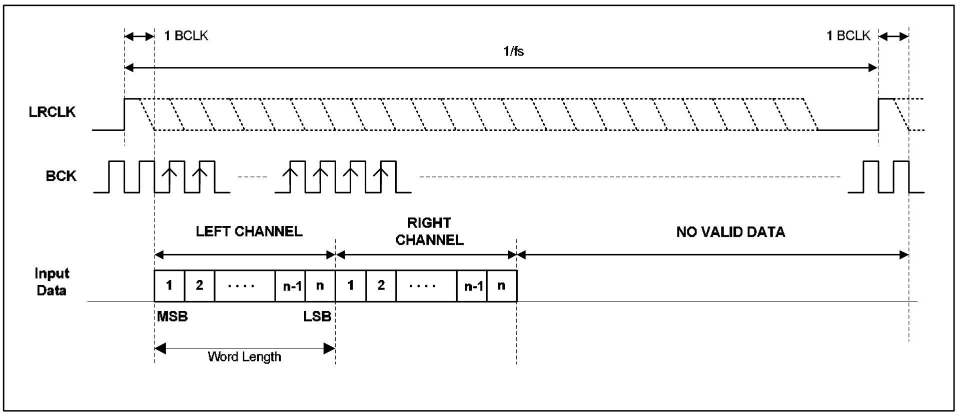


Figure 18 DSP Mode A Timing Diagram - SAIF Receiver Input Data

The MSB of the left channel of the output data changes on the first falling edge of BCLK following a low to high LRCLK transition and may be sampled on the rising edge of BCLK. The right channel data is contiguous with the left channel data.

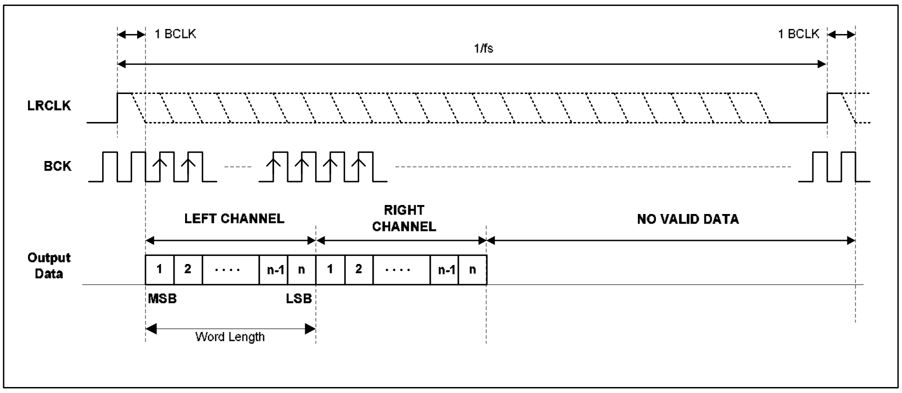


Figure 19 DSP Mode A Timing Diagram – PAIF/SAIF Transmitter Data

DSP MODE B

In DSP Mode B, the MSB of Channel 1 left data is sampled on the first BCLK rising edge following a LRCLK rising edge. Channel 1 right data then follows. For the PAIF Receiver, Channels 2, 3 and 4 follow as shown in Figure 20.

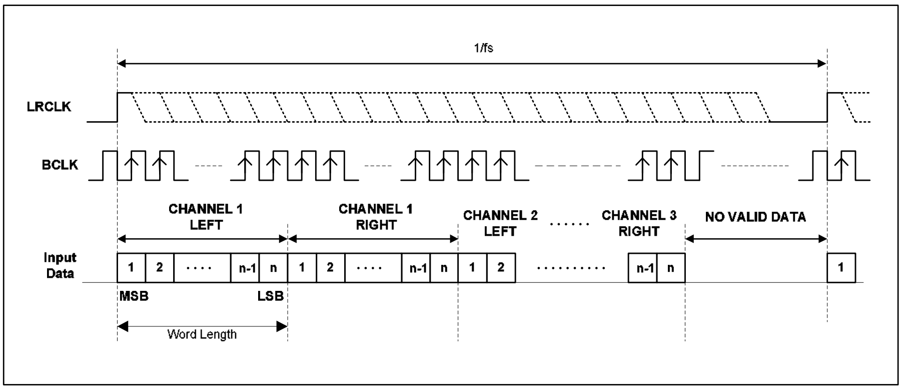


Figure 20 DSP Mode B Timing Diagram – PAIF Receiver Input Data

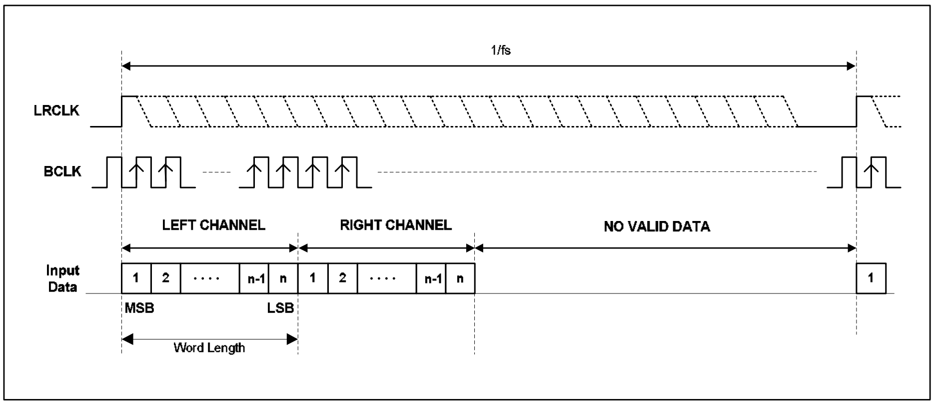


Figure 21 DSP Mode B Timing Diagram - SAIF Receiver Input Data

The MSB of the output data changes on the same falling edge of BCLK as the low to high LRCLK transition and may be sampled on the rising edge of BCLK. The right channel data is contiguous with the left channel data.

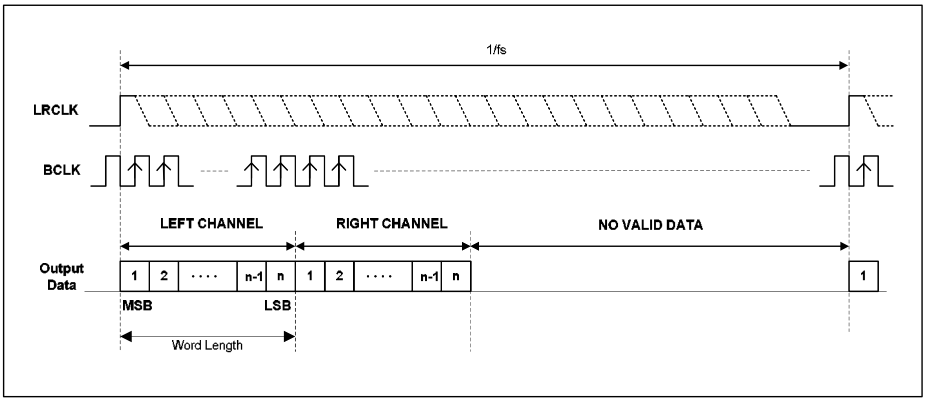


Figure 22 DSP Mode B Timing Diagram – PAIF/SAIF Transmitter Data

AUDIO INTERFACE CONTROL

The register bits controlling the audio interfaces are summarized below. Dynamically changing the audio data format may cause erroneous operation, and is not recommended.

Interface timing is such that the input data and LRCLK are sampled on the rising edge of the interface BCLK. Output data changes on the falling edge of the interface BCLK. By setting the appropriate bit clock polarity control register bits, e.g. PAIFRXBCP, the polarity of BCLK may be reversed, allowing input data and LRCLK to be sampled on the falling edge of BCLK. Setting the bit clock polarity register for a transmit interface results in output data changing on the rising edge of BCLK.

Similarly, the polarity of left/right clocks can be reversed by setting the appropriate left right polarity bits, e.g. PAIFRXLRP.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 PAIF 3 0Ch	1:0	PAIFRXFMT [1:0]	10	PAIF Receiver Audio Data Format Select 11: DSP Format 10: I^{2}S Format 01: Left justified 00: Right justified
	3:2	PAIFRXWL [1:0]	10	PAIF Receiver Audio Data Word Length 11: 32 bits (see Note 1/2) 10: 24 bits 01: 20 bits 00: 16 bits
	4	PAIFRXLRP	0	In LJ/RJ/I^{2}S modes 0 = LRCLK not inverted 1 = LRCLK inverted In DSP Format: 0 = DSP Mode A 1 = DSP Mode B
	5	PAIFRXBCP	0	PAIF Receiver BCLK polarity 0 = BCLK not inverted 1 = BCLK inverted
R13 PAIF 4 0Dh	1:0	PAIFTXFMT [1:0]	10	PAIF Transmitter Audio Data Format Select 11: DSP Format 10: I^{2}S Format 01: Left justified 00: Right justified
	3:2	PAIFTXWL [1:0]	10	PAIF Transmitter Audio Data Word Length 11: 32 bits (see Note 1/2) 10: 24 bits 01: 20 bits 00: 16 bits
	4	PAIFTXLRP	0	In LJ/RJ/I^{2}S modes 0 = LRCLK not inverted 1 = LRCLK inverted In DSP Format: 0 = DSP Mode A 1 = DSP Mode B
	5	PAIFTXBCP	0	PAIF Receiver BCLK polarity 0 = BCLK not inverted 1 = BCLK inverted
R14 SAIF 2 0Eh	1:0	SAIFFMT [1:0]	10	SAIF Audio Data Format Select 11: DSP Format 10: I^{2}S Format 01: Left justified 00: Right justified
	3:2	SAIFWL [1:0]	10	SAIF Audio Data Word Length 11: 32 bits (see Note 1/2) 10: 24 bits 01: 20 bits 00: 16 bits

	4	SAIFLRP	0	In LJ/RJ/I^{2}S modes 0 = LRCLK not inverted 1 = LRCLK inverted In DSP Format: 0 = DSP Mode A 1 = DSP Mode B
	5	SAIFBCP	0	SAIF BCLK polarity 0 = BCLK not inverted 1 = BCLK inverted
	6	SAIF_EN	0	SAIF Enable 0 = SAIF disabled 1 = SAIF enabled

Table 15 Audio Interface Control

Notes

1. Right Justified mode does not support 32-bit data. If word length xAIFxxWL=11b in Right Justified mode, the word length is forced to 24 bits.

   In all modes, the data is signed 2's complement. The digital filters internal signal paths process 24-bit data. If the device is programmed to receive 16 or 20 bit data, the device pads the unused LSBs with zeros. If the device is programmed into 32 bit mode, the 8 LSBs are ignored.

2. In 24 bit I^{2}S mode, any data width of 24 bits or less is supported provided that LRCLK is high for a minimum of 24 BCLK cycles and low for a minimum of 24 BCLK cycles. If exactly 32 bit clocks occur in one full left/right clock period the interface will auto detect and configure a 16 bit data word length.

DAC FEATURES

DAC INPUT CONTROL

The Primary Audio Interface Receiver has a separate input pin for each stereo DAC. Any input pin can be routed to any DAC using the DACSEL register bits.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R15 DAC CONTROL 1 0Fh	1:0	DAC1SEL [1:0]	00	DAC digital input select 00 = DAC takes data from DIN1 01 = DAC takes data from DIN2 10 = DAC takes data from DIN3 11 = DAC takes data from DIN4
	3:2	DAC2SEL [1:0]	01	
	5:4	DAC3SEL [1:0]	10	
	7:6	DAC4SEL [1:0]	11	

Table 16 DAC Input Select Register

DAC OVERSAMPLING CONTROL

For sampling clock ratios of 256fs to 1152fs the DACs should be programmed to operate at 128 times oversampling rate. For sampling clock ratios of 128fs and 192fs, the DACs must be programmed to operate at 64 times oversampling rate. The DACOSR register bit selects between 128x and 64x oversampling.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 PAIF 3 0Ch	6	DACOSR	0	DAC Oversampling Rate Control 0= 128x oversampling 1= 64x oversampling

Table 17 DAC Oversampling Register

DAC OUTPUT CONTROL

The DAC output control word determines how the left and right inputs to the audio interface are applied to the left and right DACs:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R16 DAC CONTROL 2 10h	3:0	PL[3:0]	1001	PL[3:0]	Left O/P	Right O/P
				0000	Mute	Mute
				0001	Left	Mute
				0010	Right	Mute
				0011	(L+R)/2	Mute
				0100	Mute	Left
				0101	Left	Left
				0110	Right	Left
				0111	(L+R)/2	Left
				1000	Mute	Right
				1001	Left	Right
				1010	Right	Right
				1011	(L+R)/2	Right
				1100	Mute	(L+R)/2
				1101	Left	(L+R)/2
				1110	Right	(L+R)/2
				1111	(L+R)/2	(L+R)/2

Table 18 DAC Attenuation Register (PL)

ZERO FLAG OUTPUT

Each DAC channel has a “zero detect circuit” which detects when 1024 consecutive zero samples have been input. Should both channels of a DAC indicate a zero-detect (or if either DACPD or DMUTE is set for that DAC), then the Zero Flag for that DAC is asserted. The DZFM register bits determine which Zero Flag is visible on the MUTE and GPO pins.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 DAC CONTROL 2 10h	6:4	DZFM[2:0]	000	Selects the source for ZFLAG 000 - All DACs Zero Flag 001 - DAC1 Zero Flag 010 - DAC2 Zero Flag 011 - DAC3 Zero Flag 100 - DAC4 Zero Flag 101 - ZFLAG = 0 110 - ZFLAG = 0 111 - ZFLAG = 0

Table 19 DZFM Register

INFINITE ZERO DETECT

Setting the IZD register bit will enable the internal Infinite Zero Detect function:

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R16 DAC CONTROL 2 10h	7	IZD	0	Infinite zero detection circuit control and automute control 0 = Infinite zero detect automute disabled 1 = Infinite zero detect automute enabled

Table 20 IZD Register

With IZD enabled, applying 1024 consecutive zero input samples to a stereo input channel on any DAC will cause that stereo channel output to be muted. Mute will be removed as soon as either of those stereo channels receives a non-zero input.

DAC DIGITAL VOLUME CONTROL

The DAC volume may also be adjusted in the digital domain using independent digital attenuation control registers

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R20 DIGITAL ATTENUATION DACL 1 14h	7:0	LDA1[7:0]	11111111 (0dB)	Digital Attenuation control for DAC1 Left Channel (DACL1) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA1 in intermediate latch (no change to output) 1 = Apply LDA1 and update attenuation on all channels
R21 DIGITAL ATTENUATION DACR 1 15h	7:0	RDA1[6:0]	11111111 (0dB)	Digital Attenuation control for DAC1 Right Channel (DACR1) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA1 in intermediate latch (no change to output) 1 = Apply RDA1 and update attenuation on all channels.
R22 DIGITAL ATTENUATION DACL 2 16h	7:0	LDA2[7:0]	11111111 (0dB)	Digital Attenuation control for DAC2 Left Channel (DACL2) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA2 in intermediate latch (no change to output) 1 = Apply LDA2 and update attenuation on all channels.
R23 DIGITAL ATTENUATION DACR 2 17h	7:0	RDA2[7:0]	11111111 (0dB)	Digital Attenuation control for DAC2 Right Channel (DACR2) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA2 in intermediate latch (no change to output) 1 = Apply RDA2 and update attenuation on all channels.
R24 DIGITAL ATTENUATION DACL3 18h	7:0	LDA3[7:0]	11111111 (0dB)	Digital Attenuation control for DAC3 Left Channel (DACL3) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA3 in intermediate latch (no change to output) 1 = Apply LDA3 and update attenuation on all channels.
R25 DIGITAL ATTENUATION DACR3 19h	7:0	RDA3[7:0]	11111111 (0dB)	Digital Attenuation control for DAC3 Right Channel (DACR3) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA3 in intermediate latch (no change to output) 1 = Apply RDA3 and update attenuation on all channels.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R26 DIGITAL ATTENUATION DACL4 1Ah	7:0	RDA4[7:0]	11111111 (0dB)	Digital Attenuation control for DAC4 Left Channel (DACL4) in 0.5dB steps. See Table 22.
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA4 in intermediate latch (no change to output) 1 = Apply LDA4 and update attenuation on all channels.
R27 DIGITAL ATTENUATION DACR4 1Bh	7:0	MASTDA[7:0]	11111111 (0dB)	Digital Attenuation control for DAC4 Right Channel (DACR4) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	ontrols simultaneous update of all Attenuation Latches 0 = Store RDA4 in intermediate latch (no change to output) 1 = Apply RDA4 and update attenuation on all channels.
R28 MASTER DIGITAL ATTENUATION 1Ch	7:0	MASTDA[7:0]	11111111 (0dB)	Digital Attenuation control for all DAC channels in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store gain in intermediate latch (no change to output) 1 = Apply gain and update attenuation on all channels.

Table 21 Digital Attenuation Registers

Note: The volume update circuit of the WM8581 has two sets of registers; LDAx and RDAx. These can be accessed individually, or simultaneously by writing to MASTDA - Master Digital Attenuation. Writing to MASTDA will overwrite the contents of LDAx and RDAx.

L/RDAx[7:0]	ATTENUATION LEVEL
00(hex)	-∞ dB (mute)
01(hex)	-127.5dB
:	:
:	:
:	:
FE(hex)	-0.5dB
FF(hex)	0dB

Table 22 Digital Volume Control Gain Levels

Setting the DACATC register bit causes the left channel attenuation settings to be applied to both left and right channel DACs from the next audio input sample. No update to the attenuation registers is required for DACATC to take effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 DAC CONTROL 5 13h	6	DACATC	0	Attenuator Control 0 = All DACs use attenuations as programmed. 1 = Right channel DACs use corresponding left DAC attenuations

Table 23 DAC Attenuation Register

The digital volume control also incorporates a zero cross detect circuit which detects a transition through the zero point before updating the digital volume control with the new volume. This mechanism helps prevents pops and clicks during volume transitions, and is enabled by control bit DZCEN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 DAC CONTROL 5 13h	5	DZCEN	0	DAC Digital Volume Zero Cross Enable 0 = Zero Cross detect disabled 1 = Zero Cross detect enabled

Table 24 Digital Zero Cross Register

MUTE MODES

The WM8581 has individual mutes for each of the four DAC channels. Setting DMUTE for a channel will apply a 'soft-mute' to the input of the digital filters for that channel. DMUTE[0] mutes DAC1 channel, DMUTE[1] mutes DAC2 channel, DMUTE[2] mutes DAC3 channel and DMUTE[3] mutes DAC4 channel. Setting the MUTEALL register bit will apply a 'soft-mute' to the input of all the DAC digital filters.

The MUTE pin can also be used to apply soft-mute to the DAC selected by the DZFM register bits. However, if the MPDENB register bit is set, the MUTE pin will activate a soft-mute for all DACs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R19 DAC CONTROL 5 13h	3:0	DMUTE[3:0]	0000	DAC channel soft mute enables: DMUTE[0] = 1, enable soft-mute on DAC1. DMUTE[1] = 1, enable soft-mute on DAC2. DMUTE[2] = 1, enable soft-mute on DAC3. DMUTE[3] = 1, enable soft-mute on DAC4.
	4	MUTEALL	0	DAC channel master soft mute. Mutes all DAC channels: 0 = disable soft-mute on all DACs. 1 = enable soft-mute on all DACs.
	7	MPDENB	0	MUTE pin decode enable: 0 = MUTE activates soft-mute on DAC selected by DZFM 1 = MUTE activates softmute on all DACs

Table 25 Mute Registers

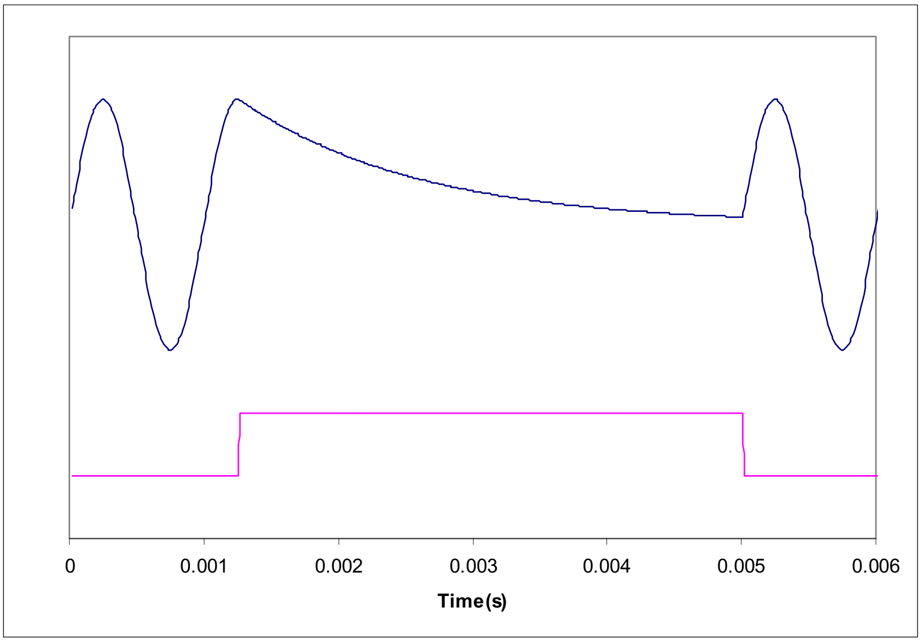


Figure 23 Application and Release of Mute

Figure 23 shows the application and release of MUTE whilst a full amplitude sinusoid is being played at 48kHz sampling rate. When MUTE (lower trace) is asserted, the output (upper trace) begins to decay exponentially from the DC level of the last input sample. The output will decay towards V_{MID} with a time constant of approximately 64 input samples. If MUTE is applied to all channels for 1024 or more input samples the DAC will be muted if IZD is set. When MUTE is de-asserted, the output will restart immediately from the current input sample.

All other means of muting the DAC channels will cause a much more abrupt muting of the output.

DE-EMPHASIS MODE

A digital de-emphasis filter may be applied to each DAC channel. The de-emphasis filter for each stereo channel is enabled under the control of DEEMP[3:0]. DEEMP[0] enables the de-emphasis filter for DAC 1, DEEMP[1] enables the de-emphasis filter for DAC 2, DEEMP[2] enables the de-emphasis filter for DAC 3 and DEEMP[3] enables the de-emphasis filter for DAC 4.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R17 DAC CONTROL 3 11h	3:0	DEEMP[3:0]	0000	De-emphasis mode select: DEEMP[0] = 1, enable De-emphasis on DAC1. DEEMP[1] = 1, enable De-emphasis on DAC2. DEEMP[2] = 1, enable De-emphasis on DAC3. DEEMP[3] = 1, enable De-emphasis on DAC4.
	4	DEEMPALL	0	0 = De-emphasis controlled by DEEMP[3:0] 1 = De-emphasis enabled on all DACs

Table 26 De-emphasis Register

Refer to Figure 40, Figure 40, Figure 41, Figure 42, Figure 43, Figure 44 and Figure 45 for details of the De-Emphasis modes at different sample rates.

DAC OUTPUT PHASE

The DAC Phase control word determines whether the output of each DAC is non-inverted or inverted

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R18 DAC CONTROL 4 12h	7:0	PHASE [7:0]	11111111	Controls phase of DAC outputs 0 = non-inverted 1 = inverted PHASE[0] = 1 inverts phase of DAC1L output PHASE[1] = 1 inverts phase of DAC1R output PHASE[2] = 1 inverts phase of DAC2L output PHASE[3] = 1 inverts phase of DAC2R output PHASE[4] = 1 inverts phase of DAC3L output PHASE[5] = 1 inverts phase of DAC3R output PHASE[6] = 1 inverts phase of DAC4L output PHASE[7] = 1 inverts phase of DAC4R output

Table 27 DAC Output Phase Register

ADC FEATURES

ADC HIGH-PASS FILTER DISABLE

The ADC digital filters incorporate a digital high-pass filter. By default, this is enabled but can be disabled by setting the ADCHPD register bit to 1. This allows the input to the ADC to be DC coupled.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 ADC CONTROL 1 1Dh	4	ADCHPD	0	ADC high-pass filter disable 0 = high-pass filter enabled 1 = high-pass filter disabled

Table 28 ADC Functions Register

ADC OVERSAMPLING RATE SELECT

The internal ADC signal processing operates at an oversampling rate of 128fs for all MCLK:LRCLK ratios. The exception to this is for operation with a 128fs or 192fs master clock, where the internal oversampling rate of the ADC is 64fs.

For ADC operation at 96kHz in 256fs or 384fs mode it is recommended that the user set the ADCOSR bit. This changes the ADC signal processing oversampling rate from 128fs to 64fs. Similarly, for ADC operation at 192kHz in 128fs or 192fs mode it is recommended that the user set the ADCOSR bit to change the oversampling rate from 64fs to 32fs.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 ADC CONTROL 1 1Dh	3	ADCOSR	0	ADC oversample rate select 0 = 128/64x oversampling 1 = 64/32x oversampling

Table 29 ADC Functions Register

ADC MUTE

As with the DAC, each ADC channel also has a mute control bit, which mutes the inputs to the ADC.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 ADC CONTROL 1 1Dh	0	AMUTEL	0	ADC Mute select 0 : Normal Operation 1: mute ADC left
	1	AMUTER	0	ADC Mute select 0 : Normal Operation 1: mute ADC right
	2	AMUTEALL	0	ADC Mute select 0 : Normal Operation 1: mute both ADC channels

Table 30 ADC Mute Register

DIGITAL ROUTING OPTIONS

The WM8581 has extremely flexible digital interface routing options, which are illustrated in Figure 24. It has a S/PDIF Receiver, S/PDIF Transmitter, four Stereo DACs, a Stereo ADC, a Primary Audio Interface and a Secondary Audio Interface.

Each DAC has its own digital input pin DIN1/2/3/4. Internal multiplexers in the Primary Audio Interface Receiver allow the data received on any DIN pin to be routed to any DAC. Any DIN pin routed to DAC1 can also be routed to the S/PDIF transmitter and Secondary Audio Interface Transmitter. DAC1 may also be used to convert received S/PDIF data, or data received from the Secondary Audio Interface. DACs 2-4 take data only from the Primary Audio Interface. The Audio Interfaces can also output ADC data or received S/PDIF data.

The S/PDIF transmitter can output S/PDIF received data, ADC data, or data from either Audio Interface.

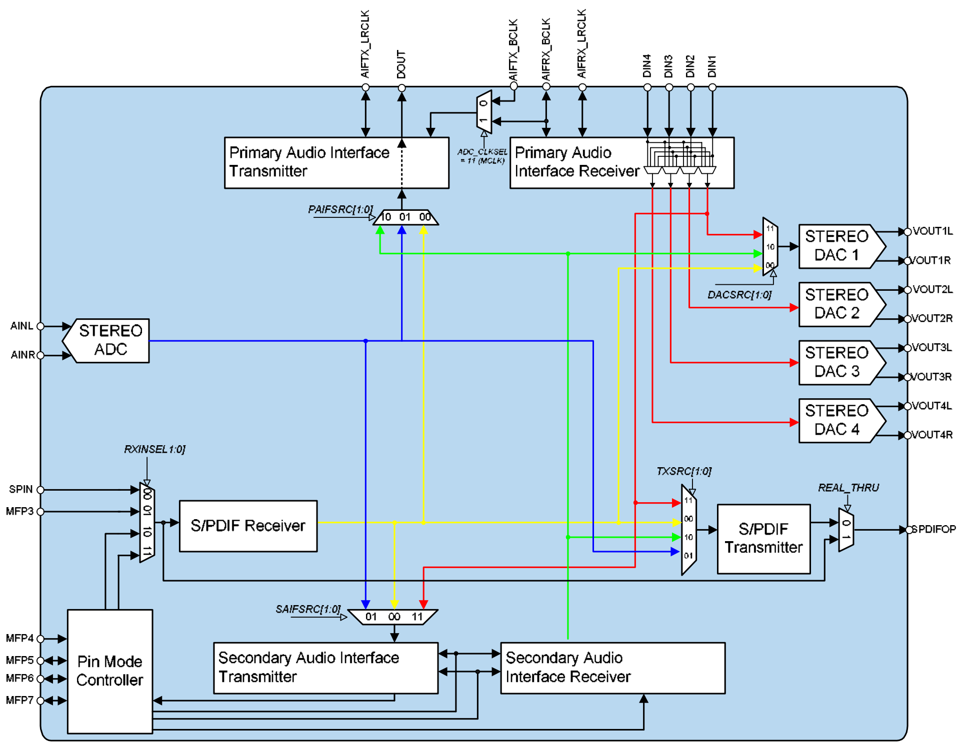


Figure 24 Digital Routing

The registers described below configure the digital routing options.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12	8:7	DAC_SRC [1:0]	11	DAC1 Source: 00 = S/PDIF received data. 10 = SAIF Rx data 11 = PAIF Rx data Note: When DAC_SRC = 00, DAC2/3/4 may be turned off, depending on RX2DAC_MODE.
R13	8:7	PAIFTX_SRC [1:0]	01	Primary Audio Interface Tx Source: 00 = S/PDIF received data. 01 = ADC digital output data. 10 = SAIF Rx data
R14	8:7	SAIFTX_SRC [1:0]	00	Secondary Audio Interface Tx Source: 00 = S/PDIF received data. 01 = ADC digital output data. 11 = PAIF Rx data
R30	1:0	TXSRC [1:0]	00	S/PDIF Transmitter Data Source. 00 = S/PDIF received data('thru-path') 01 = ADC digital output data. 10 = SAIF Rx data 11 = PAIF Rx data
	3	REAL_THRU	0	S/PDIF Thru Mode Control 0 = SPDIFOP pin sources output of S/PDIF Tx 1 = SPDIFOP pins sources output of S/PDIF IN Mux

Table 31 Interface Source Select Registers

CLOCK SELECTION

To accompany the flexible digital routing options, the WM8581 offers a clock configuration scheme for each interface. The user can choose the interface clock from MCLK, ADCMCLK, PLLACLK or PLLBCLK. For some interfaces, the rate can be controlled either by external LRCLK (slave mode), internal LRCLK (master mode) or by control register. The available options are described below.

DAC INTERFACE

The DAC_CLKSEL register selects the DAC clock source from MCLK, PLLACLK or PLLBCLK. If the digital routing has been set such that the DAC1 is sourcing the S/PDIF Receiver, then PLLACLK is automatically selected, and DACs 2/3/4 are powered down. The rate that the DACs operate at is determined by the DAC Rate module. It calculates the rate based on the digital routing setup. When sourcing from the PAIF Receiver, PAIFRX_LRCLK (internal or external) is used in the rate calculation. . When sourcing from the SAIF Receiver, SAIF_LRCLK (internal or external) is used in the rate calculation. The SFRM_CLK is used in the rate calculation when the DAC1 sources from the S/PDIF Receiver, however this can be changed by setting the RX2DAC_MODE register bit. With RX2DAC_MODE set, the PAIFRX_LRCLK determines the rate, and DACs 2/3/4 source the PAIF Receiver (and are no longer automatically powered down).

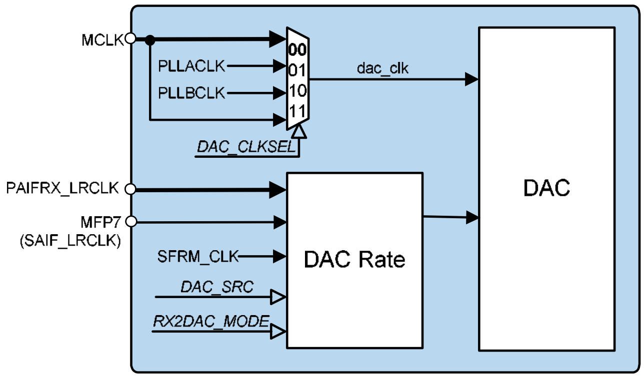


Figure 25 DAC Clock Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8	1:0	DAC_CLKSEL	00	DAC clock source 00 = MCLK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin
R15	8	RX2DAC_MODE	0	DAC Rate and Power down control (only valid when DAC_SRC = 00) 0 = SFRM_CLK determines rate, DACs 2/3/4 powered down 1 = PAIFRX_LRCLK determines rate, DACs 2/3/4 source PAIFRX

Table 32 DAC Clock Control

ADC INTERFACE

The ADC_CLKSEL register selects the ADC clock source from ADCMCLK, PLLACLK, PLLBCLK, or ADCMCLK. However, if the S/PDIF receiver is powered up, the PLLACLK and PLLBCLK are invalid for ADC operation, so the choice is limited to ADCMCLK (default) or MCLK. The rate that the ADC operates at is determined by the ADC Rate module. It calculates the rate based on the digital routing setup. If the ADC is sourced by the PAIF Transmitter, PAIFTX_LRCLK is used in the rate calculation. If the ADC is sourced by the SAIF Transmitter (and PAIF Transmitter has another source), SAIF_LRCLK is used in the rate calculation. If the S/PDIF Transmitter (only) is sourcing the ADC, then the rate is set by the ADC_RATE register bits.

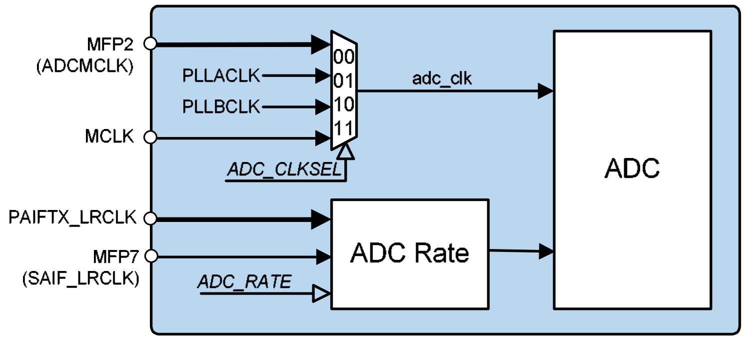


Figure 26 ADC Clock Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8	3:2	ADC_CLKSEL	00	ADC clock source 00 = ADCMLCK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin
R29	7:5	ADCRATE[2:0]	010	ADC Rate Control (only used when the S/PDIF Tx is the only interface sourcing the ADC) 000 = 128fs 001 = 192fs 010 = 256fs 011 = 384fs 100 = 512fs 101 = 768fs 110 = 1152fs

Table 33 ADC Clock Control

S/PDIF INTERFACES

The TX_CLKSEL register selects the clock for the S/PDIF Transmitter from ADCMCLK, PLLACLK, PLLBCLK, or MCLK. The S/PDIF Receiver only uses PLLACLK. If the digital routing has been configured such that the S/PDIF Transmitter is sourcing the S/PDIF Receiver, then PLLACLK is automatically selected. The rate that the S/PDIF Transmitter operates at is determined by the S/PDIF Tx Rate module. It calculates the rate based on the digital routing setup. When sourcing from the S/PDIF Receiver, the SFRM_CLK is used in the rate calculation. When sourcing from the PAIF Receiver, PAIFRX_LRCLK is used in the rate calculation. When sourcing from the SAIF Receiver, SAIFRX_LRCLK is used in the rate calculation. When sourcing the ADC, the rate is determined by either the PAIFTX_LRCLK (if the PAIF Tx also sources the ADC) or the ADC_RATE register.

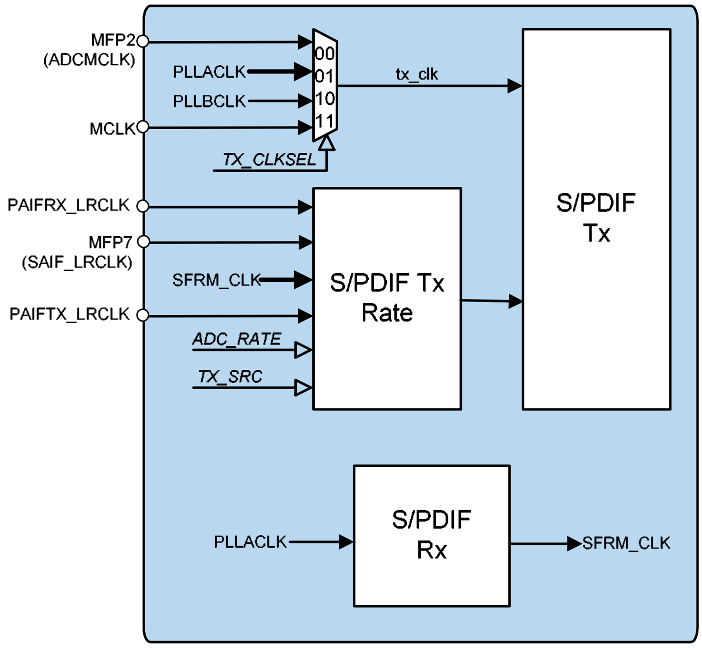


Figure 27 S/PDIF Clock Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R8	5:4	TX_CLKSEL	01	S/PDIF TX clock source 00 = ADCMLCK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin

Table 34 S/PDIF Transmitter Clock Control

PRIMARY AUDIO INTERFACE RECEIVER (PAIF RX)

The PAIF Receiver requires a left-right-clock (LRCLK) and a bit-clock (BCLK). These can be supplied externally (slave mode) or they can be generated internally by the WM8581 (master mode). The master mode LRCLK/BCLK are created by the Master Mode Clock Gen module. The control of this module is described on page 34. The clock supplied to this module is selected by the PAIFRXMS_CLKSEL register and can be MCLK, PLLACLK, or PLLBCLK.

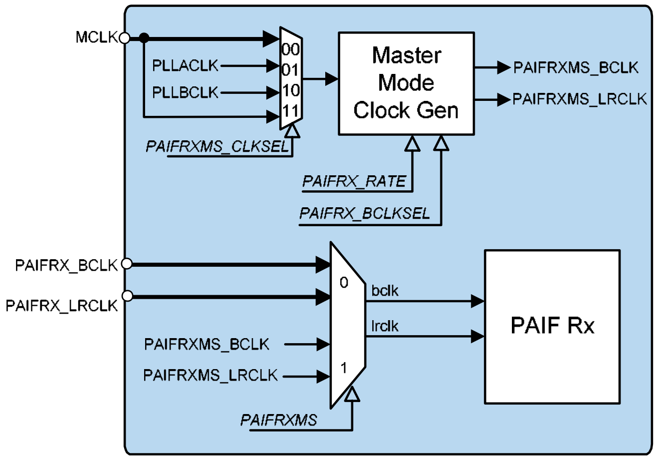


Figure 28 PAIF Receiver Clock Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R9	7:6	PAIFRXMS_ CLKSEL	00	PAIFRX Master Mode clock source 00 = MCLK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin

Table 35 PAIF Receiver Master Mode Clock Control

PRIMARY AUDIO INTERFACE TRANSMITTER (PAIF TX)

The PAIF Transmitter requires a left-right-clock (LRCLK) and a bit-clock (BCLK). These can be supplied externally (slave mode) or they can be generated internally by the WM8581 (master mode). The master mode LRCLK/BCLK are created by the Master Mode Clock Gen module. The control of this module is described on page 34. The clock supplied to this module can be ADCMCLK, PLLACLK, PLLBCLK, or MCLK and is selected by the internal signal *paiftxms_clksel*'. If the PAIF Transmitter is sourcing the S/PDIF Receiver, it is recommended that the interface operate in master mode. For this path, *paiftxms_clksel* selects PLLACLK. For all other digital routing options, *paiftxms_clksel* selects whichever clock the *adc_clk* is using.

If in slave mode, and *adc_clk* is set to be MCLK, then the PAIFRX_BCLK is used as the BCLK for the PAIF Transmitter.

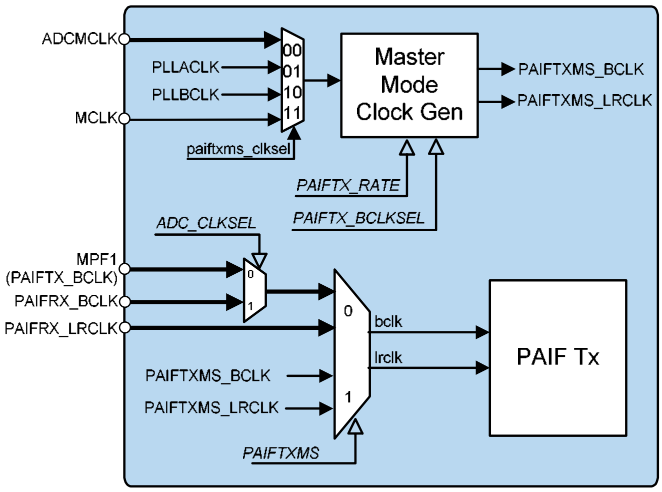


Figure 29 PAIF Transmitter Clock Selection

SECONDARY AUDIO INTERFACES (SAIF RX & SAIF TX)

The Transmit and Receive sides of the Secondary Audio Interface share a common LRCLK and a common BCLK. These can be supplied externally (slave mode) or they can be generated internally by the WM8581 (master mode). The master mode LRCLK/BCLK are created by the Master Mode Clock Gen module. The control of this module is described on page 34. The clock supplied to this module can be ADCMCLK, PLLACLK, PLLBCLK, or MCLK and is selected using the SAIFMS_CLKSEL register. If the digital routing has been configured such that the SAIF Transmitter is sourcing the S/PDIF Receiver, then PLLACLK is automatically selected, and it is recommended that the interface operate in master mode. However, if the SAIF Transmitter sources something other than the S/PDIF Receiver, and the S/PDIF Receiver is powered up, the PLLACLK and PLLBCLK are invalid for SAIF operation, so the choice is limited to ADCMCLK (default) or MCLK.

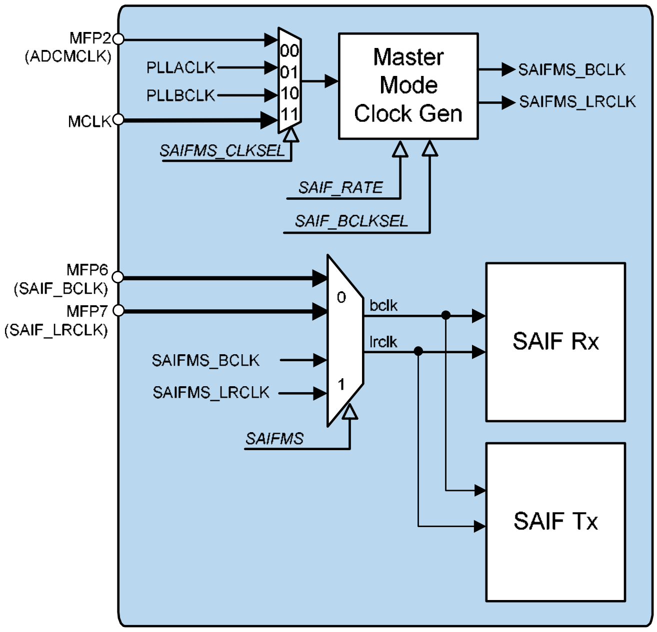


Figure 30 SAIF Clock Selection

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R11	7:6	SAIFMS_ CLKSEL	11	SAIF Master Mode clock source 00 = ADCMCLK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin

Table 36 SAIF Master Mode Clock Control

PHASE-LOCKED LOOPS AND S/PDIF CLOCKING (SOFTWARE MODE)

The WM8581 is equipped with two independent phase-locked loop clock generators and a comprehensive clocking scheme which provides maximum flexibility and function and many configurable routing possibilities for the user in software mode. An overview of the software mode clocking scheme is shown in Figure 31.

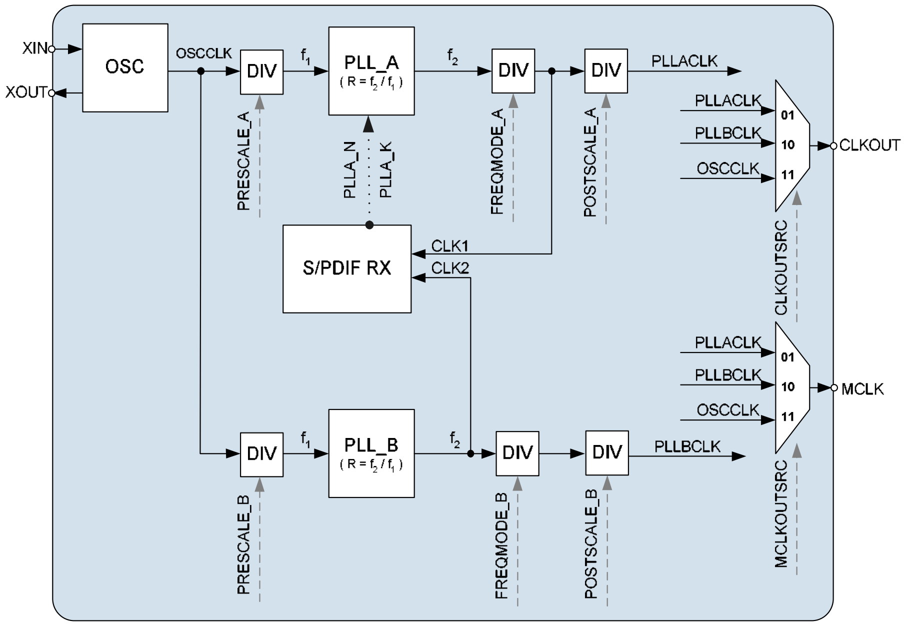


Figure 31 PLL and Clock Select Circuit

OSCILLATOR

The function of the oscillator is to generate the OSCCLK oscillator clock signal. This signal may be used as:

- The clock source for the PLLs.
- A selectable clock source for the MCLK pin, when the pin is configured as an output.
- A selectable clock source for the CLKOUT pin, when enabled.

Whenever the PLLs or the S/PDIF receiver is enabled, the OSCCLK signal must be present to enable the PLLs to generate the necessary clock signals.

The oscillator uses a Pierce type oscillator drive circuit. This circuit requires an external crystal and appropriate external loading capacitors. The oscillator circuit contains a bias generator within the WM8581 and hence an external bias resistor is not required. Crystal frequencies between 10 and 14.4MHz or 16.28MHz and 27MHz can be used in software mode. In this case the oscillator XOUT must be powered up using the OSCPD bit. The recommended circuit is shown in the recommended components diagram, please refer to Figure xx.

Alternatively, an external CMOS compatible clock signal can be applied to the XIN pin in the absence of a crystal. This is not recommended when using the PLL as the PLL requires a jitter-free OSCCLK signal for optimum performance. In this case the oscillator XOUT can be powered down using the OSCPD bit.

The oscillator XOUT pin has one control bit as shown in Table 37.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 PWRDN 2 33h	0	OSCPD	0	Oscillator XOUT Power Down 0 = Power Up XOUT (crystal mode) 1 = Power Down XOUT (CMOS clock input mode)

Table 37 Oscillator Control

PHASE-LOCKED LOOP (PLL)

The WM8581 has two on-chip phase-locked loop (PLL) circuits which can be used to synthesise two independent clock signals (PLLACLK and PLLBCLK) from the external oscillator clock. The PLLs can be used to:

- Generate clocks necessary for the S/PDIF receiver to lock on to and recover S/PDIF data from an incoming S/PDIF data stream.
- Generate clocks which may be used to drive the MCLK and/or CLKOUT pins.
- Generate clocks which may be used by the S/PDIF transmitter to encode and transmit a S/PDIF data stream.
- Generate clocks which may be used as the master clock source for the the ADC and DACs.
- Generate clocks which may be used by the master mode clock generator to generate the BCLK and LRCLK signals for the digital audio interfaces.

The PLLs can be enabled or disabled using the register bits shown in Table 38.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R51 PWRDN 2 33h	1	PLLAPD	1	PLL Power Down Control 0 = Power Up PLL 1 = Power Down PLL
	2	PLLBPD	1	

Table 38 PLL Power Down Control

The PLLs have two modes of operation:

- **PLL S/PDIF Receive Mode (Selected if S/PDIF Receiver Enabled)**

In S/PDIF receive mode, PLLA is automatically controlled by the S/PDIF receiver to allow the receiver to use PLLA to track and lock on to the incoming S/PDIF data stream. In this case, CLK1 is automatically maintained at a constant frequency of 256fs relative to the sample rate of the recovered S/PDIF stream. PLLB must be configured to produce CLK2, a specific reference clock for the S/PDIF receiver.

PLLACLK may be used as a 256fs or 128fs (selectable – refer to Table 43) master clock source when in S/PDIF receiver mode. PLLBCLK is not available and must not be selected as the clock source for any internal function when the S/PDIF receiver is enabled.

If the sample frequency of the incoming stream is changed and PLLA is forced to unlock in order to track to the new sample frequency, the PLLACLK signal will be stopped until the S/PDIF receiver has locked to the incoming stream at the new sample frequency. If the incoming S/PDIF stream stops, the PLLA_ N and PLLA_K values will be frozen and the PLLACLK will continue at the frequency set by the last recovered S/PDIF stream.

Refer to Table 39 and Table 41 for details of the registers available for configuration in this mode. Refer to the S/PDIF Receive Mode Clocking section on page 52 for full details.

- **PLL User Mode (Selected if S/PDIF Receiver Disabled)**

In user mode, the user has full control over the function and operation of both PLLA and PLLB. In this mode, the user can accurately specify the PLL N and K multiplier values and the pre and post-scale divider values and can hence fully control the generated clock frequencies.

Refer to Table 39 and Table 41 for details of the registers available for configuration in this mode.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 PLLA 1/ DEVID1 00h	8:0	PLLA_K[8:0]	100100001	Fractional (K) part of PLLA frequency ratio (R). Value K is one 22-digit binary number spread over registers R0, R1 and R2 as shown.
R1 PLLA 2/ DEVID2 01h	7:0	PLLA_K[17:9]	101111101	
R2 PLLA 3/ DEVREV 02h	3:0	PLLA_K[21:18]	1101	
	7:4	PLLA_N[3:0]	0111	Integer (N) part of PLLA frequency ratio (R). Use values in the range 5 PLLA_N 13 as close as possible to 8
R4 PLLB 1 04h	8:0	PLLB_K[8:0]	100100001	Fractional (K) part of PLLB frequency ratio (R). Value K is one 22-digit binary number spread over registers R4, R5 and R6 as shown. **Note: PLLB_K must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receive Mode Clocking section for details.**
R5 PLLB 2 05h	8:0	PLLB_K[17:9]	101111110	
R6 PLLB 3 06h	3:0	PLLB_K[21:18]	1101	
	7:4	PLL_N[3:0]	0111	Integer (N) part of PLLB frequency ratio (R). Use values in the range 5 PLLB_N 13 as close as possible to 8 **Note: PLLB_N must be set to specific values when the S/PDIF receiver is used. Refer to S/PDIF Receive Mode Clocking section for details.**

Table 39 User Mode PLL_K and PLL_N Multiplier Control

Parameter	PLL User Mode	PLL S/PDIF Receiver Mode
PRESCALE_A	Manual	Write PRESCALE_B Value
PRESCALE_B	Manual	Configure Specified PLLB Frequency
PLLA_N	Manual	Automatically Controlled
PLLA_K	Manual	Automatically Controlled
PLLB_N	Manual	Configure Specified PLLB Frequency
PLLB_K	Manual	Configure Specified PLLB Frequency
FREQMODE_A	Manual	Automatically Controlled
FREQMODE_B	Manual	Not Used
POSTSCALE_A	Manual	256fs/128fs PLLACLK Select
POSTSCALE_B	Manual	Not Used

Table 40 PLL Control Register Function in PLL User and PLL S/PDIF Receiver Modes

PLL CONFIGURATION

The PLLs perform a configurable frequency multiplication of the input clock signal (f_1). The multiplication factor of the PLL (denoted by ‘R’) is variable and is defined by the relationship: R = ($f_2 \div f_1$).

The multiplication factor for each PLL is set using register bits PLLx_N and PLLx_K (refer to Table 39). The multiplication effect of both the N and K multipliers are additive (i.e. if N is configured to provide a multiplication factor of 8 and K is configured to provide a multiplication factor of 0.192, the overall multiplication factor is 8 + 0.192 = 8.192).

In order to choose and configure the correct values for PLLx_N and PLLx_K, multiplication factor R must first be calculated. Once value R is calculated, the value of PLLx_N is the integer (whole number) value of R, ignoring all digits to the right of the decimal point. For example, if R is calculated to be 8.196523, PLL_N is simply 8.

Once PLLx_N is calculated, the PLLx_K value is simply the integer value of (2^{22} (R-PLLx_N)). For example, if R is 8.196523 and PLLx_N is 8, PLLx_K is therefore (2^{22} (8.196523-8)), which is 824277 (ignoring all digits to the right of the decimal point).

Note: the PLLs are designed to operate with best performance (shortest lock time and optimum stability) when f_2 is between 90 and 100MHz and PLLx_N is 8. However, acceptable PLLx_N values lie in the range 5 PLLx_N 13.

Each PLL has an output divider to allow the f_2 clock signal to be divided to a frequency suitable for use as the source for the MCLK and CLKOUT outputs, the S/PDIF transmitter and the internal ADC and DACs. The divider output is configurable and is set by the FREQMODE_A or FREQMODE_B bits in conjunction with the POSTSCALE_A and POSTSCALE_B bits. Each PLL is also equipped with a pre-scale divider which offers frequency divide by one or two before the OSCCLK signal is input into the PLL. Please refer to Table 41 for details.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R3 PLLA 4 03h	0	PRESCALE_A	0	PLL Pre-scale Divider Select 0 = Divide by 1 (PLL input clock = oscillator clock) 1 = Divide by 2 (PLL input clock = oscillator clock ÷ 2) Note: PRESCALE_A must be set to the same value as PRESCALE_B in PLL S/PDIF receiver mode.
R7 PLLB 4 07h	0	PRESCALE_B	0	
R3 PLLA 4 03h	4:3	FREQMODE_A [1:0]	10	PLL Output Divider Select PLL S/PDIF Receiver Mode FREQMODE_A is automatically controlled. FREQMODE_B is not used. PLL User Mode Used in conjunction with the POSTSCALE_x bits. Refer to Table 42.
R7 PLLB 4 07h	4:3	FREQMODE_B [1:0]	10	
R3 PLLA 4 03h	1	POSTSCALE_A	0	PLL Post-scale Divider Select PLL S/PDIF Receiver Mode POSTSCALE_A is used to configure a 256fs or 128fs PLLACLK, POSTSCALE_B is not used. Refer to Table 43. PLL User Mode Used in conjunction with the FREQMODE_x bits. Refer to Table 42.
R7 PLLB 4 07h	1	POSTSCALE_B	0	

Table 41 Pre and Post PLL Clock Divider Control

FREQMODE_x[1:0]	f_2 TO PLLxCLK DIVISION FACTOR	
	POSTSCALE_x	
	0	1
00	÷2	÷4
01	÷4	÷8
10	÷8	÷16
11	÷12	÷24

Table 42 PLL User Mode Clock Divider Configuration

POSTSCALE_A	PLLACLK FREQUENCY
0	256fs
1	128fs

Table 43 PLL S/PDIF Receiver Mode Clock Divider Configuration

PLL CONFIGURATION EXAMPLE

Consider the situation where the oscillator clock (OSCCLK) input frequency is fixed at 12MHz and the required PLLBCLK frequency is 12.288MHz.

1. Calculate the f_2, FREQMODE_B and POSTSCALE_B Values

The PLL is designed to operate with best performance when the f_2 clock is between 90 and 100MHz. The necessary PLLBCLK frequency is 12.288MHz. Choose POSTSCALE_B and FREQMODE_B values to set the f_2 frequency in the range of 90 to 100MHz. In this case, the default values (POSTSCALE_B = 0 and FREQMODE_B[1:0] = 10) will configure the f_2 to PLLBCLK divider as 8 and hence will set the f_2 frequency at 98.304MHz; this value is within the 90 to 100MHz range and is hence acceptable.

- POSTSCALE_B = 0
- FREQMODE_B [1:0] = 10b
- f_2 = 98.304MHz

2. Calculate R Value

Using the relationship: R = ($f_2 \div f_1$), the value of R can be calculated.

- R = ($f_2 \div f_1$)
- R = (98.304 ÷ 12)
- R = 8.192

3. Calculate PLLB_N Value

The value of PLLB_N is the integer (whole number) value of R, ignoring all digits to the right of the decimal point. In this case, R is 8.192, hence PLLB_N is 8.

4. Calculate PLL_K Value

The PLLB_K value is simply the integer value of (2^{22} (R-PLLB_N)).

- PLLB_K = integer part of (2^{22} x (8.192 – 8))
- PLLB_K = integer part of 805306.368
- PLLB_K = 805306 (decimal) / C49BA (hex)

A number of example configurations are shown in Table 44. Many other configurations are possible; Table 44 shows only a small number of valid possibilities. As both PLLs are identical, the same configuration procedure applies for both.

OSC CLK (MHz)	PRE-SCALE _x	F_1 (MHz)	F_2 (MHz)	R	PLLx_N (Hex)	PLLx_K (Hex)	FREQ MODE_x [1:0]	POST-SCALE_x	PLLxCLK (MHz)
12	0	12	98.304	8.192	8	C49BA	00	1	24.576
12	0	12	98.304	8.192	8	C49BA	01	0	24.576
12	0	12	98.304	8.192	8	C49BA	01	1	12.288
12	0	12	98.304	8.192	8	C49BA	10	0	12.288
12	0	12	98.304	8.192	8	C49BA	10	1	6.144
12	0	12	98.304	8.192	8	C49BA	11	0	8.192
12	0	12	98.304	8.192	8	C49BA	11	1	4.096
24	1	12	90.3168	7.5264	7	21B089	00	1	22.5792
24	1	12	90.3168	7.5264	7	21B089	01	0	22.5792
24	1	12	90.3168	7.5264	7	21B089	01	1	11.2896
24	1	12	90.3168	7.5264	7	21B089	10	0	11.2896
24	1	12	90.3168	7.5264	7	21B089	10	1	5.6448
24	1	12	90.3168	7.5264	7	21B089	11	0	7.5264
24	1	12	90.3168	7.5264	7	21B089	11	1	3.7632
27	1	13.5	98.304	7.2818	7	1208A5	00	1	24.576
27	1	13.5	98.304	7.2818	7	1208A5	01	1	12.288
27	1	13.5	90.3168	6.6901	6	2C2B24	00	1	22.5792
27	1	13.5	90.3168	6.6901	6	2C2B24	01	1	11.2896

Table 44 User Mode PLL Configuration Examples

When considering settings not shown in this table, the key configuration parameters which must be selected for optimum operation are:

- 90MHz f_2 100MHz
- 5 PLLx_N 13
- OSCCLOCK = 10 to 14.4MHz or 16.28 to 27MHz

CLOCK OUTPUT (CLKOUT) AND MCLK OUTPUT (MCLK)

The clock output (CLKOUT) pin can be used as a clock output. This pin is intended to be used as a clock source pin for providing the central clock reference for an audio system.

The CLKOUT clock source can be selected from OSCCLK, PLLACLK or PLLBCLK. The control bits for the CLKOUT signal are shown in Table 45.

The MCLK pin can be configured as an input or output – the WM8581 should be powered down when switching MCLK between an input and an output. As an output, MCLK can be sourced from OSCCLK, PLLACLK or PLLBCLK.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R7 PLLB 4 07h	6:5	MCLKOUTSRC	00	MCLK pin output source 00 = Input – Source MCLK pin 01 = Output – Source PLLACLK 10 = Output – Source PLLBCLK 11 = Output – Source OSCCLK
	8:7	CLKOUTSRC	11	CLKOUT pin source 00 = No Output (tristate) 01 = Output – Source PLLACLK 10 = Output – Source PLLBCLK 11 = Output – Source OSCCLK

Table 45 MCLK and CLKOUT Control

S/PDIF RECEIVE MODE CLOCKING

In S/PDIF receive mode, the PLLA_N and PLLA_K values are automatically controlled by the S/PDIF receiver to allow the receiver to use PLLA to lock on to and track the incoming S/PDIF data stream. PLLB must be configured to produce a specific reference clock frequency for the S/PDIF receiver.

The S/PDIF receiver has four clocking modes based on the incoming S/PDIF stream sample rate. The modes are:

- Mode 1: Incoming S/PDIF Sample Rate = 192kHz +/- 1%
- Mode 2: Incoming S/PDIF Sample Rate = 88.2kHz -1% to 96kHz +1%
- Mode 3: Incoming S/PDIF Sample Rate = 44.1kHz -1% to 48kHz +1%
- Mode 4: Incoming S/PDIF Sample Rate = 32kHz +/- 1%

Before the S/PDIF receiver is enabled, it is important that the PLLB_N and PLLB_K register values (and the PRESCALE_x values as appropriate) are manually configured in a specific default state. The PLLB_N and PLLB_K register values (and the PRESCALE_x values as appropriate) must also be manually re-configured when a change of the clocking mode is detected and the change is to mode 1 or from mode 1. Note that the PRESCALE_A value must always be set to the same value as PRESCALE_B.

The specified PLLB f_2 frequencies that must be configured using the PLLB_N and PLLB_K register values (and the PRESCALE_x values as appropriate) for reception of specific S/PDIF sample rates are as follows:

- Mode 1 (192kHz Sample Rate): PLLB f_2 = **98.304MHz**
- Modes 2/3/4 (32/44.1/48/88.2/96kHz Sample Rates): PLLB f_2 = **94.3104MHz**

The FREQMODE_B[1:0] bits and POSTSCALE_B bit are not used in PLL S/PDIF recever mode.

The PLL register settings are configured by default to allow 32/44.1/48/88.2/96kHz (modes 2/3/4) sample rate S/PDIF receiver operation using a 12MHz crystal clock. The appropriate PLLB register values must be updated if:

- Any crystal clock frequency other than 12MHz is used.

  OR

- A S/PDIF stream with 192kHz sample rate (mode 1) is detected.

In either case, reprogramming of the PLLB_N and PLLB_K values (and the PRESCALE_x values as appropriate) is necessary.

Refer to Table 46 for details of a number of recommended PLLB configurations. Many other configurations are possible; please refer to PLL Configuration section for details regarding how to calculate alternative settings.

OSC CLK (MHz)	**PRE-SCALE_X**	**S/PDIF RECEIVER SAMPLE RATE(S) (kHz)**	**F1** (MHz)	**F2** (MHz)	**R**	**PLLB_N** (Hex)	**PLLB_K** (Hex)	**COMMENT**
11.2896	0	32 / 44.1 / 48 / 88.2 / 96	11.2896	94.3104	8.3537	8	16A3B3	Set N, K
11.2896	0	192	11.2896	98.304	8.7075	8	2D4766	Set N, K
12	0	32 / 44.1 / 48 / 88.2 / 96	12	94.3104	7.8592	7	36FD21	Default Setting
12	0	192	12	98.304	8.192	8	C49BA	Set N, K
12.288	0	32 / 44.1 / 48 / 88.2 / 96	12.288	94.3104	7.675	7	2B3333	Set K
12.288	0	192	12.288	98.304	8	8	0	Set N, K
19.2	1	32 / 44.1 / 48 / 88.2 / 96	9.6	94.3104	9.824	9	346C6A	Set Prescales, N, K
19.2	1	192	9.6	98.304	10.24	A	F5C28	Set Prescales, N, K
24	1	32 / 44.1 / 48 / 88.2 / 96	12	94.3104	7.8592	7	36FD21	Set Prescales
24	1	192	12	98.304	8.192	8	C49BA	Set Prescales, N, K
27	1	32 / 44.1 / 48 / 88.2 / 96	13.5	94.3104	6.986	6	3F19E5	Set Prescales, N, K
27	1	192	13.5	98.304	7.2818	7	1208A5	Set Prescales, K

Table 46 S/PDIF Receive Mode PLLB Initial Configuration Examples

The recommended configuration sequences are as follows:

TO INITIALLY CONFIGURE THE SYSTEM FOR S/PDIF RECEIVER STARTUP:

1. Write appropriate calculated values (relative to oscillator frequency) to PRESCALE_A, PRESCALE_B, PLLB_N and PLLB_K for 32/44.1/48/88.2/96kHz (modes 2/3/4) S/PDIF receiver sample rate operation.
2. Enable PLLA and PLLB by clearing the PLLAPD and PLLBPD bits.
3. Enable S/PDIF receiver by clearing the SPDIFRXPD and SPDIFPD bits.
4. Read S/PDIF Status Register REC_FREQ[1:0] bits to identify recovered S/PDIF sample frequency and clocking mode.
5. If indicated sample rate is 192kHz, write appropriate calculated values (relative to oscillator frequency) to PRESCALE_A, PRESCALE_B, PLLB_N and PLLB_K (as appropriate) for 192kHz (mode 1) S/PDIF receiver sample rate operation.

TO CONFIGURE THE SYSTEM WHEN CLOCKING MODE (SAMPLE RATE) CHANGES TO OR FROM MODE 1 (192KHZ):

Any sample rate change between clocking modes (for example, from 44.1kHz (mode 3) to 192kHz (mode 1)) will be flagged to the application processor via the INT interrupt flag. The application processor must then read the Interrupt Status Register. If the UPD_REC_FREQ flag is set, indicating that the clocking mode has changed, proceed as follows:

1. Read S/PDIF Status Register REC_FREQ[1:0] bits to identify recovered S/PDIF sample rate frequency and clocking mode.
2. Write appropriate calculated values (relative to oscillator frequency) to PRESCALE_A, PRESCALE_B, PLLB_N and PLLB_K based on indicated recovered S/PDIF sample frequency and clocking mode.

This procedure is only strictly necessary when switching to or from 192kHz (mode 1) because the PRESCALE_A, PRESCALE_B, PLLB_N and PLLB_K values are the same for 32/44.1/48/88.2/96kHz (modes 2/3/4) sample rate operation. It is, however, good interrupt service routine practice to write the appropriate PRESCALE_A, PRESCALE_B, PLLB_N and PLLB_K values when every clocking mode change is detected.

PHASE-LOCKED LOOPS AND S/PDIF CLOCKING (HARDWARE MODE)

In hardware mode, the user has no access to the internal clocking control registers and hence a default configuration is loaded at reset to provide maximum functionality.

The S/PDIF receiver is enabled and hence the PLLs operate in S/PDIF receiver mode and all PLL and S/PDIF receiver control is fully automatic. All supported S/PDIF receiver sample rates can be used.

FREQMODE_x and POSTSCALE_x control is fully automatic to ensure that the MCLK output is maintained at 256fs relative to the S/PDIF received sample rate.

In hardware mode, the OSCCLK **must** be 12MHz and hence the external crystal (or applied XIN clock) must be 12MHz. No other OSCCLK frequencies are supported in hardware mode.

S/PDIF TRANSCEIVER

FEATURES

- IEC-60958-3 compatible with 32k frames/s to 192k frames/s support
- Support for Reception and Transmission of S/PDIF data
- Clock synthesis PLL with reference clock input and ultra-low jitter output
- Input mux with support for up to four S/PDIF inputs
- Register controlled Channel Status recovery and transmission
- Register read-back of recovered Channel Status bits and error flags
- Detection of non-audio data, sample rate, and pre-emphasised data
- Programmable GPO for error flags, frame status flags and clocks

An IEC-60958-3 compatible S/PDIF transceiver is integrated into the WM8581. Operation of the S/PDIF function may be synchronous or asynchronous to the rest of the digital audio circuits.

The receiver performs data and clock recovery, and sends recovered data either to an external device such as a DSP (via the Digital Audio Interfaces), or if the data is audio PCM, it can route the stereo recovered data to DAC1. The recovered clock may be routed out of the WM8581 onto a pin for external use, and may be used to clock the internal DAC as required.

The transmitter generates S/PDIF frames where audio data may be sourced from the ADC, S/PDIF Receiver, or the Digital Audio Interfaces.

S/PDIF FORMAT

S/PDIF is a serial, bi-phase-mark encoded data stream. An S/PDIF frame consists of two sub-frames. Each sub-frame is made up of:

- Preamble – a synchronization pattern used to identify the start of a 192-frame block or sub-frame
- 4-bit Auxiliary Data (AUX) – ordered LSB to MSB
- 20-bit Audio Data (24-bit when combined with AUX) – ordered LSB to MSB
- Validity Bit – a 1 indicates invalid data in that sub-frame
- User Bit – over 192-frames, this forms a User Data Block,
- Channel Bit – over 192-frames, this forms a Channel Status Block
- Parity Bit – used to maintain even parity over the sub-frame (except the preamble)

An S/PDIF Block consists of 192 frames. Channel and User blocks are incorporated within the 192-frame S/PDIF Block. For Consumer mode only the first 40-frames are used to make up the Channel and User blocks. Figure 32 illustrates the S/PDIF format.

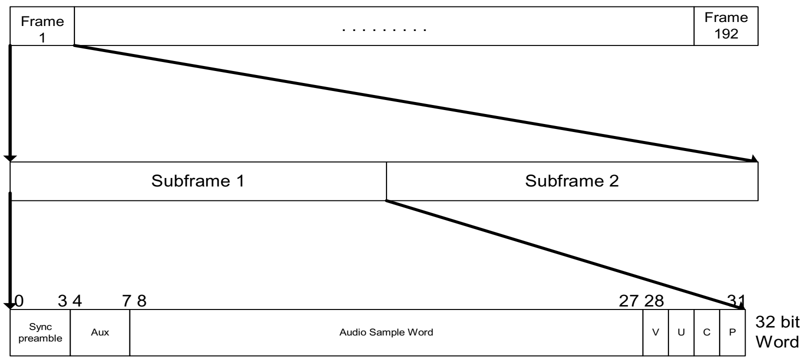


Figure 32 S/PDIF Format

S/PDIF TRANSMITTER

The S/PDIF transmitter generates the S/PDIF frames, and outputs on the SPDIFOP pin. The audio data for the frame can be taken from one of four sources, selectable using the TXSRC register. The transmitter can be powered down using the SPDIFTXD register bit. The S/PDIF Transmitter can be bypassed by setting the REAL_THROUGH register control bit. When set, the SPDIFOP pin sources the output of the S/PDIF input mux.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R30 SPDTXCHAN 0 1Eh	1:0	TXSRC[1:0]	00	S/PDIF Transmitter Data Source 00 = S/PDIF received data (see REAL_THROUGH) 01 = ADC digital output data. 10 = Secondary Audio Interface 11 = Audio Interface received data
	2	OVWCHAN	0	Overwrite Channel Status Only used if TXSRC=00. Overwrites the received channel status data using data read from S/PDIF transmitter channel status register 0 = Channel data equal to recovered channel data. 1 = Channel data taken from channel status registers.
	3	REAL_ THROUGH	0	S/PDIF Through Mode Control 0 = SPDIFOP pin sources output of S/PDIF Transmitter 1 = SPDIFOP pins sources output of S/PDIF IN Mux
R51 PWRDN 2 33h	4	SPDIFTXD	1	S/PDIF Transmitter powerdown 0 = S/PDIF Transmitter enabled 1 = S/PDIF Transmitter disabled

Table 47 S/PDIF Transmitter Control

The WM8581 also transmits the preamble and VUCP bits (Validity, User Data, Channel Status and Parity bits).

Validity Bit

Set to 0 (to indicate valid data) – unless TXSRC=00 (S/PDIF receiver), where Validity is the value recovered from the S/PDIF input stream by the S/PDIF receiver.

User Data

Set to 0 as User Data configuration is not supported in the WM8581 – if TXSRC=00 (S/PDIF receiver) User Data is the value recovered from the S/PDIF input stream by the S/PDIF receiver.

Channel Status

The Channel Status bits form a 192-frame block - transmitted at 1 bit per sub-frame. Each sub-frame forms its own 192-frame block. The WM8581 is a consumer mode device and only the first 40 bits of the block are used. All data transmitted from the WM8581 is stereo, so the channel status data is duplicated for both channels. The only exception to this is the channel number bits (23:20) which can be changed to indicate whether the channel is left or right in the stereo image. Bits within this block can be configured by setting the Channel Status Bit Control registers (see Table 48 to Table 52). If TXSRC=00 (S/PDIF receiver), the Channel Status bits are transmitted with the same values recovered by the receiver – unless OVWCHAN is set, in which case they are set by the S/PDIF transmitter channel status registers.

Parity Bit

This bit maintains even parity for data as a means of basic error detection. It is generated by the transmitter.

For further details of all channel status bits, refer to IEC-60958-3.

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R31 SPDTXCHAN 1 1Fh	0	CON/PRO	0	0	0 = Consumer Mode 1 = Professional Mode (not supported by WM8581)
	1	AUDIO_N	1	0	0 = S/PDIF transmitted data is audio PCM. 1 = S/PDIF transmitted data is not audio PCM.
	2	CPY_N	2	0	0 = Transmitted data has copyright asserted. 1 = Transmitted data has no copyright assertion.
	5:3	DEEMPH[2:0]	5:3	000	000 = Data from Audio interface has no pre-emphasis. 001 = Data from Audio interface has pre-emphasis. 010 = Reserved (Audio interface has pre-emphasis). 011 = Reserved (Audio interface has pre-emphasis). All other modes are reserved and should not be used.
	7:6	CHSTMODE [1:0]	7:6	00	00 = Only valid mode for consumer applications.

Table 48 S/PDIF Transmitter Channel Bit Control 1

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R32 SPDTXCHAN 2 20h	7:0	CATCODE [7:0]	15:8	00000000	Category Code. Refer to S/PDIF specification IEC60958-3 for details. 00h indicates “general” mode.

Table 49 S/PDIF Transmitter Channel Bit Control 2

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>CHANNEL STATUS BIT</th><th>DEFAULT</th><th colspan="2">DESCRIPTION</th></tr>
<tr><td rowspan="13">R33
SPDTXCHAN 3
21h</td><td>3:0</td><td>SRCNUM [3:0]</td><td>19:16</td><td>0000</td><td colspan="2">Source Number. No definitions are attached to data.</td></tr>
<tr><td rowspan="6">5:4</td><td rowspan="6">CHNUM1[1:0]</td><td rowspan="12">23:20</td><td rowspan="6">00</td><td colspan="2">Channel Number for Subframe 1</td></tr>
<tr><td>CHNUM1</td><td>Channel Status Bits[23:20]</td></tr>
<tr><td>00</td><td>0000 = Do not use channel number</td></tr>
<tr><td>01</td><td>0001 = Send to Left Channel</td></tr>
<tr><td>10</td><td>0010 = Send to Right Channel</td></tr>
<tr><td>11</td><td>0000 = Do not use channel number</td></tr>
<tr><td rowspan="6">7:6</td><td rowspan="6">CHNUM2[1:0]</td><td rowspan="6">00</td><td colspan="2">Channel Number for Subframe 2</td></tr>
<tr><td>CHNUM2</td><td>Channel Status Bits[23:20]</td></tr>
<tr><td>00</td><td>0000 = Do not use channel number</td></tr>
<tr><td>01</td><td>0001 = Send to Left Channel</td></tr>
<tr><td>10</td><td>0010 = Send to Right Channel</td></tr>
<tr><td>11</td><td>0000 = Do not use channel number</td></tr>
</table>

Table 50 S/PDIF Transmitter Channel Bit Control 3

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R34 SPDTXCHAN 4 22h	3:0	FREQ[3:0]	27:24	0001	Sampling Frequency. See S/PDIF specification IEC60958-3 for details. 0001 = Sampling Frequency not indicated.
	5:4	CLKACU[1:0]	29:28	11	Clock Accuracy of Generated clock. 00 = Level II 01 = Level I 10 = Level III 11 = Interface frame rate not matched to sampling frequency.

Table 51 S/PDIF Transmitter Channel Bit Control 4

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>CHANNEL STATUS BIT</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="3">R35
SPDTXCHAN 5
23h</td><td>0</td><td>MAXWL</td><td>32</td><td>1</td><td>Maximum Audio sample word length
0 = 20 bits
1 = 24 bits</td></tr>
<tr><td>3:1</td><td>TXWL[2:0]</td><td>35:33</td><td>101</td><td>Audio Sample Word Length.
000 = Word Length Not Indicated<table><tr><th>TXWL[2:0]</th><th>MAXWL==1</th><th>MAXWL==0</th></tr><tr><td>001</td><td>20 bits</td><td>16 bits</td></tr><tr><td>010</td><td>22 bits</td><td>18 bits</td></tr><tr><td>100</td><td>23 bits</td><td>19 bits</td></tr><tr><td>101</td><td>24 bits</td><td>20 bits</td></tr><tr><td>110</td><td>21 bits</td><td>17 bits</td></tr></table>All other combinations reserved</td></tr>
<tr><td>7:4</td><td>ORGSAMP [3:0]</td><td>39:36</td><td>0000</td><td>Original Sampling Frequency. See S/PDIF specification for details.
0000 = original sampling frequency not indicated</td></tr>
</table>

Table 52 S/PDIF Transmitter Channel Bit Control 5

S/PDIF RECEIVER

INPUT SELECTOR

The S/PDIF receiver has one dedicated input, SPDIFIN1. This pin is a IEC-60958-3-compatible comparator input by default or, if SPDIFIN1MODE is set, the pin will be a CMOS-compatible input. There are three other pins which can be configured as either S/PDIF inputs or general purpose outputs (GPOs). The four S/PDIF inputs are multiplexed to allow one input to go to the S/PDIF receiver for decoding. The S/PDIF receiver can be powered down using the SPDIFRXD register bit.

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="2">R36
SPDMODE
24h</td><td>0</td><td>SPDIFIN1MODE</td><td>1</td><td>Selects the input circuit type for the SPDIFIN1 input
0 = CMOS-compatible input
1 = Comparator input. Compatible with 500mVpp AC coupled consumer S/PDIF input signals as defined in IEC60958-3.</td></tr>
<tr><td>2:1</td><td>RXINSEL[1:0]</td><td>00</td><td>S/PDIF Receiver input mux select.
The general purpose inputs must be configured using GPOxOP to be either CMOS or comparator inputs if selected by RXINSEL.
00 = Select SPDIFIN1
01 = Select SPDIFIN2 (MFP3)
10 = Select SPDIFIN3 (MFP4)
11 = Select SPDIFIN4 (MFP5)</td></tr>
<tr><td rowspan="2">R39
GPO2
26h</td><td>3:0</td><td>GPO3OP[3:0]</td><td>0010</td><td rowspan="3">GPO pin Configuration Select.
1110 = Set GPO as S/PDIF input (CMOS-compatible input).
1111 = Set GPO as S/PDIF input (compatible with 500mVpp AC coupled consumer S/PDIF input signals as defined in IEC-60958-3).
For GPO defaults, see Table 65.</td></tr>
<tr><td>7:4</td><td>GPO4OP[3:0]</td><td>0011</td></tr>
<tr><td>R40
GPO3
27h</td><td>3:0</td><td>GPO5OP[3:0]</td><td>0100</td></tr>
<tr><td>R51
PWRDN 2
33h</td><td>5</td><td>SPDIFRXD</td><td>1</td><td>S/PDIF Receiver powerdown
0 = S/PDIF Receiver enabled
1 = S/PDIF Receiver disabled</td></tr>
</table>

Table 53 S/PDIF Receiver Input Selection Register

AUDIO DATA HANDLING

The S/PDIF receiver recovers the data and VUCP bits from each sub-frame. If the S/PDIF input data is in a non-compressed audio format the data can be internally routed to the stereo data input of DAC1. The WM8581 can detect when the data is in a non-compressed audio format and will automatically mute the DAC. See *Non-Audio Detection* for more detail.

The received data can also be output over the digital audio interfaces in any of the data formats supported. This can be performed while simultaneously using DAC1 for playback. The received data may also be re-transmitted via the S/PDIF transmitter.

USER DATA

The WM8581 can output recovered user data received using GPO pins. See Table 65 for General Purpose Pin control information.

CHANNEL STATUS DATA

The channel status bits are recovered from the incoming data stream and are used to control various functions of the device. The recovered MAXWL and RXWL bits are used to truncate the recovered 24-bit audio word to so that only the appropriate numbers of bits are used by the other interfaces (except the S/PDIF transmitter which always processes the full 24-bit recovered word).

Should the recovered DEEMPH channel status be set, and the S/PDIF receiver is routed to DAC1, the de-emphasis filter is activated for DAC1.

The S/PDIF receiver reads channel status data from channel 1 only. The channel status data is stored in five read-only registers which can be read via the serial interface (see *Serial Interface Readback*). When new channel status data has been recovered and stored in registers, the Channel Status Update (CSUD) bit is set to indicate that the status registers have updated and are ready for readback. After readback, CSUD will be cleared until the registers are next updated. The CSUD flag can be configured to be output on any of the GPO pins. The register descriptions for the channel status bits are given below.

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R44 SPDRXCHAN 1 2Ch (read-only)	0	CON/PRO	0	-	0 = Consumer Mode 1 = Professional Mode The WM8581 is a consumer mode device. Detection of professional mode may give erroneous behaviour.
	1	AUDIO_N	1	-	Recovered S/PDIF Channel status bit 1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.
	2	CPY_N	2	-	0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.
	3	DEEMPH	3	-	0 = Recovered S/PDIF data has no pre-emphasis. 1 = Recovered S/PDIF data has pre-emphasis.
	5:4	Reserved	5:4	-	Reserved for additional de-emphasis modes.
	7:6	CHSTMODE [1:0]	7:6	-	00 = Only valid mode for consumer applications.

Table 54 S/PDIF Receiver Channel Status Register 1

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R45 SPDRXCHAN 2 2Dh (read-only)	7:0	CATCODE [7:0]	15:8	-	Category Code. Refer to S/PDIF specification IEC60958-3 for details. 00h indicates “general” mode.

Table 55 S/PDIF Receiver Channel Status Register 2

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R46 SPDRXCHAN 3 2Eh (read-only)	3:0	SRCNUM [3:0]	19:16	-	Indicates number of S/PDIF source. Refer to S/PDIF specification IEC60958-3 for details.
	7:4	CHNUM1[3:0]	23:20	-	Channel number for channel 1. 0000 = Take no account of channel number (channel 1 defaults to left DAC) 0001 = channel 1 to left channel 0010 = channel 1 to right channel

Table 56 S/PDIF Receiver Channel Status Register 3

REGISTER ADDRESS	BIT	LABEL	CHANNEL STATUS BIT	DEFAULT	DESCRIPTION
R47 SPDRXCHAN 4 2Fh (read-only)	3:0	FREQ[3:0]	27:24	-	Sampling Frequency. Refer to S/PDIF specification IEC60958-3 for details. 0001 = Sampling Frequency not indicated.
	5:4	CLKACU[1:0]	29:28	-	Clock Accuracy of received clock. 00 = Level II 01 = Level I 10 = Level III 11 = Interface frame rate not matched to sampling frequency.

Table 57 S/PDIF Receiver Channel Status Register 4

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>CHANNEL STATUS BIT</th><th>DEFAULT</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td rowspan="10">R48
SPDRXCHAN 5
30h
(read-only)</td><td>0</td><td>MAXWL</td><td>32</td><td>-</td><td colspan="3">Maximum Audio sample word length
0 = 20 bits
1 = 24 bits</td></tr>
<tr><td rowspan="8">3:1</td><td rowspan="8">RXWL[2:0]</td><td rowspan="8">35:33</td><td rowspan="8">-</td><td colspan="3">Audio Sample Word Length.
000: Word Length Not Indicated</td></tr>
<tr><td>RXWL[2:0]</td><td>MAXWL==1</td><td>MAXWL==0</td></tr>
<tr><td>001</td><td>20 bits</td><td>16 bits</td></tr>
<tr><td>010</td><td>22 bits</td><td>18 bits</td></tr>
<tr><td>100</td><td>23 bits</td><td>19 bits</td></tr>
<tr><td>101</td><td>24 bits</td><td>20 bits</td></tr>
<tr><td>110</td><td>21 bits</td><td>17 bits</td></tr>
<tr><td colspan="3">All other combinations are reserved and may give erroneous operation. Data will be truncated internally when these bits are set.</td></tr>
<tr><td>7:4</td><td>ORGSAMP
[3:0]</td><td>39:36</td><td>-</td><td colspan="3">Original Sampling Frequency. Refer to S/PDIF specification IEC60958-3 for details.
0000 = original sampling frequency not indicated</td></tr>
</table>

Table 58 S/PDIF Receiver Channel Status Register 5

STATUS FLAGS

There are several status flags generated by the S/PDIF Receiver, described below.

FLAG	DESCRIPTION	VISIBILITY
UNLOCK	Indicates that the S/PDIF Clock Recovery circuit is unlocked, or the incoming S/PDIF signal is not present. 0 = Locked onto incoming S/PDIF stream. 1 = Not locked to the incoming S/PDIF stream, or incoming stream is not present.	S/PDIF Status Register, GPO pins, SWMODE pin (when in hardware mode)
INVALID	Indicates that recovered S/PDIF data is marked as invalid. 0 = Data marked as valid 1 = Data marked as invalid	Interrupt Status Register
TRANS_ERR	Indicates that recovered S/PDIF frame has parity errors or bi-phase encoding errors, or that sub-frames were recovered out of sequence 0 = No data errors or bi-phase encoding errors detected and sub-frame sequence correct 1 = Data errors or bi-phase encoding errors detected or subframe sequence incorrect (missing preamble)	Interrupt Status Register
AUDIO_N	Recovered Channel Status bit-1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.	Channel Status Register, S/PDIF Status Register
PCM_N	Indicates that non-audio code (defined in IEC-61937) has been detected. 0 = Sync code not detected. 1 = Sync code detected – received data is not audio PCM.	S/PDIF Status Register
CPY_N	Recovered Channel Status bit-2 (active low) 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.	Channel Status Register, S/PDIF Status Register, GPO pins
DEEMPH	Recovered Channel Status bit-3 0 = Recovered S/PDIF data has no pre-emphasis. 1 = Recovered S/PDIF data has pre-emphasis	Channel Status Register, S/PDIF Status Register, GPO pins
REC_FREQ[1:0]	Indicates recovered S/PDIF sample rate. 00 = 192kHz 01 = 96kHz / 88.2kHz 10 = 48kHz / 44.1kHz 11 = 32kHz	S/PDIF Status Register
INTB	Interrupt signal (see section Interrupt Generation)	GPO pins
V	Recovered validity-bit for current sub-frame	GPO pins
U	Recovered user-bit for current sub-frame	GPO pins
C	Recovered channel-bit for current sub-frame	GPO pins
P	Recovered parity-bit for current sub-frame	GPO pins
SFRM_CLK	Indicates current sub-frame: 1 = Sub-frame A 0 = Sub-frame B	GPO pins
192BLK	Indicates start of 192 frame-block. High for duration of frame-0.	GPO pins
CSUD	Indicates that the 192 frame-block of channel status data has updated.	GPO pins
REC_FREQ192	Indicates that the recovered S/PDIF clock frequency is 192kHz	GPO pins
ZFLAG	Indicates ‘zero-detection’ in DACs. See page 45 for more details	MUTE pin, GPO pins
NON_AUDIO	Logical OR of PCM_N and AUDIO_N	GPO pins, SDO pin (when in hardware mode)

Table 59 Status Flag Description

HARDWARE INTERRUPT GENERATION (INTB)

The hardware interrupt INTB flag (active low) indicates that an event has occurred on UNLOCK, INVALID, TRANS_ERR, NON_AUDIO, CPY_N, DEEMPH, CSUD or REC_FREQ. To determine which flag caused the interrupt, the Interrupt Status Register should be read when INTB is asserted. INVALID, TRANS_ERR and CSUD generate an interrupt when the flag transitions from low to high. UNLOCK, NON_AUDIO, CPY_N, DEEMPH and REC_FREQ will generate an interrupt on any change in status. INTB will remain asserted until it is cleared by reading the interrupt status register. If INVALID, TRANS_ERR or CSUD are still active when the interrupt status register is read, INTB remains asserted.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R43 INTSTAT 2Bh (read-only)	0	UPD_UNLOCK	-	UNLOCK flag update signal 0 = INTB not caused by update to UNLOCK flag 1 = INTB caused by update to UNLOCK flag
	1	INT_INVALID	-	INVALID flag interrupt signal 0 = INTB not caused by INVALID flag 1 = INTB caused by INVALID flag
	2	INT_CSUD	-	CSUD flag interrupt signal 0 = INTB not caused by CSUD flag 1 = INTB caused by CSUD flag
	3	INT_TRANS _ERR	-	TRANS_ERR flag interrupt signal 0 = INTB not caused by TRANS_ERR flag 1 = INTB caused by TRANS_ERR flag
	4	UPD_NON_AUDIO	-	NON_AUDIO update signal 0 = INTB not caused by update to NON_AUDIO flag 1 = INTB caused by update to NON_AUDIO flag
	5	UPD_CPY_N	-	CPY_N update signal 0 = INTB not caused by update to CPY_N flag 1 = INTB caused by update to CPY_N flag
	6	UPD_DEEMPH	-	DEEMPH update signal 0 = INTB not caused by update to DEEMPH flag 1 = INTB caused by update to DEEMPH flag
	7	UPD_REC_FREQ	-	REC_FREQ update signal 0 = INTB not caused by update to REC_FREQ flag 1 = INTB caused by update to REC_FREQ flag

Table 60 Interrupt Status Register

Where the INTB has been asserted by an update signal (UPD_UNLOCK, UPD_NON_AUDIO, UPD_CPY_N, UPD_DEEMPH, UPD_REC_FREQ) the S/PDIF Status Register can be read to reveal the status of the flag. See Table 61.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R49 SPDSTAT 31h (read-only)	0	AUDIO_N	-	Recovered Channel Status bit-1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.
	1	PCM_N	-	Indicates that non-audio code (defined in IEC-61937) has been detected. 0 = Sync code not detected. 1 = Sync code detected – received data is not audio PCM.
	2	CPY_N	-	Recovered Channel Status bit-2 (active low). 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data.
	3	DEEMPH	-	Recovered Channel Status bit-3 0 = Recovered S/PDIF data has no pre-emphasis. 1 = Recovered S/PDIF data has pre-emphasis
	5:4	REC_FREQ [1:0]	--	Indicates recovered S/PDIF clock frequency: 00 = 192kHz 01 = 96kHz / 88.2kHz 10 = 48kHz / 44.1kHz 11 = 32kHz
	6	UNLOCK	-	Indicates that the S/PDIF Clock Recovery circuit is unlocked or that the input S/PDIF signal is not present. 0 = Locked onto incoming S/PDIF stream. 1 = Not locked to the incoming S/PDIF stream or the incoming S/PDIF stream is not present.

Table 61 S/PDIF Status Register

The interrupt and update signals used to generate INTB can be masked as necessary. The MASK register bit prevents flags from asserting INTB and from updating the Interrupt Status Register (R43). Masked flags update the S/PDIF Status Register (R49).

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R37 INTMASK 25h	8:0	MASK[8:0]	000000000	When a flag is masked, it does not update the Interrupt Status Register or assert INTB. 0 = unmask, 1 = mask. MASK[0] = mask control for UPD_UNLOCK MASK[1] = mask control for INT_INVALID MASK[2] = mask control for INT_CSUD MASK[3] = mask control for INT_TRANS_ERR MASK[4] = mask control for UPD_AUDIO_N MASK[5] = mask control for UPD_PCM_N MASK[6] = mask control for UPD_CPY_N MASK[7] = mask control for UPD_DEEMPH MASK[8] = mask control for UPD_REC_FREQ

Table 62 Interrupt Mask Control Register

ERROR HANDLING

Should a TRANS_ERR or INVALID flag be asserted, it is assumed the recovered S/PDIF sub-frame is corrupted or invalid. If either flag is masked using the mask register, the WM8581 will overwrite the recovered frame (i.e. both sub-frames) with either all-zeros or the last valid data sample; depending on how FILLMODE has been set. If both flags are unmasked, data is not modified and the user must handle corrupted data appropriately.

ALWAYSVALID must be set to 0, else the INVALID flag will be ignored. For the S/PDIF Receiver to S/PDIF transmitter path, only masked INVALID flags will cause data to be overwritten – TRANS_ERR flags have no effect.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 GPO1 26h	8	FILLMODE	0	Determines what S/PDIF Receiver should do with corrupted or invalid data: 0 = Data from S/PDIF Receiver remains static at last valid sample. 1 = Data from S/PDIF Receiver is output as all zeros.
R39 GPO2 27h	8	ALWAYSVALID	0	Used to ignore the INVALID flag. See Table 64. 0 = Use INVALID flag. 1 = Ignore INVALID flag.

Table 63 S/PDIF Receiver Error Handling Registers

MASK	ALWAYSVALID	DATA OVERWRITE	INTB ASSERT
0	0	No	Yes
0	1	No	No
1	0	Yes	No
1	1	No	No

Table 64 Data Overwrite / INTB Assert Criteria

NON-AUDIO DETECTION

Non-Audio data is indicated by the AUDIO_N and PCM_N flags. AUDIO_N is recovered from the Channel Status block. PCM_N is set on detection of the 96-bit IEC-61937 non-audio data sync code, embedded in the data section of the S/PDIF frame. If DAC1 is sourcing the S/PDIF Receiver and either the AUDIO_N or PCM_N flags are asserted, DAC1 is automatically muted using the softmute feature. As described above, any change of AUDIO_N or PCM_N status will cause an INTB interrupt (UPD_NON_AUDIO) to be generated. If the MASK register bit for AUDIO_N or PCM_N is set, then the associated signal will not generate an interrupt (UPD_NON_AUDIO) but the DAC will be muted.

S/PDIF INPUT/ GPO PIN CONFIGURATION

The WM8581 has seven pins which can be configured as GPOs using the registers shown in Table 65. The GPO pins can be used to output status data decoded by the S/PDIF receiver. These same pins may be used as S/PDIF inputs as described in Table 53.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R38 GPO1 26h	3:0	GPO1OP[3:0]	0000	0000 = INTB 0001 = V 0010 = U 0011 = C 0100 = P 0101 = SFRM_CLK 0110 = 192BLK 0111 = UNLOCK 1000 = CSUD
	7:4	GPO2OP[3:0]	0001	
R39 GPO2 27h	3:0	GPO3OP[3:0]	0010	
	7:4	GPO4OP[3:0]	0011	
R40 GPO3 28h	3:0	GPO5OP[3:0]	0100	
	7:4	GPO6OP[3:0]	0101	

R41 GPO4 29h	3:0	GPO7OP[3:0]	0110	1001 = REC_FREQ192 1010 = ZFLAG 1011 = NON_AUDIO 1100 = CPY_N 1101 = DEEMP 1110 = Set GPO as S/PDIF input (CMOS-compatible input). Only applicable for GPO3/4/5. 1111 = Set GPO as S/PDIF input (‘comparator’ input for AC coupled consumer S/PDIF signals). Only applicable for GPO3/4/5

Table 65 GPO Control Registers

POWERDOWN MODES

The WM8581 has powerdown control bits allowing specific parts of the chip to be turned off when not in use.

The ADC is powered down by setting the ADCPD register bit. The three stereo DACs each have a separate powerdown control bit, DACPD[2:0], allowing individual stereo DACs to be powered down when not in use. DACPD can be overwritten by setting ALLDACPD to powerdown all DACs

The S/PDIF transmitter is powered down by setting SPDIFTXD. Setting SPDIFRXD powers down the S/PDIF receiver.

The PLL, Oscillator and S/PDIF clock recovery circuits are powered down by setting PLLPD, OSCPD and SPDIFPD respectively.

Setting all of ADCPD, DACPD[2:0], SPDIFTXD, SPDIFRXD and OUTPD[3:0] will powerdown everything except the references VMIDADC, ADCREF and VMIDDAC. These may be powered down by setting PWDN. Setting PWDN will override all other powerdown control bits. It is recommended that the ADC and DAC are powered down before setting PWDN. The default is for all powerdown bits to be set except OSCPD and PWDN.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R50 PWRDN 1 32h	0	PWDN	0	Master powerdown (overrides all powerdown registers) 0 = All digital circuits running, outputs are active 1 = All digital circuits in power down mode, outputs muted
	1	ADCPD	1	ADC powerdown 0 = ADC enabled 1 = ADC disabled
	4:2	DACPD[2:0]	111	DAC powerdowns 0 = DAC enabled 1 = DAC disabled DACPD[0] = DAC1 DACPD[1] = DAC2 DACPD[2] = DAC3
	6	ALLDACPD	1	Overrides DACPD[3:0] 0 = DACs under control of DACPD[3:0] 1= All DACs are disabled.
R51 PWRDN 2 33h	0	OSCPD	0	OSC output powerdown 0 = OSC output enabled 1 = OSC output disabled A CMOS input can be applied to the OSC input when powered down.
	1	PLLAPD	1	0 = PLLA enabled 1 = PLLA disabled

	2	PLLBPD	1	0 = PLLB enabled 1 = PLLB disabled
	3	SPDIFPD	1	S/PDIF Clock Recovery PowerDown 0 = S/PDIF enabled 1 = S/PDIF disabled
	4	SPDIFTXD	1	S/PDIF Transmitter powerdown 0 = S/PDIF Transmitter enabled 1 = S/PDIF Transmitter disabled
	5	SPDIFRXD	1	S/PDIF Receiver powerdown 0 = S/PDIF Receiver enabled 1 = S/PDIF Receiver disabled

Table 66 Powerdown Registers

INTERNAL POWER ON RESET CIRCUIT

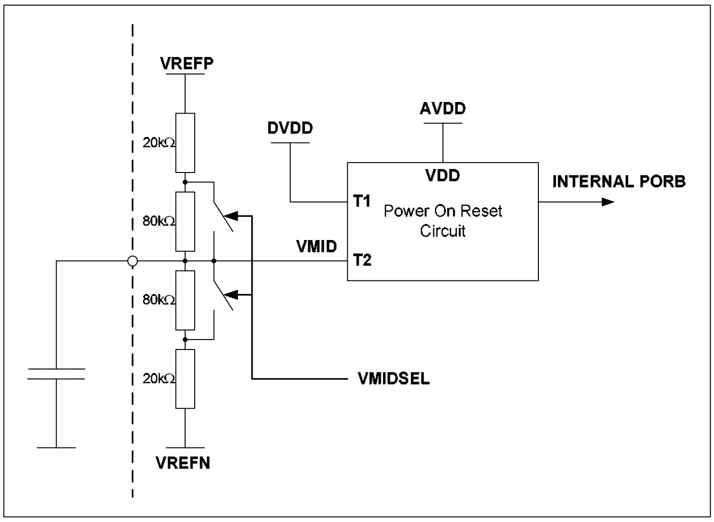


Figure 33 Internal Power On Reset Circuit Schematic

The WM8581 includes an internal Power-On Reset Circuit, which is used to reset the digital logic into a default state after power up.

Figure 33 shows a schematic of the internal POR circuit. The POR circuit is powered from AVDD. The circuit monitors DVDD and VMID and asserts PORB low if DVDD or VMID are below the minimum threshold Vpor_off.

On power up, the POR circuit requires AVDD to be present to operate. PORB is asserted low until AVDD, DVDD and VMID voltages have risen above their reset thresholds. When these three conditions have been met, PORB is released high. When PORB is released high, all registers are in their default state and writes to the digital interface may take place.

On power down, PORB is asserted low whenever DVDD or VMID drop below the minimum threshold Vpor_off.

If AVDD is removed at any time, the internal Power On Reset circuit is powered down and the PORB output will follow the AVDD voltage.

In most applications, the time required for the device to release PORB high will be determined by the charge time of the VMID node.

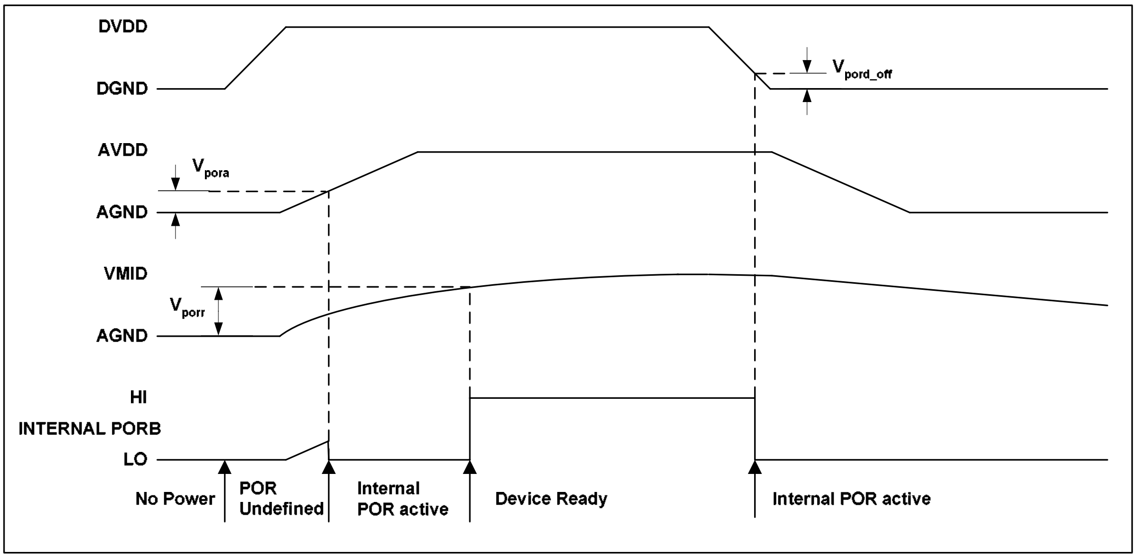


Figure 34 Typical Power up sequence where DVDD is powered before AVDD

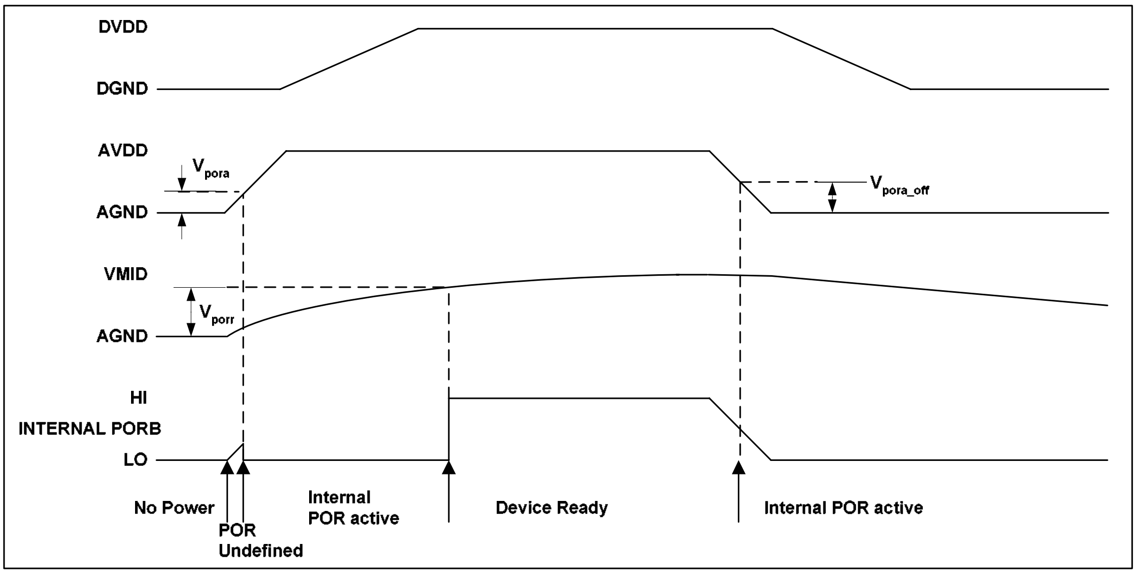


Figure 35 Typical Power up sequence where AVDD is powered before DVDD

SYMBOL	MIN	TYP	MAX	UNIT
V_{pora}	0.5	0.7	1.0	V
V_{porr}	0.5	0.7	1.1	V
V_{pora_off}	1.0	1.4	2.0	V
V_{pord_off}	0.6	0.8	1.0	V

Table 67 Typical POR Operation

In a real application, the designer is unlikely to have control of the relative power up sequence of AVDD and DVDD. Using the POR circuit to monitor VMID ensures a reasonable delay between applying power to the device and Device Ready.

Figure 34 and Figure 35 show typical power up scenarios in a real system. Both AVDD and DVDD must be established, and VMID must have reached the threshold Vporr before the device is ready and can be written to. Any writes to the device before Device Ready will be ignored.

Figure 34 shows DVDD powering up before AVDD. Figure 35 shows AVDD powering up before DVDD. In both cases, the time from applying power to Device Ready is dominated by the charge time of VMID.

A 4.7µF capacitor (minimum) is recommended for decoupling on VMID. The charge time for VMID will dominate the time required for the device to become ready after power is applied. The time required for VMID to reach the threshold is a function of the VMID resistor string and the decoupling capacitor. To reduce transient audio effects during power on, the stereo DACs on the WM8581 have their outputs clamped to VMID at power-on. This increases the capacitive loading of the VMID resistor string, as the DAC output AC coupling capacitors must be charged to VMID, and hence the required charge time. To ensure minimum device startup time, the VMIDSEL bit is set by default, thus reducing the impedance of the resistor string. If required, the VMID string can be restored to a high impedance state to save power once the device is ready.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R29 ADC CONTROL 1 1Dh	8	VMIDSEL	1	VMID Impedance Selection 0 = High impedance, power saving 1 = Low impedance, fast power-on

DEVICE ID READBACK

Reading from registers R0, R1 and R2 returns the device ID and revision number. R0 returns 80h, R1 returns 85h, R2 returns the device revision number. Device ID readback is not possible in continuous readback mode (CONTREAD=1).

HARDWARE CONTROL MODE

The WM8581 can be controlled in Hardware Control Mode or Software Control Mode. The method of control is determined by the state of the HWMODE pin. If the HWMODE pin is low, Software Control Mode is selected. If the HWMODE pin is high, Hardware Control Mode is selected.

In Hardware Control Mode the user has limited control over the features of the WM8581. Most of the features will assume their default settings but some can be modified using external pins.

HWMODE		SWMODE	
0	1	0	1
Software Control	Hardware Control	2-wire control	3-wire control

Table 68 Hardware/Software Mode Setup

DIGITAL ROUTING CONTROL

See page 22 for a more detailed explanation of the Digital Routing Options within the WM8581. In Software Control Mode, the values of register bits DAC_SRC, PAIFTX_SRC and TXSRC configure the signal path routing between interfaces. In hardware mode, similar control can be achieved via pins DR1, DR2, DR3 and DR4 as detailed in Table 69 and Table 70.

PIN	0	1
DR1	DAC_SRC=S/PDIF receiver	DAC_SRC=PAIF receiver
DR2	PAIFTX_SRC=S/PDIF receiver	PAIFTX_SRC=ADC output

Table 69 DR1 / DR2 Operation

DR4	DR3	S/PDIF TRANSMITTER DATA SOURCE
0	0	S/PDIF received data
0	1	ADC digital output data
1	0	SAIF receiver data
1	1	PAIF receiver data

Table 70 DR3 / DR4 Operation

The Secondary Audio Interface (SAIF) is not operational in Hardware Mode.

STATUS PINS

In Hardware control mode, SDO, SWMODE and MFP8/9/10 pins provide S/PDIF status flag information.

PIN	FLAG	DESCRIPTION
SWMODE	UNLOCK	Indicates that the S/PDIF Clock Recovery circuit is unlocked or that the input S/PDIF signal is not present. 0 = Locked to incoming S/PDIF stream. 1 = Not locked to the incoming S/PDIF stream, or incoming stream not present.
SDO	NON_AUDIO	Logical OR of PCM_N and AUDIO_N: PCM_N indicates that non-audio code (defined in IEC-61937) has been detected. AUDIO_N is the recovered Channel Status bit-1.
MFP8	C	Recovered channel-bit for current sub-frame
MFP9	SFRM_CLK	Indicates current sub-frame: 1 = Sub-frame A 0 = Sub-frame B
MFP10	192BLK	Indicates start of 192-frame block. High for duration of frame 0, low after frame 0.

Table 71 Hardware Mode Status Pins

DIGITAL AUDIO INTERFACE CONTROL

In Hardware Control Mode, CSB and SCLK become controls to configure the Primary Audio Interface data format and word length. The configuration applies to both transmit and receive sides of the interface. Table 72 below shows the options available.

CSB	SCLK	FORMAT & WORD LENGTH
0	0	24-bit right justified
0	1	20-bit right justified
1	0	24-bit left justified
1	1	24-bit I^2S

Table 72 Audio Interface Hardware Mode Control

DAC MUTE CONTROL

In Hardware Control mode, the MUTE pin activates the softmute function on all the DACs. In Software Control mode, MUTE activates softmute on the DAC selected by the DZFM register (when the MPDENB bit is low). See page 34 for a detailed description of the softmute function and the other methods of activating softmute.

When floating, the MUTE pin becomes an output for the ZFLAG flag.

MUTE	DESCRIPTION
0	Normal Operation
1	Mute DAC channels
Floating	MUTE is an output to indicate when Zero Detection occurs on all DACs (ZFLAG). H = detected, L = not detected.

Table 73 MUTE Pin Control Options

PRIMARY AUDIO INTERFACE (TX) MASTER MODE CONTROL

In Hardware Control Mode, the SDIN pin is used to enable the master mode function on the Primary Audio Interface transmitter. This has the same operation as the PAIFTX_MS register bit. The PAIFTX_RATE default settings of 256fs, and 64 BCLKs/LRCLK for BCLKSEL, are used in Hardware Control Mode. See page **Error! Bookmark not defined.** for more information on master mode operation.

SDIN	AUDIO INTERFACE (TX)
0	Slave
1	Master

Table 74 Audio Interface (Transmitter) Master Mode Hardware Mode Control

S/PDIF ERROR HANDLING

Should the incoming S/PDIF sub-frame contain a parity error or a bi-phase encoding error, it is assumed the sub-frame has become corrupted. Similarly, if VALIDITY is detected as 1, it is assumed the data within the S/PDIF frame is invalid. Under these conditions, the S/PDIF Receiver repeats the last valid sample in place of the corrupted/invalid samples. (Note: For the S/PDIF receiver to S/PDIF transmitter path, only VALIDITY errors will cause data to be overwritten – parity and bi-phase errors have will not cause data to be overwritten).

POWERDOWN CONTROL

In Software Control Mode, the device is powered-down by default. In Hardware Control Mode, the chip is powered-up by default but can be powered up by setting the ALLPD(MFP7) input high. (Note that in Software Control Mode, this pin takes the function of SAIF_LRCLK or GPO7).

ALLPD (MFP7)	
0	1
Powerup	Powerdown

Table 75 Hardware Mode Powerdown Control

REGISTER MAP

The complete register map is shown below. The detailed description can be found in the relevant text of the device description. The WM8581 can be configured using the Control Interface. All unused bits should be set to ‘0’.

REGISTER	NAME	ADDRESS	B8	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
R0	PLLA 1/DEVID1	00	PLLA_K[8:0]									100100001
R1	PLLA 2/DEVID2	01	PLLA_K[17:9]									101111110
R2	PLLA 3/DEVREV	02	0	PLLA_N[3:0]				PLLA_K[21:18]				001111101
R3	PLLA 4	03	0	0	0	0	FREQMODE_A[1:0]		FRACEN_A	POSTSCALE_A	PRESCALE_A	000010100
R4	PLLB 1	04	PLLB_K[8:0]									100100001
R5	PLLB 2	05	PLLB_K[17:9]									101111110
R6	PLLB 3	06	0	PLLB_N[3:0]				PLLB_K[21:18]				001111101
R7	PLLB 4	07	CLKOUTSRC[1:0]		MCLKOUTSRC[1:0]		FREQMODE_B[1:0]		FRACEN_B	POSTSCALE_B	PRESCALE_B	110010100
R8	CLKSEL	08	0	0	0	TX_CLKSEL[1:0]		ADC_CLKSEL[1:0]		DAC_CLKSEL[1:0]		000010000
R9	PAIF 1	09	0	PAIFRXMS_CLKSEL[1:0]		PAIFRXMS	PAIFRX_BCLKSEL[1:0]		PAIFRX_RATE[2:0]			000000010
R10	PAIF 2	0A	0	0	0	PAIFTXMS	PAIFTX_BCLKSEL[1:0]		PAIFTX_RATE[2:0]			000000010
R11	SAIF 1	0B	0	SAIFMS_CLKSEL[1:0]		SAIFMS	SAIF_BCLKSEL[1:0]		SAIF_RATE[2:0]			011000010
R12	PAIF 3	0C	DAC_SRC[1:0]		DACOSR	PAIFRXBCP	PAIFRXLRP	PAIFRXWL[1:0]		PAIFRXFMT[1:0]		110001010
R13	PAIF 4	0D	PAIFTX_SRC[1:0]		0	PAIFTXBCP	PAIFTXLRP	PAIFTXWL[1:0]		PAIFTXFMT[1:0]		010001010
R14	SAIF 2	0E	SAIFTX_SRC[1:0]		SAIF_EN	SAIFBCP	SAIFLRP	SAIFWL[1:0]		SAIFFMT[1:0]		000001010
R15	DAC CONTROL 1	0F	RXDAC_MODE	DAC4SEL[1:0]		DAC3SEL[1:0]		DAC2SEL[1:0]		DAC1SEL[1:0]		011100100
R16	DAC CONTROL 2	10	0	IZD	DZFM[2:0]			PL[3:0]				000001001
R17	DAC CONTROL 3	11	0	0	0	0	DEEMPALL	DEEMP[3:0]				000000000
R18	DAC CONTROL 4	12	0	PHASE[7:0]								011111111
R19	DAC CONTROL 5	13	0	MPDENB	DACATC	DZCEN	MUTEALL	DMUTE[3:0]				000000000
R20	DIGITAL ATTENUTATION DACL 1	14	UPDATE	LDA1[7:0]								011111111
R21	DIGITAL ATTENUTATION DACR 1	15	UPDATE	RDA1[7:0]								011111111
R22	DIGITAL ATTENUTATION DACL 2	16	UPDATE	LDA2[7:0]								011111111
R23	DIGITAL ATTENUTATION DACR 2	17	UPDATE	RDA2[7:0]								011111111
R24	DIGITAL ATTENUTATION DACL 3	18	UPDATE	LDA3[7:0]								011111111
R25	DIGITAL ATTENUTATION DACR 3	19	UPDATE	RDA3[7:0]								011111111
R26	DIGITAL ATTENUTATION DACR 4	1A	UPDATE	LDA4[7:0]								011111111
R27	DIGITAL ATTENUTATION DACR 4	1B	UPDATE	RDA4[7:0]								011111111
R28	MASTER DIGITAL ATTENUTATION	1C	UPDATE	MASTDA[7:0]								011111111
R29	ADC CONTROL 1	1D	VMIDSEL	ADCRATE[2:0]			ADCHPD	ADCOSR	AMUTEALL	AMUTER	AMUTEL	001000000
R30	SPDTXCHAN 0	1E	0	0	0	0	0	REAL_ THROUGH	OVWCHAN	TXSRC[1:0]		000000000
R31	SPDTXCHAN 1	1F	0	CHSTMODE[1:0]		DEEMPH[2:0]			CPY_N	AUDIO_N	CON/PRO	000000000
R32	SPDTXCHAN 2	20	0	CATCODE[7:0]								000000000
R33	SPDTXCHAN 3	21	0	CHNUM2[1:0]		CHNUM1[1:0]		SRCNUM[3:0]				000000000
R34	SPDTXCHAN 4	22	0	0	0	CLKACU[1:0]		FREQ[3:0]				000110001
R35	SPDTXCHAN 5	23	0	ORGSAMP[3:0]				TXWL[2:0]			MAXWL	000001011

R36	SPDMODE	24	0	0	0	1	1	1	RXINSEL[1:0]		SPDIFIN1MODE	000111001
R37	INTMASK	25	MASK[8:0]									000000000
R38	GPO1	26	FILLMODE	GPO2OP[3:0]				GPO1OP[3:0]				000010000
R39	GPO2	27	ALWAYSVALID	GPO4OP[3:0]				GPO30P[3:0]				000110010
R40	GPO3	28	0	GPO6OP[3:0]				GPO5OP[3:0]				001010100
R41	GPO4	29	0	0	1	1	1	GPO70P[3:0]				001110110
R42	Reserved	2A	0	1	0	0	1	1	0	0	0	010011000
R43	INTSTAT	2B	Error Flag Interupt Status Register									-
R44	SPDRXCHAN 1	2C	Channel Status Register 1									-
R45	SPDRXCHAN 2	2D	Channel Status Register 2									-
R46	SPDRXCHAN 3	2E	Channel Status Register 3									-
R47	SPDRXCHAN 4	2F	Channel Status Register 4									-
R48	SPDRXCHAN 5	30	Channel Status Register 5									-
R49	SPDSTAT	31	S/PDIF Status Register									-
R50	PWRDN 1	32	0	0	ALLDACPD	DACPD[3:0]				ADCPD	PWDN	001111110
R51	PWRDN 2	33	0	0	0	SPDIFRXD	SPDIFTXD	SPDIFPD	PLLBPD	PLLAPD	OSCPD	000111110
R52	READBACK	34	0	0	0	0	READEN	CONTREAD	READMUX[2:0]			000000000
R53	RESET	35	RESET									n/a

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R0 PLLA 1/ DEVID1 00h	8:0	PLLA_K[8:0]	100100001	Fractional (K) part of PLLA input/output frequency ratio (treat as one 22-digit binary number). Reading from these registers will return the device ID. R0 returns 10000101 = 81h R1 returns 10000000 = 85h Device ID readback is not possible in continuous readback mode (CONTREAD=1).
R1 PLLA 2/ DEVID2 01h	8:0	PLLA_K[17:9]	101111110	
R2 PLLA 3/ DEVREV 02h	3:0	PLLA_K[21:18]	1101	
	7:4	PLLA_N[3:0]	0111	Integer (N) divisor part of PLLA input/output frequency ratio. Use values greater than 5, less than 13. Reading from this register will return the device revision number.
R3 PLLA 4 03h	0	PRESCALE_A	0	0 = no pre-scale 1 = divide MCLK by 2 prior to PLLA
	1	POSTSCALE_A	0	0 = no post scale 1= divide MCLK by 2 after PLLA
	2	FRACEN_A	1	0 = Integer N PLLA 1 = Fractional K PLLA
	4:3	FREQMODE_A[1:0]	10	Range Selector for PLLACLK (not valid when TXSRC=00) 00 = 192KHz 01 = 88.2KHz to 96KHz 10 = 44.1KHz to 48KHz 11 = 32KHz
R4 PLLB 1 04h	8:0	PLLB_K[8:0]	100100001	Fractional (K) part of PLLB input/output frequency ratio (treat as one 22-digit binary number).
R5 PLLB 2 05h	8:0	PLLB_K[17:9]	101111110	

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R6 PLLB 3 06h	3:0	PLLB_K[21:18]	1101	
	7:4	PLLB_N[3:0]	0111	Integer (N) divisor part of PLLB input/output frequency ratio. Use values greater than 5, less than 13.
R7 PLLB 4 07h	0	PRESCALE_B	0	0 = no pre-scale 1 = divide MCLK by 2 prior to PLLB
	1	POSTSCALE_B	0	0 = no post scale 1= divide MCLK by 2 after PLLB
	2	FRACEN_B	1	0 = Integer N PLLB 1 = Fractional K PLLB
	4:3	FREQMODE_B [1:0]	10	Range Selector for PLLBCLK (not valid when TXSRC=00) 00 = 192KHz 01 = 88.2KHz to 96KHz 10 = 44.1KHz to 48KHz 11 = 32KHz
	6:5	MCLKOUTSRC	00	MCLK pin output source 00 = MCLK pin configured as an input. The system should be powered down before changing from this register setting. 01 = PLLACLK 10 = PLLBCLK 11 = OSCCLK
	8:7	CLKOUTSRC	11	CLKOUT pin source 00 = no output (tristate) 01 = PLLACLK 10 = PLLBCLK 11 = OSCCLK
R8 CLKSEL 08h	1:0	DAC_CLKSEL	00	DAC clock source 00 = MCLK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin
	3:2	ADC_CLKSEL	00	ADC clock source 00 = ADCMLCK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin
	5:4	TX_CLKSEL	01	S/PDIF Transmitter clock source 00 = ADCMLCK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin
R9 PAIF 1 09h	2:0	PAIFRX_RATE [2:0]	010	Master Mode LRCLK Rate 000 = 128fs 001 = 192fs 010 = 256fs 011 = 384fs 100 = 512fs 101 = 768fs 110 = 1152fs

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4:3	PAIFRX_BCLKSEL [1:0]	00	Master Mode BCLK Rate 00 = 64 BCLKs/LRCLK 01 = 128 BCLKs/LRCLK 10 = 256 BCLKs/LRCLK 11 = BCLK = System Clock
	5	PAIFRXMS	0	PAIF Receiver Master/Slave Mode Select 0 = Slave Mode 1 = Master Mode
	7:6	PAIFRXMS_ CLKSEL	00	PAIF Receiver Master Mode clock source 00 = MCLK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin
R10 PAIF 2 0Ah	2:0	PAIFTX_RATE [2:0]	010	Master Mode LRCLK Rate 000 = 128fs 001 = 192fs 010 = 256fs 011 = 384fs 100 = 512fs 101 = 768fs 110 = 1152fs
	4:3	PAIFTX_BCLKSEL [1:0]	00	Master Mode BCLKRate 00 = 64 BCLKs/LRCLK 01 = 128 BCLKs/LRCLK 10 = 256 BCLKs/LRCLK 11 = BCLK = System Clock
	5	PAIFTXMS	0	PAIF Transmitter Master/Slave Mode Select: 0 = Slave Mode 1 = Master Mode
R11 SAIF1 0Bh	2:0	SAIF_RATE [2:0]	010	Master Mode LRCLK Rate 000 = 128fs 001 = 192fs 010 = 256fs 011 = 384fs 100 = 512fs 101 = 768fs 110 = 1152fs
	4:3	SAIF_BCLKSEL [1:0]	00	Master Mode BCLK Rate 00 = 64 BCLKs/LRCLK 01 = 128 BCLKs/LRCLK 10 = 256 BCLKs/LRCLK 11 = BCLK = System Clock
	5	SAIFMS	0	SAIF Master/Slave Mode Select 0 = Slave Mode 1 = Master Mode
	7:6	SAIFMS_ CLKSEL [1:0]	11	SAIF Master Mode clock source 00 = ADCMCLK pin 01 = PLLACLK 10 = PLLBCLK 11 = MCLK pin

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R12 PAIF 3 0Ch	1:0	PAIFRXFMT [1:0]	10	PAIF Receiver Audio Data Format Select 11: DSP Format 10: I^2S Format 01: Left justified 00: Right justified
	3:2	PAIFRXWL [1:0]	10	PAIF Receiver Audio Data Word Length 11: 32 bits (see Note) 10: 24 bits 01: 20 bits 00: 16 bits
	4	PAIFRXLRP	0	In LJ/RJ/I^2S modes 0 = LRCLK not inverted 1 = LRCLK inverted In DSP Format: 0 = DSP Mode A 1 = DSP Mode B
	5	PAIFRXBCP	0	PAIF Receiver BCLK polarity 0 = BCLK not inverted 1 = BCLK inverted
	6	DACOSR	0	DAC Oversampling Rate Control 0= 128x oversampling 1= 64x oversampling
	8:7	DAC_SRC [1:0]	11	DAC1 Source: 00 = S/PDIF received data. 10 = SAIF Receiver data 11 = PAIF Receiver data Note: When DAC_SRC = 00, DAC2/3/4 may be turned off, depending on RX2DAC_MODE
R13 PAIF 4 0Dh	1:0	PAIFTXFMT [1:0]	10	PAIF Transmitter Audio Data Format Select 11: DSP Format 10: I^2S Format 01: Left justified 00: Right justified
	3:2	PAIFTXWL [1:0]	10	PAIF Transmitter Audio Data Word Length 11: 32 bits (see Note) 10: 24 bits 01: 20 bits 00: 16 bits
	4	PAIFTXLRP	0	In LJ/RJ/I^2S modes 0 = LRCLK not inverted 1 = LRCLK inverted In DSP Format: 0 = DSP Mode A 1 = DSP Mode B
	5	PAIFTXBCP	0	PAIF Receiver BCLK polarity 0 = BCLK not inverted 1 = BCLK inverted
	8:7	PAIFTX_SRC [1:0]	01	Primary Audio Interface Transmitter Source 00 = S/PDIF received data. 01 = ADC digital output data. 10 = SAIF Receiver data

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R14 SAIF 2 0Eh	1:0	SAIFFMT [1:0]	10	SAIF Audio Data Format Select 11: DSP Format 10: I^2S Format 01: Left justified 00: Right justified
	3:2	SAIFWL [1:0]	10	SAIF Audio Data Word Length 11: 32 bits (see Note) 10: 24 bits 01: 20 bits 00: 16 bits
	4	SAIFLRP	0	In LJ/RJ/I^2S modes 0 = LRCLK not inverted 1 = LRCLK inverted In DSP Format: 0 = DSP Mode A 1 = DSP Mode B
	5	SAIFBCP	0	SAIF BCLK polarity 0 = BCLK not inverted 1 = BCLK inverted
	6	SAIF_EN	0	SAIF Enable 0 = SAIF disabled 1 = SAIF enabled
	8:7	SAIFTX_SRC [1:0]	00	Secondary Audio Interface Transmitter Source 00 = S/PDIF received data. 01 = ADC digital output data. 11 = PAIF Receiver data
R15 DAC CONTROL 1 0Fh	1:0	DAC1SEL [1:0]	00	DAC digital input select 00 = DAC takes data from DIN1 01 = DAC takes data from DIN2 10 = DAC takes data from DIN3 11 = DAC takes data from DIN4
	3:2	DAC2SEL [1:0]	01	
	5:4	DAC3SEL [1:0]	10	
	7:6	DAC4SEL [1:0]	11	
	8	RX2DAC_MODE	0	DAC oversampling rate and power down control (only valid when DAC_SRC = 00, S/PDIF receiver) 0 = SFRM_CLK determines oversampling rate, DACs 2/3 powered down 1 = PAIFRX_LRCLK determines oversampling rate, DACs 2/3 source PAIF Receiver

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
R16 DAC CONTROL 2 10h	3:0	PL[3:0]	1001	PL[3:0]	Left O/P	Right O/P
				0000	Mute	Mute
				0001	Left	Mute
				0010	Right	Mute
				0011	(L+R)/2	Mute
				0100	Mute	Left
				0101	Left	Left
				0110	Right	Left
				0111	(L+R)/2	Left
				1000	Mute	Right
				1001	Left	Right
				1010	Right	Right
				1011	(L+R)/2	Right
				1100	Mute	(L+R)/2
				1101	Left	(L+R)/2
				1110	Right	(L+R)/2
				1111	(L+R)/2	(L+R)/2
	6:4	DZFM[2:0]	000	Selects the source for ZFLAG 000 - All DACs Zero Flag 001 - DAC1 Zero Flag 010 - DAC2 Zero Flag 011 - DAC3 Zero Flag 100 - DAC4 Zero Flag 101 - ZFLAG = 0 110 - ZFLAG = 0 111 - ZFLAG = 0		
	7	IZD	0	Infinite zero detection circuit control and automute control 0 = Infinite zero detect automute disabled 1 = Infinite zero detect automute enabled		
R17 DAC CONTROL 3 11h	3:0	DEEMP[3:0]	0000	De-emphasis mode select DEEMP[0] = 1, enable De-emphasis on DAC1 DEEMP[1] = 1, enable De-emphasis on DAC2 DEEMP[2] = 1, enable De-emphasis on DAC3 DEEMP[3] = 1, enable De-emphasis on DAC 4		
	4	DEEMPALL	0	0 = De-emphasis controlled by DEEMP[3:0] 1 = De-emphasis enabled on all DACs		
R18 DAC CONTROL 4 12h	5:0	PHASE [7:0]	11111111	Controls phase of DAC outputs PHASE[0] = 1 inverts phase of DAC1L output PHASE[1] = 1 inverts phase of DAC1R output PHASE[2] = 1 inverts phase of DAC2L output PHASE[3] = 1 inverts phase of DAC2R output PHASE[4] = 1 inverts phase of DAC3L output PHASE[5] = 1 inverts phase of DAC3R output PHASE[6] = 1 inverts phase of DAC4L output PHASE[7] = 1 inverts phase of DAC4R output		
R19 DAC CONTROL 5 13h	2:0	DMUTE[3:0]	0000	DAC channel soft mute enables DMUTE[0] = 1, enable soft-mute on DAC1 DMUTE[1] = 1, enable soft-mute on DAC2 DMUTE[2] = 1, enable soft-mute on DAC3 DMUTE[3] = 1, enable soft-mute on DAC4		

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	4	MUTEALL	0	DAC channel master soft mute. Mutes all DAC channels 0 = disable soft-mute on all DACs 1 = enable soft-mute on all DACs
	5	DZCEN	0	DAC Digital Volume Zero Cross Enable 0 = Zero Cross detect disabled 1 = Zero Cross detect enabled
	6	DACATC	0	Attenuator Control 0 = All DACs use attenuations as programmed. 1 = Right channel DACs use corresponding left DAC attenuations
	7	MPDENB	0	MUTE pin decode enable 0 = MUTE activates soft-mute on DAC selected by DZFM 1 = MUTE activates softmute on all DACs
R20 DIGITAL ATTENUATION DACL 1 14h	7:0	LDA1[7:0]	11111111 (0dB)	Digital Attenuation control for DAC1 Left Channel (DACL1) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA1 in intermediate latch (no change to output) 1 = Apply LDA1 and update attenuation on all channels
R21 DIGITAL ATTENUATION DACR 1 15h	7:0	RDA1[6:0]	11111111 (0dB)	Digital Attenuation control for DAC1 Right Channel (DACR1) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA1 in intermediate latch (no change to output) 1 = Apply RDA1 and update attenuation on all channels
R22 DIGITAL ATTENUATION DACL 2 16h	7:0	LDA2[7:0]	11111111 (0dB)	Digital Attenuation control for DAC2 Left Channel (DACL2) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA2 in intermediate latch (no change to output) 1 = Apply LDA2 and update attenuation on all channels
R23 DIGITAL ATTENUATION DACR 2 17h	7:0	RDA2[7:0]	11111111 (0dB)	Digital Attenuation control for DAC2 Right Channel (DACR2) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA2 in intermediate latch (no change to output) 1 = Apply RDA2 and update attenuation on all channels
R24 DIGITAL ATTENUATION DACL 3 18h	7:0	LDA3[7:0]	11111111 (0dB)	Digital Attenuation control for DAC3 Left Channel (DACL3) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA3 in intermediate latch (no change to output) 1 = Apply LDA3 and update attenuation on all channels
R25 DIGITAL ATTENUATION DACR 3 19h	7:0	RDA3[7:0]	11111111 (0dB)	Digital Attenuation control for DAC3 Right Channel (DACR3) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA3 in intermediate latch (no change to output) 1 = Apply RDA3 and update attenuation on all channels
R26 DIGITAL ATTENUATION DACL 4 1Ah	7:0	LDA4[7:0]	11111111 (0dB)	Digital Attenuation control for DAC4 Left Channel (DACL4) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store LDA4 in intermediate latch (no change to output) 1 = Apply LDA4 and update attenuation on all channels
R27 DIGITAL ATTENUATION DACR 4 1Bh	7:0	RDA4[7:0]	11111111 (0dB)	Digital Attenuation control for DAC4 Right Channel (DACR4) in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store RDA4 in intermediate latch (no change to output) 1 = Apply RDA4 and update attenuation on all channels

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R28 MASTER DIGITAL ATTENUATION 1Ch	7:0	MASTDA[7:0]	11111111 (0dB)	Digital Attenuation control for all DAC channels in 0.5dB steps. See Table 22
	8	UPDATE	Not latched	Controls simultaneous update of all Attenuation Latches 0 = Store gain in intermediate latch (no change to output) 1 = Apply gain and update attenuation on all channels
R29 ADC CONTROL 1 1Dh	0	AMUTEL	0	ADC Mute select 0 : Normal Operation 1: mute ADC left
	1	AMUTER	0	ADC Mute select 0 : Normal Operation 1: mute ADC right
	2	AMUTEALL	0	ADC Mute select 0 : Normal Operation 1: mute both ADC channels
	3	ADCOSR	0	ADC oversample rate select 0 = 128/64 x oversampling 1 = 64/32 x oversampling
	4	ADCHPD	0	ADC high-pass filter disable: 0 = high-pass filter enabled 1 = high-pass filter disabled
	7:5	ADCRATE[2:0]	010	ADC Rate Control (only used when the S/PDIF Transmitter is the only interface sourcing the ADC) 000 = 128fs 001 = 192fs 010 = 256fs 011 = 384fs 100 = 512fs 101 = 768fs 110 = 1152fs
	8	VMIDSEL	1	VMID Impedance Selection 0 = High impedance, power saving 1 = Low impedance, fast power-on
R30 SPDTXCHAN 0 1Eh	1:0	TXSRC[1:0]	10	S/PDIF Transmitter Data Source 00 = S/PDIF received data (see REAL_THROUGH) 01 = ADC digital output data. 10 = Secondary Audio Interface 11 = Audio Interface received data
	2	OVWCHAN	0	Only used if TXSRC==00. Overwrites the ‘through-path’ Channel Bit with values determined by the channel-bit control registers. 0 = Channel data equal to recovered channel data. 1 = Channel data taken from channel status registers.
	3	REAL_ THROUGH	0	S/PDIF Through Mode Control 0 = SPDIFOP pin sources output of S/PDIF Transmitter 1 = SPDIFOP pins sources output of S/PDIF IN Mux
R31 SPDTXCHAN 1 1Fh	0	CON/PRO	0	0 = Consumer Mode 1 = Professional Mode (not supported by WM8581)
	1	AUDIO_N	0	0 = S/PDIF transmitted data is audio PCM. 1 = S/PDIF transmitted data is not audio PCM.
	2	CPY_N	0	0 = Transmitted data has copyright asserted. 1 = Transmitted data has no copyright assertion.

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td rowspan="2"></td><td>5:3</td><td>DEEMPH[2:0]</td><td>000</td><td>000 = Data from Audio interface has no pre-emphasis.
001 = Data from Audio interface has pre-emphasis.
010 = Reserved (Audio interface has pre-emphasis).
011 = Reserved (Audio interface has pre-emphasis).
All other modes are reserved and should not be used.</td></tr>
<tr><td>7:6</td><td>CHSTMODE [1:0]</td><td>00</td><td>00 = Only valid mode for consumer applications.</td></tr>
<tr><td>R32
SPDTXCHAN 2
20h</td><td>7:0</td><td>CATCODE [7:0]</td><td>00000000</td><td>Category Code. Refer to S/PDIF specification for details.
00h indicates “general” mode</td></tr>
<tr><td rowspan="3">R33
SPDTXCHAN 3
21h</td><td>3:0</td><td>SRCNUM [3:0]</td><td>0000</td><td>Source Number. No definitions are attached to data.</td></tr>
<tr><td>5:4</td><td>CHNUM1[1:0]</td><td>00</td><td>Channel Number for Subframe 1<table><tr><th>CHNUM1</th><th>Channel Status Bits[23:20]</th></tr><tr><td>00</td><td>0000 = Do not use channel number</td></tr><tr><td>01</td><td>0001 = Send to Left Channel</td></tr><tr><td>10</td><td>0010 = Send to Right Channel</td></tr><tr><td>11</td><td>0000 = Do not use channel number</td></tr></table></td></tr>
<tr><td>7:6</td><td>CHNUM2[1:0]</td><td>00</td><td>Channel Number for Subframe 2<table><tr><th>CHNUM2</th><th>Channel Status Bits[23:20]</th></tr><tr><td>00</td><td>0000 = Do not use channel number</td></tr><tr><td>01</td><td>0001 = Send to Left Channel</td></tr><tr><td>10</td><td>0010 = Send to Right Channel</td></tr><tr><td>11</td><td>0000 = Do not use channel number</td></tr></table></td></tr>
<tr><td rowspan="2">R34
SPDTXCHAN 4
22h</td><td>3:0</td><td>FREQ[3:0]</td><td>0001</td><td>Sampling Frequency. See S/PDIF specification for details.
0001 = Sampling Frequency not indicated.</td></tr>
<tr><td>5:4</td><td>CLKACU[1:0]</td><td>11</td><td>Clock Accuracy of Generated clock.
00 = Level II
01 = Level I
10 = Level III
11 = Interface frame rate not matched to sampling frequency.</td></tr>
<tr><td rowspan="3">R35
SPDTXCHAN 5
23h</td><td>0</td><td>MAXWL</td><td>1</td><td>Maximum Audio sample word length
0 = 20 bits
1 = 24 bits</td></tr>
<tr><td>3:1</td><td>TXWL[2:0]</td><td>101</td><td>Audio Sample Word Length.
000 = Word Length Not Indicated<table><tr><th>TXWL[2:0]</th><th>MAXWL==1</th><th>MAXWL==0</th></tr><tr><td>001</td><td>20 bits</td><td>16 bits</td></tr><tr><td>010</td><td>22 bits</td><td>18 bits</td></tr><tr><td>100</td><td>23 bits</td><td>19 bits</td></tr><tr><td>101</td><td>24 bits</td><td>20 bits</td></tr><tr><td>110</td><td>21 bits</td><td>17 bits</td></tr></table>All other combinations reserved</td></tr>
<tr><td>7:4</td><td>ORGSAMP [3:0]</td><td>0000</td><td>Original Sampling Frequency. See S/PDIF specification for details.
0000 = original sampling frequency not indicated</td></tr>
<tr><td>R36
SPDMODE
24h</td><td>0</td><td>SPDIFIN1MODE</td><td>1</td><td>Selects the input circuit type for the SPDIFIN1 input
0 = CMOS-compatible input
1 = Comparator input. Compatible with 500mVpp AC coupled consumer S/PDIF input signals as defined in IEC-60958-3.</td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	2:1	RXINSEL[1:0]	00	S/PDIF Receiver input mux select. Note that the general purpose inputs must be configured using GPOxOP to be either CMOS or comparator inputs if selected by RXINSEL. 00 = SPDIFIN1 01 = SPDIFIN2 (MFP3) 10 = SPDIFIN3 (MFP4) 11 = SPDIFIN4 (MFP5)
R37 INTMASK 25h	8:0	MASK[8:0]	000000000	When a flag is masked, it does not update the Error Register or contribute to the interrupt pulse. 0 = unmask, 1 = mask. MASK[0] = mask control for UPD_UNLOCK MASK[1] = mask control for INT_INVALID MASK[2] = mask control for INT_CSUD MASK[3] = mask control for INT_TRANS_ERR MASK[4] = mask control for UPD_AUDIO_N MASK[5] = mask control for UPD_PCM_N MASK[6] = mask control for UPD_CPY_N MASK[7] = mask control for UPD_DEEMPH MASK[8] = mask control for UPD_REC_FREQ
R38 GPO1 26h	3:0	GPO1OP[3:0]	0000	0000 = INTB 0001 = V 0010 = U 0011 = C 0100 = P 0101 = SFRM_CLK 0110 = 192BLK 0111 = UNLOCK 1000 = CSUD 1001 = REC_FREQ192 1010 = ZFLAG 1011 = NON_AUDIO 1100 = CPY_N 1101 = DEEMP 1110 = Set GPO as S/PDIF input (standard CMOS input buffer). Only applicable for GPO3/4/5. 1111 = Set GPO as S/PDIF input ('comparator' input for AC coupled consumer S/PDIF signals). Only applicable for GPO3/4/5
	7:4	GPO2OP[3:0]	0001	
	8	FILLMODE	0	Determines what S/PDIF Receiver should do with corrupted or invalid data: 0 = Data from S/PDIF Receiver remains static at last valid sample. 1 = Data from S/PDIF Receiver is output as all zeros.

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
R39 GPO2 27h	3:0	GPO3OP[3:0]	0010	0000 = INTB 0001 = V 0010 = U 0011 = C 0100 = P 0101 = SFRM_CLK 0110 = 192BLK 0111 = UNLOCK 1000 = CSUD 1001 = REC_FREQ192 1010 = ZFLAG 1011 = NON_AUDIO 1100 = CPY_N 1101 = DEEMP 1110 = Set GPO as S/PDIF input (standard CMOS input buffer). Only applicable for GPO3/4/5. 1111 = Set GPO as S/PDIF input (‘comparator’ input for AC coupled consumer S/PDIF signals). Only applicable for GPO3/4/5
	7:4	GPO4OP[3:0]	0011	
	8	ALWAYSVALID	0	Used to ignore the INVALID flag. 0 = Use INVALID flag. 1 = Ignore INVALID flag.
R40 GPO3 28h	3:0	GPO5OP[3:0]	0100	0000 = INTB 0001 = V 0010 = U 0011 = C 0100 = P 0101 = SFRM_CLK 0110 = 192BLK 0111 = UNLOCK 1000 = CSUD 1001 = REC_FREQ192 1010 = ZFLAG 1011 = NON_AUDIO 1100 = CPY_N 1101 = DEEMP 1110 = Set GPO as S/PDIF input (standard CMOS input buffer). Only applicable for GPO3/4/5. 1111 = Set GPO as S/PDIF input (‘comparator’ input for AC coupled consumer S/PDIF signals). Only applicable for GPO3/4/5
	7:4	GPO6OP[3:0]	0101	
R41 GPO4 29h	3:0	GPO7OP[3:0]	0110	
R43 INTSTAT 2Bh	0	UPD_UNLOCK	-	UNLOCK flag update signal 0 = INTB not caused by update to UNLOCK flag 1 = INTB caused by update to UNLOCK flag
	1	INT_INVALID	-	INVALID flag interrupt signal 0 = INTB not caused by INVALID flag 1 = INTB caused by INVALID flag
	2	INT_CSUD	-	CSUD flag interrupt signal 0 = INTB not caused by CSUD flag 1 = INTB caused by CSUD flag
	3	INT_TRANS_ERR	-	TRANS_ERR flag interrupt signal 0 = INTB not caused by TRANS_ERR flag 1 = INTB caused by TRANS_ERR flag

<table>
<tr><th>REGISTER ADDRESS</th><th>BIT</th><th>LABEL</th><th>DEFAULT</th><th>DESCRIPTION</th></tr>
<tr><td></td><td>4</td><td>UPD_NON_AUDIO</td><td>-</td><td>NON_AUDIO update signal
0 = INTB not caused by update to NON_AUDIO flag
1 = INTB caused by update to NON_AUDIO flag</td></tr>
<tr><td></td><td>5</td><td>UPD_CPY_N</td><td>-</td><td>CPY_N update signal
0 = INTB not caused by update to CPY_N flag
1 = INTB caused by update to CPY_N flag</td></tr>
<tr><td></td><td>6</td><td>UPD_DEEMPH</td><td>-</td><td>DEEMPH update signal
0 = INTB not caused by update to DEEMPH flag
1 = INTB caused by update to DEEMPH flag</td></tr>
<tr><td></td><td>7</td><td>UPD_REC_FREQ</td><td>-</td><td>REC_FREQ update signal
0 = INTB not caused by update to REC_FREQ flag
1 = INTB caused by update to REC_FREQ flag</td></tr>
<tr><td>R44
SPDRXCHAN 1
2C</td><td>0</td><td>CON/PRO</td><td>-</td><td>0 = Consumer Mode
1 = Professional Mode
The WM8581 is a consumer mode device. Detection of professional mode may give erroneous behaviour.</td></tr>
<tr><td></td><td>1</td><td>AUDIO_N</td><td>-</td><td>Recovered S/PDIF Channel status bit 1.
0 = Data word represents audio PCM samples.
1 = Data word does not represent audio PCM samples.</td></tr>
<tr><td></td><td>2</td><td>CPY_N</td><td>-</td><td>0 = Copyright is asserted for this data.
1 = Copyright is not asserted for this data.</td></tr>
<tr><td></td><td>3</td><td>DEEMPH</td><td>-</td><td>0 = Recovered S/PDIF data has no pre-emphasis.
1 = Recovered S/PDIF data has pre-emphasis.</td></tr>
<tr><td></td><td>5:4</td><td>Reserved</td><td>-</td><td>Reserved for additional de-emphasis modes.</td></tr>
<tr><td></td><td>7:6</td><td>CHSTMODE [1:0]</td><td>-</td><td>00 = Only valid mode for consumer applications.</td></tr>
<tr><td>R45
SPDRXCHAN 2
2Dh</td><td>7:0</td><td>CATCODE [7:0]</td><td>-</td><td>Category Code. Refer to S/PDIF specification for details.
00h indicates “general” mode.</td></tr>
<tr><td>R46
SPDRXCHAN 3
2Eh</td><td>3:0</td><td>SRCNUM [3:0]</td><td>-</td><td>Indicates number of S/PDIF source.</td></tr>
<tr><td></td><td>7:4</td><td>CHNUM1[3:0]</td><td>-</td><td>Channel number for channel 1.
0000 = Take no account of channel number (channel 1 defaults to left DAC)
0001 = channel 1 to left channel
0010 = channel 1 to right channel</td></tr>
<tr><td>R47
SPDRXCHAN 4
2Fh</td><td>3:0</td><td>FREQ[3:0]</td><td>-</td><td>Sampling Frequency. See S/PDIF specification for details.
0001 = Sampling Frequency not indicated.</td></tr>
<tr><td></td><td>5:4</td><td>CLKACU[1:0]</td><td>-</td><td>Clock Accuracy of received clock.
00 = Level II
01 = Level I
10 = Level III
11 = Interface frame rate not matched to sampling frequency.</td></tr>
<tr><td>R48
SPDRXCHAN 5
30h</td><td>0</td><td>MAXWL</td><td>-</td><td>Maximum Audio sample word length
0 = 20 bits
1 = 24 bits</td></tr>
<tr><td></td><td>3:1</td><td>RXWL[2:0]</td><td>-</td><td>Audio Sample Word Length.
000: Word Length Not Indicated
<table>
<tr><th>RXWL[2:0]</th><th>MAXWL==1</th><th>MAXWL==0</th></tr>
<tr><td>001</td><td>20 bits</td><td>16 bits</td></tr>
<tr><td>010</td><td>22 bits</td><td>18 bits</td></tr>
<tr><td>100</td><td>23 bits</td><td>19 bits</td></tr>
</table></td></tr>
</table>

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION		
				101	24 bits	20 bits
				110	21 bits	17 bits
				All other combinations are reserved and may give erroneous operation. Data will be truncated internally when these bits are set		
	7:4	ORGSAMP [3:0]	-	Original Sampling Frequency. See S/PDIF specification for details. 0000 = original sampling frequency not indicated		
R49 SPDSTAT 31h	0	AUDIO_N	-	Recovered Channel Status bit-1. 0 = Data word represents audio PCM samples. 1 = Data word does not represent audio PCM samples.		
	1	PCM_N	-	Indicates that non-audio code (defined in IEC-61937) has been detected. 0 = Sync code not detected. 1 = Sync code detected – received data is not audio PCM.		
	2	CPY_N	-	Recovered Channel Status bit-2. 0 = Copyright is asserted for this data. 1 = Copyright is not asserted for this data. Note this signal is inverted and will cause an interrupt on logic 0.		
	3	DEEMPH	-	Recovered Channel Status bit-3 0 = Recovered S/PDIF data has no pre-emphasis. 1 = Recovered S/PDIF data has pre-emphasis		
	5:4	REC_FREQ [1:0]	--	Indicates recovered S/PDIF clock frequency: 00 = 192kHz 01 = 96kHz / 88.2kHz 10 = 48kHz / 44.1kHz 11 = 32kHz		
	6	UNLOCK	-	Indicates that the S/PDIF Clock Recovery circuit is unlocked or that the input S/PDIF signal is not present. 0 = Locked onto incoming S/PDIF stream. 1 = Not locked to the incoming S/PDIF stream or the incoming S/PDIF stream is not present.		
R50 PWRDN 1 32h	0	PWDN	0	Chip Powerdown Control (works in tandem with the other powerdown registers): 0 = All digital circuits running, outputs are active 1 = All digital circuits in power save mode, outputs muted		
	1	ADCPD	1	ADC powerdown: 0 = ADC enabled 1 = ADC disabled		
	4:2	DACPD[3:0]	1111	DAC powerdowns (0 = DAC enabled, 1 = DAC disabled) DACPD[0] = DAC1 DACPD[1] = DAC2 DACPD[2] = DAC3 DACPD[3] = DAC4		
	6	ALLDACPD	1	Overrides DACPD[3:0] 0 = DACs under control of DACPD[3:0] 1= All DACs are disabled.		
R51 PWRDN 2 33h	0	OSCPD	0	OSC power down 0 = OSC enabled 1 = OSC disabled		
	1	PLLAPD	1	0 = PLLA enabled 1 = PLLA disabled		
	2	PLLBPD	1	0 = PLLB enable 1 = PLLB disable		

REGISTER ADDRESS	BIT	LABEL	DEFAULT	DESCRIPTION
	3	SPDIFPD	1	S/PDIF Clock Recovery PowerDown 0 = S/PDIF enabled 1 = S/PDIF disabled
	4	SPDIFTXD	1	S/PDIF Transmitter powerdown 0 = S/PDIF Transmitter enabled 1 = S/PDIF Transmitter disabled
	5	SPDIFRXD	1	S/PDIF Receiver powerdown 0 = S/PDIF Receiver enabled 1 = S/PDIF Receiver disabled
R52 READBACK 34h	2:0	READMUX [2:0]	000	Determines which status register is to be read back: 000 = Error Register 001 = Channel Status Register 1 010 = Channel Status Register 2 011 = Channel Status Register 3 100 = Channel Status Register 4 101 = Channel Status Register 5 110 = S/PDIF Status Register
	3	CONTREAD	0	Continuous Read Enable. 0 = Continuous read-back mode disabled 1 = Continuous read-back mode enabled
	4	READEN	0	Read-back mode enable. 0 = read-back mode disabled 1 = read-back mode enabled
R53 RESET 35h	8:0	RESET	n/a	Writing to this register will apply a reset to the device registers.

DIGITAL FILTER CHARACTERISTICS

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Filter					
Passband	±0.01 dB	0		0.4535fs	
	-6dB		0.5fs		
Passband ripple				±0.01	dB
Stopband		0.5465fs			
Stopband Attenuation	f > 0.5465fs	-65			dB
DAC Filter					
Passband	±0.05 dB			0.444fs	
	-3dB		0.487fs		
Passband ripple				±0.05	dB
Stopband		0.555fs			
Stopband Attenuation	f > 0.555fs	-60			dB

Table 76 Digital Filter Characteristics

DAC FILTER RESPONSES

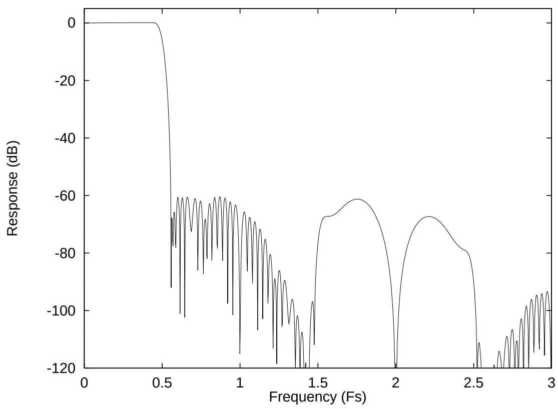


Figure 36 DAC Digital Filter Frequency Response – 44.1, 48 and 96KHz

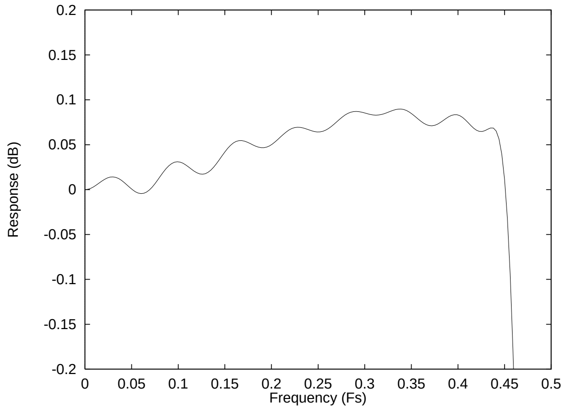


Figure 37 DAC Digital Filter Ripple –44.1, 48 and 96kHz

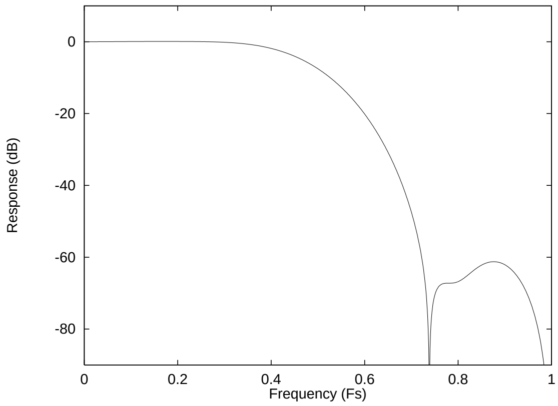


Figure 38 DAC Digital Filter Frequency Response – 192KHz

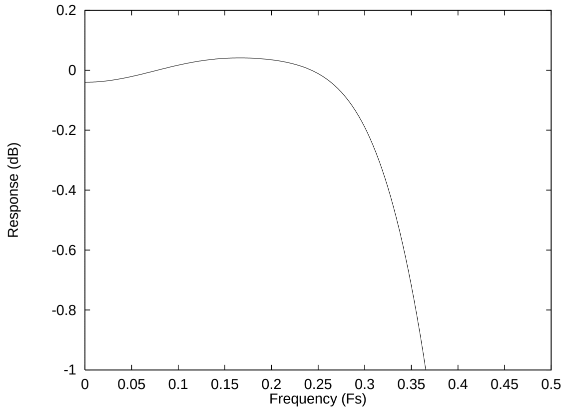


Figure 39 DAC Digital Filter Ripple – 192kHz

DIGITAL DE-EMPHASIS CHARACTERISTICS

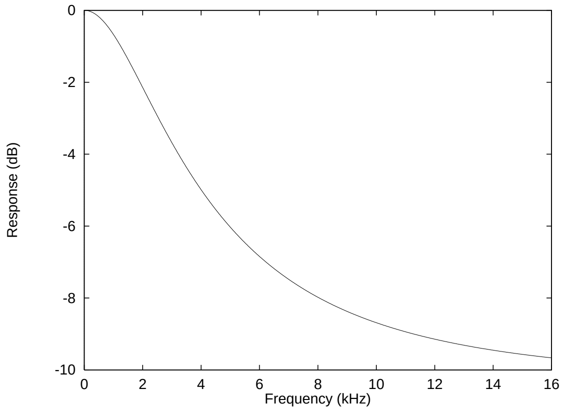


Figure 40 De-Emphasis Frequency Response (32kHz)

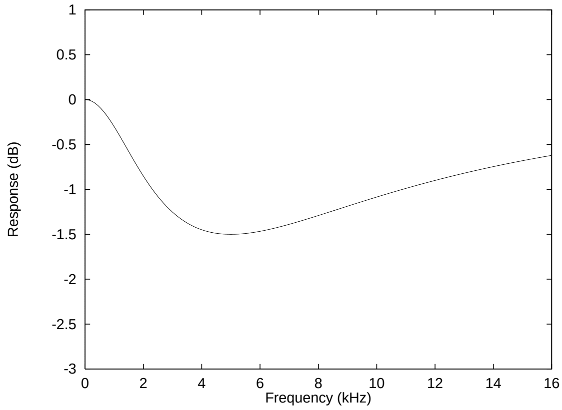


Figure 41 De-Emphasis Error (32KHz)

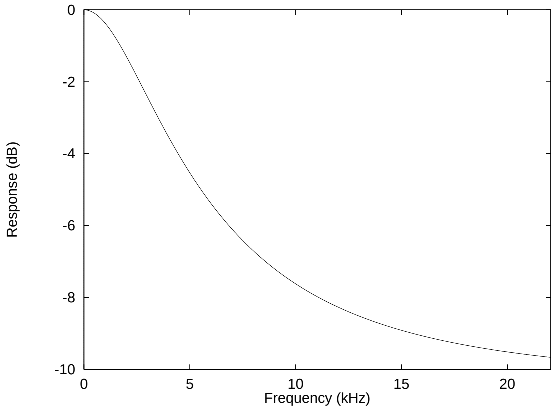


Figure 42 De-Emphasis Frequency Response (44.1KHz)

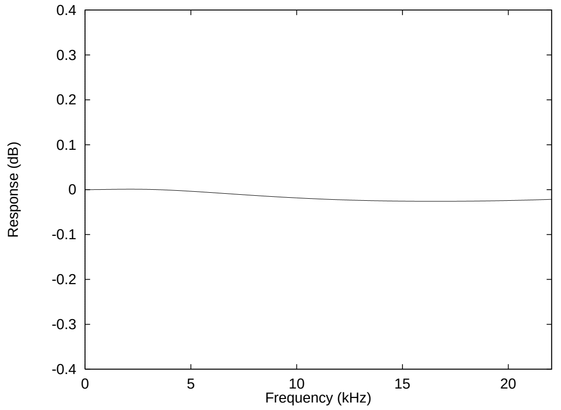


Figure 43 De-Emphasis Error (44.1KHz)

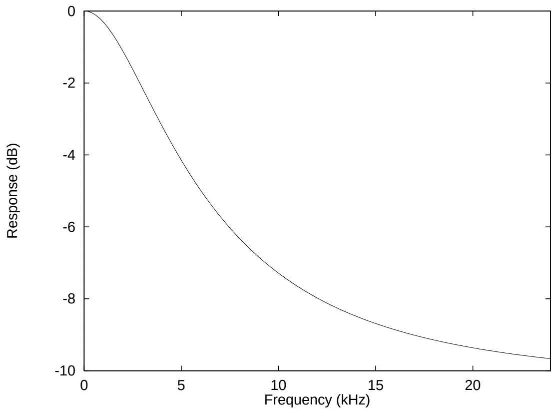


Figure 44 De-Emphasis Frequency Response (48kHz)

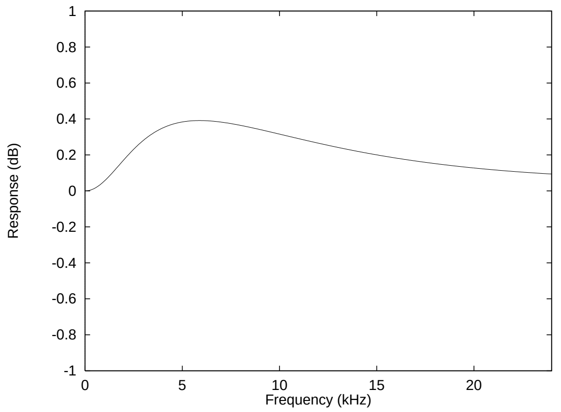


Figure 45 De-Emphasis Error (48kHz)

ADC FILTER RESPONSES

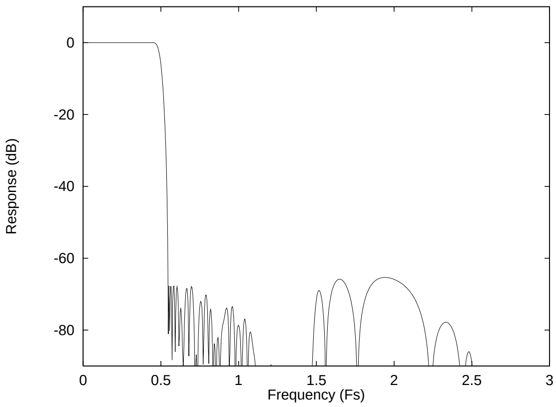


Figure 46 ADC Digital Filter Frequency Response

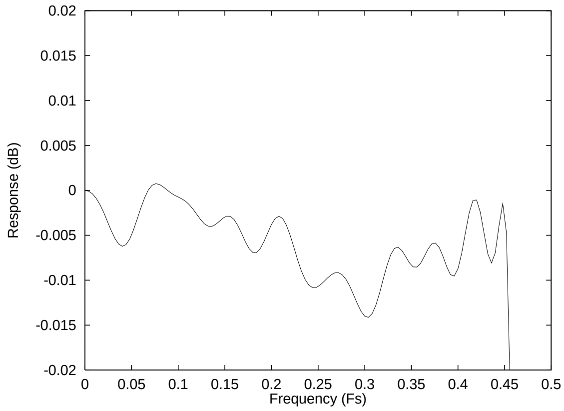


Figure 47 ADC Digital Filter Ripple

ADC HIGH PASS FILTER

The WM8581 has a selectable digital high pass filter to remove DC offsets. The filter response is characterised by the following polynomial.

$$H(z) = \frac{1 - z^{-1}}{1 - 0.9995z^{-1}}$$

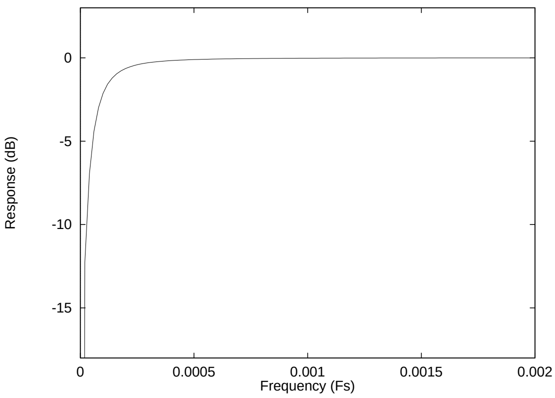


Figure 48 ADC Highpass Filter Response

RECOMMENDED EXTERNAL COMPONENTS

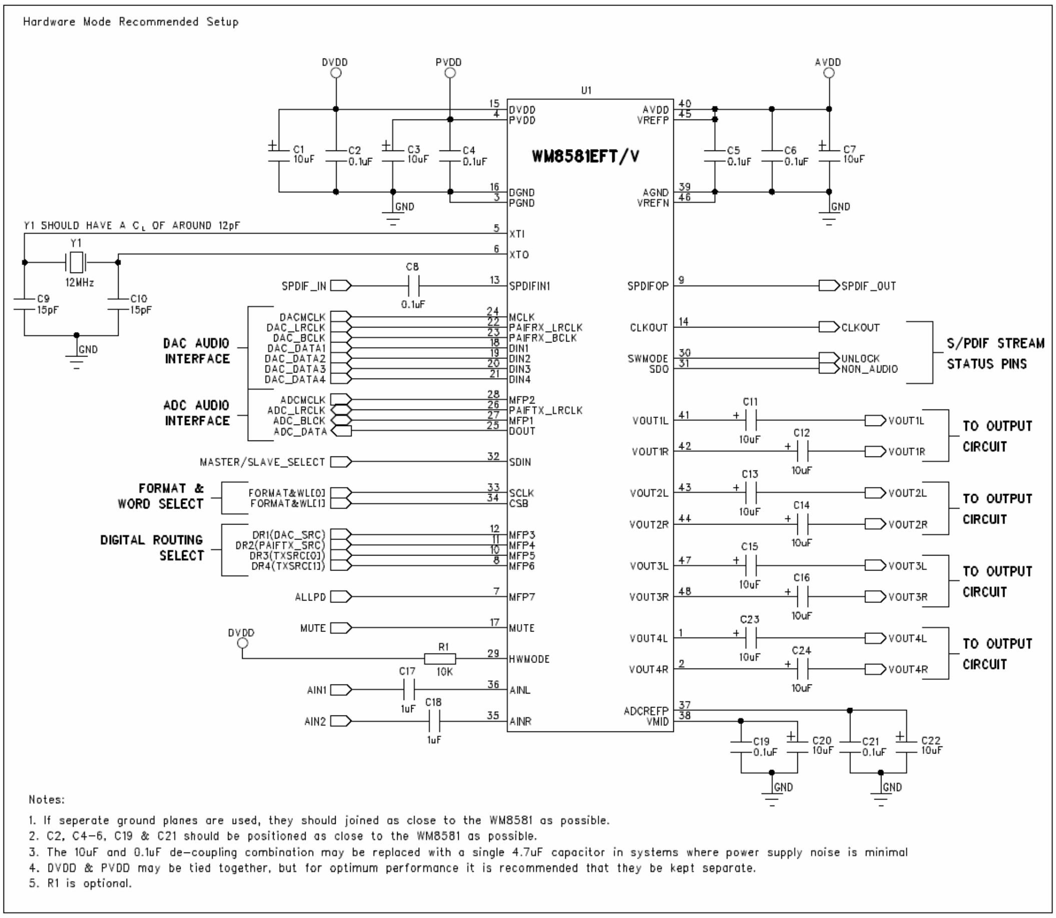
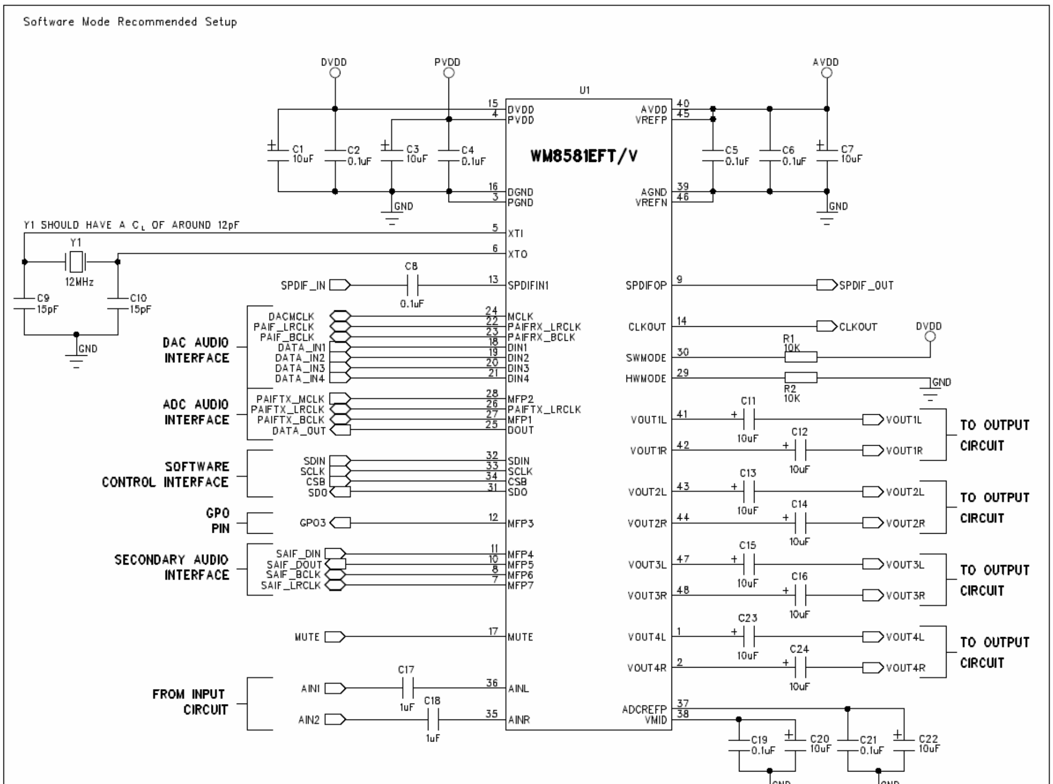


Figure 49 Recommended External Components - Hardware



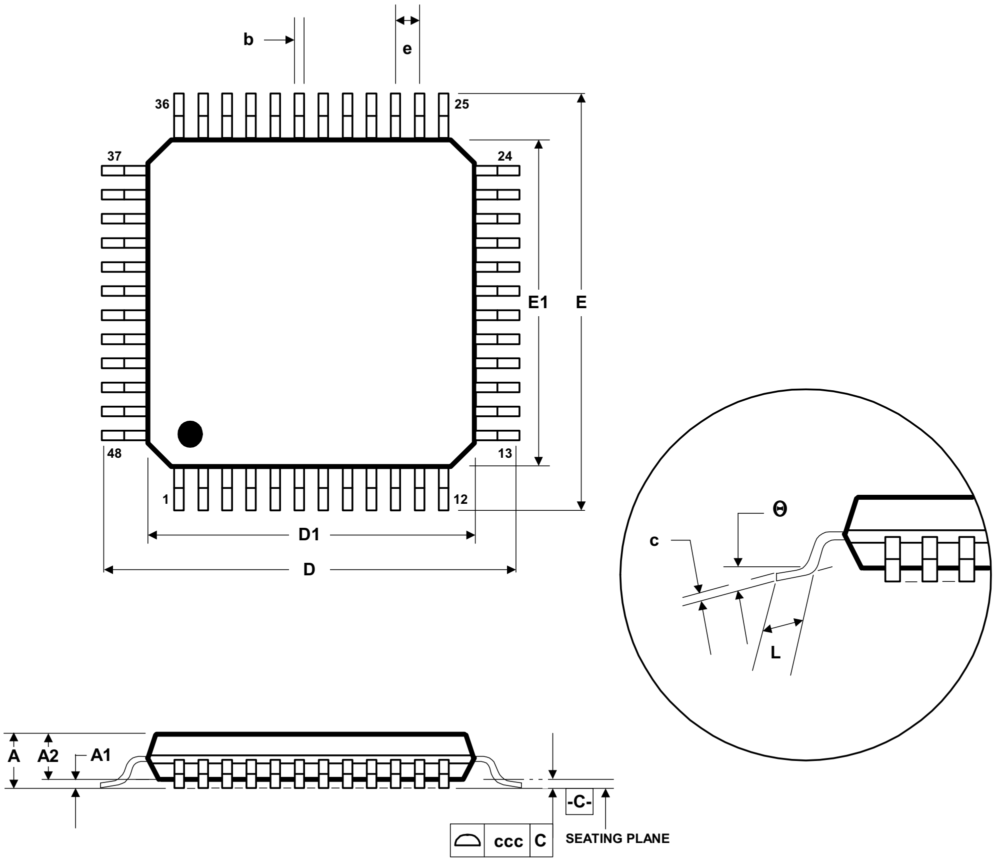
Notes:

1. If seperate ground planes are used, they should joined as close to the WM8581 as possible.
2. C2, C4-6, C19 & C21 should be positioned as close to the WM8581 as possible.
3. The 10uF and 0.1uF de-coupling combination may be replaced with a single 4.7uF capacitor in systems where power supply noise is minimal
4. DVDD & PVDD may be tied together, but for optimum performance it is recommended that they be kept separate.
5. Only one MFP configuration is shown and others are possible. Refer to "Multi-Function Pin Configuration" diagram.
6. R1 and R2 are optional.

Figure 50 Recommended External Components - Software

PACKAGE DIMENSIONS

FT: 48 PIN TQFP (7 x 7 x 1.0 mm) **DM004.C**



Symbols	Dimensions (mm)		
	MIN	**NOM**	**MAX**
A	-----	-----	1.20
A_1	0.05	-----	0.15
A_2	0.95	1.00	1.05
b	0.17	0.22	0.27
c	0.09	-----	0.20
D	9.00 BSC		
D_1	7.00 BSC		
E	9.00 BSC		
E_1	7.00 BSC		
e	0.50 BSC		
L	0.45	0.60	0.75
Θ	0^o	3.5^o	7^o
Tolerances of Form and Position			
ccc	0.08		
REF:	JEDEC.95, MS-026		

NOTES:
A. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
B. THIS DRAWING IS SUBJECT TO CHANGE WITHOUT NOTICE.
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSION, NOT TO EXCEED 0.25MM.
D. MEETS JEDEC.95 MS-026, VARIATION = ABC. REFER TO THIS SPECIFICATION FOR FURTHER DETAILS.

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ADDRESS:

Wolfson Microelectronics plc

Westfield House

26 Westfield Road

Edinburgh

EH11 2QB

United Kingdom

Tel :: +44 (0)131 272 7000

Fax :: +44 (0)131 272 7001

Email :: sales@wolfsonmicro.com