PM5382

S/UNI-16X155

SATURN USER NETWORK INTERFACE (16X155)

REFERENCE DESIGN

PRELIMINARY

PUBLIC REVISION HISTORY

Issue No.	Issue Date	Details of Change
1	August 2001	Document created

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1 INTRODUCTION

The PM5382 S/UNI-16X155 standard product supports 16 SATURN User Network Interfaces with SONET/SDH processing, ATM and Packet mapping functions at the STS-3c (STM-1) 155.52 Mbit/s rate with on-chip clock and data recovery and clock synthesis. The S/UNI-16X155 is intended for use in equipment implementing Asynchronous Transfer Mode (ATM) User-Network Interfaces (UNI), ATM Network-Network Interfaces (NNI), and Packet Over SONET/SDH (POS) interfaces. The POS interface can be used to support several packet based protocols, including the Point-to-Point Protocol (PPP). The S/UNI-16x155 may find application at either end of switch-to-switch links or switch-to-terminal links, both in public network (WAN) and private network (LAN) situations.

This S/UNI-16X155 reference design provides a physical interface implementation of a 16 Port SONET/SDH line card for both ATM and POS applications. It provides sixteen single-mode or multi-mode optical interfaces at OC-3c rate, and a POS/PHY Level 3/UTOPIA Level 3, 104MHz, 32-bit wide system side synchronous interface. The in-system programmable FPGA provides a simple means to manipulate ATM cells and POS packets. The reference design board is also compatible with the S/UNI-4x622 device and can be assembled to support 4 OC-12c links. Refer to the S/UNI-4x622 Reference Design (PMC-2000064) and the Application Note *Integrating Designs Using the S/UNI-16x155 and S/UNI-4x622* (PMC-2000539) for further information regarding this device and integrated design recommendations.

The PM5382 is packaged in a 520 pin Super Ball Grid Array (SBGA) as shown below. For detailed information on the PM5382 device, please refer to the Standard Product Datasheet.

The terms “CompactPCI™” and “cPCI” are used interchangeably within this document and should be considered equivalent.

1.1 Reference Design Functionality

- Supports 16 Single-Mode or Multi-Mode OC-3c 155.52 Mbit/s SONET/SDH Physical Layer ATM or POS Interfaces.
- Performs dropside loop back of ATM cells or POS Packets.

- Provides a Utopia Level 3, 104 MHz, 32-bit ATM Multi-PHY System Interface to an external high-speed connector.
- Provides a POS-PHY Level 3, 104 MHz, 32-bit Packet Over SONET/SDH Multi-PHY System Interface to an external high-speed connector.
- Supports 1+1 or 1:n Automatic Protection Switching (APS).
- Provides hardware support for implementing a 16 port OC-3 linecard using a S/UNI-16x155 or a 4 port OC-12 linecard using a S/UNI-4x622 device.

1.2 Reference Design Features

The reference design is based on a cPCI form factor card. The reference design will consist of

- one PM5382 S/UNI-16x155.
- Sixteen OC-3 small form factor (SFF) optical data link transceivers.
- FPGA to support ATM & POS drop-side loop back and transparent operation.
- PLX cPCI Bridge for interfacing to the host processor.
- reference oscillators required for SONET and UL3/POS-PHY L3 interfaces.
- external 77.76 MHz reference clock interface for inter-board synchronization.
- powered by +3.3 Volts supply. +5.0 Volt components are avoided where possible.

2 APPLICATIONS

The S/UNI-16X155 Reference Design demonstrates the physical interface implementation for both ATM and POS applications. The list below shows the networking equipment that can incorporate the S/UNI-16X155 device:

- WAN and Edge ATM switches physical interfaces
- LAN switches and hubs physical interfaces
- Packet switches and hubs physical interfaces.

The S/UNI-16X155 Reference Design can be used in four modes:

- ATM Drop Side Loop Back
- ATM Transparent
- POS Drop Side Loop Back
- POS Transparent.

Each of these modes is described in detail in the following sections.

APS (Automatic Protection Switching) may be enabled during any one of these modes, and is described separately.

Support for WANS (WAN Synchronization) is provided, and is described separately.

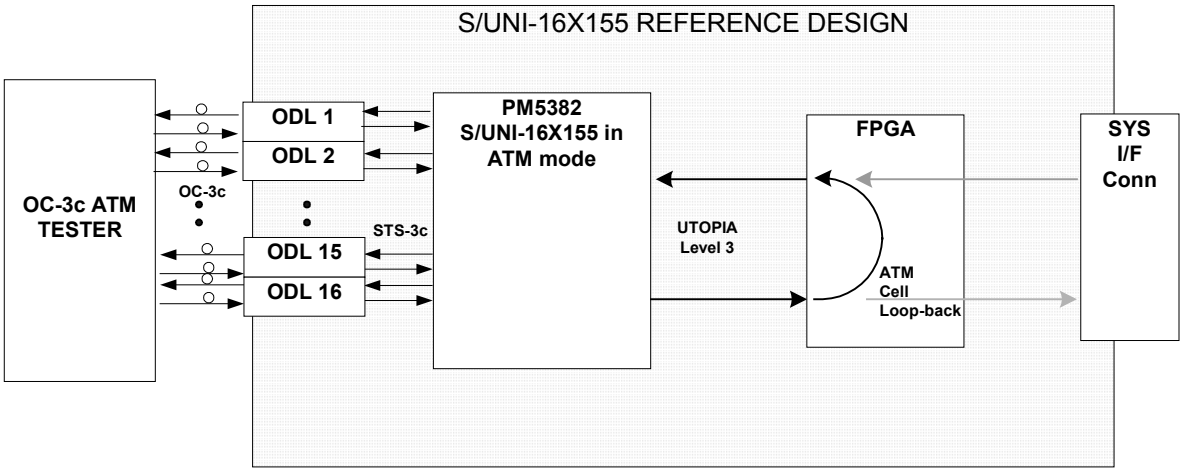
2.1 ATM Drop Side Loop Back

Each optical data link (ODL) transceiver will provide a received STS-3c signal to the S/UNI-16x155. Clock and Data recovery will be performed independently for each of the 16 input signals, and ATM cells will be extracted from the STS-3c payloads. After payload descrambling and error processing, ATM cells will be provided to the Utopia Level 3 (UL3) compliant RX interface on the PM5382.

The FPGA can be configured to loop the received ATM cells back to the UL3 compliant TX interface on the PM5382. This loop back is performed on a PHY by PHY basis (i.e. each ATM cell will be looped back to the ODL transceiver from which it was received.)

The UL3 compliant TX interface will accept ATM cells from the FPGA. The ATM cell payload will be scrambled and inserted into the transmitted STS-3c payload. Each of the 16 optical transceivers will accept one STS-3c signal for transmission via the optical data link.

Figure 1: ATM Drop Side Loop Back



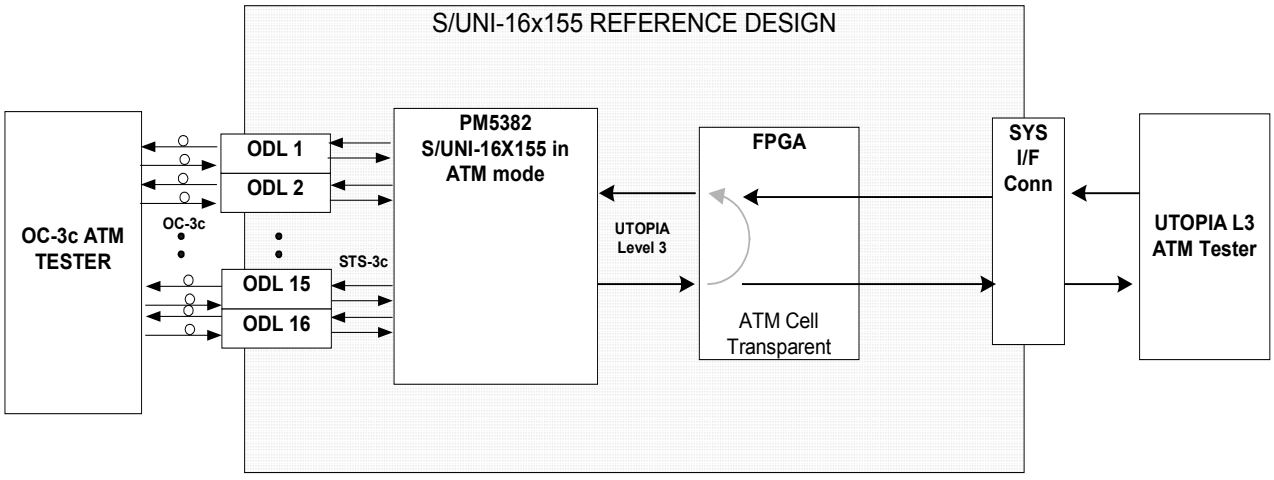
2.2 ATM Transparent

Each ODL transceiver will provide a received STS-3c signal to the S/UNI-16x155. Clock and Data recovery will be performed on the input signals, and ATM cells will be extracted from the STS-3c payloads. After payload descrambling and error processing, ATM cells will be provided to the Utopia Level 3 (UL3) compliant RX interface on the PM5382.

The FPGA can be configured to direct the cells to the UL3 compliant RX interface provided by the System Interface connector. This interface will provide ATM cells to an external system such as an ATM tester or Link layer device, and accept cells originating from the external system.

The UL3 compliant TX interface will accept cells via the FPGA. The ATM cell payload will be scrambled and inserted into the transmitted STS-3c payload. Each of the 16 optical transceivers will accept one STS-3c signal for transmission via the optical data link.

Figure 2: ATM Transparent



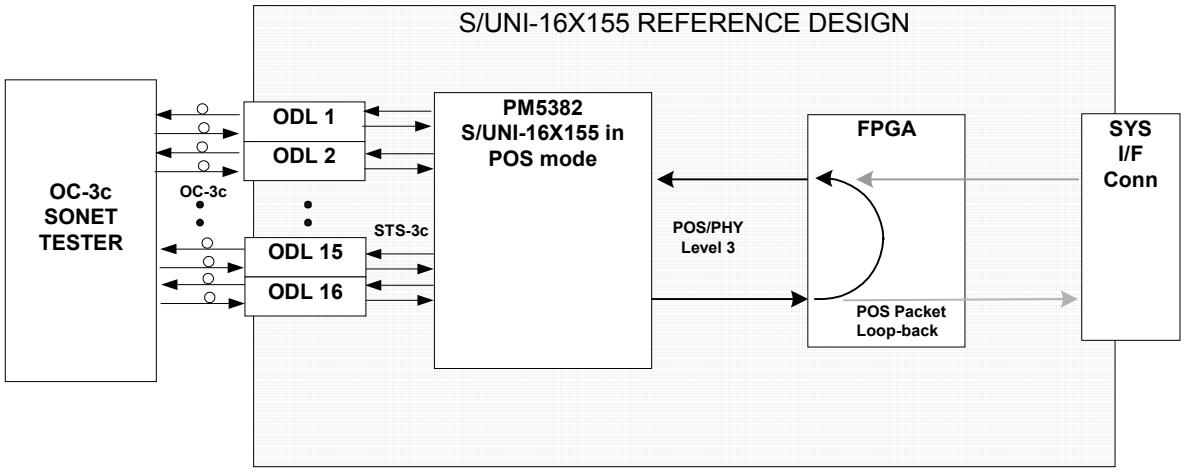
2.3 POS Drop Side Loop Back

Each ODL transceiver will provide a received STS-3c signal to the S/UNI-16x155. Clock and Data recovery will be performed for each of the input signals, and POS packets will be extracted from the STS-3c payloads. After payload descrambling and error processing, POS packets will be provided to the POS-PHY Level 3 compliant RX interface on the PM5382.

The FPGA can be configured to loop the received POS packets back to the PL3 compliant TX interface on the PM5382. This loop back is performed on a PHY by PHY basis.

The POS-PHY L3 compliant TX interface will accept POS packets from the FPGA. The POS packet payload will be scrambled and inserted into the transmitted STS-3c payload. Each of the 16 optical transceivers will accept one STS-3c signal for transmission via the optical data link.

Figure 3: POS Drop Side Loop Back



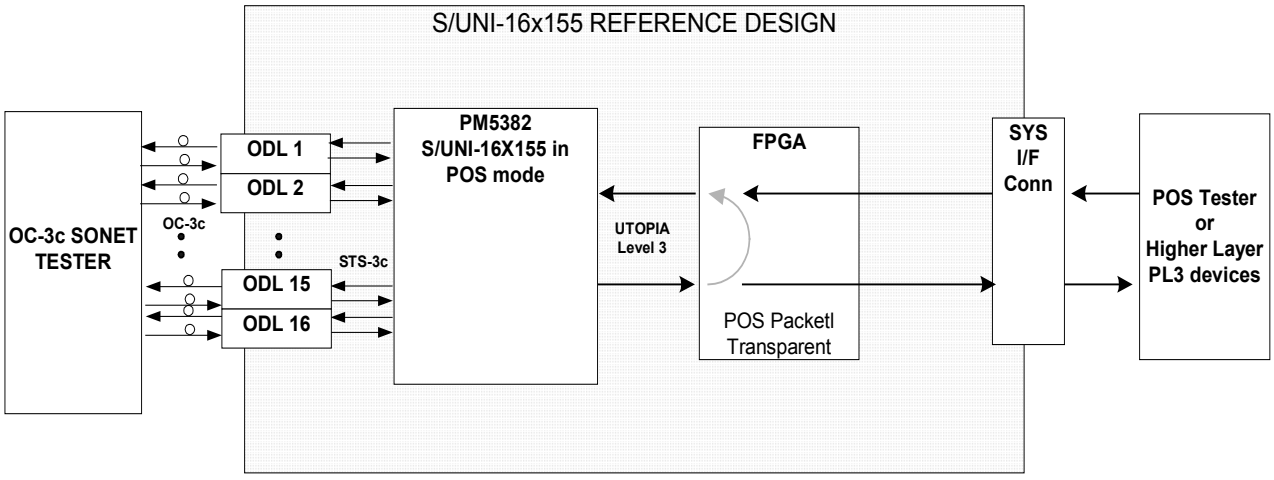
2.4 POS Transparent

Each ODL transceiver will provide a received STS-3c signal to the S/UNI-16x155. Clock and Data recovery will be performed for each of the input signals, and POS packets will be extracted from the STS-3c payloads. After payload descrambling and error processing, ATM cells will be provided to the POS-PHY Level 3 (PL3) compliant RX interface on the PM5382.

The FPGA can be configured to direct the POS traffic to the PL3 compliant TX System interface on the backplane connector. This interface will provide POS packets to an external system such as a POS tester or Link Layer device, as well as accept packets from the external system.

The POS-PHY L3 compliant TX interface on the PM5382 will accept packets via the FPGA. The POS packets will be scrambled, and inserted into the transmitted STS-3c payload. Each of the 16 optical transceivers will accept one STS-3c signal for transmission via the optical data link.

Figure 4: POS Transparent



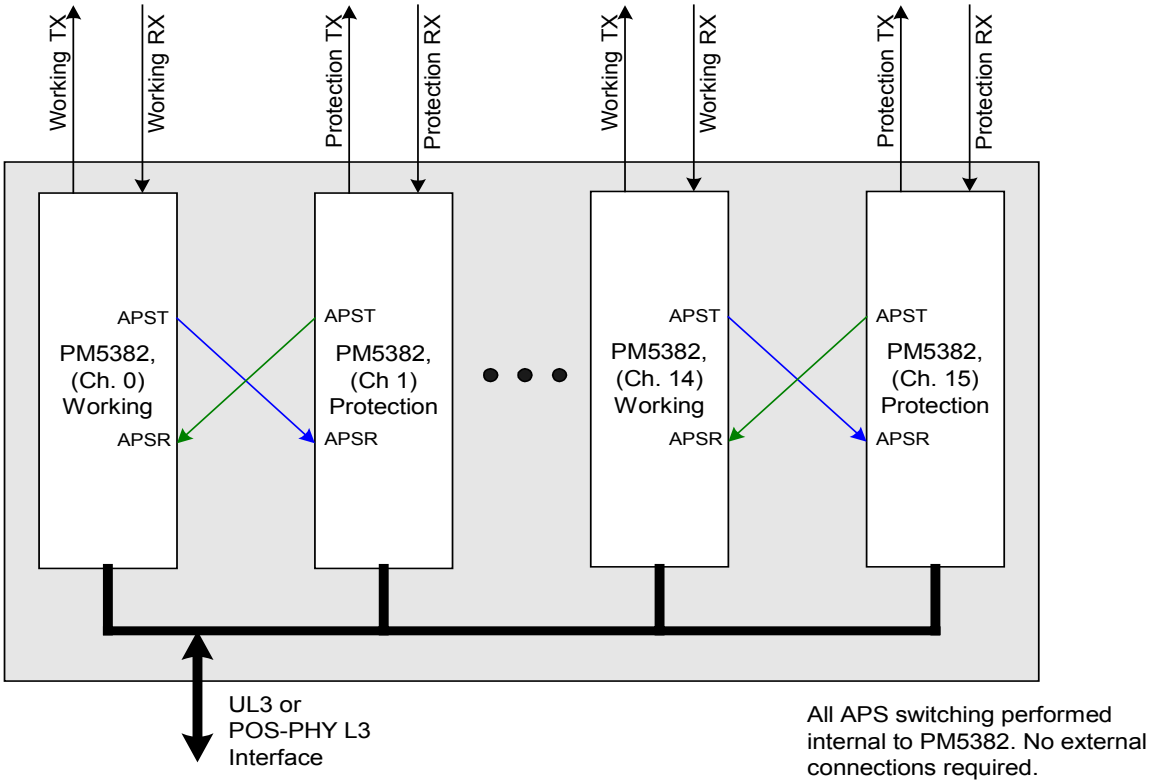
2.5 Automatic Protection Switching (APS)

The S/UNI-16x155 has the ability to exchange transmit path data with another S/UNI-16x155 in order to implement an APS interface. The APS support logic may also be used to reassign at the path level the channel numbers in a single S/UNI-16x155. With this logic, 1+1 or 1:N APS configurations can be implemented internal to a single PM5382.

2.5.1 Single Board 1+1 APS

The APS logic on the S/UNI-16x155 allows implementation of 1+1 APS without any external connections. Eight of the sixteen channels supported by the PM5382 are configured as working circuits, while the remaining eight are configured as protection circuits. Should the “Working TX” or “Working RX” optical links be interrupted, the “Protection TX” and “Protection RX” links will be utilized.

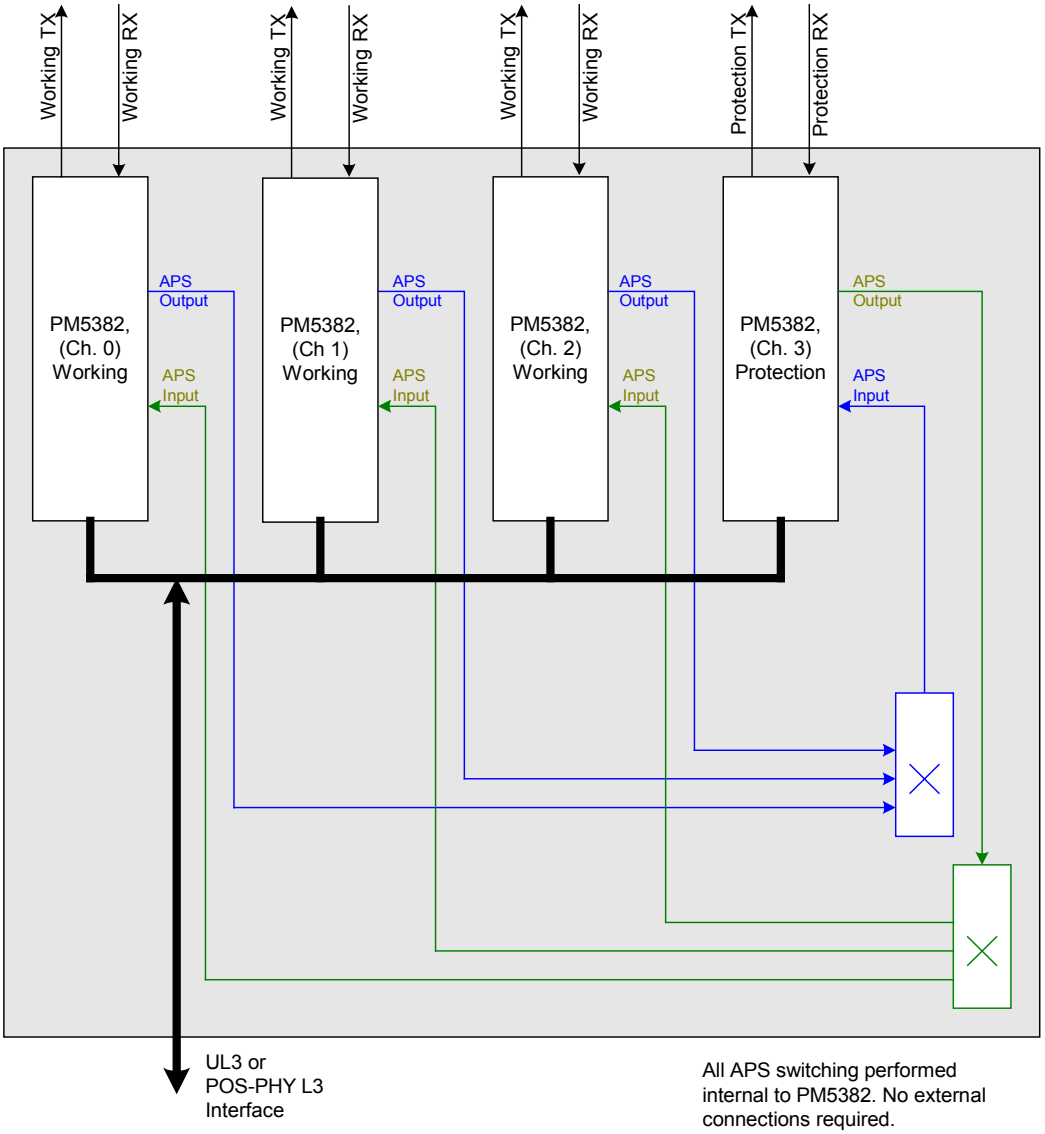
Figure 5: Single Board 1+1 APS



2.5.2 Single Board 1:N APS

This mode allows a single reference design to demonstrate 1:N APS functionality with N-1 channels supported by the PM5382 configured as working circuits, and a remaining channel configured as a protection circuit. Should the “Working TX” or “Working RX” optical links be interrupted, the “Protection TX” and “Protection RX” links will be utilized to restore the highest priority “Working” link.

Figure 6: Single Board 1:3 APS Example



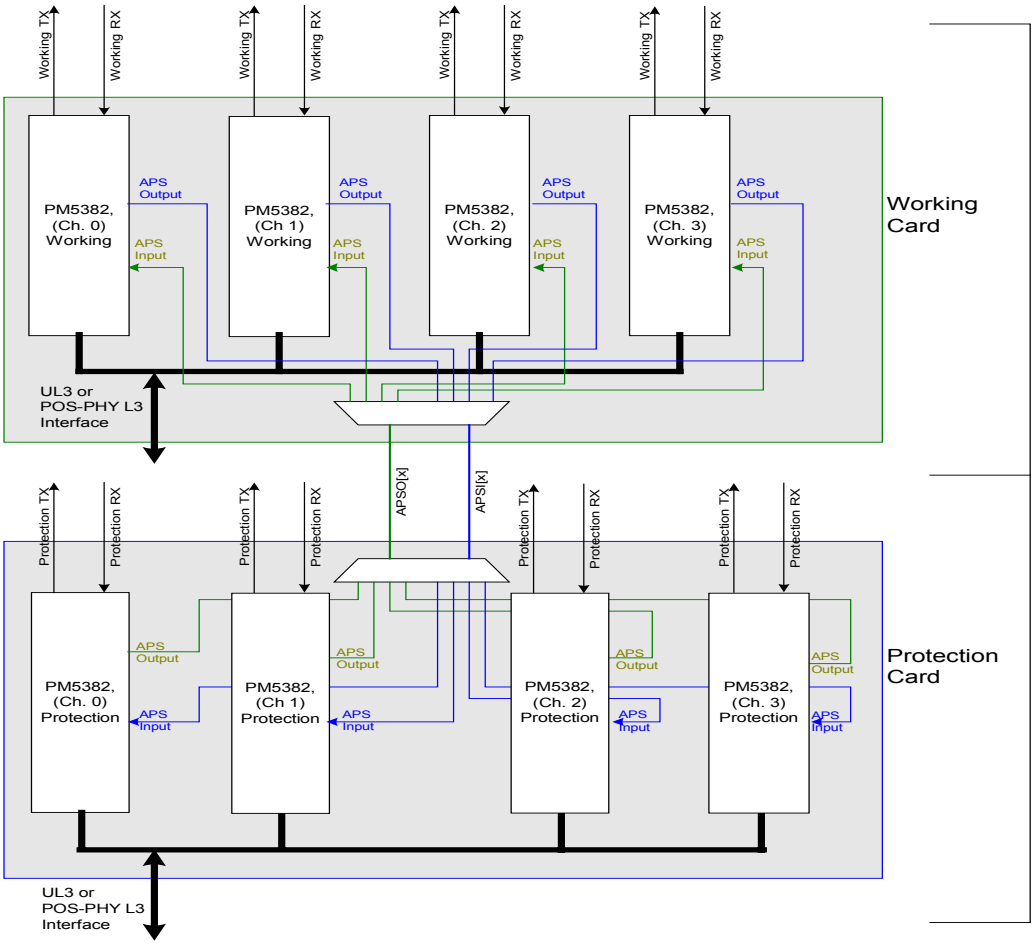
2.5.3 Multiple Board 1+1 APS

When implementing APS across two devices, four 622.08Mbit/sec links are used. Each link carries path information for four channels of the PM5382 device. The receive APS logic can be configured to map the channels within the link data stream to specific outputs as required.

For protection schemes implemented using multiple devices, care should be taken to ensure that the REFCLKs on all the boards are frequency locked to guarantee the data recovery units will function properly.

Figure 7 below outlines a 1+1 protection scheme. Four channels of a possible 16 are shown for simplicity.

Figure 7: Multiple Board 1+1 APS



2.6 WAN Synchonization Functionality

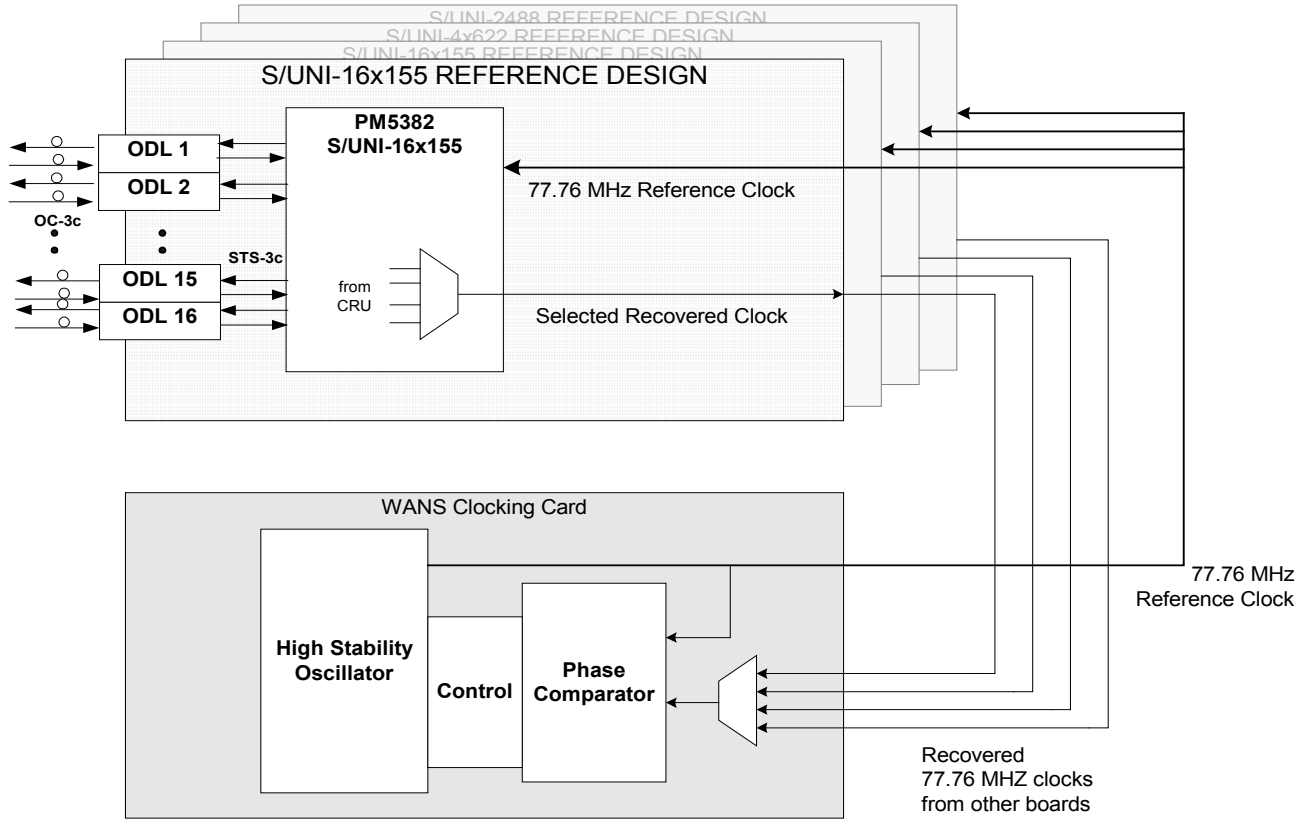
The S/UNI-16x155 Reference Design can be used to facilitate WAN Synchronization (WANS) Functionality in two different ways:

2.6.1 Synchronization Using Recovered Clock Signals

The WANS block on the S/UNI-16x155 performs a digital phase comparison between a recovered receive clock from one of the STS-3c channels and an external reference clock, usually implemented with a VCXO. This external reference clock is used to generate transmit timing for all channels.

On the S/UNI-16x155 Reference Design, the recovered clock signal is routed to an external connector that can interface to a separate timing card. The adjusted reference clock is distributed from the timing card to all cards in the system.

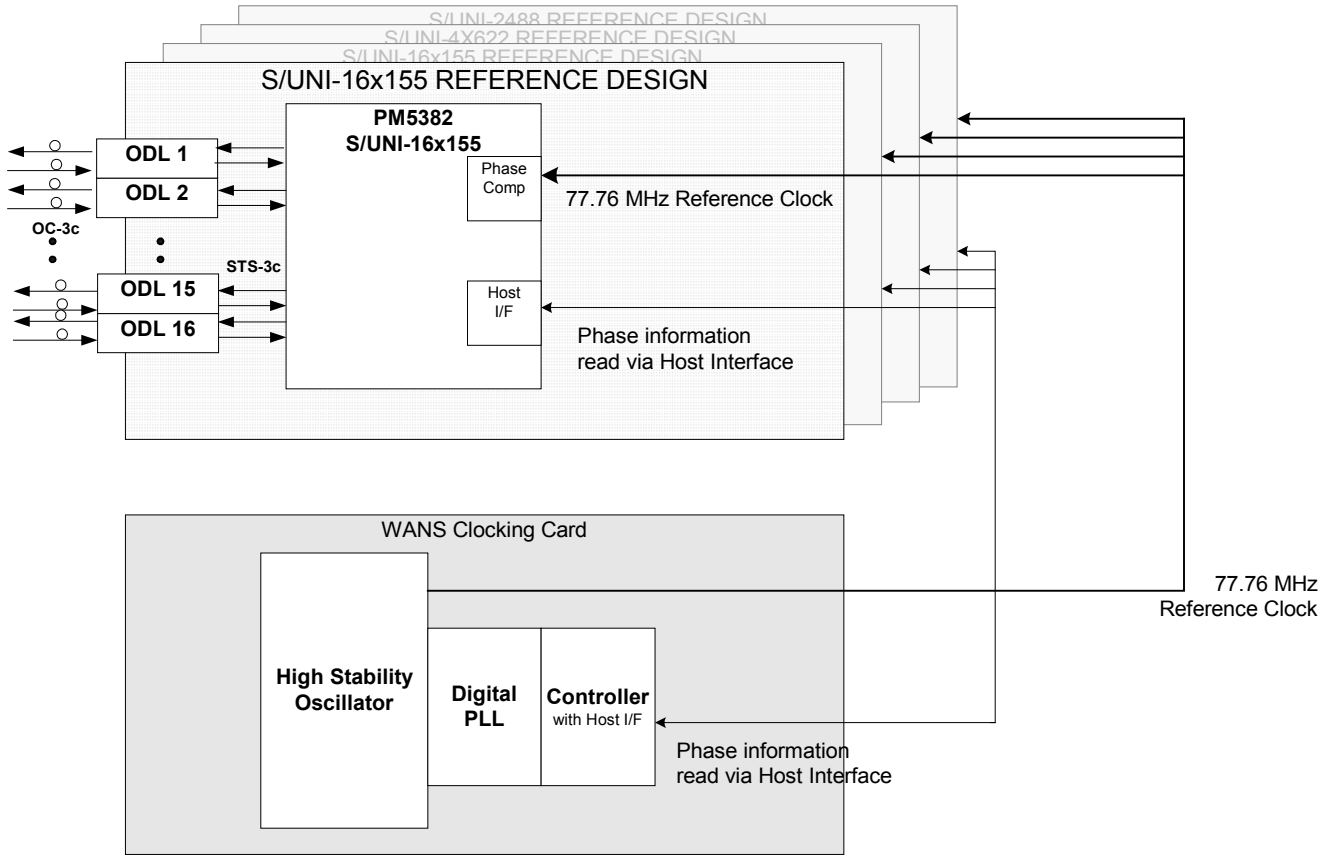
Figure 8: Synchronization Using Recovered Clock Signal



2.6.2 Synchronization Using Phase Comparator

The PM5382 is also able to compare the phase of the locally provided 77.76 MHz Reference Clock to that of the data clocks recovered from the incoming OC-3c signal. An external clocking card would then use phase information to lock a local high stability reference oscillator. Performing the phase comparisons within the PM5382 eliminates the need to transmit all recovered clocks back to the clocking card.

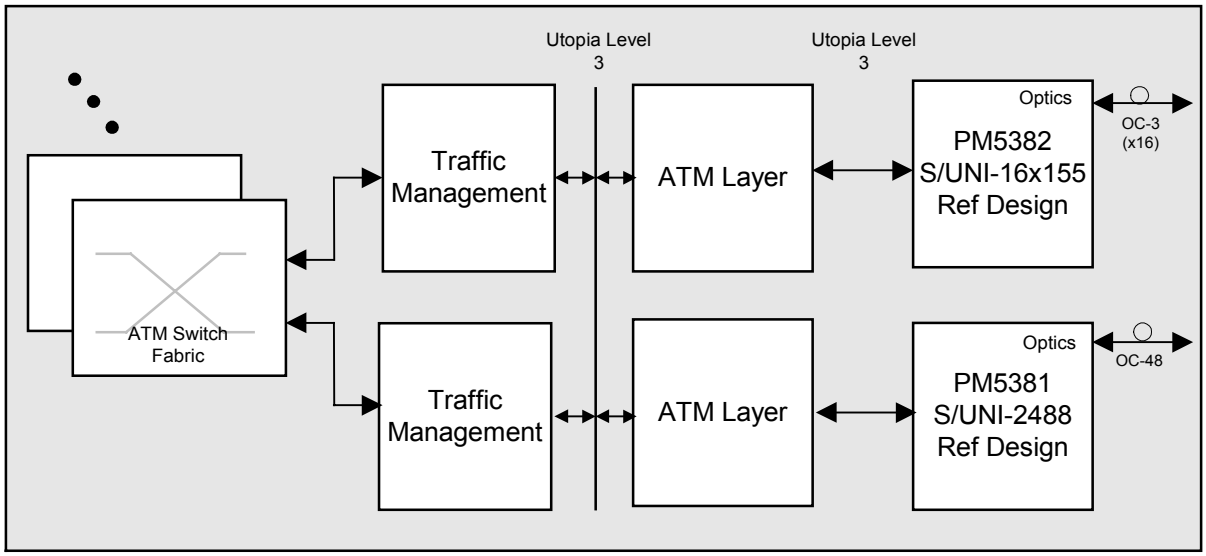
Figure 9: Synchronization Using Phase Comparator



2.7 Reference Design with other ATM Devices

This reference board may potentially be used within a larger system utilizing PMC-Sierra's ATM chip sets.

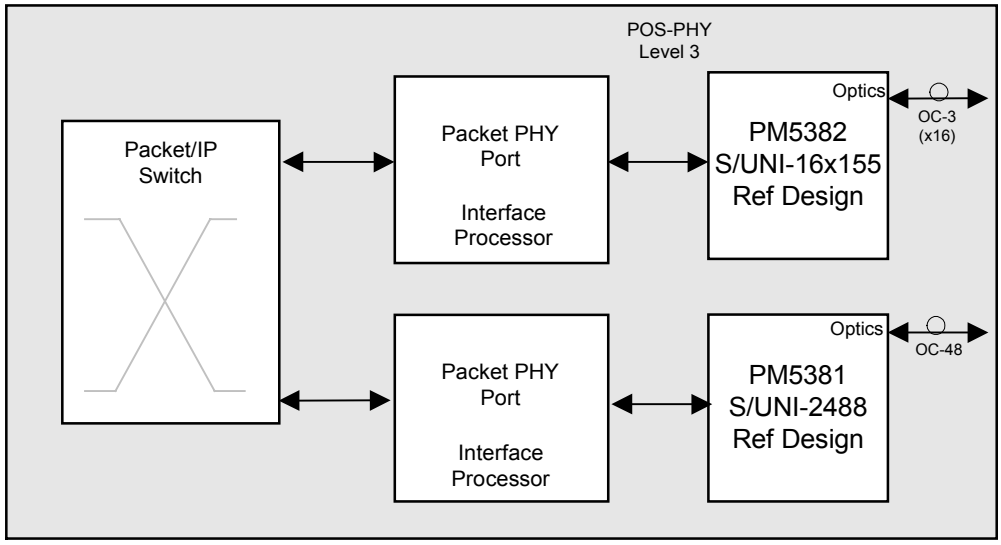
Figure 10: Ref Design with other ATM Chipsets



2.8 Reference Design with Packet Switch

This reference board may potentially be used within a larger system utilizing packet switch and link layer processors as shown below.

Figure 11: Ref Design with POS Link Layer Device



3 REFERENCES

1. ATM Forum - STR-PHY-UL3-01.00, “UTOPIA Level 3”, July 1999.

2. Bell Communication Research – SONET Transport Systems: Common Generic Criteria, GR-253-CORE, Issue 2, December 1995.

3. CompactPCI™ specification, PICMG 2.0 R2.1, September 2, 1997.

4. PMC-Sierra, Inc., PMC-200-0495 “PM5382 S/UNI-16x155 Data Sheet”, Issue 1,.September, 2000.

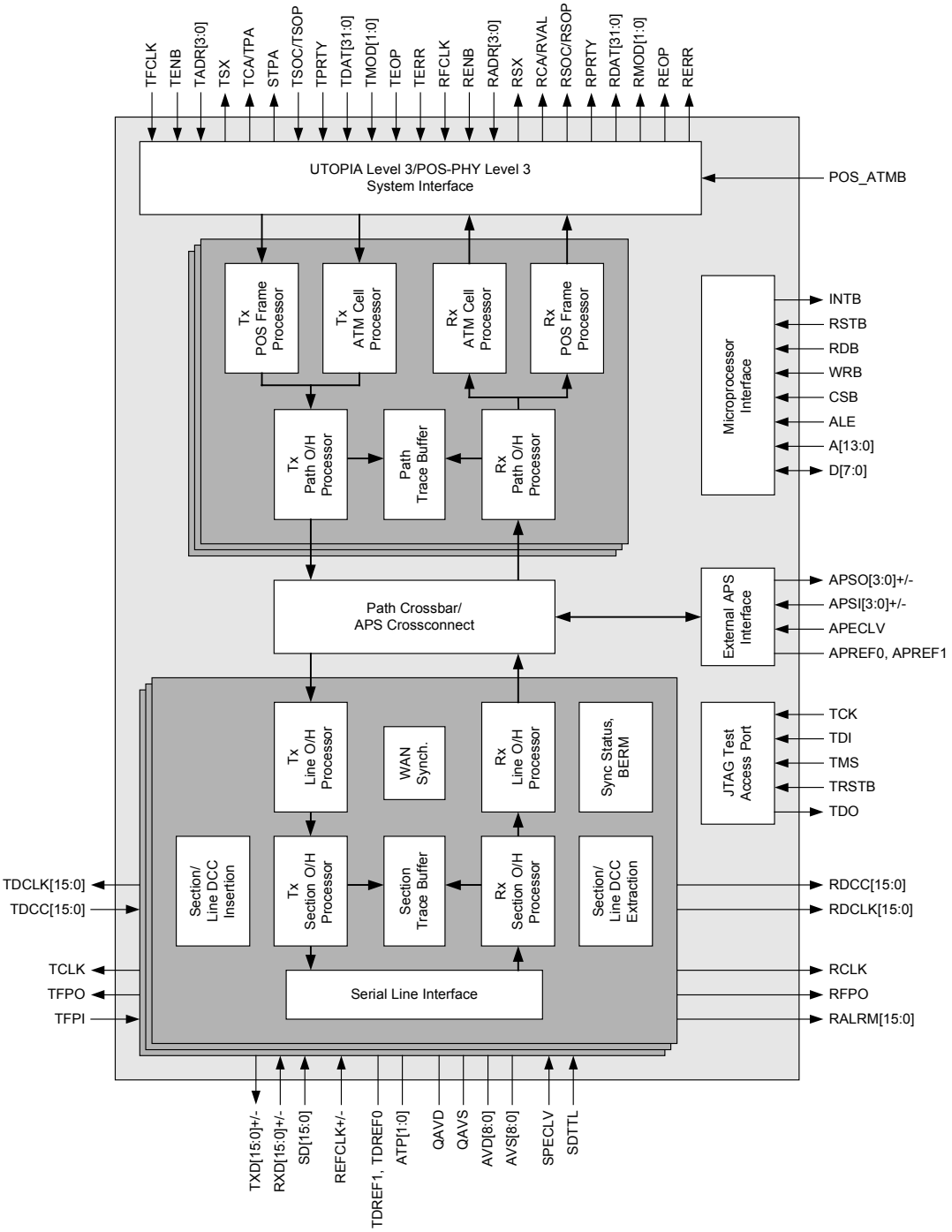
5. PMC-Sierra, Inc., PMC-200-0056 “PM5358 S/UNI-4X622 Data Sheet”, Issue 1, January 5, 2000.

6. PMC-Sierra, Inc., PMC-200-0539 “Integrating Board Designs Using the S/UNI-16x155 and S/UNI-4x622”, Issue 1, April 2000.

7. PMC-Sierra, Inc., PMC-980495 “POS-PHY Level 3”, Issue 4, November 1999.

4 DEVICE BLOCK DIAGRAM

Figure 12: S/UNI-16X155 Block Diagram

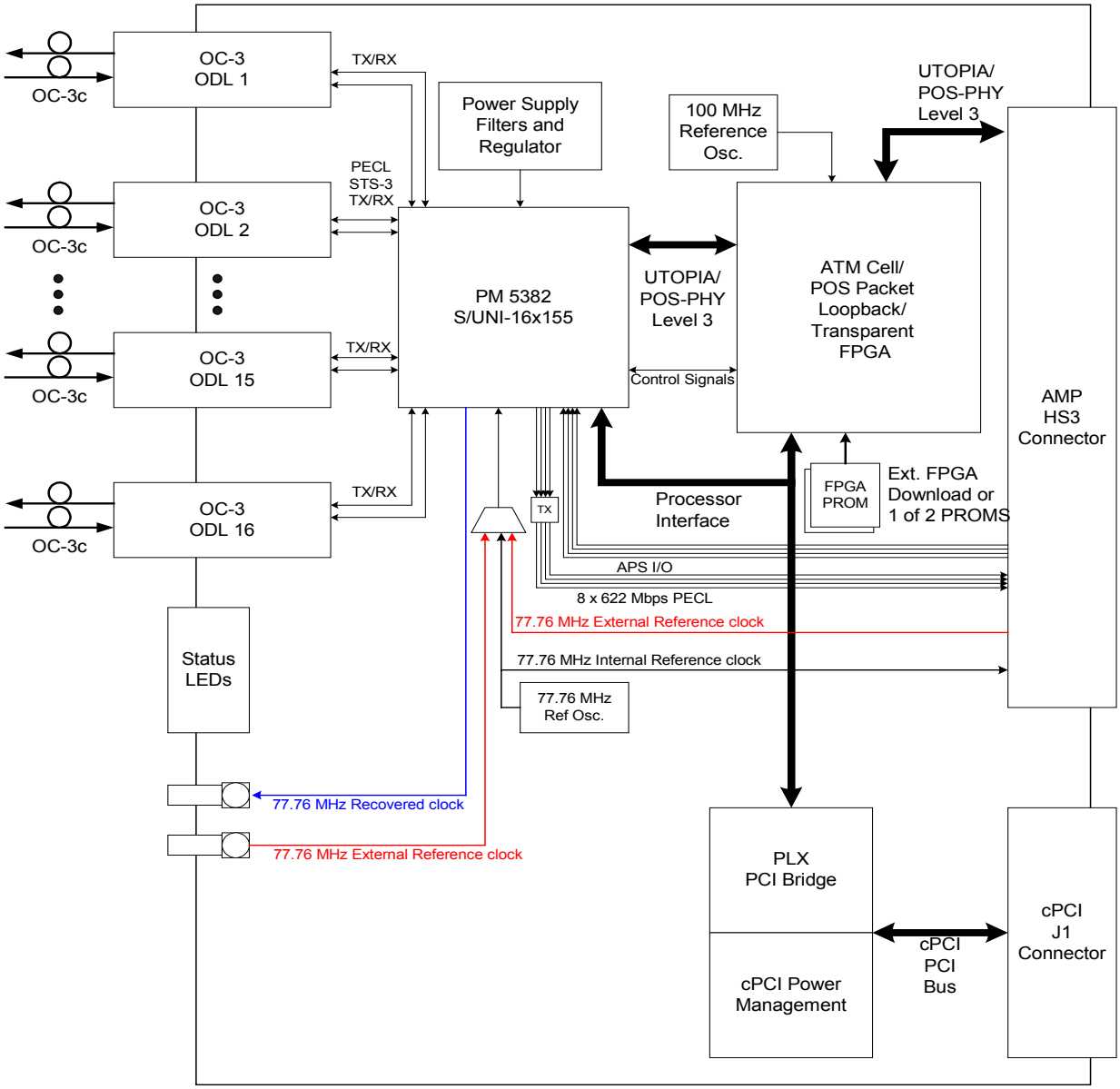


5 REFERENCE DESIGN FUNCTIONAL DESCRIPTION

5.1 BLOCK DIAGRAM

This figure depicts the major functional blocks of the Reference Design.

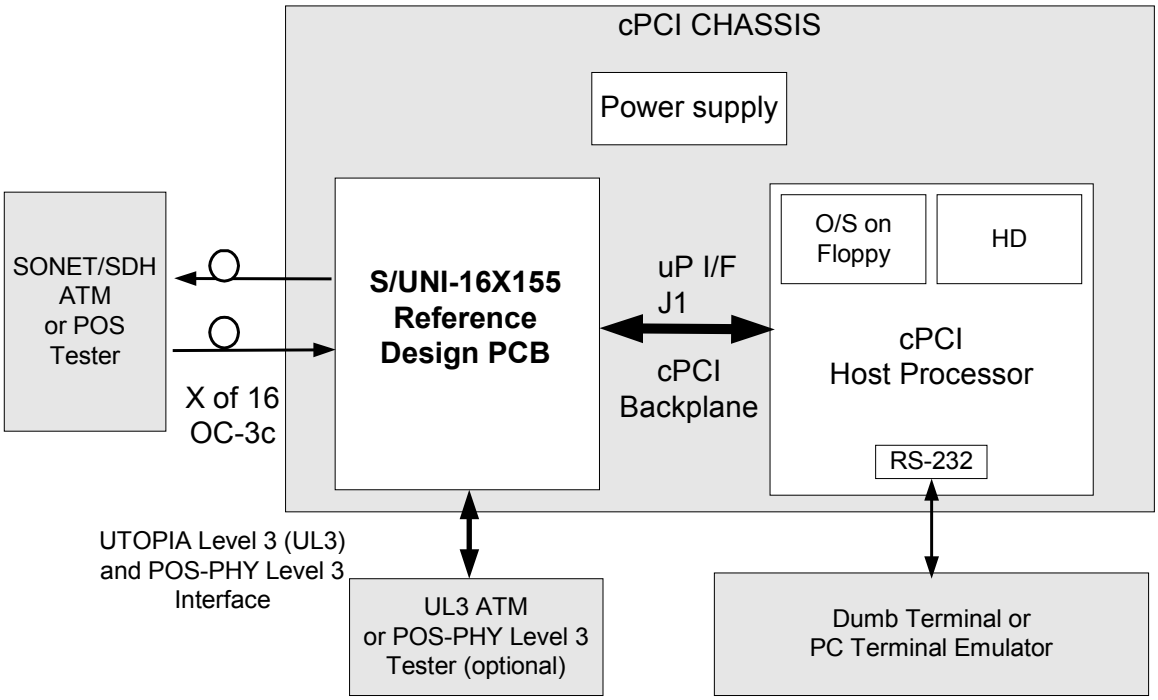
Figure 13: Reference Design Block Diagram



6 SYSTEM FUNCTIONAL DESCRIPTION

This Reference Design conforms to cPCI standards and implements a cPCI interface for configuration and control. A minimal implementation of the system is composed of a cPCI chassis, the S/UNI-16x155 Reference Design PCB, Pentium PCI board with operating system SW, and an external PC with terminal emulation software. In addition, an external SONET ATM and/or POS tester is required to generate and receive ATM or POS data to/from the S/UNI-16X155 framer.

Figure 14: SYSTEM LEVEL BLOCK Diagram



7 IMPLEMENTATION DESCRIPTION

7.1 ROOT DRAWING, Sheet 1

This sheet provides an overview of the major functional blocks of the S/UNI-16x155 reference design. The schematic was designed in a hierarchical format. The interconnections between the top level SUNI_BLOCK, FPGA BLOCK, SYS_INTERFACE, POWER_BLOCK, CPCI_BLOCK, and OPTICS_CARD are identified on the Root sheet, and labeled with a "\I" designation on all subsequent sheets.

7.2 SUNI BLOCK Sheet 2

7.2.1 Optical Transceiver Interfaces

The S/UNI-16x155 Reference Design is based on a 9U form factor CPCI card and uses Small Form Factor (SFF) ODL modules that adhere to the Multiple Source Agreement (MSA) standard 2 x 5 pinout. Vendors supplying MSA-compliant ODLs include: AMP, Methode, MRV, Infineon, or Agilent Technologies (Hewlett Packard).

7.3 S/UNI BLOCK, Sheet 2

Sheet 2 shows the circuits for the optical modules for channels 0-4 and channel 7 on the S/UNI-16x155. All of the transmitted data (TXD) and received data (RXD) signals on this sheet are routed with controlled impedance 50 ohm transmission lines. Each differential pair is length matched.

A minimum of passive components are required to interface the S/UNI-16x155 PECL I/Os to the optical tranceivers. Figure 15 and Figure 16 below outline the recommended terminations for 3.3V and 5V devices respectively. Note that the RXD+/- signals are internally terminated with a 100 ohm resistor. The SPECLV input is used to configure the PECL inputs to 3.3V or 5V tolerance. The SDTTL input is used to configure the Signal Detect inputs to accept either PECL or TTL input levels.

The TXD+/- outputs are AC coupled so the ECL inputs of the optical module are free to swing around the ECL bias voltage (VBB). Generally the bias voltage is set 1.3V below the supply voltage. The bias voltage can be generated using a resistor divider (shown in Figure 17).

The TXD+/- outputs on the S/UNI-16x155 swing approximately 3.3V and require the combination of the series source resistor and the termination resistors to divide the output voltage down to a nominal 800mV swing. The series resistor attenuates the signal and dampens any signal reflections from the optics module. For calculations, the source impedance of the TXD+/- outputs is between 15 and 20 ohms.

Vias should be avoided on the signal path between the optical module and the S/UNI-16x155 as they can affect the jitter performance of the interface. Vias may be used for the termination networks.

Figure 15: Interfacing the S/UNI-16x155 to 3.3V Optics.

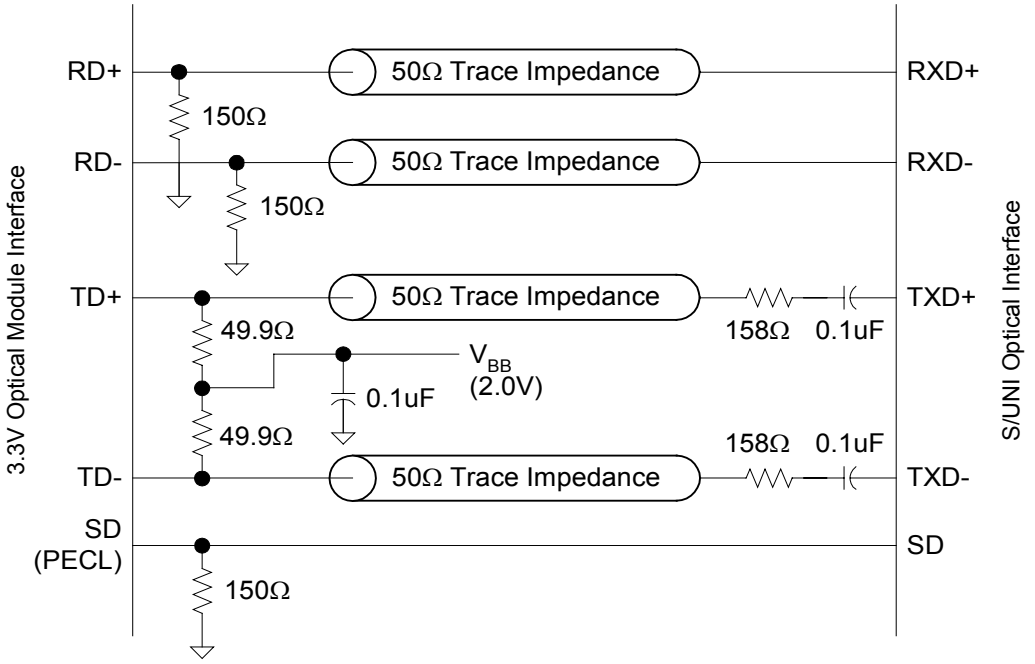


Figure 16: Interfacing the S/UNI-16x155 to 5V Optics.

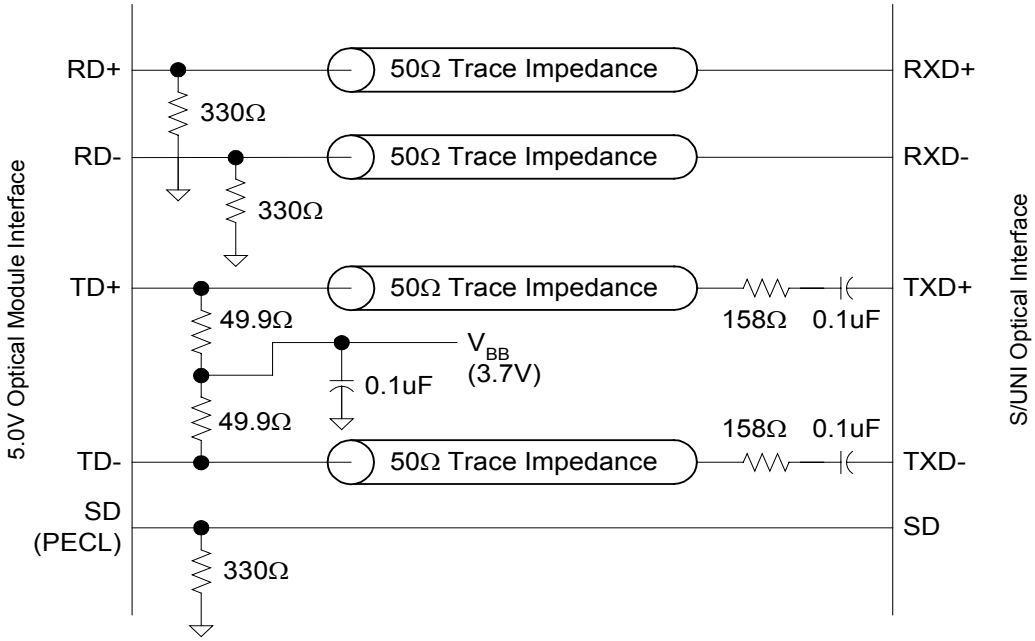
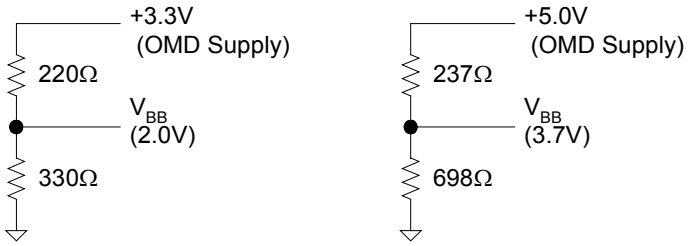


Figure 17: ECL Bias Voltage Circuits.



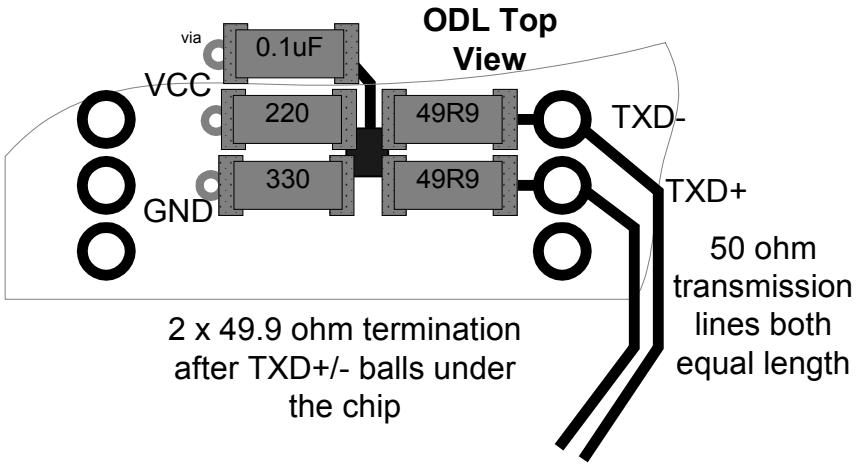
The bias voltage circuits can be shared between optical modules to reduce component count. Ensure that the divider is well decoupled and connected in a star configuration to the termination networks. Other configurations may cause data dependent jitter to be coupled between the optical modules.

On the S/UNI-16x155 Reference Design, the resistor dividers are shared between the following modules:

- Channel 0, 1, 2 and 15.
- Channel 3, 4 and 5.
- Channel 6, 7 and 8.
- Channel 9, 10 and 11.
- Channel 12, 13 and 14.

Figure 18 below outlines the termination component layout of the S/UNI-16x155 reference design optical modules. Placing the termination components on the solder side of the board after the pins reduces the effects of transmission line stubs and improves signal quality.

Figure 18: OC-3 Optical Transceiver Termination Layout



The ODL power supplies are filtered as recommended by the manufacturer. The TX and RX supplies are filtered with a 1µH series coil, and a 0.1µF ceramic cap.

If the power supply is 'noisy', greater than 100mVp-p, additional filtering may be required.

The 3.3V supply for the optical modules is provided by a DATEL UNR3V5 8 Amp DC/DC converter to reduce the current load on the cPCI 3.3V rails. The S/UNI-16x155 reference design will require 4.7A worst case and 3.2A nominal for the 16 optical module power supplies.

7.4 S/UNI BLOCK Sheet 3

Sheet three shows the optical module connections for channels 5, 6, 9, and 14. It also provides an extra optical module that is populated only in S/UNI-4x622 applications. An additional optical module is required as the S/UNI-4x622 channel 2 PECL transmit pins are shared with the S/UNI-16x155 channel 5 receive pins and the S/UNI-4x622 channel 2 receive pins are shared with the S/UNI-16x155 channel 6 transmit pins. Because the transmit and receive pins are not common signals on the two devices an extra optical module footprint was added and can be populated in S/UNI-4x622 applications. See Section 8 and application note PMC-2000539 for additional details on the S/UNI-4x622 assembly option of the S/UNI-16x155 reference design.

7.5 S/UNI BLOCK Sheet 4

Sheet four shows the connections for the remaining optical channels 8, 10, 11, 12, 13 and 15.

7.6 SUNI BLOCK, Sheet 5

7.6.1 UTOPIA/POS-PHY Level 3 Interface

The PM5382 supports a 32 bit 104 MHz UTOPIA Level 3 interface while operating in ATM mode. During POS (Packet Over SONET) operation, the PM5382 provides a 32 bit 104 MHz POS-PHY Level 3 interface.

In this reference design, output signals from the PM5382 are source terminated with a 33 ohm resistor. The series source terminations eliminate reflections from the high impedance, far end of the trace. No end terminations are used. All connections are made with short 50Ω traces.

7.6.2 APS Interface

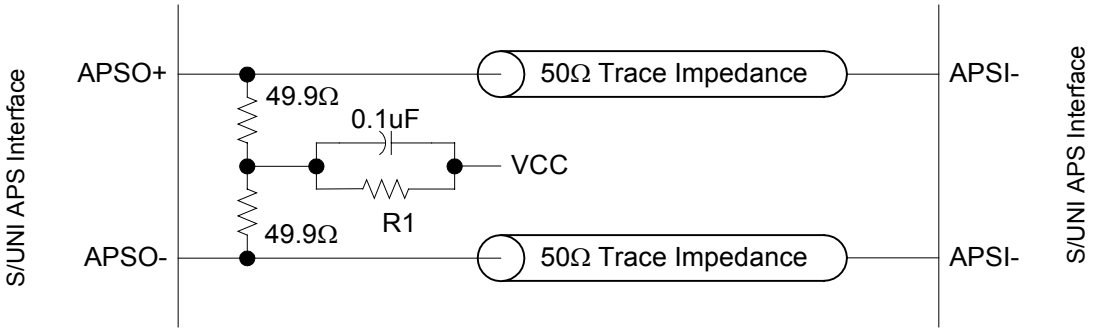
The APS interface on the S/UNI-16x155 allows two devices to exchange SONET/SDH path data streams. The transmit interface generates a SONET/SDH serial data stream with valid section and path overheads. The receive interface accepts a SONET/SDH serial data stream with valid section and path overheads ignoring all line overhead information. This allows performance monitoring and alarm generation to be done in a similar manner to the serial line side interfaces.

The APS serial interface and the REFCLK input operate similarly to the optical interfaces, except that they run at 622.08MHz. The APECLV input controls the ECL levels for all of the APS pins. Figure 19, and Figure 20 outline the recommended termination configurations. For interfaces with trace lengths less than 4cm in length, no buffering is required as shown in Figure 19. These traces are double terminated at both source and sink, so the APREF resistor should be set to 1KΩ. For traces of longer length, running over a backplane for instance, an ECL buffer should be used to ensure proper signal levels at the APSI+/- inputs with minimum undershoot or overshoot. For these single ended terminations the APREF resistor should be set to 2KΩ.

The S/UNI-16x155 reference design routes the APS outputs to the backplane connector and sources the APS inputs from the backplane. The terminations are single ended with an MC100LVEL17 differential receiver to drive the APSO+/- signals.

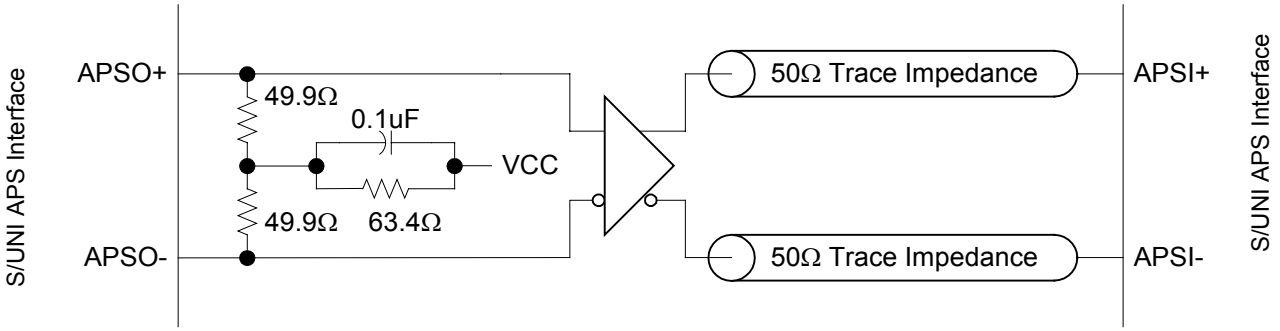
All APSO+/- and APSI+/- traces are routed using 50 ohm controlled impedance traces and each differential pair should be length matched.

Figure 19: Double Ended APS Terminations



For VCC = 3.3V, R1 should be 19.2Ω. For VCC=5V R1 should be 63.4Ω.

Figure 20 Single Ended APS Terminations



7.7 S/UNI Block, Sheet 6

7.7.1 Microprocessor Interface

The PM5382 supports an 8 bit microprocessor interface that can be accessed by either a local microprocessor, or a remote host processor. Access to the entire register set of the S/UNI-16x155 requires a 12 bit address range of 0x0000-0x11FF. A13 is used to select the test mode registers.

Separate busses for address and data or a multiplexed address/data bus configuration may be used, as the device contains an internal address latch. When separate busses are used, the ALE (Address Latch Enable) pin should be tied high through a resistor.

This reference design uses separate address and data busses that are driven by the PCI9054 cPCI bridge. The FPGA implements glue logic to generate proper control signals to interface to the PM5382 micro interface. More details regarding the cPCI controller may be found in Section 7.13.1, CPCI Interface Controller.

7.7.2 JTAG Interface

The PM5382 also supports JTAG functionality for boundary scan. The JTAG functionality is not used in this reference design, but the JTAG pins are brought out to a header so that they can be accessed easily. When the JTAG pins are not used, the inputs should be tied high through a resistor. The TRSTB signal should be tied to the RSTB signal.

7.7.3 Receive Alarm Outputs

The PM5382 provides one receive alarm output per channel. Each of these signals can be configured to indicate multiple alarm conditions. These alarm conditions are fully described in the S/UNI-16x155 Data Sheet.

In this reference design, the 16 receive alarm signals are routed to the FPGA and their status can be read in register 0x2400, the S/UNI RALRM Register.

7.7.4 Clocks

The PM5382 makes the recovered Receive Clock and outgoing Transmit Clock signals available for any one channel, as selected by Register 0x2200 – S/UNI Clock Control Register.

In this reference design, the Recovered Clock (RCLK) signal is padded to a level of 1 Volt peak to peak into 50Ω, and is brought to the front panel for distribution to an external clocking card. All other signals are brought to test points. The TFPI pin is an input pin, and needs to be pulled low when not in use.

7.7.5 Section and Line Status DCC Signals

The PM5382 provides access to both the Section data communications channel (DCC) signals as well as the Line DCC signals for all 16 channels. When configured for section DCC, the RDCC output is the extracted section DCC bytes, D1, D2, D3. The TDCC inputs can be used to insert section DCC bytes D1, D2, D3 into the data stream. In line DCC mode, RDCC outputs the line DCC bytes D4 to D12. Similarly, the TDCC inputs can be used to insert the line DCC bytes D4 to D12.

These signals are not used in this reference design, but are brought out to a SAMTEC QSE matched impedance connector for optional external access. The TDCC pins should be pulled low when not in use.

7.8 S/UNI Block, Sheet 7

7.8.1 Power Supply Filter and Regulator Sheet

This sheet shows all power supply filtering and regulation components required for PM5382 operation. The PM5382 requires 4 different voltage sources for operation.

- +3.3 Volt I/O Digital Power (VDD)
  +3.3V Digital I/O power is supplied via the cPCI bus interface. VDD is well decoupled to ground, VSS.

- +2.5 Volt Core Digital Power (VDDI)
  +2.5 Digital Core power is regulated from the +3.3 Volt supply provided by the cPCI bus interface. VDDI is well decoupled to ground.

  A National Semiconductor LP3965ES-2.5 fixed linear regulator is used to regulate the ~1.6 A of current required for the S/UNI-16x155 core supply. The regulator will use the PCB as a heatsink, allowing it remain at a safe operating temperature. This device was selected for its exceptionally low dropout voltage, and low thermal resistance.

- +3.3 Volt Analog Power (AVD)
  +3.3 Volt Analog power is supplied via the cPCI interface. Digital and Analog 3.3V supplies are split as soon as power leaves the Hot Swap Controller and are routed separately. AVD is well decoupled to ground, and filtered with a combination of resistors and capacitors.

- +3.3 Volt Quiet Analog Power (QAVD)
  As little (no) current is drawn on this supply line, it is filtered passively. QAVD is decoupled to ground.

Analog circuitry responsible for clock and data recovery must be free of noise to ensure reliable operation. Less sensitive analog power pins are grouped together and filtered with a single 0.1 µF capacitor. The more sensitive analog power pins of the S/UNI-16x155 are filtered using a low pass RC circuit. If there is a lot of power supply noise, >100mVp-p in the 3.3V rail, and a 5V supply is available, then a linear regulator approach is recommended.

7.8.2 Passive RC Low Pass Power Supply Filter

If there is no 5V supply available and the 3.3V supply is not very noisy (less than 100mVp-p at all frequencies), passively filtering the analog supply is acceptable. Several capacitors may be paralleled to achieve the filtering across the desired frequency band. The 10µF capacitors should be X5R ceramics and not Tantalum. A 0.1µF X5R or X7R is used for high frequency noise reduction. The reference design uses this passive filter method.

The X5R type capacitors have excellent low and high frequency response as seen in the graph below. The lower the impedance is, the better the capacitor for filtering. The X5R capacitors are similar to X7R except the high temperature spec is +85°C instead of 125°C for the X7R. These X5R ceramics are available up to 10µF at 6.3 Volts. Taiyo Yuden is a quality source for these passive devices.

Figure 21: Tantalum & X5R Ceramic Cap Impedance vs. Frequency

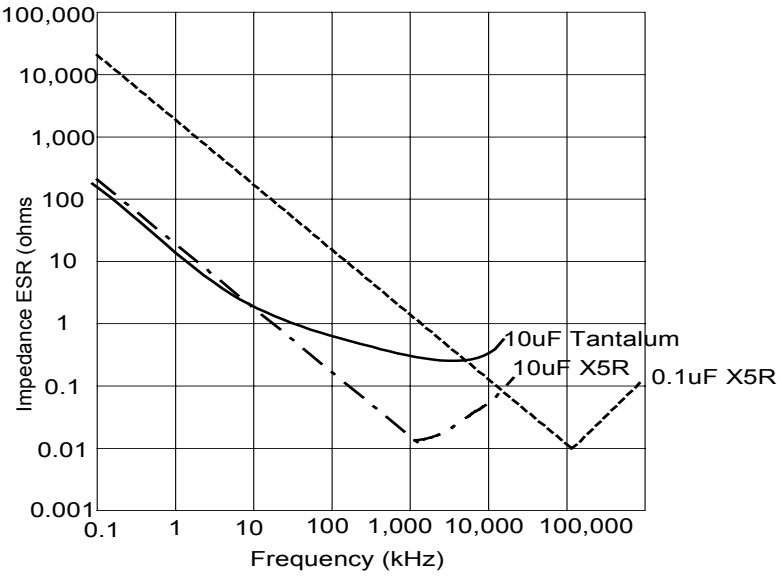
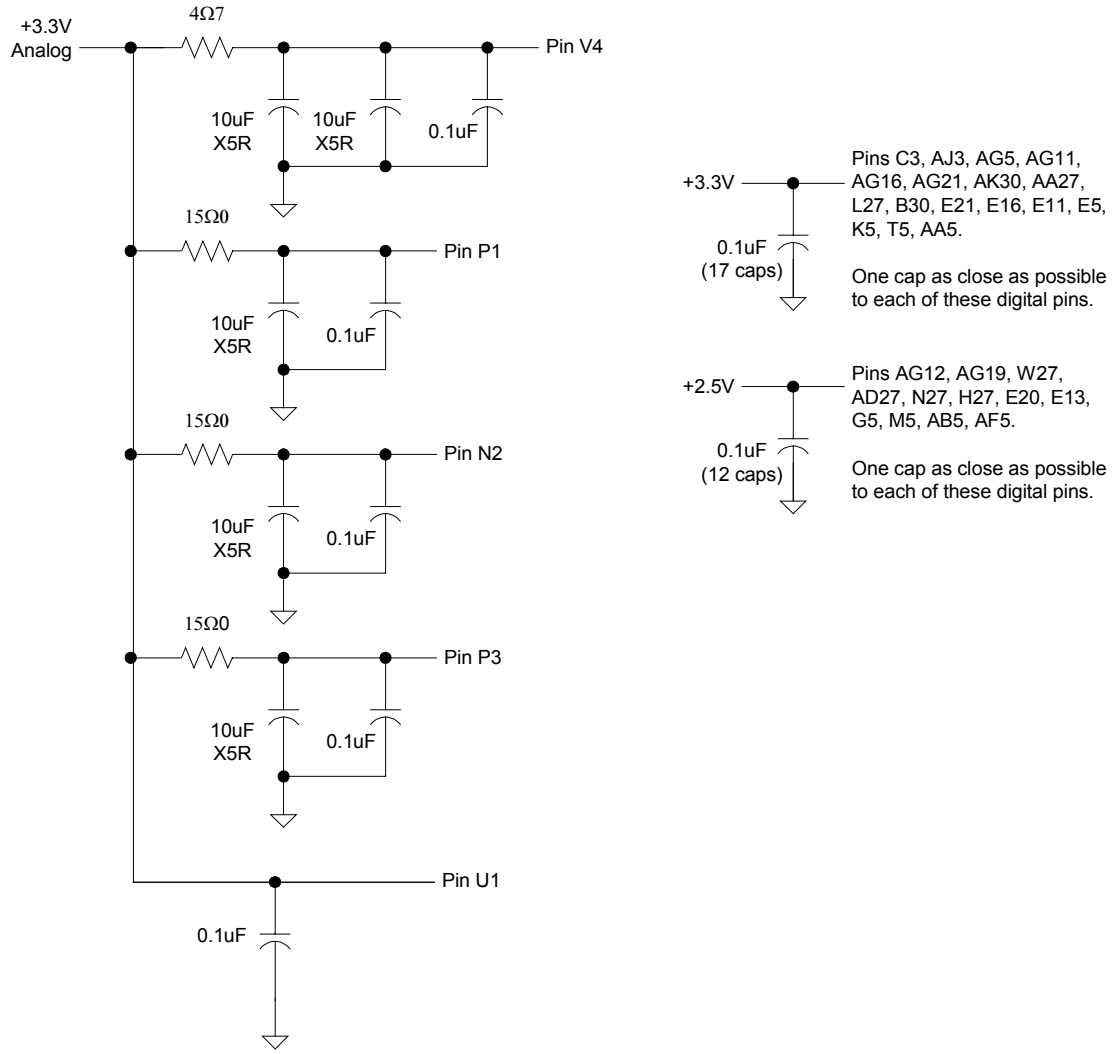


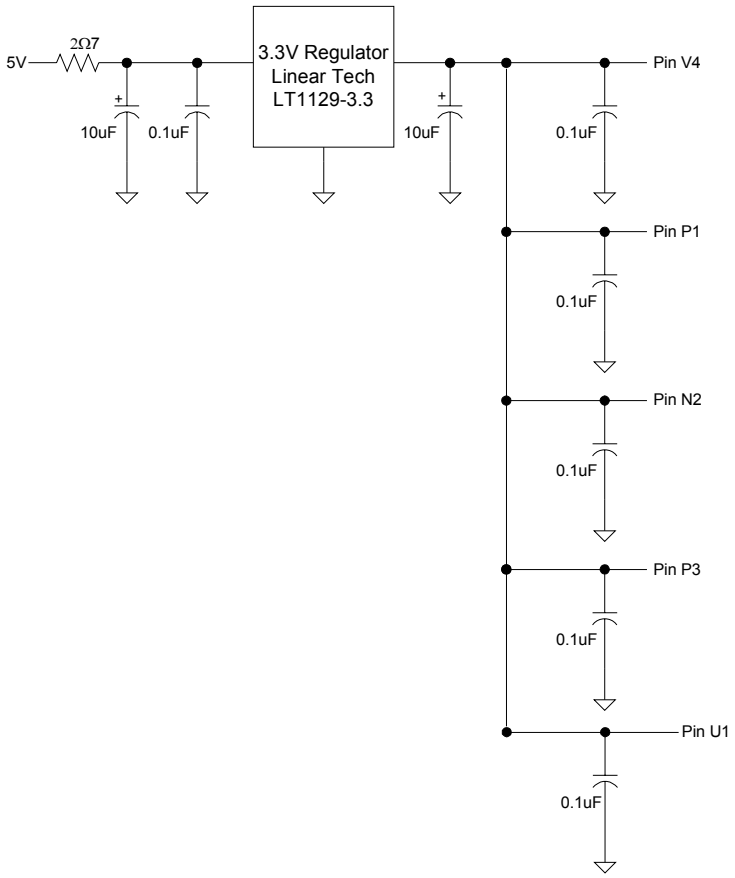
Figure 22: Passive RC Power Supply Filtering



7.8.3 Linear Regulator Filter Method

If a 5V supply is available, and the 3.3V supply is noisy, (>100mVp-p), a low dropout linear regulator can be used to generate the analog supply. Further noise attenuation is achieved with a front end RC pre-filter (2.7 ohm + 10 µF) and a high frequency 0.1µF ceramic at the input to the regulator. A 10 µF Tantalum is required at the output for regulator stability.

Figure 23: Linear Regulator Analog Power Supply Filtering



7.9 FPGA Block , Sheet 8

The FPGA supports a number of functions on the S/UNI-16x155 Reference Design. These include:

- ATM (UL3) or POS (PL3) system side loopback.
- Reset Logic.
- Clock mode selection.
- LED control for status monitoring.

As two full UL3/PL3 interfaces are implemented on the FPGA to allow for loopback, cell/packet processing, and transparent interfacing to the system side, the FPGA requires a very high number of I/Os. This reference design uses a Xilinx Virtex-E FPGA. The XCV200E-6BG352 provides up to 260 I/Os in a low power 1.8V and 3.3V 352 pin BGA package. This device supports UL3 and PL3 cores to reduce FPGA development time and simplify design.

Table 1 below outlines the distribution of I/Os on the device.

Table 1: FPGA Pin Assignment

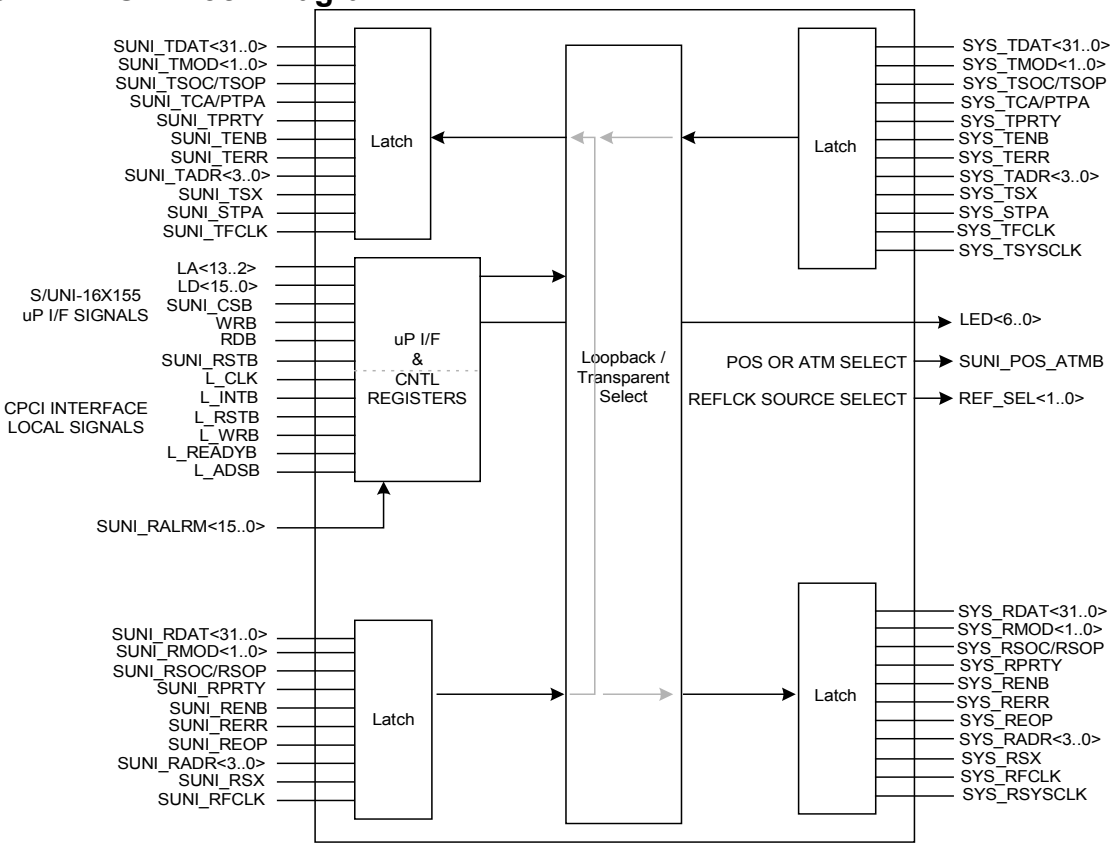
Signal group	No. of pins	Function
S/UNI-16x155 UL./PL3 I/F	42 TX, 42 RX. 84 Total.	UTOPIA/POS-PHY Level 3 data bus + control signals
SYS UL./PL3 I/F	42 TX, 42 RX. 84 Total.	UTOPIA/POS-PHY Level 3 data bus + control signals
Host I/F	44 I/O pins	16 data lines, 14 address lines, 14 chip select and control lines.
On-board control	2 I/O pins 2 I/O pins 1 I/O pins 16 I/O pins	Recovered Clock Multiplexer control Reference Clock Multiplexer control POS/ATM Select Alarm Signals
Status LEDs	8 I/O pins	Control 8 LED display on front panel

Additional ‘glue-logic’ functions such as address decoding is implemented in the FPGA.

All unused I/O pins are routed to test points.

Figure 24 below shows a block diagram of the FPGA architecture used on the S/UNI-16x155 Reference Design.

Figure 24: FPGA Block Diagram



7.9.1 Control Register Function

The S/UNI-16x155 FPGA functionality is controlled via the S/UNI Control Register. The register functions are outlined below.

Register 0x2000H: S/UNI Control Register

Bit	Type	Function	Default
Bit 15	R/W	RESET	0
Bit 14	R/W	POS_ATMB	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5		Unused	X
Bit 4		Unused	X
Bit 3	R/W	TXENA	0
Bit 2	R/W	RXENA	0
Bit 1	R/W	XPRNT_ENA	0
Bit 0	R/W	LPBK_ENA	1

Bits 0 and 1 configure the loopback/transparent functionality of the FPGA. The following combinations are valid.

- 0x01: LPBK_ENA. The receive bus (either UTOPIA or POS-PHY Level 3, depending on state of POS_ATMB bit) is looped back to the S/UNI-16x155 transmit interface.
- 0x10: XPRNT_ENA. The FPGA passes the RX and TX interfaces transparently to/from the backplane connector.
- 0x11: Loop and Pass. In this mode the Receive data will be looped back to the TX inputs and passed to the backplane connector.
- 0x00: Not used. Could be used to implement cell/packet generation or processing functionality as desired.

RXENA:

RXENA is used to enable the receive UL3/PL3 interface. Setting this bit to a 1 enables the interface.

TXENA:

TXENA is used to enable the transmit UL3/PL3 interface. Setting this bit to a 1 enables the interface.

POS_ATMB:

The POS_ATMB bit is used to select the operating mode of the S/UNI-16x155. Setting this bit to a 1 selects POS mode for Packet transfer via the POS-PHY Level 3 interface. Setting this bit to a 0 selects ATM mode for ATM cell transfer via the UTOPIA Level 3 interface.

RESET:

Global soft reset. Setting this bit to a 1 resets the S/UNI-16x155. RESET does not clear automatically. When set, the device is held in reset. To clear the reset condition the user must clear the RESET bit.

Register 0x2200H: S/UNI Clock Control Register

Bit	Type	Function	Default
Bit 15	R/W	REF_SEL1	0
Bit 14	R/W	REF_SEL0	0
Bit 13		Unused	X
Bit 12		Unused	X
Bit 11		Unused	X
Bit 10		Unused	X
Bit 9		Unused	X
Bit 8		Unused	X
Bit 7		Unused	X
Bit 6		Unused	X
Bit 5	R/W	SYRFSRC	0
Bit 4	R/W	SYTFSRC	0
Bit 3	R/W	SRFSRC	0
Bit 2	R/W	STFSRC	0
Bit 1	R/W	FRFSRC	0
Bit 0	R/W	FTFSRC	1

FTFSRC:

The FTFSRC bit selects the clock source for the FPGA UL3/PL3 S/UNI side transmit interface. Setting this bit to a 0 selects the FPGA_TFCLK1 source generated by the on board 100MHz oscillator. Setting this bit to a 1 selects the SYS_TFCLK source from the backplane connector.

FRFSRC:

The FRFSRC bit selects the clocks source for the FPGA UL3/PL3 S/UNI side receive interface. Setting this bit to a 0 selects the FPGA_RFCLK1 source generated by the on board 100MHz oscillator. Setting this bit to a 1 selects the SYS_RFCLK source from the backplane connector.

STFSRC:

The STFSRC bit selects the source of the SUNI_F_TFCLK output. This output can be routed via solder bridge SB2 to provide the SUNI_TFCLK input to the transmit UL3/PL3 interface on the PM5382. Setting this bit to a 0 selects the

FPGA_TFCLK1 source generated by the on board 100MHz oscillator. Setting this bit to a 1 selects the SYS_RFCLK source from the backplane connector.

SRFSRC:

The SRFSRC bit selects the source of the SUNI_F_RFCLK output. This output can be routed via solder bridge SB3 to provide the SUNI_RFCLK input to the receive UL3/PL3 interface on the PM5382. Setting this bit to a 0 selects the FPGA_RFCLK1 source generated by the on board 100MHz oscillator. Setting this bit to a 1 selects the SYS_RFCLK source from the backplane connector.

SYTFSRC:

The SYTFSRC bit selects the clock source for the FPGA UL3/PL3 system side transmit interface. Setting this bit to a 0 selects the FPGA_TFCLK1 source generated by the on board 100MHz oscillator. Setting this bit to a 1 selects the SYS_TFCLK source from the backplane connector.

SYRFSRC:

The SYRFSRC bit selects the clocks source for the FPGA UL3/PL3 receive interfaces. Setting this bit to a 0 selects the FPGA_RFCLK1 source generated by the on board 100MHz oscillator. Setting this bit to a 1 selects the SYS_RFCLK source from the backplane connector.

REF_SEL<1..0>:

The REF_SEL bits are used to select between three sources for the 77.76MHz reference clock input to the S/UNI-16x155.

- 0x00: Reference clock source from backplane connector.
- 0x01: External clock source via SMB connector.
- 0x10: On board 77.76MHz PECL oscillator. This signal is also routed to the SYS_REF_OUT signal on the backplane connector.

Register 0x2400H: S/UNI RALRM Register

Bit	Type	Function	Default
Bit 15	R	RALRM15	0
Bit 14	R	RALRM14	0
Bit 13	R	RALRM13	0
Bit 12	R	RALRM12	0
Bit 11	R	RALRM11	0
Bit 10	R	RALRM10	0
Bit 9	R	RALRM9	0
Bit 8	R	RALRM8	0
Bit 7	R	RALRM7	0
Bit 6	R	RALRM6	0
Bit 5	R	RALRM5	0
Bit 4	R	RALRM4	0
Bit 3	R	RALRM3	0
Bit 2	R	RALRM2	0
Bit 1	R	RALRM1	0
Bit 0	R	RALRM0	0

The S/UNI RALRM register indicates the current value of the receive alarm signals associated with each channel on the S/UNI-16x155. If no alarms are active the RALRM signal will be low. RALRM is can be configured to go high if various conditions are present on the channel. Please refer to the S/UNI-16x155 datasheet PMC-2000495 for further information on RALRM function.

Register 0x2600H: LED Register

Bit	Type	Function	Default
Bit 15	R	Reserved	0
Bit 14	R	Reserved	0
Bit 13	R	Reserved	0
Bit 12	R	Reserved	0
Bit 11	R	Reserved	0
Bit 10	R	Reserved	0
Bit 9	R	Reserved	0
Bit 8	R	Reserved	0
Bit 7	R	Reserved	0
Bit 6	R	Reserved	0
Bit 5	R	Reserved	0
Bit 4	R/W	LED_REG4	0
Bit 3	R/W	LED_REG3	0
Bit 2	R/W	LED_REG2	0
Bit 1	R/W	LED_REG1	0
Bit 0	R/W	LED_REG0	0

The LED Register provides software control over the front panel LEDs on the S/UNI-16x155 Reference Design.

7.9.2 ATM Loop-back Logic

In ATM Loop-back mode, the FPGA polls the PM5382 to determine which PHYs have cells ready for transfer. The PM5382 RX interface is polled by placing addresses on the RxAddr<3..0> lines and monitoring the response on RCA.

Once a particular PHY has been determined to have a complete ATM cell in its RX FIFO, data is clocked out of PM5382, latched, and simultaneously clocked into the PM5382 TX FIFO. No TX FIFO flow control is performed, but would require logic similar to RX polling.

(TX polling would be used to identify all PHYs capable of accepting at least one cell. Prior to the initiation of a transfer from the RX FIFO, the status of the TX

FIFO would be verified. If the TX FIFO couldn't accept the RX cell, the RX logic would 'skip' the 'blocked' PHY and continue polling for the next available PHY.)

Once the transfer of cell data has been initiated, the FPGA will poll to determine if any other PHYs have cells ready for transfer. If another PHY is found to have a complete cell in its RX FIFO before the end of the current transfer, that cell will be transferred to the appropriate TX FIFO as soon as the current transfer is finished. If no other PHYs have complete cells ready, the FPGA will sequentially poll all PHYs until a complete cell is available.

7.9.3 POS Loopback Logic

In POS Loop-back mode, the PM5382 initiates the transfers from the RX FIFO. The user can enable the receive side transfer by setting the RXENA bit in the S/UNI Control Register. Setting this bit will assert the RENB signal on the PM5382 PL3 interface. Transfers will begin with the PM5382 specifying the PHY for which the transfer is occurring. The FPGA will latch the PHY address, and clock it into the PM5382 TX interface one clock cycle later. The FPGA will subsequently latch each double word of packet data from the RX interface, and clock it into the PM5382 TX interface one clock cycle later. The user also has control over the state of the TX interface via the TXENA bit in the S/UNI Control Register.

7.9.4 ATM and POS Transparent

When set to Transparent Mode in either ATM or POS mode, the FPGA latches the bus signals from the S/UNI-16x155 RX interface and system TX interface and clocks them out to the system RX interface and S/UNI-16x155 TX interface respectively, on the following clock cycle.

7.9.5 Processor Interface Logic

- performs address decoding, and provides chip select to S/UNI-16x155.
- handles local bus signals for PLX PCI bridge.

7.9.6 S/UNI-16x155 UL3/PL3 Interface

Each output on the UL3/PL3 (transmit) interface is source terminated with a 33 Ω resistor. On the receive side, the signals are source terminated at the PM5382 and no end terminations are used since the trace lengths between the S/UNI-16x155 and the Virtex device are relatively short.

7.9.7 Status LEDs and Reset Circuit

Sheet 8 also provides the status LEDs and the pushbutton reset circuit for the S/UNI-16x155 Reference Design. A single LED is wired to the DONE pin and will turn on after the FPGA is successfully configured. The remaining LEDs are software configurable via the LED_REG register in the FPGA. Bits 4 and 5 output the loopack or transparent functional state of the FPGA. Table 2 below outlines the function of the remaining LEDs.

Table 2: LED Display Function

Bit (D4)	Function	Bit (D3)	Function
Bit 3	LED_REG<4>	Bit 7	Done
Bit 2	LED_REG<3>	Bit 6	LED_REG<0>
Bit 1	LED_REG<2>	Bit 5	XPRNT_ENA
Bit 0	LED_REG<1>	Bit 4	LPBK_ENA

The pushbutton reset is provided via a MAX811 voltage monitor device that will assert a reset signal when the voltage supply is below 3.08V. The minimum reset pulse is 140ms. By logically ORing the RESET_PB signal with RSTOB (from the cPCI bus) and the RESET bit within the FPGA, the system reset signal (SUNI_RSTB) is generated.

A 16x2 100mil header provides access to the microprocessor interface bus for debugging purposes.

Matched impedance MICTOR connectors that have been used in past reference designs for access to the PL3 bus are not used in this design due to the constraints they put on routing and the excessive lead times of the parts themselves. No headers are provided on the board due to space contstraints, but if probing of the UL3/PL3 bus is required the user can pass all UL3/PL3 bus signals through the FPGA and probe the signals at the backplane connector (Transparent Mode). A small test jig could be built to interface to a logic analyzer if desired.

7.10 FPGA Block, Sheet 9

7.10.1 System Side UL3/PL3 Interface

Sheet 9 provides the remainder of the S/UNI UL3/PL3 interface signals and the system side UL3/PL3 interface. As on the S/UNI interface, all outputs are source terminated with 33 Ω resistors.

7.11 FPGA Block, Sheet 8

7.11.1 Configuration Circuit

The S/UNI-16x155 Reference Design FPGA can be configured in 3 ways:

- Via a One Time Programmable EPROM.
- Via an XCHECKER cable.
- Via the JTAG port.

Jumpers allow the user to select between EPROM configuration or configuration via the XCHECKER cable. By default the FPGA will download configuration information from the EPROM. To configure the device via the XCHECKER cable, install all jumpers on J4 and remove the EPROM. If the EPROM is installed and the configuration is downloaded via the XCHECKER cable, the downloaded configuration will be overwritten by the contents of the EPROM.

The JTAG port is always active and takes priority over the other configuration modes, if used.

7.11.2 Power Supply Decoupling

The Virtex family of devices are capable of operating at speeds well above 200MHz. With a number of I/Os switching simultaneously at high speeds, a stable power supply is essential to achieve good performance and signal quality. The XCV200E is part of the Virtex-E family of 0.18µ devices which uses 3.3V for I/O and 1.8V for core power. On the S/UNI-16x155 reference design the 3.3V digital supply is provided by the cPCI interface and is well decoupled to ground. The 1.8V digital supply provided via a local linear regulator is also well decoupled to ground. Based on Xilinx recommendations, eight 10uF bulk capacitors are placed near each I/O bank to further decouple the device. Finally, four bulk 0.47uF capacitors are placed at the corners.

7.12 FPGA Block, Sheet 9

7.12.1 100 MHz UL3/PL3 Clock Distribution

A 100 MHz oscillator, 100 ppm, is used for the Utopia Level 3 and POS-PHY Level 3 interface. No series termination resistor is used between the oscillator output and the input to due to the extremely short trace length.

A clock distribution driver is used to provide low skew clocks to the PM5382, the FPGA, and to the external HS3 connector. The PI49FCT3807D (the 110MHz rated FCT3807C would suffice) was selected as the clock driver as it provides up to 10 outputs with a maximum skew of 350 ps and can operate from a +3.3 Volt supply. The +3.3 Volt supply is bypassed with two capacitors to help reduce power supply glitches when all 10 outputs switch simultaneously at 100 MHz.

Each output from the FCT3807 is source terminated through a 33 Ω resistor in order to match the impedance of the 50 Ω traces distributing the clock signal. Correct termination of the clock signals is especially important to ensure monotonic, glitch-free, clocking of the S/UNI device, the FPGA, and the external system.

7.12.2 100 MHz Clock Source Switching

The clock architecture on the S/UNI-16x155 Reference Design has been developed to operate as either a clock master or a clock slave when connected to an external system. The 100MHz UL3/PL3 clock is distributed to the FPGA and the S/UNI device via solder bridges. By configuring the solder bridges to source the clock from the on board oscillator or from the FPGA, the board can operate as a clock master or clock slave.

If the external system is the clock master, The FPGA routes the TFCLK and RFCLK signals from the backplane to the S/UNI-16x155, taking advantage of the built in Delay Lock Loop architecture to improve clock performance.

7.12.3 Reference Clock Oscillator and Selection Circuitry

The PM5382 requires a 77.76 MHz Reference Clock from which to synthesize the line rate clock.

One source for this clock is an on-board oscillator. Any jitter at the S/UNI-16X155 Reference Clock input may be seen at the TXD+/- data outputs and this translates into Optical output jitter. The 3.3V Connor Winfield EE14-541, 77.7600MHz Oscillator is specified at 10ps RMS output jitter and its PECL

outputs have rise/fall times of 550ps. The Connor Winfield 5V EH13-541 is specified with much higher rise/fall times of 2.3ns max. No appreciable difference in intrinsic jitter results have been noted during testing of other reference designs using these oscillators.

In order to minimize the effects of noise on the 3.3V power supply rail, the power to the 77.76 MHz oscillator is filtered by a passive RC network. The values of this RC network are selected to provide a significant amount of noise reduction, while keeping IR loss to a minimum.

The 77.76 MHz Reference Clock used by the PM5382 is selected through a 4 Input, differential PECL multiplexer. This multiplexer selects between the following signals:

- 77.76 MHz signal from the on-board oscillator.
- 77.76 MHz external Reference Clock from front mounted coaxial input. The inverting input of the multiplexer is biased to the centre of logic switching voltage by the VBB output pin.
- 77.76 MHz external Reference Clock from the HS3 connector. The differential signal from the HS3 connector is terminated with a 100 ohm resistor across the differential inputs to the multiplexer.

The S/UNI Clock Control Register within the FPGA is used to control the selection of a Reference Clock.

Power supply filtering has been applied to the PECL Differential Multiplexer used to select the REF_CLK signal, and to the PECL Driver used to buffer the SYS_REF_OUT signal. In situations where there is an excessive amount of noise on the 3.3V supply line (greater than 100 mV peak to peak), an alternative method of providing clean 3.3V power to the reference oscillator and PECL components should be considered. A low-dropout, three terminal regulator such as the LT1117 or LP3963 could be used to provide a noise-free 3.3 Volt power supply from the +5 volt rail.

All of the REF_CLK signals are 50 ohm, differential, low-voltage PECL.

7.12.4 Recovered Clock

The 77.76 MHz recovered data clock is provided to a front mounted coaxial connector. The source of the recovered clock is selected through the RSEL[1:0} bits in register 0x2400, the S/UNI Clock Control Register.

The RCLK signal provided by the PM5382 is an LVCMOS-level signal with up to 8mA of drive current. By using a resistive pad at the output of the RCLK, the drive impedance can be changed to 50 ohm. The output signal level is decreased to a nominal level of 1 volt peak to peak.

7.13 CPCI Interface Block, Sheet 12

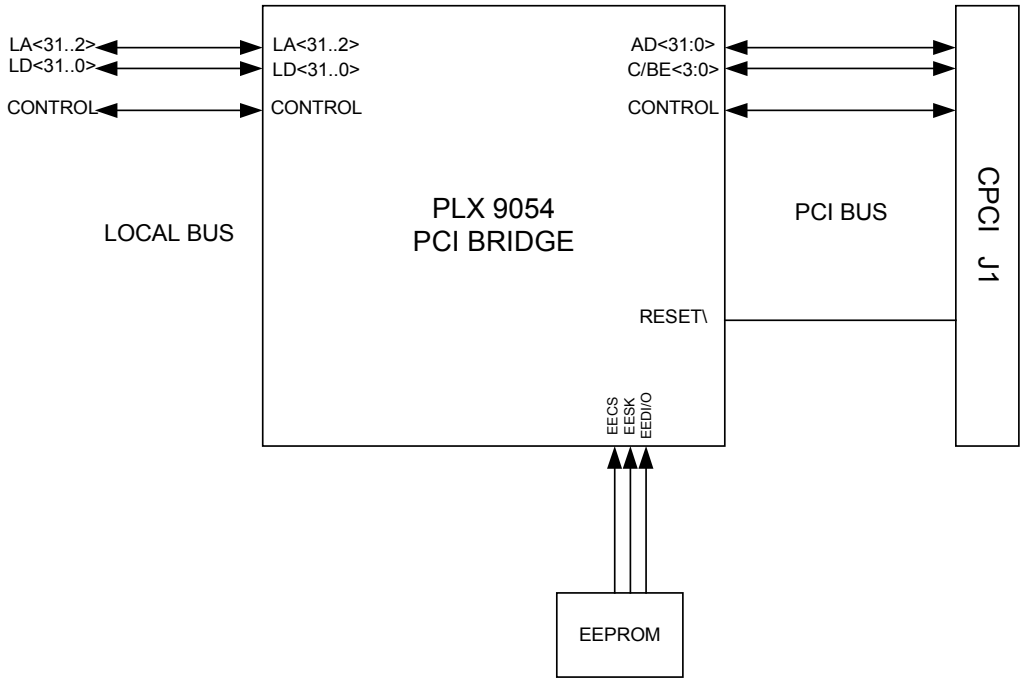
7.13.1 CPCI Interface Controller

The cPCI Host Processor Interface is based on the PCI 9054 device. This device is a 3.3V/5V compliant PCI v2.2 32-bit, 33MHz Bus Master Interface Controller, that provides flexible local bus configurations and Hot Swap capability.

The PCI 9054 operates with a 32-bit non-multiplexed bus (C-mode) on the local bus side. All bus accesses are 32 bit, so the least significant bits of the address bus (LA<0..1>) should be permanently pulled low. The 9054 provides 16 or 8 bit access using LA<0..1>, if required. This feature will not be used on the reference design.

A serial EEPROM is used for device configuration after a reset or upon power-up. This design uses the Fairchild Semiconductor 93CS66LEN (2K) serial EEPROM.

Figure 25: Host Processor cPCI Interface

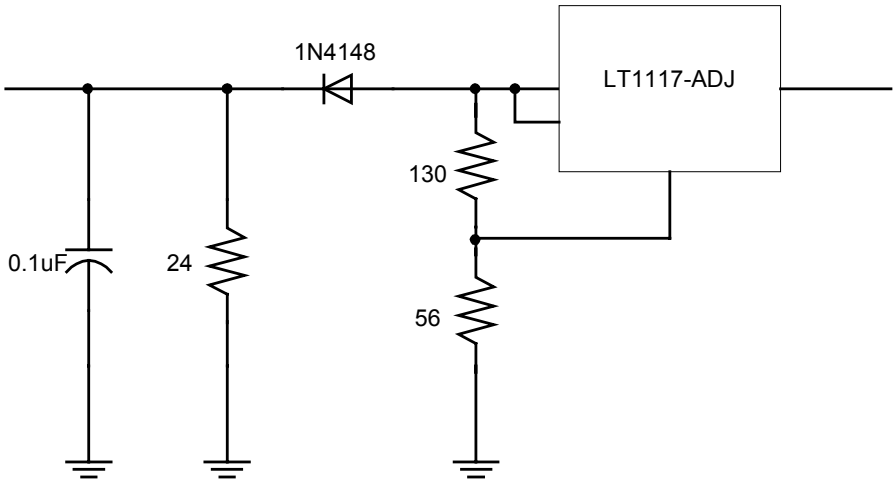


7.13.2 CPCI Bus Precharge Circuit

A Linear Technology LT1117 adjustable regulator is used to provide the potential for precharging the cPCI data bus lines.

A resistive divider is used to adjust the output of the voltage regulator to a nominal output of 1.78 Volts. The DL4148 diode will drop approximately 0.7 Volts, resulting in a precharge voltage near 1 Volt.

Figure 26: cPCI Bus Precharge Circuit



7.14 CPCI Interface Block, Sheet 13

7.14.1 CPCI J1 Connector

An AMP Z-PACK connector is used to provide a cPCI compliant J1 interface

7.14.2 ESD Strip

An ESD strip in integrated into the PCB along the front edge.

7.15 cPCI Power Block, Sheet 14

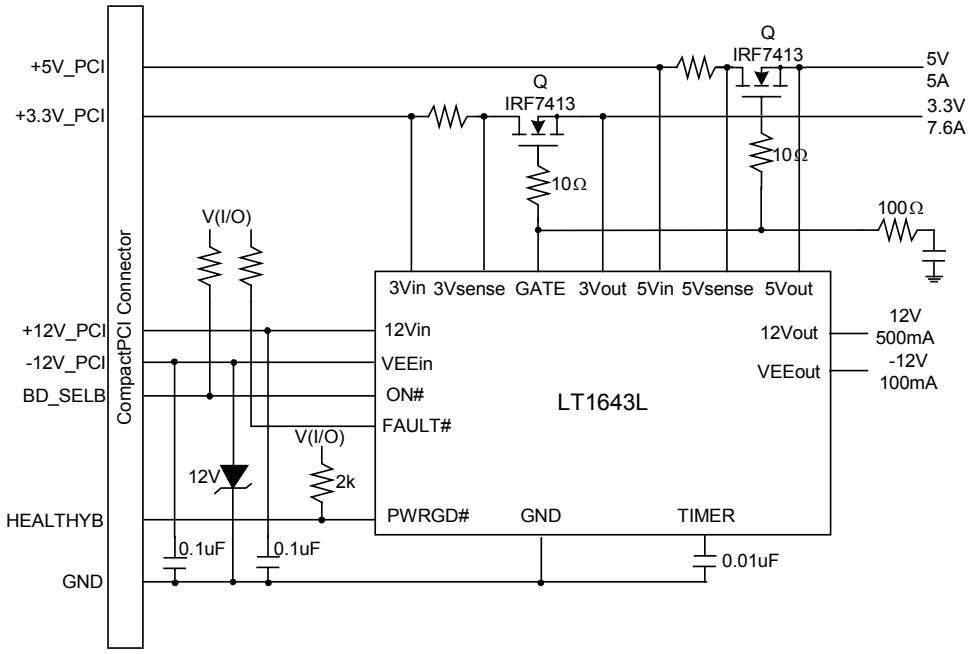
The standard cPCI interface system blocks will be used. These blocks perform the following functions:

7.15.1 Hot Swap Controller System Block

The Hot Swap Controller is used to allow a board to be safely inserted or removed from a live cPCI slot. The Hot Swap controller on the Power Supply Board System Block is implemented using the Linear Technology LTC1643L-1 The Hot swap controller allows the supply voltages to be ramped up at a programmable rate. The hot swap controller also detects over-current and over-voltage conditions, and shuts down power to the board until those conditions are rectified.

The LTC1643-1 ignores the +12V and –12V supplies when generating the /PWRGD signal. External N-channel MOSFETS are used to control the 3.3V and 5V supplies. When the 3.3V and 5V supplies are valid, /PWRGD is asserted.

Figure 27: cPCI Hot Swap Controller



7.16 System Interface, Sheet 14

7.16.1 UTOPIA/POS-PHY Level 3 Interface

The S/UNI-16X155-POS UTOPIA/POS-PHY L3 interface is connected to the drop side HS3 connector through switches as described in Section 7.10. The pin names shown below have the prefix “SYS_” added on the signal names of the schematic.

The HS3 connector uses a PMC-Sierra, Inc. proprietary pin out for the UTOPIA Level 3 bus as shown in the following two tables

Table 3: UL3/PL3 High Speed RX Interface

Pin Name	Type	Pin No.	Function
RDAT[0] RDAT[1] RDAT[2] RDAT[3] RDAT[4] RDAT[5] RDAT[6] RDAT[7] RDAT[8] RDAT[9] RDAT[10] RDAT[11] RDAT[12] RDAT[13] RDAT[14] RDAT[15] RDAT[16] RDAT[17] RDAT[18] RDAT[19] RDAT[20] RDAT[21] RDAT[22] RDAT[23] RDAT[24] RDAT[25] RDAT[26] RDAT[27] RDAT[28] RDAT[29] RDAT[30] RDAT[31]	Output	B4 A4 E5 D5 C5 B5 A6 E6 D6 C6 B6 A6 E7 D7 C7 B7 A7 E8 D8 C8 B8 A9 E9 D9 C9 B9 A9 E10 D10 C10 B10 A10	UTOPIA: Receive Cell Data Bus For Utopia Level 3 this bus carries the ATM cell octets that are read from the receive FIFO POS-PHY: Receive Packet Data Bus For POS-PHY Level 3 this bus carries Packets that are read from the selected receive FIFO.
RPRTY	Output	A3	Receive Bus Parity The receive parity signal indicates the parity of the RDAT bus.
RENB	Input	D1	Receive Write Enable The RENB signal is an active low input which is used to initiate reads from the receive FIFO.

Pin Name	Type	Pin No.	Function
RCA RVAL	Output	B3	UTOPIA: Receive Cell Available This signal indicates an available cell. POS-PHY: Receive Data Valid RAVL indicates signals RDAT, RSOP, REOP, RMOD, RPRTY and RERR are valid. This signal is not used in UTOPIA mode.
RSOC RSOP	Output	D4	UTOPIA: Receive Start of Cell This signal marks the start of cell on the RDAT bus. POS-PHY: Receive Start of Packet This signal marks the start of packet on the RDAT bus.
RERR	Output	C4	POS-PHY: Receive Error This signal indicates that the current packet has been aborted. This signal is not used in Utopia ATM mode.
REOP	Output	E4	POS-PHY: Receive End of Packet This signal marks the end of packet on the RDAT bus. This signal is not used in UTOPIA mode.
RMOD[1] RMOD[0]	Output	D3 C3	POS-PHY: Receive Word Modulo Indicates number of bytes in the last RDAT bus transaction of a packet. This signal is not used in UTOPIA mode.
RXADDR[0] RXADDR[1] RXADDR[2] RXADDR[3] RXADDR[4] RXADDR[5]	Input	A2 B2 C2 D2 E2 A1	UTOPIA: Rx PHY Address Allows selection of particular PHY on MPHY devices. Only RXADDR[0..3] are used on this board These signals are not used in POS-PHY mode.
RSX	Output	E3	POS-PHY: Receive Start of Transfer RSX indicates when the in-band PHY port address is present on RDAT bus. This signal is not used in UTOPIA mode.
RFCLK	Input	F1	104 MHz Receive Bus Slave Clock Input Provided to the PM5382 RFCLK input via CMOS switches during RX Slave mode operation.

Pin Name	Type	Pin No.	Function
RSYSCLK	Output	C1	104 MHz Receive Bus Master Clock Output Provided to the external system and timed to coincide with RFCLK signal to PM5382 during RX Master mode operation.

Table 4: UL3/PL3 High Speed TX Interface

Pin Name	Type	Pin No.	Function
TDAT[0] TDAT[1] TDAT[2] TDAT[3] TDAT[4] TDAT[5] TDAT[6] TDAT[7] TDAT[8] TDAT[9] TDAT[10] TDAT[11] TDAT[12] TDAT[13] TDAT[14] TDAT[15] TDAT[16] TDAT[17] TDAT[18] TDAT[19] TDAT[20] TDAT[21] TDAT[22] TDAT[23] TDAT[24] TDAT[25] TDAT[26] TDAT[27] TDAT[28] TDAT[29] TDAT[30] TDAT[31]	Input	C4 B4 A4 E5 D5 C5 B5 A6 E6 D6 C6 B6 A6 E7 D7 C7 B7 A7 E8 D8 C8 B8 A9 E9 D9 C9 B9 A9 E10 D10 B10 A10	UTOPIA: Transmit Cell Data Bus This bus carries the ATM cell octets that are written to the selected transmit FIFO. POS-PHY: Transmit Packet Data Bus This data bus carries the POS packet octets that are written to the selected transmit FIFO.
TPRTY	Input	D4	Transmit Bus Parity. The transmit parity signal indicates the parity of the TDAT bus.
TENB	Input	C2	Transmit Write Enable. The TENB signal is an active low input which is used to initiate writes to the transmit FIFO

Pin Name	Type	Pin No.	Function
TCA PTPA	Output	E3	UTOPIA: Transmit Cell Available This signal is used to indicate available cell FIFO space by the PHY port. POS-PHY: Polled Transmit Packet Available. This signal transitions to high when a programmable minimum number of free space is available in the transmit FIFO of the polled PHY.
STPA	Output	D3	POS-PHY: Selected Transmit Packet Available This signal transitions to high when a programmable minimum number of free space is available in the transmit FIFO of the selected PHY. This signal is not used in UTOPIA mode.
TSOC TSOP	Input	B3	UTOPIA: Transmit Start of Cell The transmit start of cell signal marks the start of cell on the TDAT bus. POS-PHY: Transmit Start of Packet This signal indicates the first byte in a packet.
TERR	Input	E4	POS-PHY: Transmit Error This signal indicates the current packet must be aborted. This signal is not used in UTOPIA mode.
TEOP	Input	C3	POS-PHY: Transmit End of Packet This signal marks the end of a packet on the TDAT bus. This signal is not used in UTOPIA mode.
TMOD[1] TMOD[0]	Input	B2 A2	POS-PHY: Transmit Word Modulo This signal indicates the size of the current word. This signal is not used in UTOPIA mode.

Pin Name	Type	Pin No.	Function
TXADDR[0] TXADDR[1] TXADDR[2] TXADDR[3] TXADDR[4] TXADDR[5]	Input	E1 D1 C1 B1 A1 E2	UTOPIA: Tx PHY Address Allows selection of particular PHY on MPHY devices. Only TXADDR[0..3] are used on this board. POS-PHY: Allows selection of a particular PHY for polling. Only TXADDR[0..3] are used on this board.
TSX	Input	A3	POS-PHY: Transmit Start of Transfer TSX indicates when the in-band PHY port address is present on TDAT bus.
TFCLK	Input	F10	104 MHz Transmit Bus Slave Clock Input Provided to the PM5382 TFCLK input via switches during TX Slave mode operation.
TSYSCLK	Output	C10	104 MHz Transmit Bus Master Clock Output Provided to the external system and timed to coincide with TFCLK signal to PM5382 during RX Master mode operation.

7.16.2 APS and SYS_REF Interfaces

The J12 HS3 connector supports the APS connections between boards as well as connections for SYS_REF clocks exchanged between boards.

Table 5: APS and SYS_REF Interface, J12

Pin Name	Type	Pin No.	Function
APSI0 APSI1 APSI2 APSI3 APSI4 APSI5 APSI6 APSI7	Input	C5 B5 C4 B4 C3 B3 C2 B2	APS Inputs
APSO0 APSO1 APSO2 APSO3 APSO4 APSO5 APSO6 APSO7	Output	E5 D5 E4 D4 E3 D3 E2 D2	APS Outputs
REF_INP REF_INN	Input	B1 C1	77.76 MHz Reference Clock Input
REF_OUTP REF_OUTN	Output	D1 E1	77.76 MHz Reference Clock Output

The high frequency characteristics of the HS3 connector preserve the signal integrity of the 622 Mbps APS PECL signals.

8 PCB CONSIDERATIONS

This section discusses the implementation requirements for a four port OC-12c linecard using a S/UNI-4x622 on the S/UNI-16x155 reference design board.

The S/UNI-4x622 and S/UNI-16x155 devices are pin compatible, and the majority of the pins are common to both devices. However, since one is a four port device, and the other is a 16 port device, there are a number of pins which are not shared and special care must be taken in board design to implement a combined design. The majority of pins which are not common between the two devices map to a no-connect on one or the other, simplifying the implementation. There are, however; a number of pins that require special attention in design and layout. The following sections outline the build options on applicable schematic sheets.

8.1 SUNI BLOCK, Sheet 2

Channel 0

S/UNI-16x155 Option:

- Assemble solder bridges SB6, SB7 and SB10.
- Install OC-3 ODL U23, power filter and termination components.

S/UNI-4x622 Option

- Assemble solder bridges SB11, SB13, SB16, SB19.
- Do not assemble U23, power filter or termination components.

Channel 1

S/UNI-16x155 Option:

- Install OC-3 ODL, filter and terminations.
- Do not install R73.

S/UNI-4x622 Option:

- Install OC-12 ODL.
- Replace R187 with a 64.3 Ω resistor. Do not install R188.

- Install R73 if the OC-12 ODL uses a TTL SD pin rather than PECL.
- Ensure that the SDTTL pin is configured correctly.

Channel 2

S/UNI-16x155 Option:

- Assemble Solder Bridges SB5, SB8 and SB9.
- Install OC-3 optics, filter and termination components.

S/UNI-16x155 Option:

- Assemble Solder Bridges SB12, SB15, SB17.
- Install 0.047uF cap C200.
- Do not assemble ODL, filter or termination components.

Channel 3

S/UNI-16x155 Option:

- Assemble SB58 and SB59
- Assemble ODL, filter and termination components.
- Do not install R199.

S/UNI-4x622 Option:

- Assemble SB24 and SB25.
- Install R199
- Do not assemble ODL, filter or termination components.

Channel 4

S/UNI-16x155 Option:

- Assemble SB14.
- Assemble ODL, filter and termination components.

S/UNI-4x622 Option:

- Assemble SB18, SB20, and SB21.
- Do not assemble ODL, filter or termination components.

Channel 7

S/UNI-16x155 Option:

- Install SB22.
- Assemble ODL, filter and termination components.
- Do not install C218.

S/UNI-4x622 Option:

- Install SB23 and C218.
- Do not assemble ODL, filter or termination components.

8.2 SUNI BLOCK, Sheet 3

Channel 6

S/UNI-16x155 Option:

- Install SB26, SB27 and SB28.
- Install ODL circuitry
- Do not install R230 or R231.

S/UNI-4x622 Option:

- Install SB29, SB30, SB31.
- Install R230, R231.
- Do not install ODL circuitry.

Channel 5

S/UNI-16x155 Option:

- Install SB60, SB61, SB62
- Assemble ODL circuitry
- Do not install 4_TXD2 terminations.

S/UNI-4x622 Option:

- Assemble SB63.
- Install R248, R248, C252 and C253.
- Do not assemble ODL circuitry.
- Assemble U36 OC-12 optics module, filter and termination components. PECL (R213 pulldown) and TTL (R83 pullup) terminations are provided for the SD pin.

Channel 9

S/UNI-16x155 Option:

- Install OC-3 ODL circuitry

S/UNI-4x622 Option:

- Assemble U34 with an OC-12 ODL.
- Assemble R218 with a 63.4Ω resistor.
- Do not install R219.
- PECL (R203 pulldown) and TTL (R82 pullup) terminations are provided for the SD pin. Ensure SDTTL is set correctly.

Channel 14

S/UNI-16x155 Option:

- Install OC-3 ODL circuitry

S/UNI-4x622 Option:

- Assemble U37 with an OC-12 ODL.
- Assemble R245 with a 63.4Ω resistor.

- Do not install R246.
- PECL (R234 pulldown) and TTL (R89 pullup) terminations are provided for the SD pin. Ensure SDTTL is set correctly.

8.3 SUNI BLOCK, Sheet 4

Do not assemble J9. The add-on board is not required for a S/UNI-4x622 implementation.

Channel 8

S/UNI-16x155 Option:

- Assemble SB34, SB37 and SB38.
- Assemble termination components

S/UNI-4x622 Option:

- Assemble SB40, SB42, SB45, SB46.

Channel 10

S/UNI-16x155 Option:

- Assemble SB49, SB50, SB51.
- Install terminations.

S/UNI-4x622 Option:

- Assemble SB54, SB55, SB56 and C267.
- Do not install terminations.

Channel 11 and Channel 12

S/UNI-16x155 Option:

- Assemble terminations.

S/UNI-4x622 Option:

- Do not assemble terminations.

Channel 13

S/UNI-16x155 Option:

- Install SB32, SB33, SB35.
- Install terminations

S/UNI-4x622 Option:

- Install SB36, SB39, SB41, SB43, SB44.
- Do not install terminations.

Channel 15

S/UNI-16x155 Option:

- Install SB47, SB48, SB64
- Install terminations

S/UNI-4x622 Option:

- Install SB52, SB53, SB57 and C265.

8.4 SUNI BLOCK, Sheet 6

DCC Signals

S/UNI-16x155 Option:

- Assemble pulldown resistors RN86, RN87, RN90, RN91.

S/UNI-4x622 Option.

- Do not assemble pulldown resistors RN86, RN87, RN90, RN91
- Assemble SB65, SB66, SB67, SB68, SB69.

8.5 SUNI BLOCK, Sheet 7

Sheet 7 shows the power supply configuration for the S/UNI-16x155 reference design and provides filtering and decoupling for a S/UNI-16x155 or S/UNI-4x622 build option.

S/UNI-16x155 Option:

- Assemble AVD0, AVD1, AVD2, and AVD7 filter circuits.
- Install decoupling capacitors listed in the schematics.

S/UNI-4x622 Option:

- In addition to the AVDx filter circuits, assemble the 4_CRU_AVD_x filter circuits and analog 3.3V decoupling capacitors.
- Install decoupling capacitors listed in the schematics.

8.6 General Design Notes

Ensure that the critical 622 nets are well isolated from potentially long 155 traces. These include:

- 4x622 Pins: RXD[2]+/-, TXD[2]+/-, C0[0,2,3], C1[0,2,3] TXREF[0,1]. All these pins map to controlled impedance 155Mbit traces on the 16x155 and care should be taken in layout to ensure the 622 traces are well isolated from the 155 traces to maintain good signal quality.

On the S/UNI-16x155 reference design, solder bridges have been added to connections for those pins that map to signal pins on the S/UNI-16x155 and power or ground pins on the S/UNI-4x622. Special care in layout is required to ensure that the 155Mbit differential PECL traces have a minimum of stub traces that can affect signal quality severely.

Zero ohm resistors can be used in place of solder bridges. On the reference design, solder bridges are used so that two different solder masks can be created to implement either build option, reducing component count, simplifying the BOM, and reducing the complexity of the assembly process.

9 SCHEMATICS REVISION 1

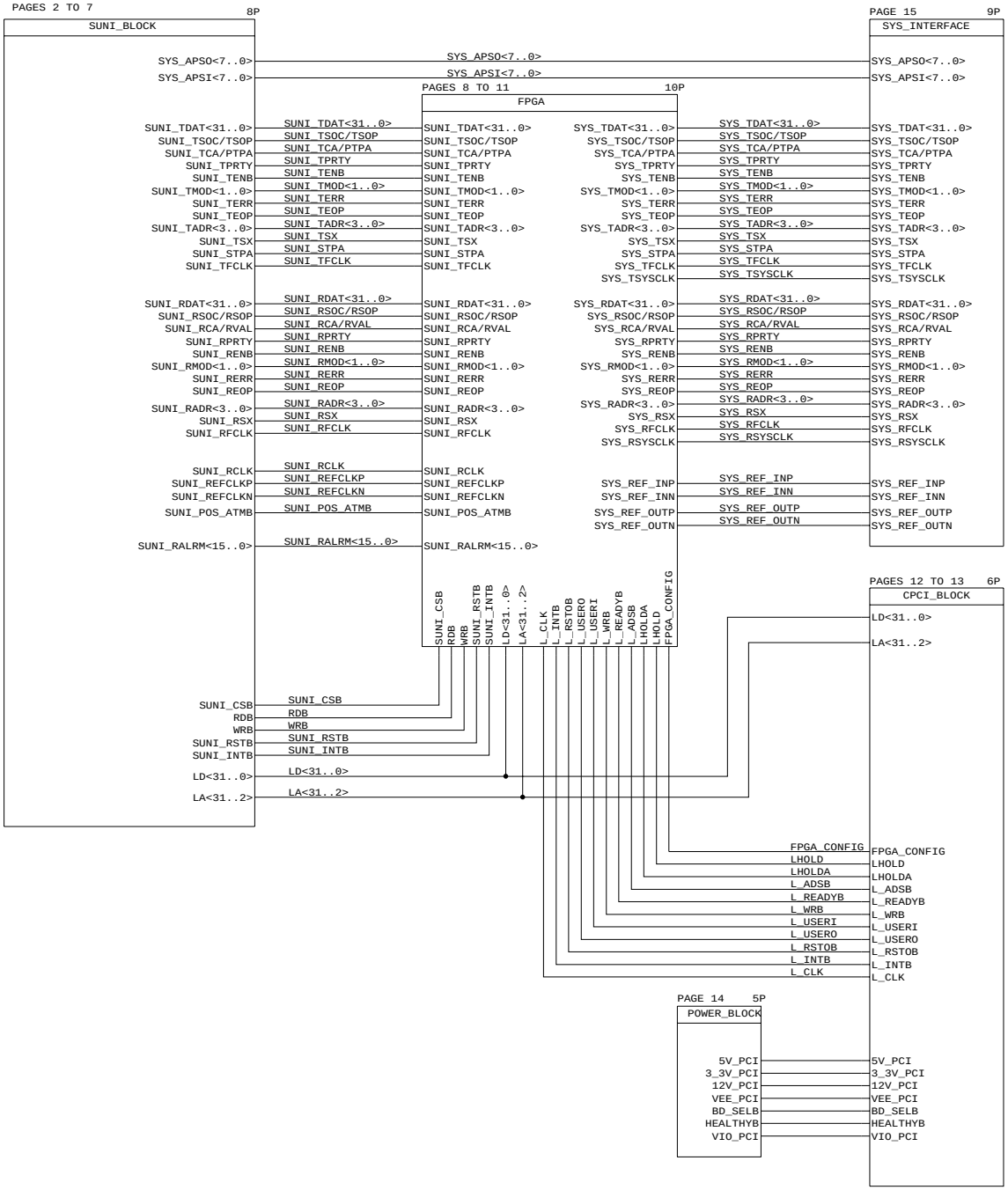
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

PAGES 16 TO 17 — 11P

OPTICS_CARD

OPTICS MODULES 8 TO 15 ARE MOUNTED ON A DAUGHTER CARD WHICH MOUNTS ONTO THE MAIN BOARD.

THIS BOARD IS A SNAP OFF PART OF THE PCB.



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Wed Oct 18 13:44:42 2000

PMC-Sierra, Inc.

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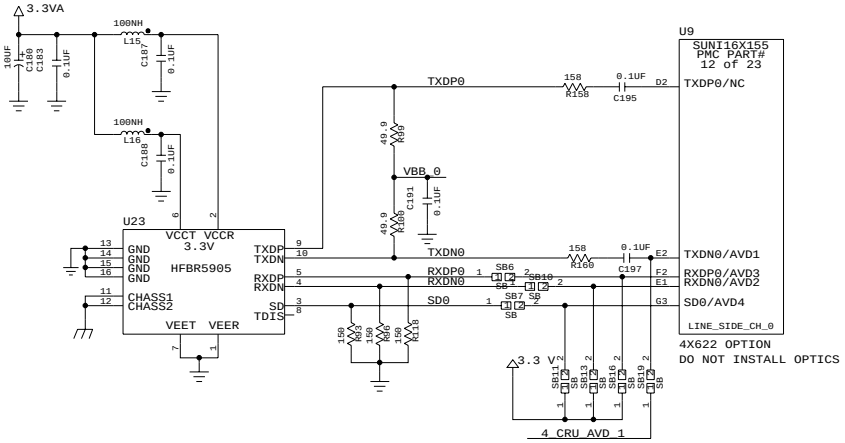

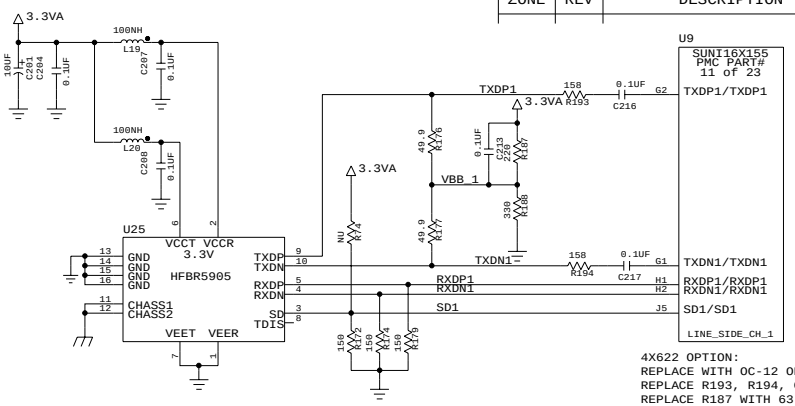

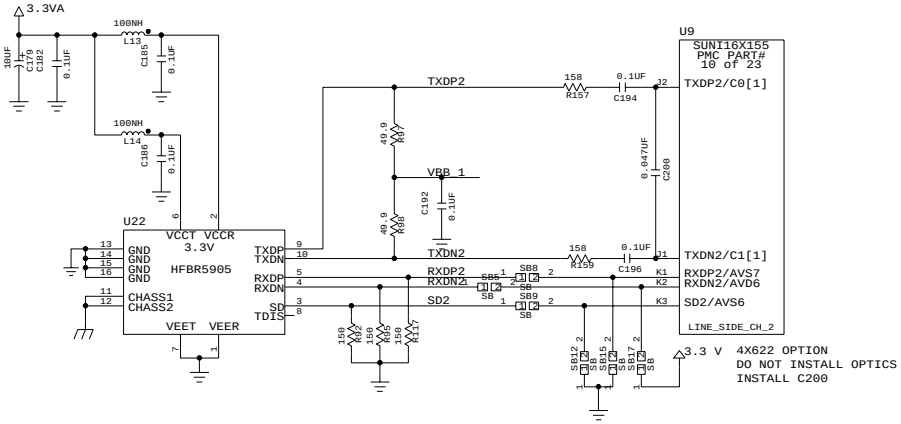

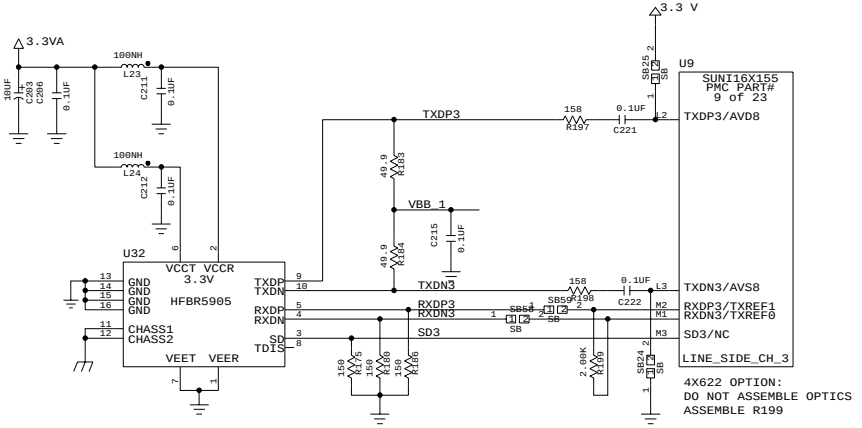

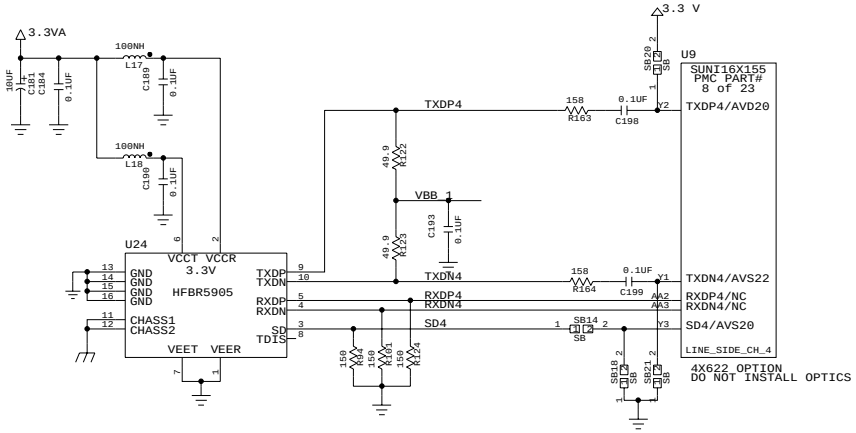

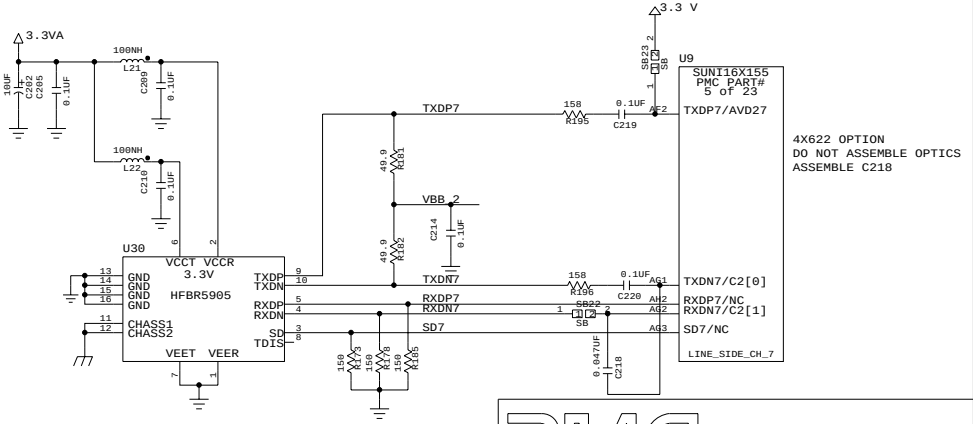

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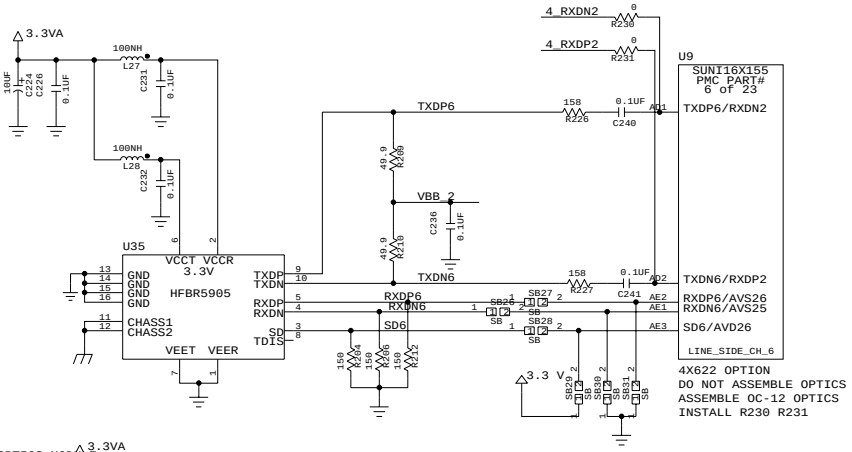

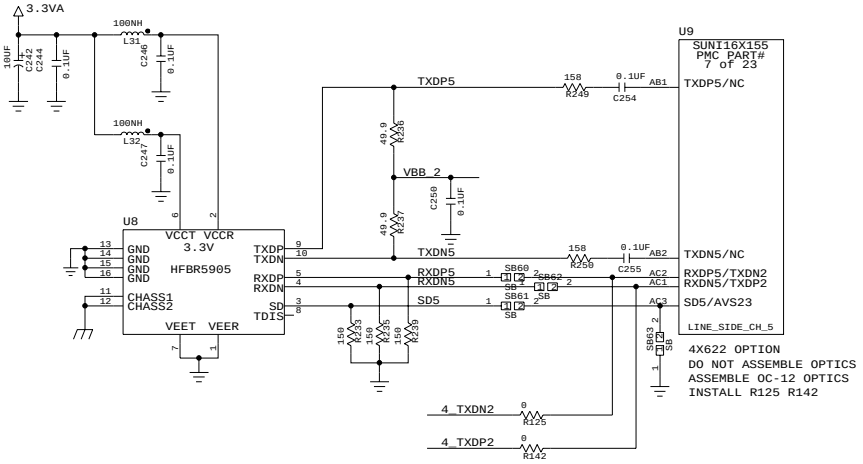

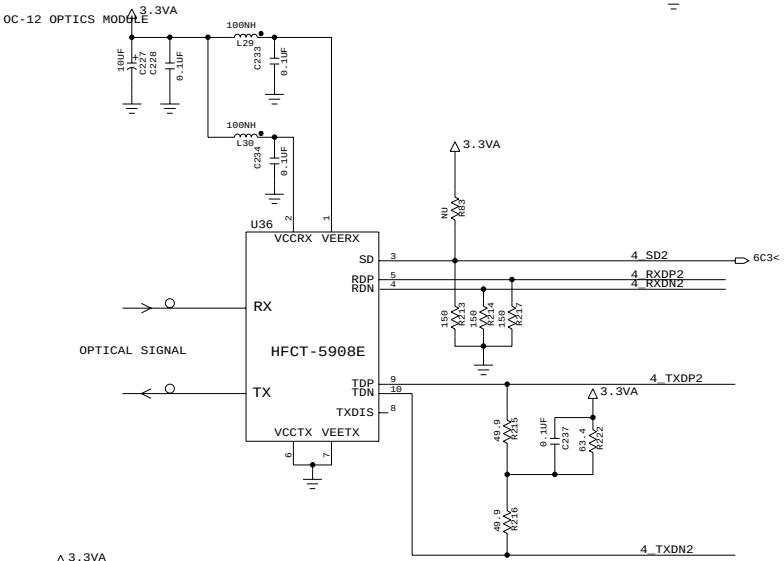

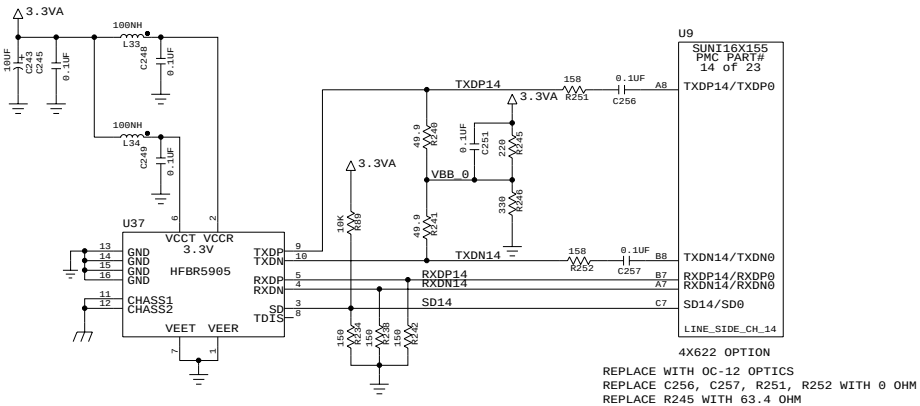

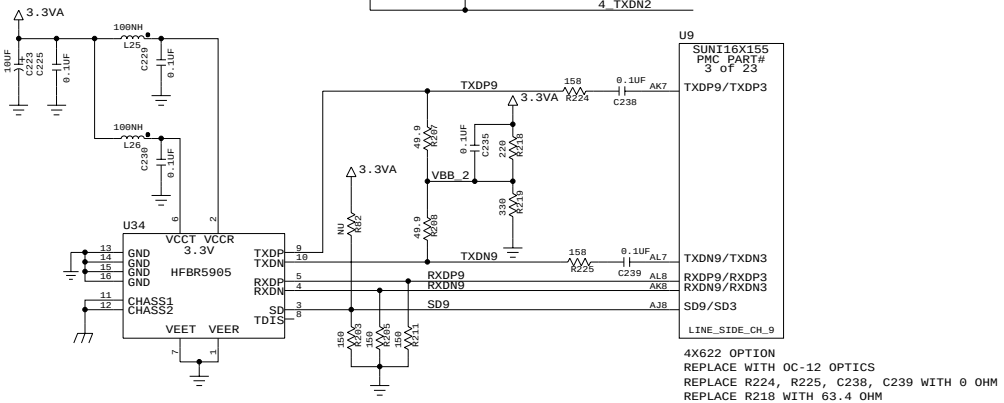

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ENGINEER: BDV	PAGE:3 OF 17

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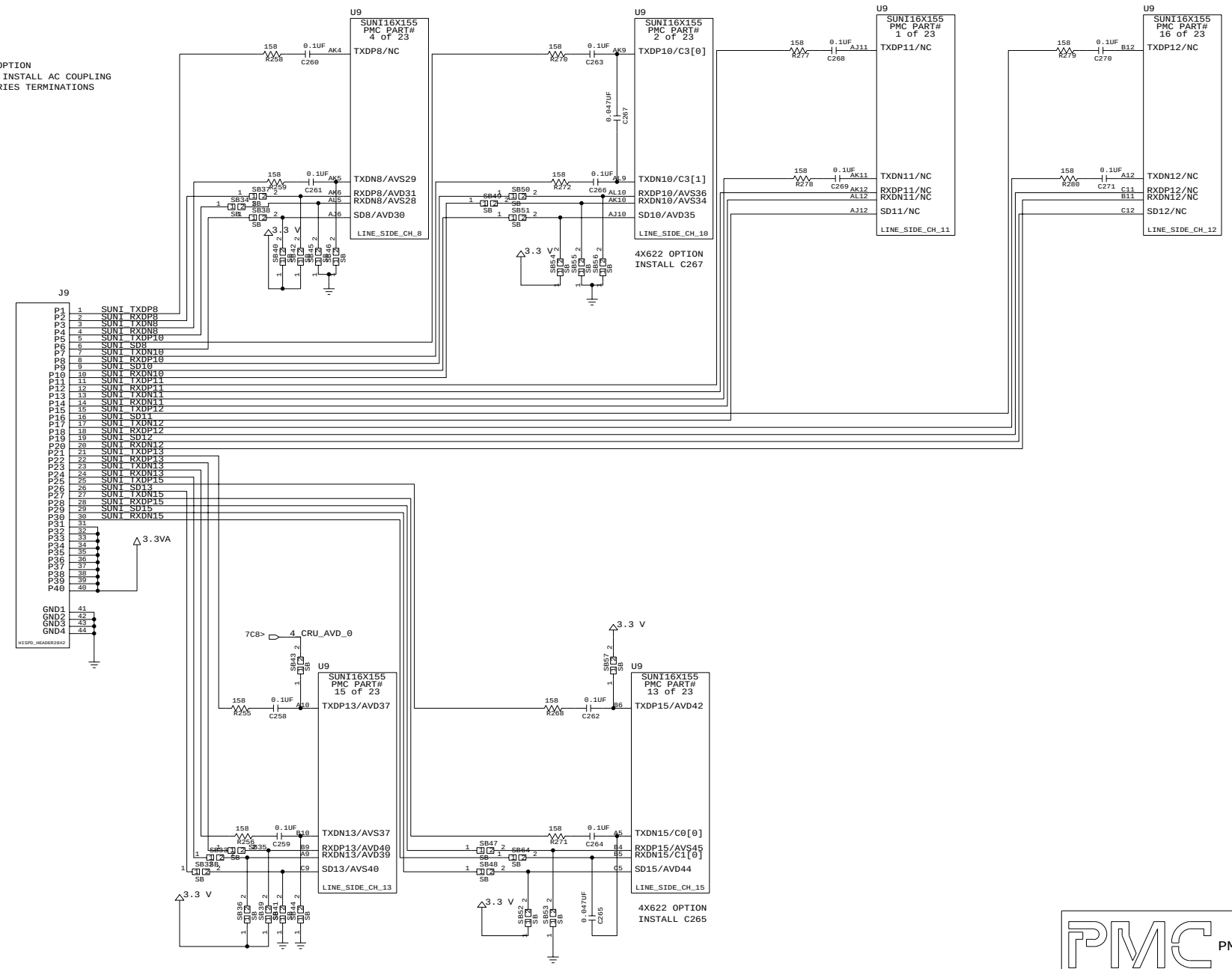
4X622 OPTION
DO NOT INSTALL AC COUPLING
AND SERIES TERMINATIONS



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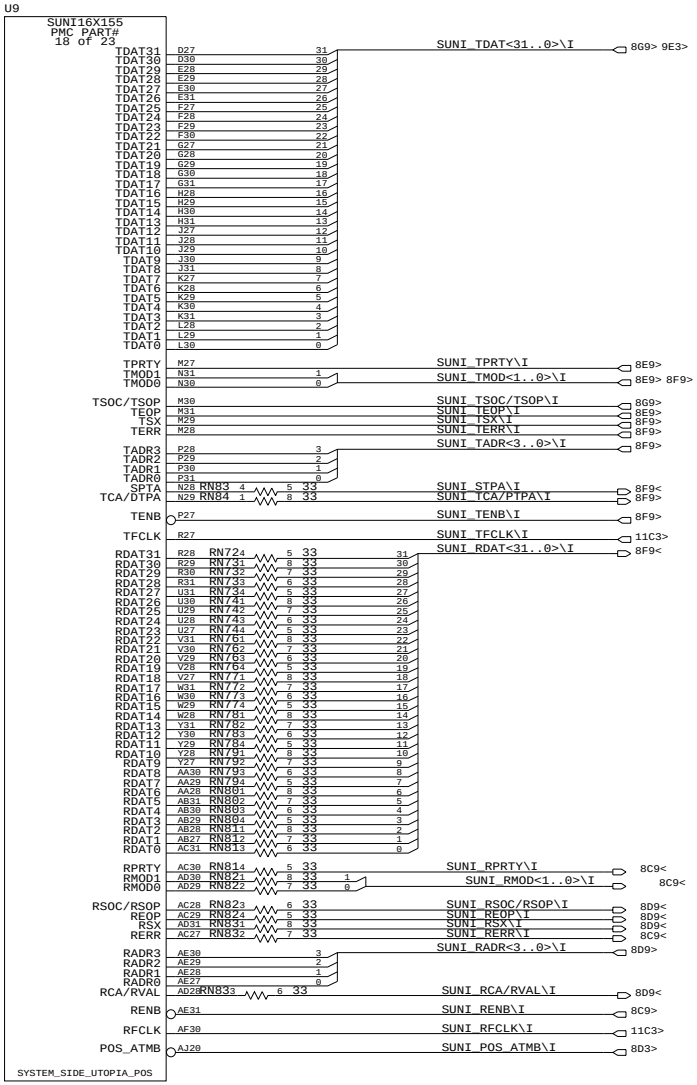

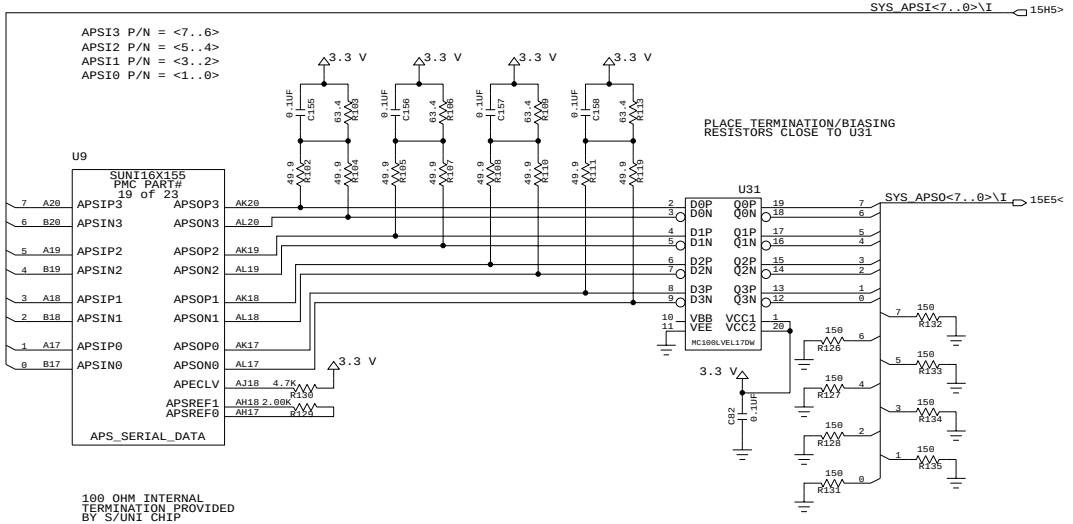

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ENGINEER: BDV GR	PAGE:5 OF 17

REVISIONS				
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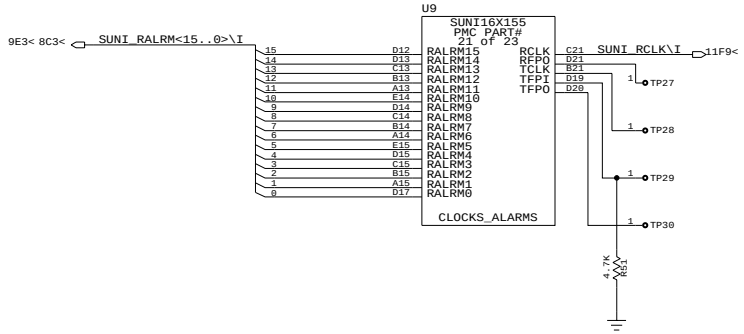
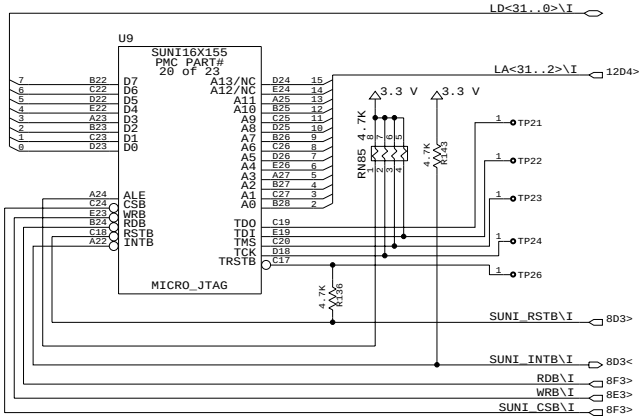
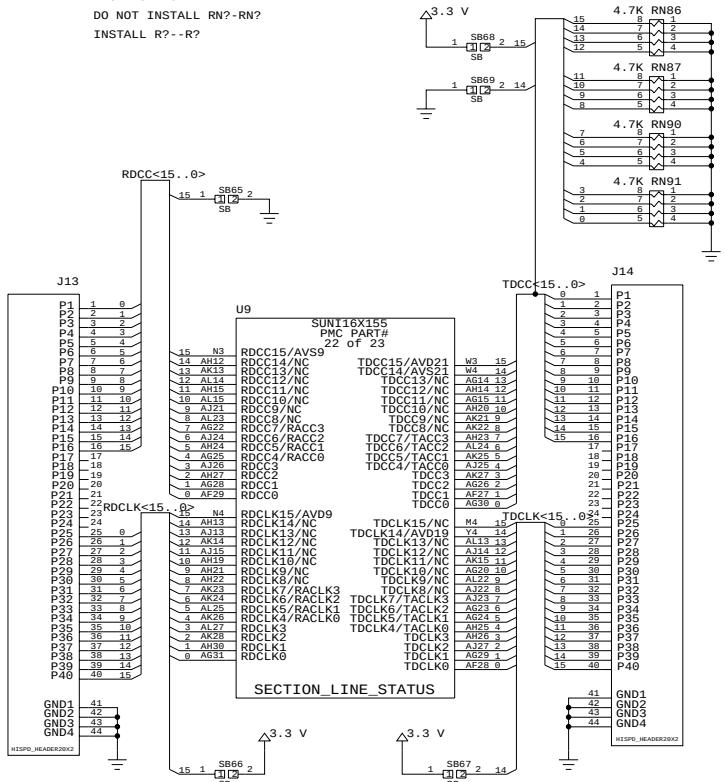
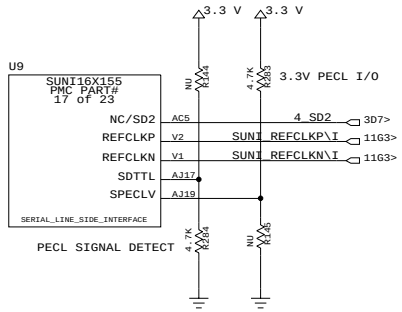
4X622 OPTION
DO NOT INSTALL RN?-RN?
INSTALL R?--R?









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ENGINEER: BDV GR	PAGE:6 OF 17

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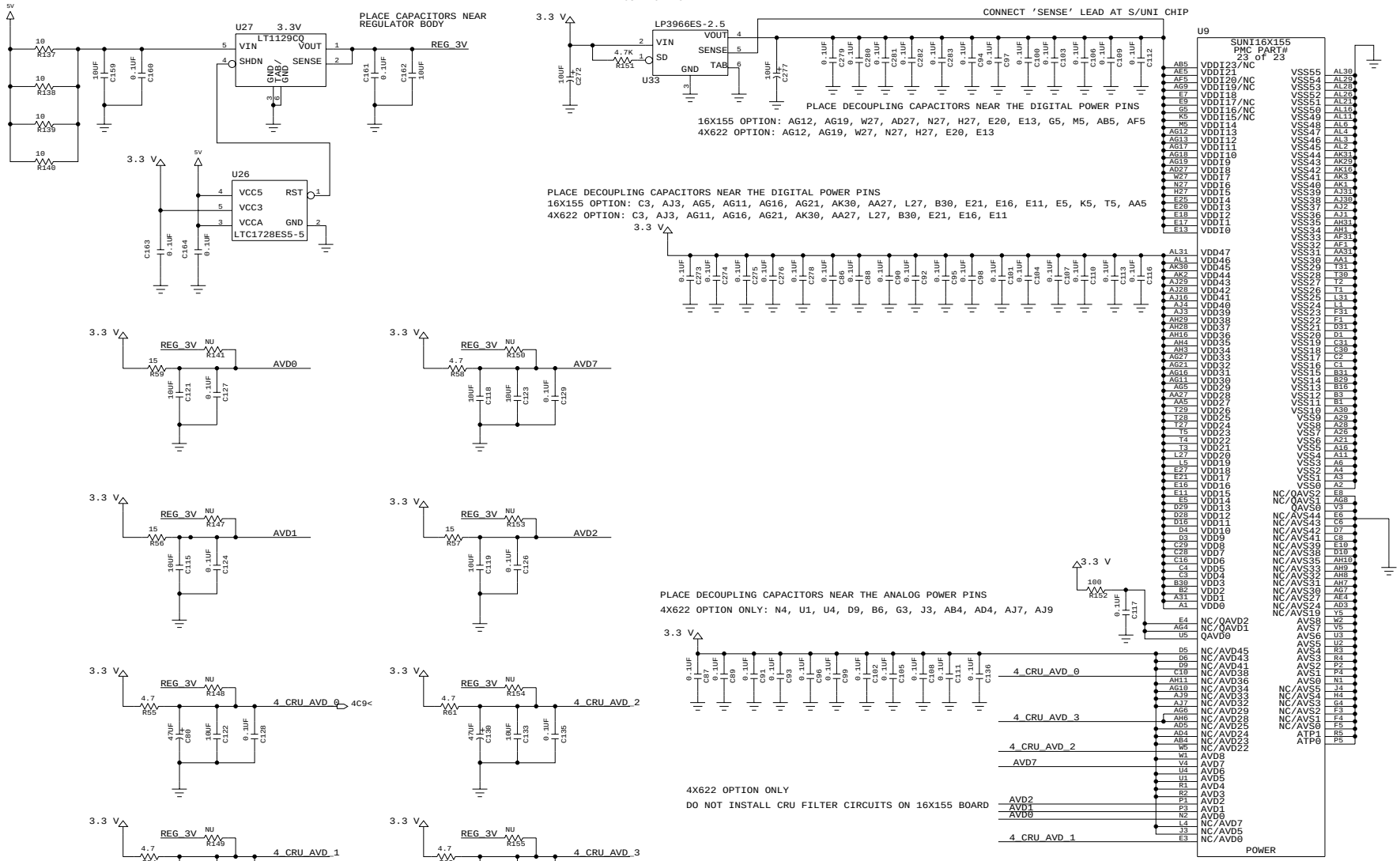
OPTIONAL LINEAR REGULATOR FOR SENSITIVE +3.3 VOLT POWER PINS

PLACE CAPACITORS NEAR REGULATOR BODY

PLACE TANT CAPACITORS NEAR REGULATOR BODY

CONNECT 'SENSE' LEAD AT S/UNI CHIP



PLACE DECOUPLING CAPACITORS NEAR THE DIGITAL POWER PINS

16X155 OPTION: AG12, AG19, W27, AD27, N27, H27, E20, E13, G5, M5, AB5, AF5

4X622 OPTION: AG12, AG19, W27, N27, H27, E20, E13

PLACE DECOUPLING CAPACITORS NEAR THE DIGITAL POWER PINS

16X155 OPTION: C3, AJ3, AG5, AG11, AG16, AG21, AK30, AA27, L27, B30, E21, E16, E11, E5, K5, T5, AA5

4X622 OPTION: C3, AJ3, AG11, AG16, AG21, AK30, AA27, L27, B30, E21, E16, E11

PLACE DECOUPLING CAPACITORS NEAR THE ANALOG POWER PINS

4X622 OPTION ONLY: N4, U1, U4, D9, B6, G3, J3, AB4, AD4, AJ7, AJ9

4X622 OPTION ONLY

DO NOT INSTALL CRU FILTER CIRCUITS ON 16X155 BOARD

USE 10V X5R CERAMIC 1210 SIZE CAPACITORS FOR ALL 10UF COMPONENTS
USE TANTALUM CAPS FOR ALL 47UF COMPONENTS

PLACE EACH 0U1 CAPACITOR CLOSE TO THE ASSOCIATED POWER PIN

THE 10UF CAPACIT AND RESISTORS DO NOT NEED TO BE PLACED CLOSE TO THE POWER PINS, AS THEY ARE FILTERING THE SUPPLY, NOT DECOUPLING IT.

DRAWING

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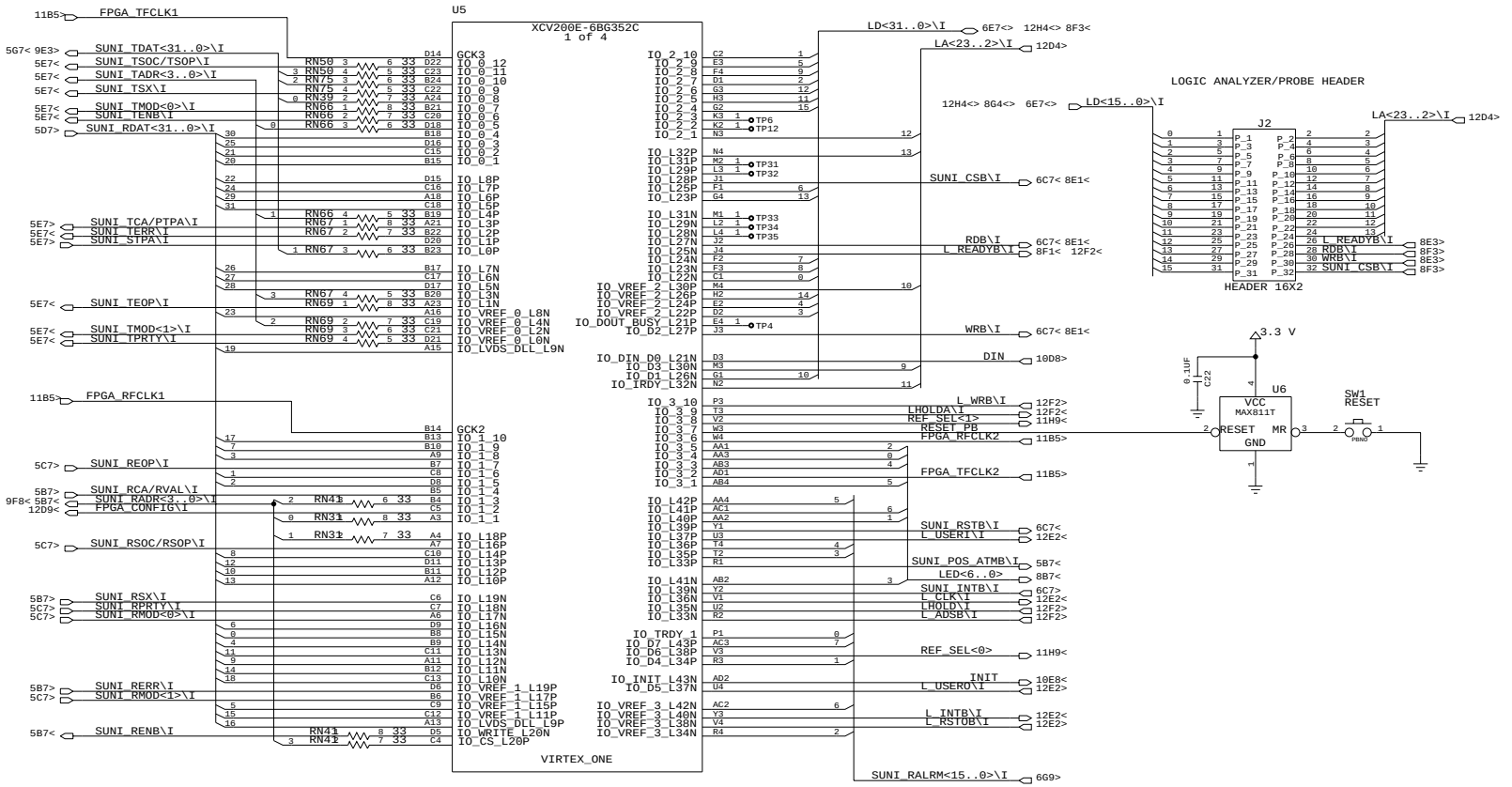
ABBREV=SUNI_BLOCK
LAST_MODIFIED=Thu Dec 14 10:38:42 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE:
TITLE: S/UNI 16X155 REFERENCE DESIGN S/UNI SUPPLY FILTERING & REG	REVISION NUMBER: 1
ENGINEER: BDV GR	PAGE:7 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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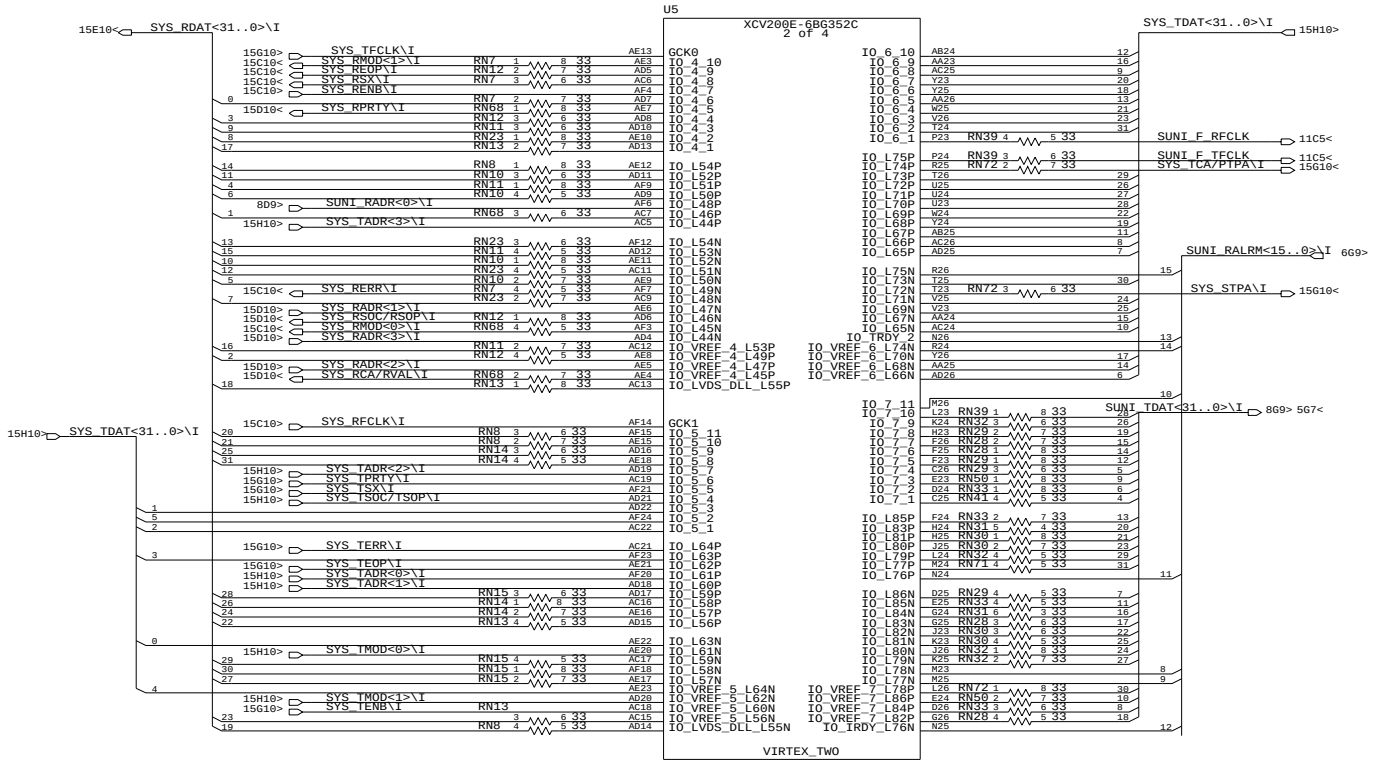
Thu Dec 14 10:37:32 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: S/UNI-16X155 REFERENCE DESIGN FPGA PL3 I/F	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:8 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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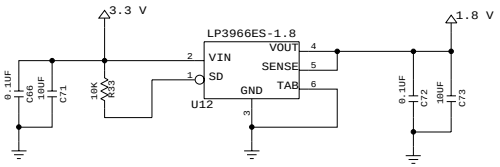
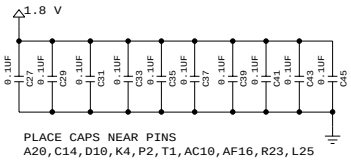
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: SUNI-16X155 REFERENCE DESIGN FPGA PL3 I/F	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:9 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

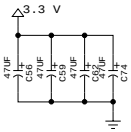
1.8V REGULATOR FOR FPGA VDDI



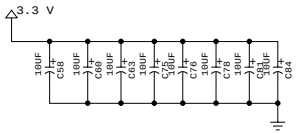


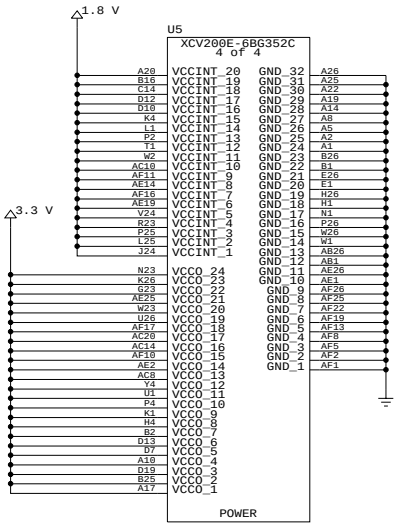
PLACE CAPS NEAR PINS
A20,C14,D10,K4,P2,T1,AC10,AF16,R23,L25

PLACE NEAR EACH CORNER OF FPGA

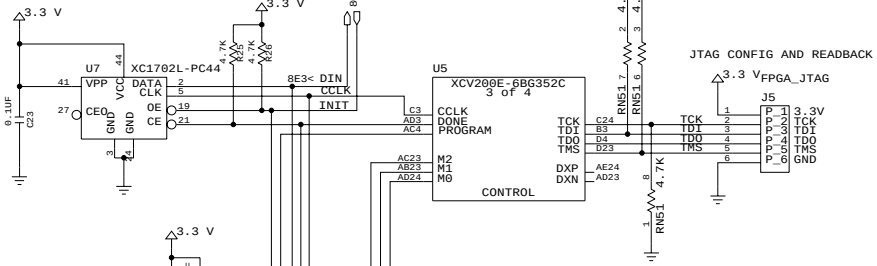


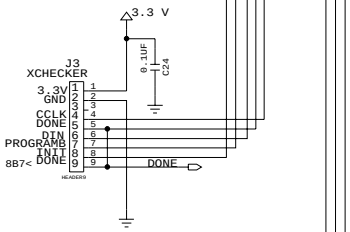
PLACE BULK DECOUPLING CAPS NEAR EACH I/O BANK OF FPGA

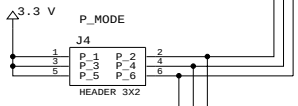


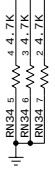


CONFIGURATION EPROM

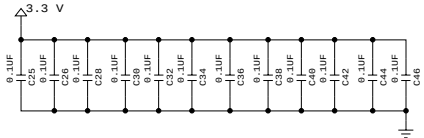








INSTALL JUMPERS FOR SLAVE SERIAL (XCHECKER) MODE
UNINSTALL JUMPERS FOR MASTER SERIAL (EPROM) DEFAULT MODE



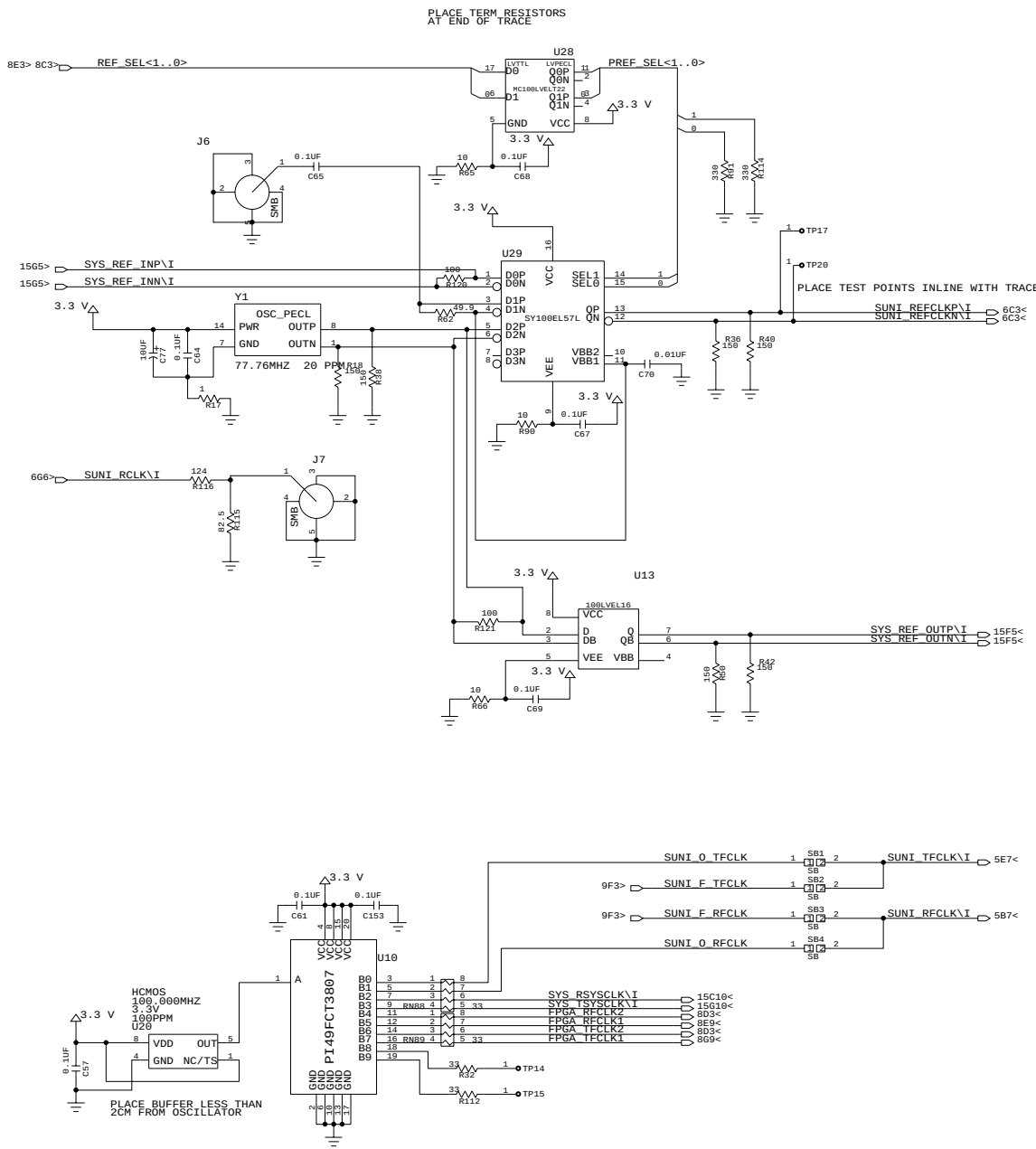
PLACE DECOUPLING CAPS NEAR PINS
B2,K1,U1,AE2,AF10,AF17,AE25,U26,K26,B25,A17,A10

DRAWING:
FPGA_BLOCK
FPGA_BLOCK
Thu Dec 14 10:37:43 2000

PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1.0	ISSUE DATE: YY/MM/DD
TITLE: S/UNI-16X155 REFERENCE DESIGN FPGA POWER & CONFIGURATION	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:10 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



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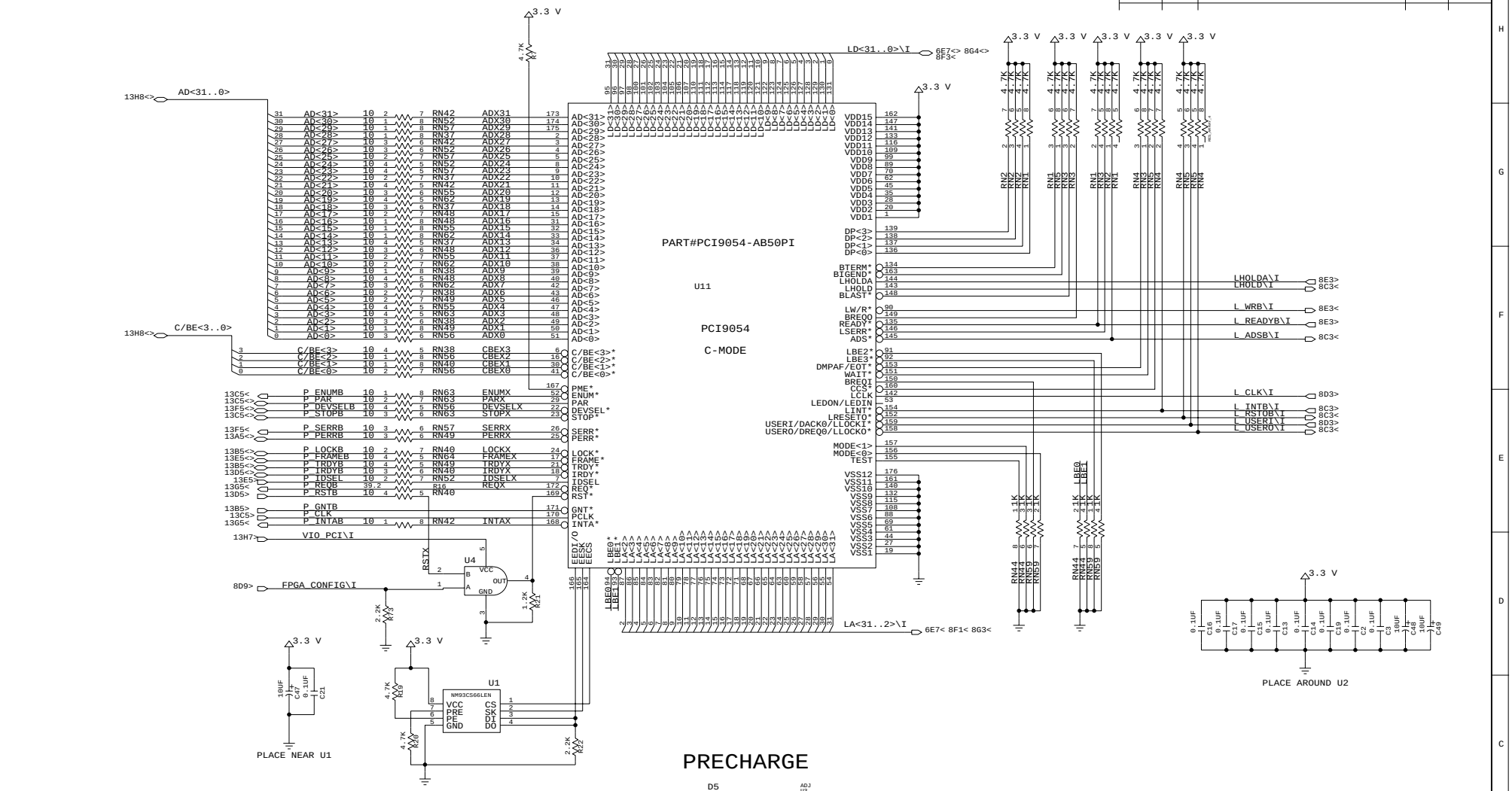
ABBREV=FPGA_BLOCK
LAST_MODIFIED=Thu Dec 14 10:37:47 2000

PMC-Sierra, Inc.

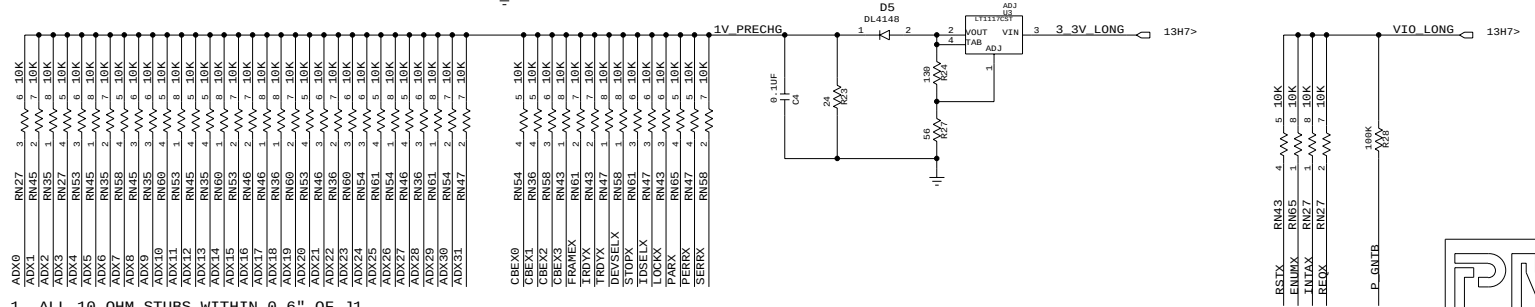
DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE:
TITLE: S/UNI-16X155 REFERENCE DESIGN REFCLK AND UL3/PL3 CLOCK	REVISION NUMBER: 1
ENGINEER: BDV GR	PAGE:11 OF 17

CPCI BRIDGE

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR



PRECHARGE



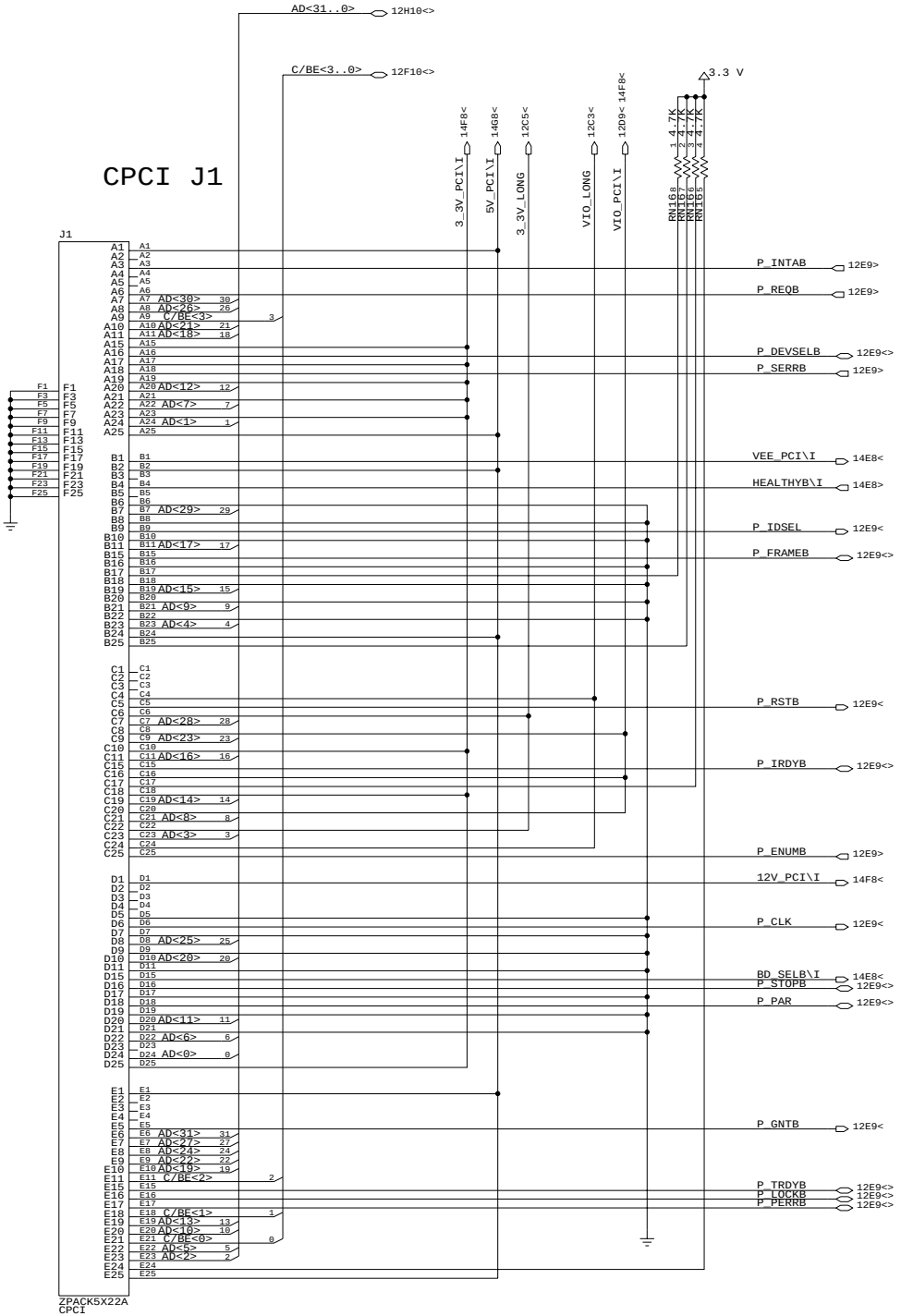
NOTES:
1. ALL 10 OHM STUBS WITHIN 0.6" OF J1
2. ALL PCI SIGNAL TRACES < 1.5" EXCEPT P_CLK
3. P_CLK TRACE MUST BE 2.5" +/- 0.1"
4. CPCI BUS TRACES ARE 65 OHM.
5. 39 OHM STUB RESISTOR ON REQB PLACED NEAR BRIDGE PIN

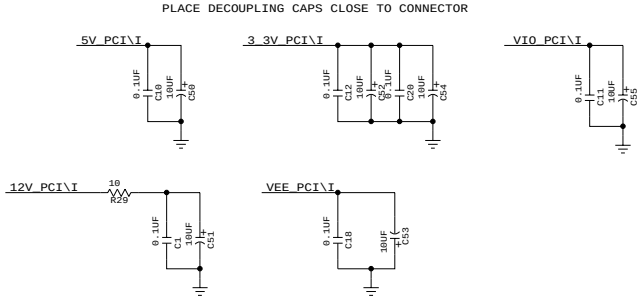
DRAWING:
TITLE=CPCI_BLOCK
ABBREV=CPCI_BLOCK
LAST_MODIFIED=Thu Dec 14 10:38:05 2000

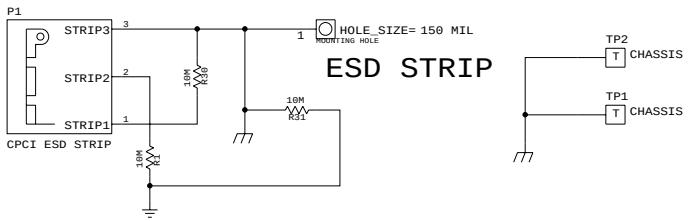
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991413 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: YY/MM/DD
TITLE: SUNI-16X155 REFERENCE DESIGN CPCI_BLOCK	REVISION NUMBER: 2
ENGINEER: PMC	PAGE:12 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







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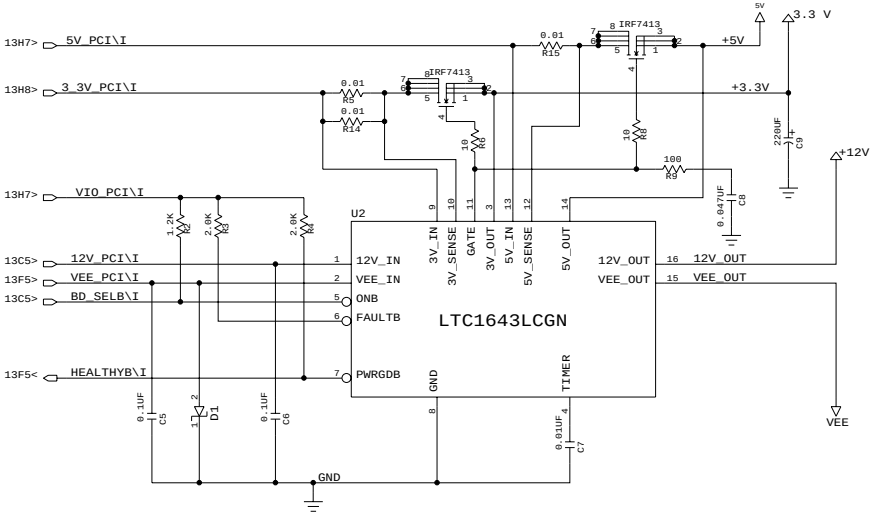
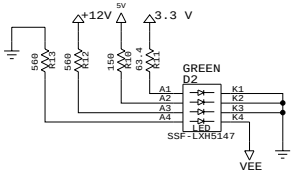
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-991413 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: YY/MM/DD
TITLE: SUNI-16X155 REFERENCE DESIGN CPCI_BLOCK	REVISION NUMBER: 2
ENGINEER: PMC	PAGE:13 OF 17

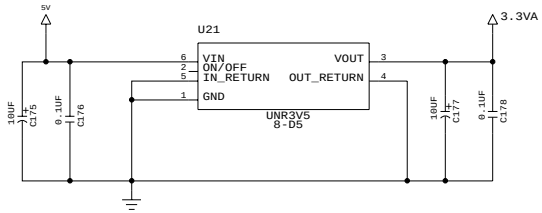
REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR

HOT SWAP CONTROLLER





3.3V SWITCHING REGULATOR FOR OPTICS MODULES



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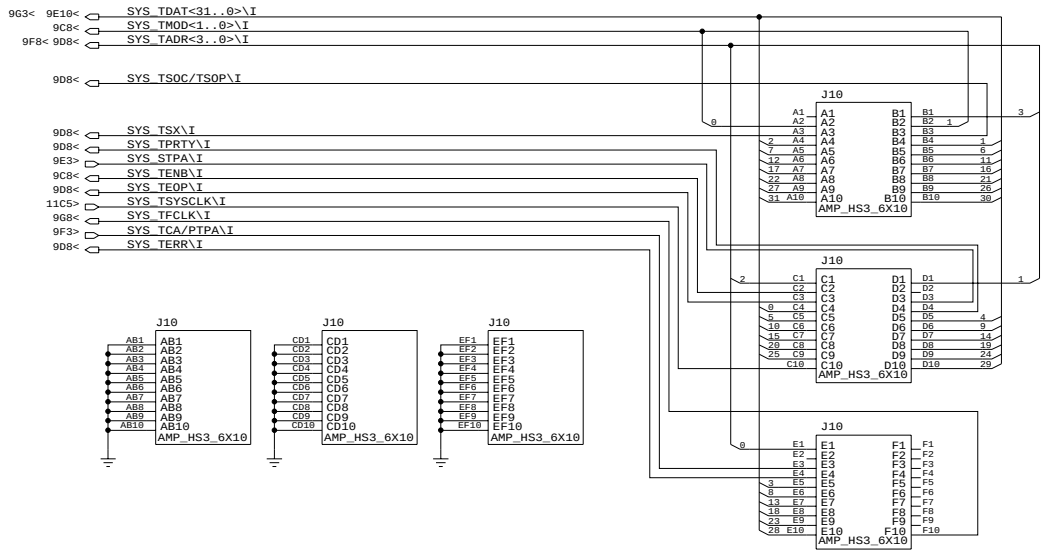
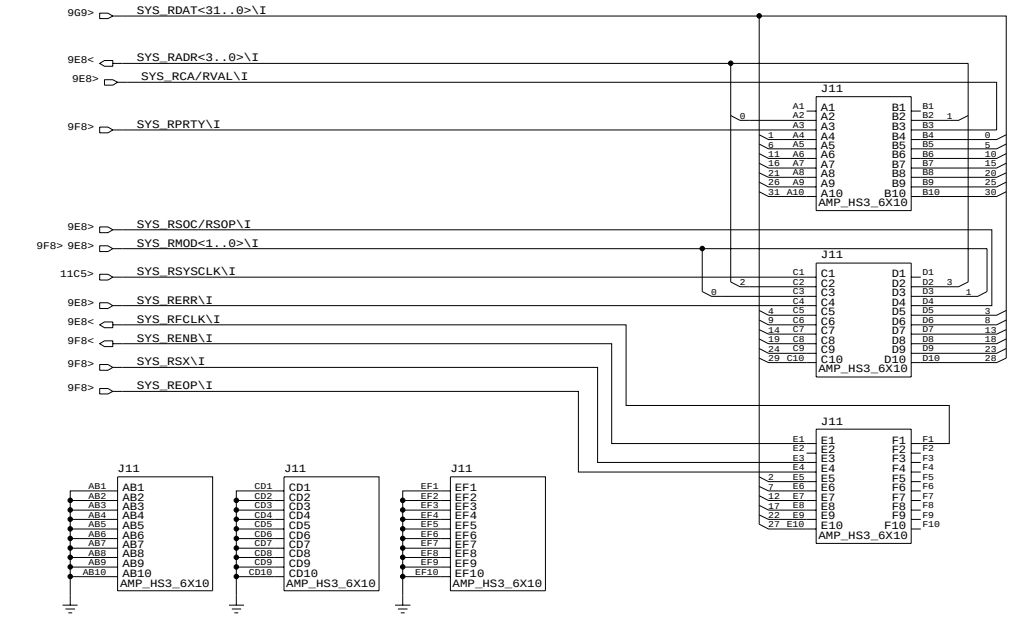
LAST_MODIFIED=Thu Dec 14 10:37:58 2000

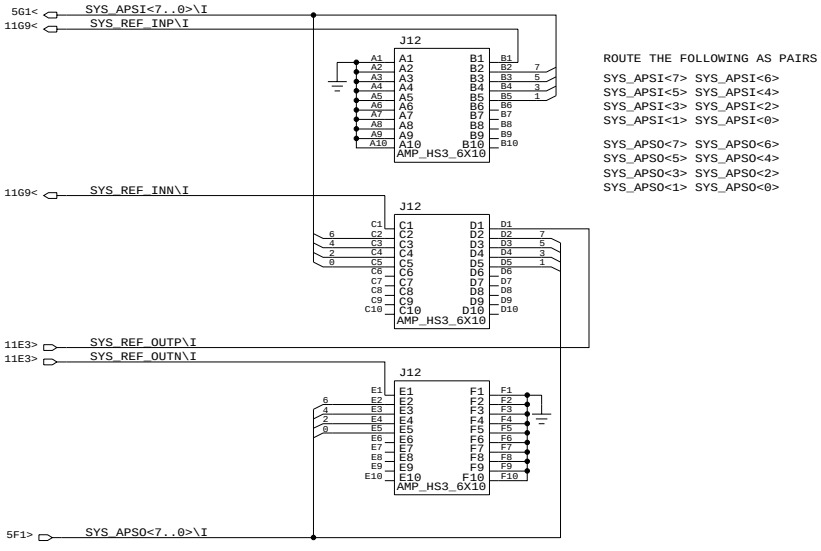
PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-1991414 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE: YY/MM/DD
TITLE: SUNI-16X155 REFERENCE DESIGN POWER_BLOCK	REVISION NUMBER: 3
ENGINEER: PMC	PAGE:14 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR







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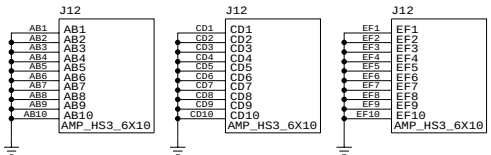

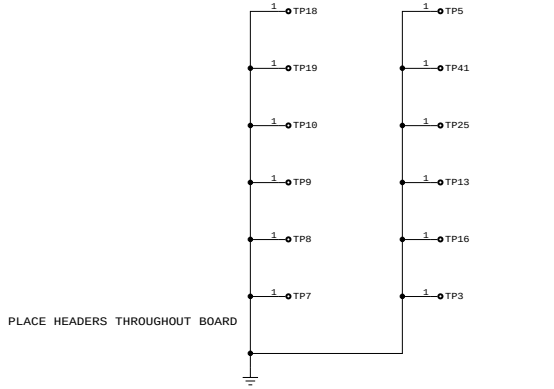

PLACE HEADERS THROUGHOUT BOARD

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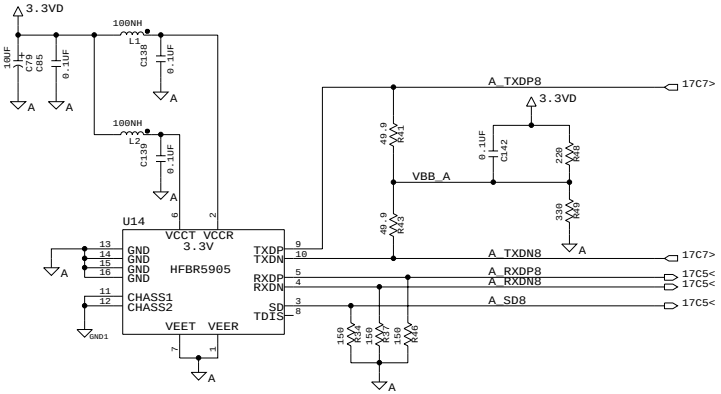
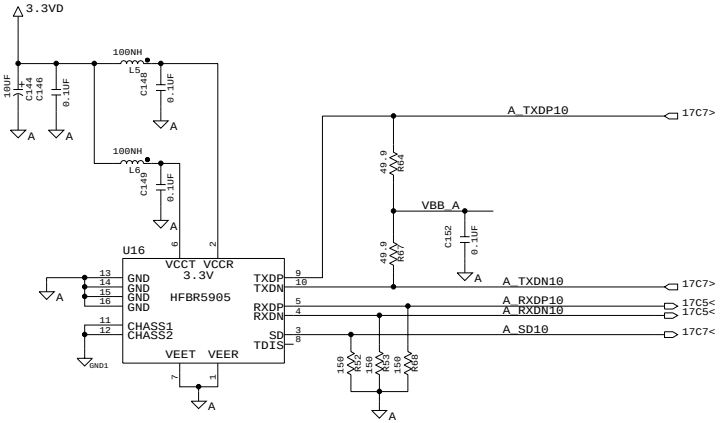
LAST_MODIFIED=Thu Dec 14 10:38:47 2000

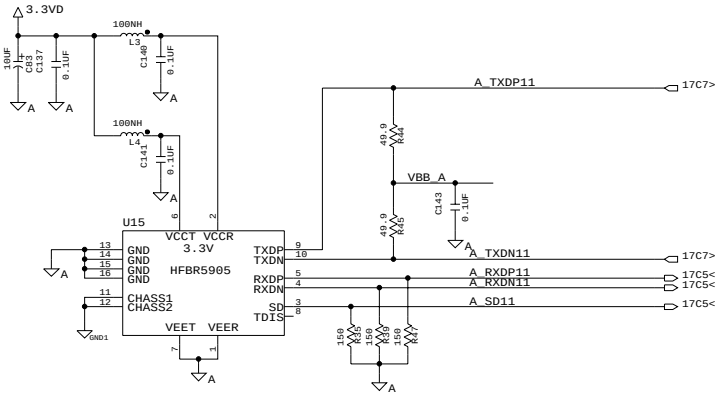
PMC-Sierra, Inc.

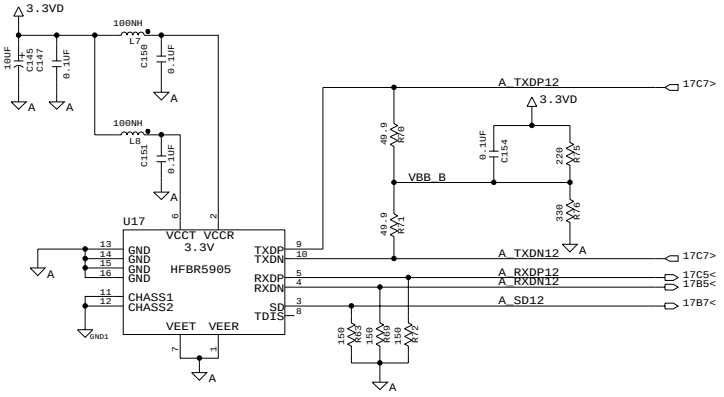
DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE:
TITLE: S/UNI-16X155 REFERENCE DESIGN SYSTEM INTERFACE	REVISION NUMBER: 1
ENGINEER: BDV GR	PAGE:15 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR









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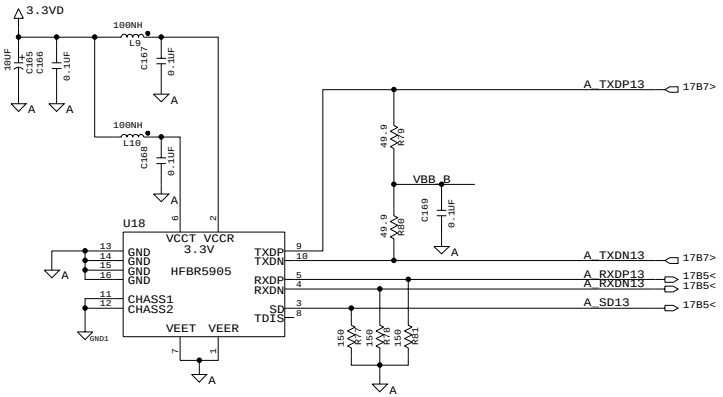
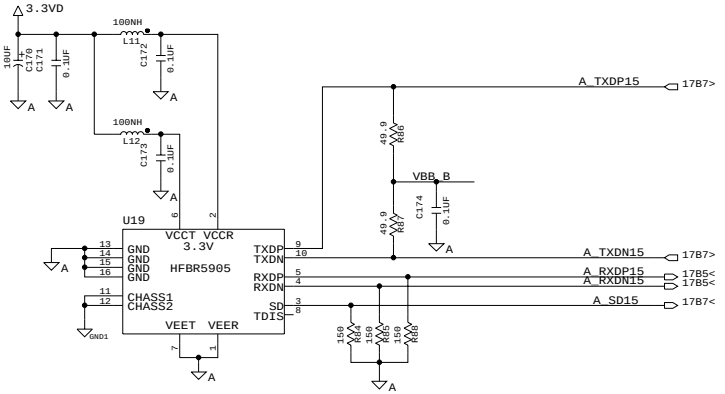
PMC-Sierra, Inc.

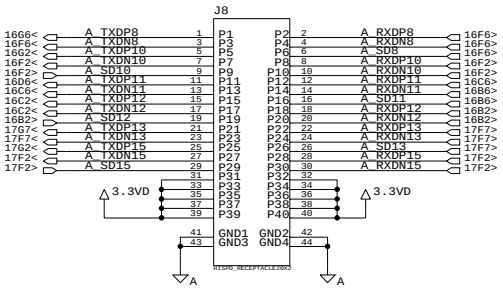
DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE:
TITLE: S/UNI 16X155 REFERENCE DESIGN OPTICS DAUGHTER CARD	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:16 OF 17

REVISIONS				
ZONE	REV	DESCRIPTION	DATE	APPR





PLACE MOUNTING HOLES ON CORNERS OF ADD ON BOARD
TO MOUNT TO MAIN BOARD



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PMC-Sierra, Inc.

DOCUMENT NUMBER: PMC-2000506 DOCUMENT ISSUE NUMBER: 1	ISSUE DATE:
TITLE: S/UNI 16X155 REFERENCE DESIGN OPTICS DAUGHTER CARD	REVISION NUMBER: 1.0
ENGINEER: BDV	PAGE:17 OF 17

10 PCB LAYOUT REVISION 1

11 BILL OF MATERIALS (BOM) REVISION 1

NO.	Part Number	Manufacturer	Ref Des	Description	Qty	Part Name - Value	Value	Build
1	ECU-V1H103KBV	PANASONIC	C70	CAP CERAMIC X7R 0603 50V 0.01UF	1	CAPS-0.01UF, 50V, X7R_603	0.01UF	16x155
2	ECJ-1VB1C104K	PANASONIC	C61, C65, C85, C86, C88, C90, C92, C94, C95, C97, C98, C100, C101, C103, C104, C106, C107, C109, C110, C112, C113, C116, C137-C143, C146-C154, C166-C169, C171-C174, C182-C199, C205, C206, C209-C212, C214-C217, C219-C222, C226, C231, C232, C236, C238-C241, C244, C246,	CAP CERAMIC X7R 0603 16V 0.1UF	116	CAPS-0.1UF, 16V, X7R_603	0.1UF	16x155

			C247, C250, C254-C264, C266, C268-C271, C273-C276, C278-C283					
3	ECS-T0JY106R	PANASONIC	C79, C83, C144, C145, C165, C170, C179-C181, C202, C203, C224, C242	CAP TANCAPA 6.3V 20% 10UF	13	CAPS_POL-10UF, 6.3V, TANCAPA	10UF	16x155
4	HFBR-5905	HEWLETT PACKARD	U8, U14-U19, U22-U25, U30, U32, U34, U35, U37	3.3V ATM TRANSCEIVER SONET OC-3/SDH STM-1	16	HFBR5905-3.3V	3.3V	16x155
5	QSE-020-01-F-D	SAMTEC	J9	CONNECTOR, SMD 2ROW, 20 POSITION/ROW, WITH GND	1	HISPD_HEADER20X2_QSE -BASE	?	16x155
6	QTE-020-03-F-D	SAMTEC	J8	RECEPTACLE FOR QSE HISPD CONNECTOR, SMD 2ROW, 20 POSITION/ROW, WITH GND	1	HISPD_RECEPTACLE20X2 _QTE-BASE	?	16x155
7	DIGI-KEY -- PCD1172CT-ND	PANASONIC	L1-L18, L21-L24, L27, L28, L31, L32	1.81	26	INDUCTOR-100NH, , PANASONIC	100NH	16x155
8	ERJ-3GSYJ103V	PANASONIC	R89	RES 0603 1/16W 5% 10K OHM	1	RES-10K, 5%, 603	10K	16x155
9	ERJ-	PANASONIC	R116	RES 0603	1	RES-124, 1%, 603	124	16x155

	3EKF1240V			1/16W 1% 124 OHM				
10	ERJ-3EKF1500V	PANASONIC	R34, R35, R37, R39, R46, R47, R52, R53, R63, R68, R69, R72, R77, R78, R81, R84, R85, R88, R92-R96, R101, R117, R118, R124, R173, R175, R178, R180, R185, R186, R204, R206, R212, R233, R235, R239	RES 0603 1/16W 1% 150 OHM	39	RES-150, 1%, 603	150	16x155
11	ERJ-3GSYJ221V	PANASONIC	R48, R75, R187, R218, R245	RES 0603 1/16W 5% 220 OHM	5	RES-220, 5%, 603	220	16x155
12	ERJ-3GSYJ331V	PANASONIC	R49, R76, R188, R219, R246	RES 0603 1/16W 5% 330 OHM	5	RES-330, 5%, 603	330	16x155
13	ERJ-3EKF49R9V	PANASONIC	R41, R43-R45, R64, R67, R70, R71, R79, R80, R86, R87, R97-R100, R122, R123, R181-R184, R209, R210, R236, R237	RES 0603 1/16W 1% 49.9 OHM	26	RES-49.9, 1%, 603	49.9	16x155
14	ERJ-	PANASONIC	R115	RES 0603	1	RES-82.5, 1%, 603	82.5	16x155

	3EKF82R5V			1/16W 1% 82.5 OHM				
15	NU	NU	R74, R82	RES NOT USED ON BOARD 0603 PACKAGE	2	RES-NU, NU, NU_603	NU	16x155
16	NU	NU	R141, R147, R150, R153	RES NOT USED ON BOARD 0805 PACKAGE	4	RES-NU, NU, NU_805	NU	16x155
17	DIGI-KEY -- P<VALUE>CCT-ND	?	R157-R160, R163, R164, R193-R198, R224-R227, R249-R252, R255, R256, R258, R259, R268, R270-R272, R277-R280	?	32	RESISTOR-158, 1%, 805	158	16x155
18	PANASONIC -- EXB-V8V472JV	?	RN86, RN87, RN90, RN91	?	4	RES_ARRAY_4_SMD-4.7K	4.7K	16x155
19	131-3701-341	JOHNSON COMPONENTS	J6, J7	50 OHM RIGHT ANGLE BULKHEAD JACK RECEPTACLE	2	SMB_RIGHT_ANGLE-BASE	?	16x155
20	PM5382 S/UNI 15X155	PMC SIERRA	U9	IC SATURN USER NETWORK INTERFACE(16X155)	1	SUNI16X155_SBGA-BASE	?	16x155
21	08055C473JATN	AVX	C200, C218, C265, C267	CAP CERAMIC X7R 0850 50V	4	CAPS-0.047UF, 50V, X7R_805	0.047UF	4X622

				0.047UF				
22	ECJ-1VB1C104K	PANASONIC	C87, C89, C91, C93, C96, C99, C102, C105, C108, C111, C125, C128, C134-C136, C228, C233, C234, C237	CAP CERAMIC X7R 0603 16V 0.1UF	19	CAPS-0.1UF, 16V, X7R_603	0.1UF	4X622
23	GRM42-2X5R106K10	MURATA	C120, C122, C132, C133	CAP CERAMIC X5R 1210 10V 10UF	4	CAPS-10UF, 10V, X5R_1210	10UF	4X622
24	ECS-T0JY106R	PANASONIC	C227	CAP TANCAPA 6.3V 20% 10UF	1	CAPS_POL-10UF, 6.3V, TANCAPA	10UF	4X622
25	ECS-H0JD476R	PANASONIC	C80, C114, C130, C131	CAP TANCAPD 6.3V 20% 47UF	4	CAPS_POL-47UF, 6.3V, TANCAPD	47UF	4X622
26	HFCT-5908E	HP	U36	ATM FIBER TRANSCEIVERS FOR SONET OC-12/SDH STM-4 2X5 PACKGE	1	HFCT5908E_THRU-BASE	HFCT-5908E	4X622
27	DIGI-KEY -- PCD1172CT-ND	PANASONIC	L29, L30	1.81	2	INDUCTOR-100NH, , PANASONIC	100NH	4X622
28	ERJ-6GEY0R00V	PANASONIC	R125, R142, R230, R231	RES 0805 1/10W 5% ZERO OHM	4	RES-0, 5%, 805	0	4X622
29	ERJ-3EKF1500V	PANASONIC	R213, R214, R217	RES 0603 1/16W 1% 150 OHM	3	RES-150, 1%, 603	150	4X622
30	ERJ-3EKF2001V	PANASONIC	R199	RES 0603 1/16W 5% 2.00K OHM	1	RES-2.00K, 1%, 603	2.00K	4X622
31	ERJ-3GSYJ4R7V	PANASONIC	R54, R55, R60, R61	RES 0603 1/16W 5%	4	RES-4.7, 5%, 603	4.7	4X622

				4.7 OHM				
32	ERJ-3EKF49R9V	PANASONIC	R215, R216	RES 0603 1/16W 1% 49.9 OHM	2	RES-49.9, 1%, 603	49.9	4X622
33	ERJ-3EKF63R4V	PANASONIC	R222	RES 0603 1/16W 1% 63.4 OHM	1	RES-63.4, 1%, 603	63.4	4X622
34	NU	NU	R83	RES NOT USED ON BOARD 0603 PACKAGE	1	RES-NU, NU, NU_603	NU	4X622
35	NU	NU	R148, R149, R154, R155	RES NOT USED ON BOARD 0805 PACKAGE	4	RES-NU, NU, NU_805	NU	4X622
36	MC100LVEL16D	MOTOROLA	U13	IC DIFFERENTIAL RECEIVER SOIC 8	1	100LVEL16_SOIC-BASE	?	BOTH
37	PI49FCT3807CQ	PERICOM	U10	IC 3.3V 1:10 CMOS CLOCK DRIVER QSOP20 C GRADE	1	49FCT3807_QSOP20_C-B ASE	?	BOTH
38	SN74AHC1G08DCKR	TI	U4	IC SINGLE 2-INPUT POSITIVE AND GATE	1	74AHC1G08_DCK-BASE	?	BOTH
39	120673-1	AMP	J10-J12	Z-PACK 6 ROW HS3 BACKPLANE CONNECTOR, RIGHT ANGLE RECEPTACLE	3	AMP_HS3_6X10_FEMALE_ RA	?	BOTH
40	ECU-V1H103KBV	PANASONIC	C7	CAP CERAMIC X7R 0603 50V 0.01UF	1	CAPS-0.01UF, 50V, X7R_603	0.01UF	BOTH
41	ECU-V1H473KBW	PANASONIC	C8	CAP CERAMIC X7R 1206 50V 0.047UF	1	CAPS-0.047UF, 50V, X7R_1206	0.047UF	BOTH
42	ECJ-	PANASONIC	C1-C6,	CAP	78	CAPS-0.1UF, 16V,	0.1UF	BOTH

	1VB1C104K		C10-C46, C57, C64, C66-C69, C72, C82, C117, C124, C126, C127, C129, C155-C158, C160, C161, C163, C164, C176, C178, C204, C207, C208, C213, C225, C229, C230, C235, C245, C248, C249, C251	CERAMIC X7R 0603 16V 0.1UF		X7R_603		
43	GRM42-2X5R106K10	MURATA	C71, C73, C115, C118, C119, C121, C123, C159, C162	CAP CERAMIC X5R 1210 10V 10UF	9	CAPS-10UF, 10V, X5R_1210	10UF	BOTH
44	ECS-H1CC106R	PANASONIC	C47-C55	CAP TANCAPC 16V 20% 10UF	9	CAPS_POL-10UF, 16V, TANCAPC	10UF	BOTH
45	ECS-T0JY106R	PANASONIC	C58, C60, C63, C75-C78, C81, C84, C175, C177, C201, C223, C243, C272, C277	CAP TANCAPA 6.3V 20% 10UF	16	CAPS_POL-10UF, 6.3V, TANCAPA	10UF	BOTH

46	ECE-V1AA221P	PANASONIC	C9	CAP ELECTRO VA SMD 10V 20% 220UF	1	CAPS_POL-220UF, 10V, ELECTRO VA A	220UF	BOTH
47	ECS-H0JD476R	PANASONIC	C56, C59, C62, C74	CAP TANCAPD 6.3V 20% 47UF	4	CAPS_POL-47UF, 6.3V, TANCAPD	47UF	BOTH
48	DL4148MS	MICROSEMI	D5	DIODE RECT 150MA 75V SMT MINIMELF	1	DL4148_SOD80C-BASE	?	BOTH
49	PZC36SAAN	SULLINS ELECTRONICS	J5	CONN HEADER STRAIGHT 36POS MALE .1" SINGLE ROW	1	HEADER6_100MIL-BASE	?	BOTH
50	PZC36DAAN	SULLINS	J2	CONN HEADER 2 ROW 0.1"X0.1" 2X16	1	HEADER_16X2_CONN_MAL E-BASE	?	BOTH
51	PZC36DAAN	SULLINS ELECTRONICS	J4	CONN HEADER STRAIGHT 6POS MALE .1" DUAL ROW 3X2	1	HEADER_3X2_100 MIL-BA SE	HEADER 3X2	BOTH
52	DIGI-KEY S1011-36-ND	?	J3	100 MIL SPACING HEADER	1	HEADER_9_100 MIL-BASE	?	BOTH
53	QSE-020-01-F-D	SAMTEC	J13, J14	CONNECTOR, SMD 2ROW, 20 POSITION/ ROW, WITH GND	2	HISPD_HEADER20X2_QSE -BASE	?	BOTH
54	DIGI-KEY -- PCD1172CT-ND	PANASONIC	L19, L20, L25, L26, L33, L34	1.81	6	INDUCTOR-100NH, , PANASONIC	100NH	BOTH
55	IRF7413	INTERNATIONA L RECTIFIER	Q1, Q2	IC POWER MOSFET	2	IRF7413_SOIC-BASE	?	BOTH
56	LP3966ES-1.8	NATIONAL SEMI	U12	3A FAST ULTRA LOW DROPOUT	1	LP3966ES-1_8_SMT_REG -BASE	?	BOTH

				LINEAR REGULATOR 1.8V TO263-5				
57	LP3966ES-2.5	NATIONAL SEMI	U33	3A FAST ULTRA LOW DROPOUT LINEAR REGULATOR 2.5V TO263-5	1	LP3966ES-2_5_SMT_REG - BASE	?	BOTH
58	LT1117CST	LINEAR TECHNOLOGIES	U3	REGULATOR ADJUSTABLE SOT223 800MA OUTPUT	1	LT1117CST_SOT-ADJ	ADJ	BOTH
59	LT1129CQ-3.3	LINEAR TECHNOLOGIES	U27	REGULATOR 3.3V FIXED MICROPOWER LOW DROPOUT	1	LT1129CQ-3_TO263-3.3 V	3.3V	BOTH
60	LTC1643L1CGN	LINEAR TECHNOLOGY	U2	IC CPCI HOT SWAP CONTROLLER W/ 12V POWERGD DISABLED	1	LTC1643L_SSOP-1-BASE	?	BOTH
61	LTC1728ES5-5	LINEAR TECHNOLOGY	U26	DISCRETE MICROPOWER PRECISION TRIPLE SUPPLY MONITORS SOT23-5	1	LTC1728ES5_5_SOIC-BA SE	?	BOTH
62	MAX811TEUS-T	MAXIM	U6	IC 4 PIN UP VOLTAGE MONITOR WITH MANUAL RESET INPUT 3.08V SOT143	1	MAX811T_SOT143-BASE	?	BOTH
63	MC100LVEL17DW	MOTOROLA	U31	QUAD LV PECL	1	MC100LVEL17DW_SOIC20 -BASE	?	BOTH

				DIFFERENTIAL LINE RECEIVER				
64	MC100LVELT22D	MOTOROLA SEMICONDUCTO R	U28	IC DUAL DIFFERENTIAL LVTTL/LVCMOS TO LVPECL TRANSLATOR SOIC8	1	MC100LVELT22D_SOIC8- BASE	?	BOTH
65	614-93-308-31-012	MILL MAX	U1	SOCKET FOR PART# NM93CS66LEN	1	NM93CS66LEN_DIP8_SOC KET-BASE	?	BOTH
66	MMD MB3100HH-100.000M HZ	?	U20	<PLEASE USE FROM APPS.LIB LIBRARY OSC_CMOS_BETA>	1	OSC_CMOS_8PIN_DUAL-H CMOS, 100.0A	100.000MHZ	BOTH
67	CONNOR WINFIELD -- EE14-541	?	Y1	77.76 MHZ, LVPECL OSCILLATOR, 20 PPM, 3.3V	1	OSC_PECL_3.3V-77.76M HZ, 20 PPM	77.76 MHZ	BOTH
68	DIGIKEY -- CKN4002-ND	?	SW1	RIGHT ANGLE PCB MOUNT SPST PUSH BUTTOM	1	PBNO_RIGHT_ANGLE-BAS E	?	BOTH
69	PCI9054-AB50PI	PLX TECHNOLOGY	U11	IC PCI-TO-LOCAL BUS	1	PCI9054_PQFP-BASE	?	BOTH
70	WSL2512-R01-1	VISHAY	R5, R14, R15	RES 2512 1W 1% 0.01 OHM	3	RES-0.01, 1%, 2512	0.01	BOTH
71	ERJ-3GSYJ1R0V	PANASONIC	R17	RES 0603 1/16W 5% 1 OHM	1	RES-1, 5%, 603	1	BOTH
72	ERJ-3GSYJ122V	PANASONIC	R2, R21	RES 0603 1/16W 5% 1.2K OHM	2	RES-1.2K, 5%, 603	1.2K	BOTH
73	ERJ-3GSYJ100V	PANASONIC	R6, R8, R29, R65, R66, R90	RES 0603 1/16W 5% 10 OHM	6	RES-10, 5%, 603	10	BOTH
74	ERJ-3EKF1000V	PANASONIC	R9, R120, R121, R152	RES 0603 1/16W 1% 100 OHM	4	RES-100, 1%, 603	100	BOTH

75	ERJ-3GSYJ104V	PANASONIC	R28	RES 0603 1/16W 5% 100K OHM	1	RES-100K, 5%, 603	100K	BOTH
76	ERJ-3GSYJ103V	PANASONIC	R33	RES 0603 1/16W 5% 10K OHM	1	RES-10K, 5%, 603	10K	BOTH
77	ERJ-8GEYJ106V	PANASONIC	R1, R30, R31	RES 1206 1/8W 5% 10M OHM	3	RES-10M, 5%, 1206	10M	BOTH
78	ERJ-3GSYJ131V	PANASONIC	R24	RES 0603 1/16W 5% 130 OHM	1	RES-130, 5%, 603	130	BOTH
79	ERJ-3GSYJ150V	PANASONIC	R56, R57, R59	RES 0603 1/16W 5% 15 OHM	3	RES-15, 5%, 603	15	BOTH
80	ERJ-3EKF1500V	PANASONIC	R10, R18, R36, R38, R40, R42, R50, R126-R128, R131-R135, R172, R174, R179, R203, R205, R211, R234, R238, R242	RES 0603 1/16W 1% 150 OHM	24	RES-150, 1%, 603	150	BOTH
81	ERJ-3EKF2001V	PANASONIC	R129	RES 0603 1/16W 5% 2.00K OHM	1	RES-2.00K, 1%, 603	2.00K	BOTH
82	ERJ-3GSYJ202V	PANASONIC	R3, R4	RES 0603 1/16W 5% 2.0K OHM	2	RES-2.0K, 5%, 603	2.0K	BOTH
83	ERJ-3GSYJ222V	PANASONIC	R22, R73	RES 0603 1/16W 5% 2.2K OHM	2	RES-2.2K, 5%, 603	2.2K	BOTH
84	ERJ-6GEYJ240V	PANASONIC	R23	RES 0805 1/10W 5% 24 OHM	1	RES-24, 5%, 805	24	BOTH
85	ERJ-3GSYJ330V	PANASONIC	R32, R112	RES 0603 1/16W 5% 33 OHM	2	RES-33, 5%, 603	33	BOTH
86	ERJ-3GSYJ331V	PANASONIC	R91, R114	RES 0603 1/16W 5% 330 OHM	2	RES-330, 5%, 603	330	BOTH
87	ERJ-3EKF39R2V	PANASONIC	R16	RES 0603 1/16W 1%	1	RES-39.2, 1%, 603	39.2	BOTH

				39.2 OHM				
88	ERJ-3GSYJ4R7V	PANASONIC	R58	RES 0603 1/16W 5% 4.7 OHM	1	RES-4.7, 5%, 603	4.7	BOTH
89	ERJ-3GSYJ472V	PANASONIC	R7, R19, R20, R25, R26, R51, R130, R136, R143, R151, R283, R284	RES 0603 1/16W 5% 4.7K OHM	12	RES-4.7K, 5%, 603	4.7K	BOTH
90	ERJ-3EKF49R9V	PANASONIC	R62, R102, R104, R105, R107, R108, R110, R111, R119, R176, R177, R207, R208, R240, R241	RES 0603 1/16W 1% 49.9 OHM	15	RES-49.9, 1%, 603	49.9	BOTH
91	ERJ-3GSYJ560V	PANASONIC	R27	RES 0603 1/16W 5% 56 OHM	1	RES-56, 5%, 603	56	BOTH
92	ERJ-3GSYJ561V	PANASONIC	R12, R13	RES 0603 1/16W 5% 560 OHM	2	RES-560, 5%, 603	560	BOTH
93	ERJ-3EKF63R4V	PANASONIC	R11, R103, R106, R109, R113	RES 0603 1/16W 1% 63.4 OHM	5	RES-63.4, 1%, 603	63.4	BOTH
94	NU	NU	R144, R145	RES NOT USED ON BOARD 0603 PACKAGE	2	RES-NU, NU, NU_603	NU	BOTH
95	DIGI-KEY -- P<VALUE>ECT-ND	?	R137-R140	?	4	RESISTOR-10, 5%, 1206	10	BOTH
96	PANASONIC -- EXB-V8V100JV	?	RN37, RN38, RN40, RN42, RN48,	?	13	RES_ARRAY_4_SMD-10	RES ARRAY_4 5% 10 OHM	BOTH

			RN49, RN52, RN55-RN57, RN62-RN64					
97	PANASONIC -- EXB-V8V103JV	?	RN27, RN35, RN36, RN43, RN45-RN47, RN53, RN54, RN58, RN60, RN61, RN65	?	13	RES_ARRAY_4_SMD-10K	RES ARRAY_4 5% 10K OHM	BOTH
98	PANASONIC -- EXB-V8V102JV	?	RN44, RN59	?	2	RES_ARRAY_4_SMD-1K	RES ARRAY_4 5% 1K OHM	BOTH
99	PANASONIC -- EXB-V8V330JV	?	RN7, RN8, RN10-RN15, RN23, RN28-RN33, RN39, RN41, RN50, RN66-RN69, RN71-RN84, RN88, RN89	?	38	RES_ARRAY_4_SMD-33	RES ARRAY_4 5% 33 OHM	BOTH
100	PANASONIC -- EXB-V8V472JV	?	RN1-RN5, RN16, RN34, RN51, RN85	?	9	RES_ARRAY_4_SMD-4.7K	4.7K	BOTH
101	750101R200	CTS	RN6	BUSSED RESISTOR NETWORK 200 OHM SIP10	1	RSIP9-200	200	BOTH
102	SSF-LXH5147LGD	LUMEX	D2-D4	LED QUAD GREEN HORIZONT	3	SSF_LXH5147-GREEN	GREEN	BOTH

				AL				
103	SY100EL57LZC	SYNERGY	U29	4:1 DIFFERENTIAL MULTIPLEXER	1	SY100EL57L_SOIC-BASE	?	BOTH
104	UNR-3.3/8-D5	DATEL	U21	DC/DC CONVERTER, 5V TO 3.3V, 26W, 8 AMP	1	UNR3V5-8-D5	8-D5	BOTH
105	540-99-044-17-400 000	MILL MAX MANUFACTURIN G	U7	IC CONFIGURABLE OTP EPROM PLCC44 SOCKETED	1	XC1702L_PC44C_SOCKET -BASE	?	BOTH
106	XCV200E-6BG352C	XILINX	U5	IC HIGH DENSITY 1.8V VIRTEX FPGA (352BGA PACKAGE)	1	XCV200E-6BG352C_BGA-BASE	?	BOTH
107	ZM4742A	DIODES INC	D1	ZENER DIODE 12.0V 5% 1.0W SURFACE MOUNT	1	ZENERDIODE-12.0V_1W	12.0V_1W	BOTH
108	352068-1	AMP	J1	CONNECTOR ZPACK CPCI 2MM HM 110 POS. TYPE A WITH GND SHIELD	1	ZPACK5X22FH_ASCPCI_2 MM	?	BOTH

NOTES

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