



FAST CMOS OCTAL TRANSPARENT LATCH

IDT54/74FCT573T/AT/CT

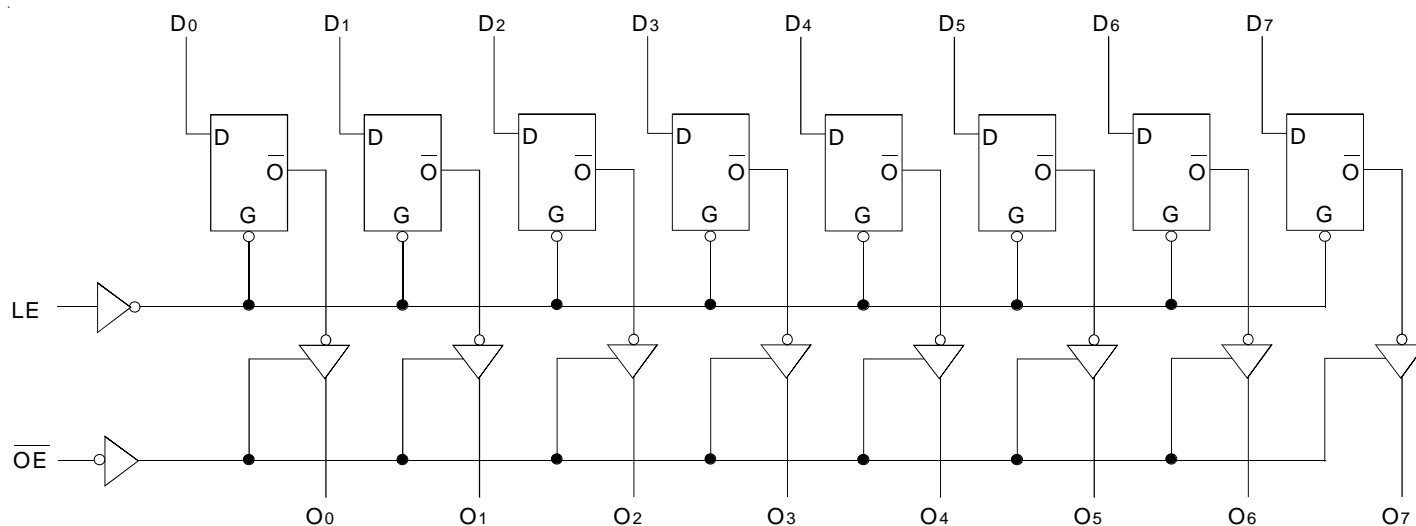
FEATURES:

- Std., A, and C grades
- Low input and output leakage $\leq 1\mu\text{A}$ (max.)
- CMOS power levels
- True TTL input and output compatibility:
 - $V_{OH} = 3.3V$ (typ.)
 - $V_{OL} = 0.3V$ (typ.)
- High Drive outputs (-15mA I_{OH} , 48mA I_{OL})
- Meets or exceeds JEDEC standard 18 specifications
- Military product compliant to MIL-STD-883, Class B and DESC listed (dual marked)
- Power off disable outputs permit "live insertion"
- Available in the following packages:
 - Industrial: SOIC, SSOP, QSOP, TSSOP
 - Military: CERDIP, LCC

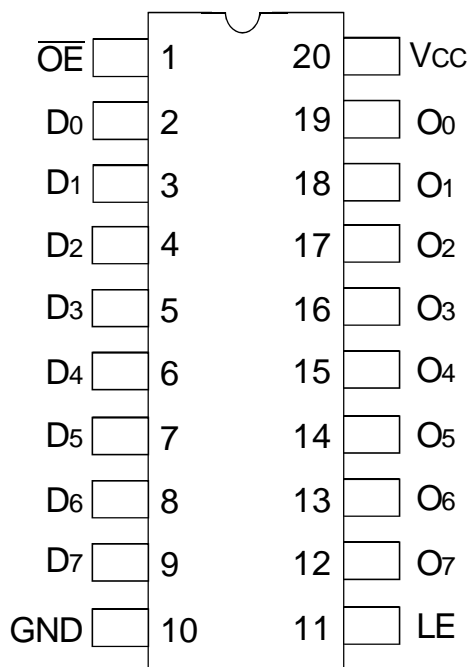
DESCRIPTION:

The FCT573T is an octal transparent latch built using an advanced dual metal CMOS technology. These octal latches have 3-state outputs and are intended for bus oriented applications. The flip-flops appear transparent to the data when Latch Enable (LE) is high. When LE is low, the data that meets the set-up time is latched. Data appears on the bus when the Output Enable (\overline{OE}) is low. When \overline{OE} is high, the bus output is in the high-impedance state.

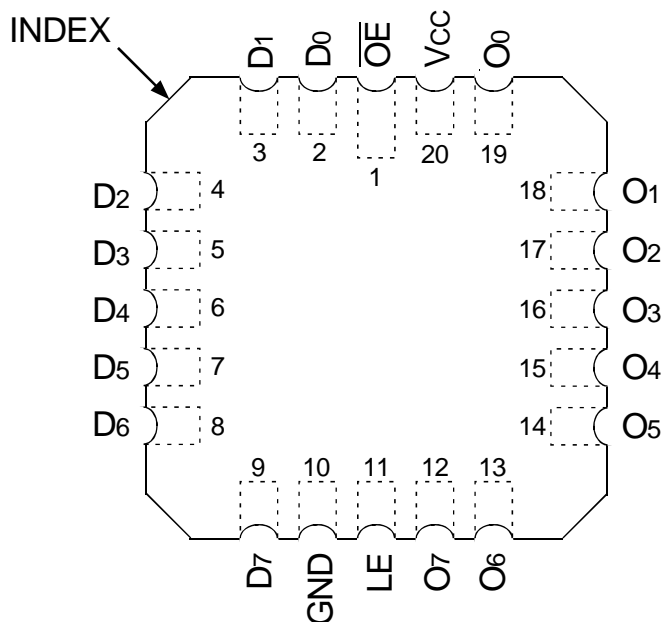
FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



CERDIP/ SOIC/ SSOP/ QSOP/ TSSOP
TOP VIEW



LCC
TOP VIEW

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Symbol	Description	Max	Unit
V _{TERM} ⁽²⁾	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} ⁽³⁾	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +120	mA

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability. No terminal voltage may exceed V_{CC} by +0.5V unless otherwise noted.
- Inputs and V_{CC} terminals only.
- Output and I/O terminals only.

CAPACITANCE (T_A = +25°C, F = 1.0MHz)

Symbol	Parameter ⁽¹⁾	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	6	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	8	12	pF

NOTE:

- This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
D _x	Data Inputs
LE	Latch Enable Input (Active HIGH)
\overline{OE}	Output Enable Input (Active LOW)
O _x	3-State Outputs

FUNCTION TABLE⁽¹⁾

Inputs			Outputs
D _x	LE	\overline{OE}	O _x
H	H	L	H
L	H	L	L
X	X	H	Z

NOTE:

- H = HIGH Voltage Level
X = Don't Care
L = LOW Voltage Level
Z = High Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 5\%$; Military: $T_A = -55^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{IH}	Input HIGH Level	Guaranteed Logic HIGH Level		2	—	—	V
V_{IL}	Input LOW Level	Guaranteed Logic LOW Level		—	—	0.8	V
I_{IH}	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 2.7\text{V}$	—	—	± 1	μA
I_{IL}	Input LOW Current ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_I = 0.5\text{V}$	—	—	± 1	μA
I_{OZH}	High Impedance Output Current (3-State output pins) ⁽⁴⁾	$V_{CC} = \text{Max.}$	$V_O = 2.7\text{V}$	—	—	± 1	μA
I_{OZL}			$V_O = 0.5\text{V}$	—	—	± 1	
I_I	Input HIGH Current ⁽⁴⁾	$V_{CC} = \text{Max.}, V_I = V_{CC} (\text{Max.})$		—	—	± 1	μA
V_{IK}	Clamp Diode Voltage	$V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$		—	-0.7	-1.2	V
V_H	Input Hysteresis	—		—	200	—	mV
I_{CC}	Quiescent Power Supply Current	$V_{CC} = \text{Max.}, V_{IN} = \text{GND or } V_{CC}$		—	0.01	1	mA

OUTPUT DRIVE CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
V_{OH}	Output HIGH Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OH} = -6\text{mA MIL}$ $I_{OH} = -8\text{mA IND}$	2.4	3.3	—	V
			$I_{OH} = -12\text{mA MIL}$ $I_{OH} = -15\text{mA IND}$	2	3	—	
V_{OL}	Output LOW Voltage	$V_{CC} = \text{Min.}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$	$I_{OL} = 32\text{mA MIL}$ $I_{OL} = 48\text{mA IND}$	—	0.3	0.5	V
I_{OS}	Short Circuit Current	$V_{CC} = \text{Max.}, V_O = \text{GND}^{(3)}$		-60	-120	-225	mA
I_{OFF}	Input/Output Power Off Leakage ⁽⁵⁾	$V_{CC} = 0\text{V}, V_{IN} \text{ or } V_O \leq 4.5\text{V}$		—	—	± 1	μA

NOTES:

1. For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
3. Not more than one output should be tested at one time. Duration of the test should not exceed one second.
4. The test limit for this parameter is $\pm 5\mu\text{A}$ at $T_A = -55^{\circ}\text{C}$.
5. This parameter is guaranteed but not tested.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	$V_{CC} = \text{Max.}$ $V_{IN} = 3.4V^{(3)}$		—	0.5	2	mA
I_{CCD}	Dynamic Power Supply Current ⁽⁴⁾	$V_{CC} = \text{Max.}$ Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	0.15	0.25	mA/ MHz
I_C	Total Power Supply Current ⁽⁶⁾	$V_{CC} = \text{Max.}$ Outputs Open $f_i = 10\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ One Bit Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	1.5	3.5	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	1.8	4.5	
		$V_{CC} = \text{Max.}$ Outputs Open $f_i = 2.5\text{MHz}$ 50% Duty Cycle $\overline{OE} = \text{GND}$ $LE = V_{CC}$ Eight Bits Toggling	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	—	3	6 ⁽⁵⁾	mA
			$V_{IN} = 3.4V$ $V_{IN} = \text{GND}$	—	5	14 ⁽⁵⁾	

NOTES:

- For conditions shown as Min. or Max., use appropriate value specified under Electrical Characteristics for the applicable device type.
 - Typical values are at $V_{CC} = 5.0V$, $+25^\circ\text{C}$ ambient.
 - Per TTL driven input: ($V_{IN} = 3.4V$). All other inputs at V_{CC} or GND .
 - This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
 - Values for these conditions are examples of ΔI_{CC} formula. These limits are guaranteed but not tested.
 - $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_i N_i)$
 $I_{CC} = \text{Quiescent Current}$
 $\Delta I_{CC} = \text{Power Supply Current for a TTL High Input } (V_{IN} = 3.4V)$
 $D_H = \text{Duty Cycle for TTL Inputs High}$
 $N_T = \text{Number of TTL Inputs at } D_H$
 $I_{CCD} = \text{Dynamic Current caused by an Input Transition Pair (HLH or LHL)}$
 $f_{CP} = \text{Clock Frequency for Register Devices (Zero for Non-Register Devices)}$
 $f_i = \text{Output Frequency}$
 $N_i = \text{Number of Outputs at } f_i$
- All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL

Symbol	Parameter	Condition ⁽¹⁾	74FCT573AT		74FCT573CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay Dx to Ox	CL = 50pF RL = 500Ω	1.5	5.2	1.5	4.2	ns
t _{PLH} t _{PHL}	Propagation Delay LE to Ox		2	8.5	2	5.5	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	6.5	1.5	5.5	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	5.5	1.5	5	ns
t _{SU}	Set-up Time, HIGH or LOW Dx to LE		2	—	2	—	ns
t _H	Hold Time, HIGH or LOW Dx to LE		1.5	—	1.5	—	ns
t _w	LE Pulse Width HIGH ⁽³⁾		5	—	5	—	ns

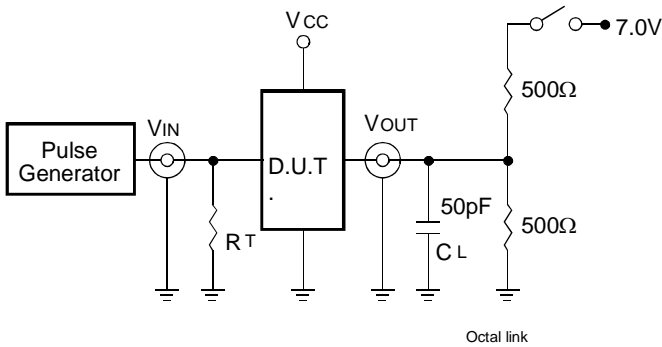
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - MILITARY

Symbol	Parameter	Condition ⁽¹⁾	54FCT573T		54FCT573AT		54FCT573CT		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay Dx to Ox	CL = 50pF RL = 500Ω	1.5	8.5	1.5	5.6	1.5	5.1	ns
t _{PLH} t _{PHL}	Propagation Delay LE to Ox		2	15	2	9.8	2	8	ns
t _{PZH} t _{PZL}	Output Enable Time		1.5	13.5	1.5	7.5	1.5	6.3	ns
t _{PHZ} t _{PLZ}	Output Disable Time		1.5	10	1.5	6.5	1.5	5.9	ns
t _{SU}	Set-up Time, HIGH or LOW Dx to LE		2	—	2	—	2	—	ns
t _H	Hold Time, HIGH or LOW Dx to LE		1.5	—	1.5	—	1.5	—	ns
t _w	LE Pulse Width HIGH ⁽³⁾		6	—	6	—	6	—	ns

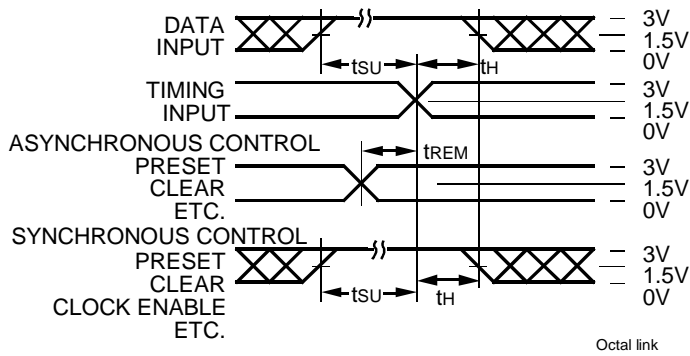
NOTES:

1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This limit is guaranteed but not tested.

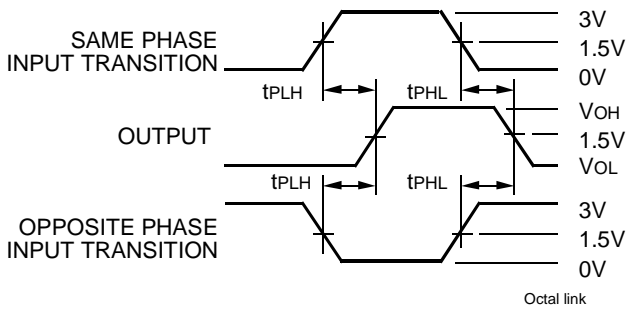
TEST CIRCUITS AND WAVEFORMS



Test Circuits for All Outputs



Set-Up, Hold, and Release Times



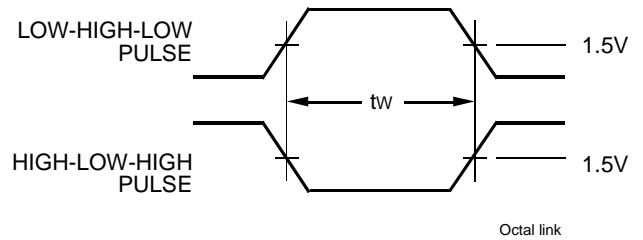
Propagation Delay

SWITCH POSITION

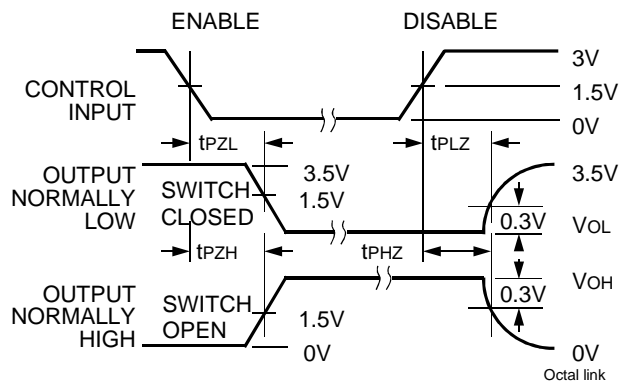
Test	Switch
Open Drain Disable Low Enable Low	Closed
All Other Tests	Open

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



Pulse Width

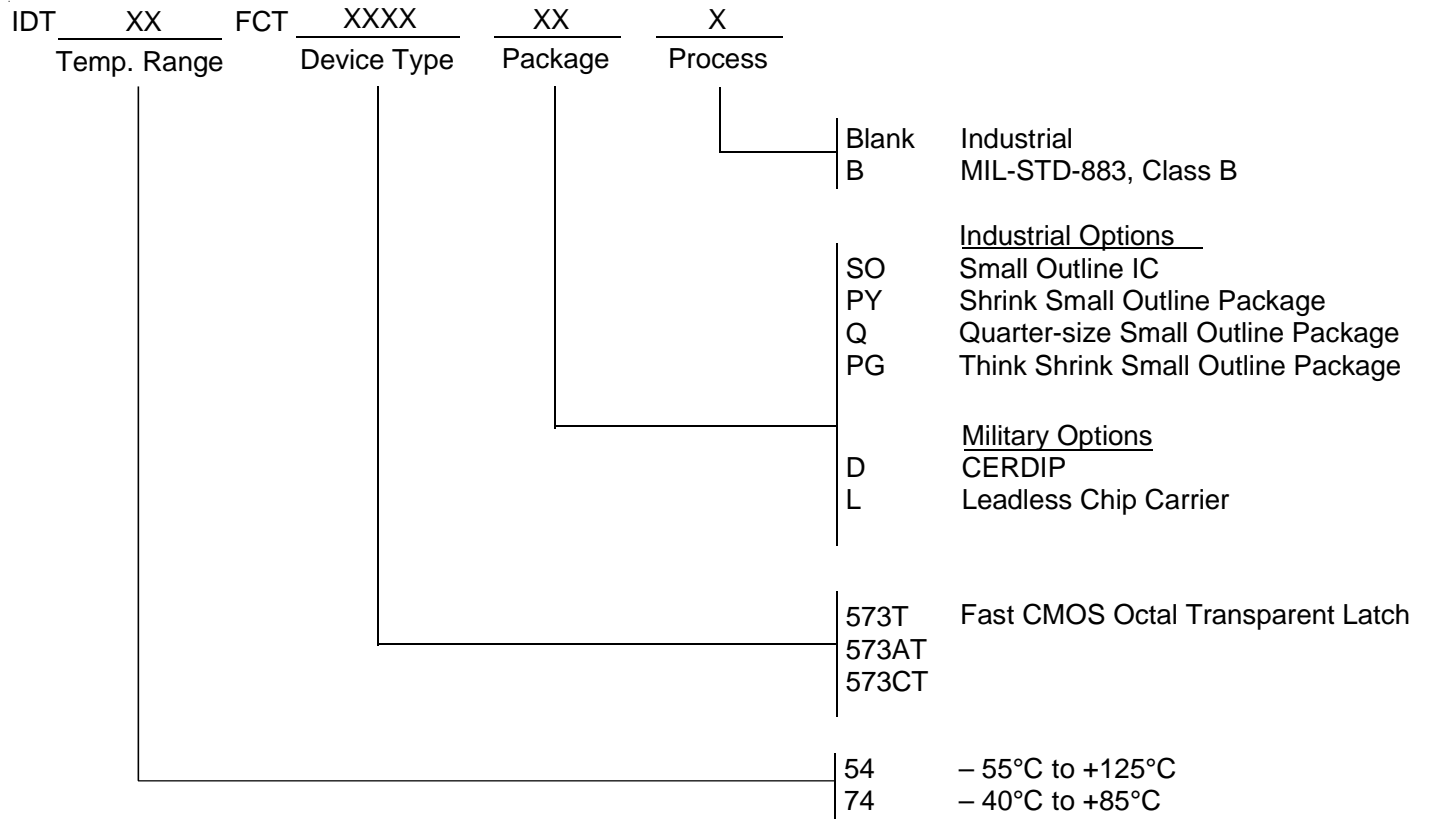


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate ≤ 1.0MHz; tr ≤ 2.5ns; tr ≤ 2.5ns.

ORDERING INFORMATION



DATA SHEET DOCUMENT HISTORY

6/24/2002 Updated as per PDNs Logic-00-07 and Logic-01-04



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