19-3383; Rev 0; 8/04

Dual, SiGe, High-Linearity, 1700MHz to 2200MHz Downconversion Mixer with LO Buffer/Switch

MAX9995

General Description

The MAX9995 dual, high-linearity, downconversion mixer provides 6.1dB gain, +25.6dBm IIP3, and 9.8dB NF for UMTS/WCDMA, DCS, and PCS base-station applications. The MAX9995 is ideal for low-side LO injection. (For a mixer variant optimized for high-side LO injection, contact the factory.)

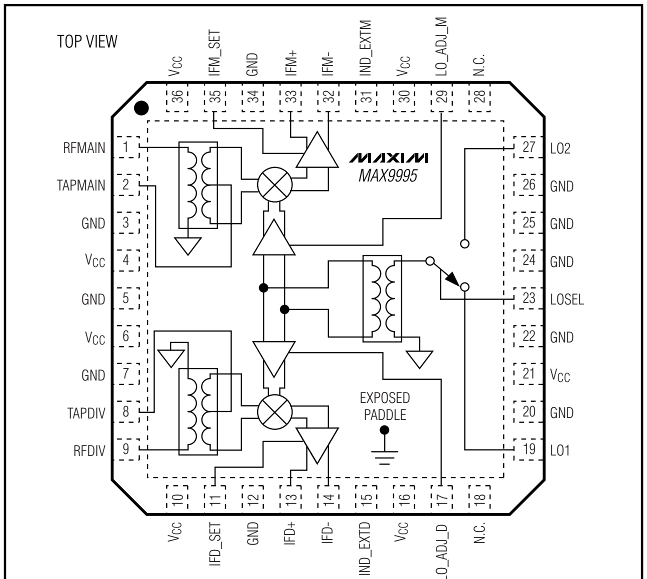
This device integrates baluns in the RF and LO ports, a dual-input LO selectable switch, an LO buffer, two double-balanced mixers, and a pair of differential IF output amplifiers. The MAX9995 requires a typical LO drive of 0dBm and supply current is guaranteed to be below 380mA.

These devices are available in a compact 36-pin thin QFN package (6mm × 6mm) with an exposed paddle. Electrical performance is guaranteed over the extended temperature range, from T_C = -40°C to +85°C.

Applications

- UMTS/WCDMA and cdma2000® 3G Base Stations
- DCS1800 and EDGE Base Stations
- PCS1900 and EDGE Base Stations
- PHS/PAS Base Stations
- Fixed Broadband Wireless Access
- Wireless Local Loop
- Private Mobile Radio
- Military Systems

Pin Configuration/Functional Diagram



6mm x 6mm THIN QFN (EXPOSED PADDLE)

EXPOSED PADDLE ON THE BOTTOM OF THE PACKAGE

Features

- ♦ 1700MHz to 2200MHz RF Frequency Range
- ♦ 1400MHz to 2000MHz LO Frequency Range (MAX9995)
- ♦ 1900MHz to 2400MHz LO Frequency Range (Contact Factory)
- ♦ 40MHz to 350MHz IF Frequency Range
- ♦ 6.1dB Conversion Gain
- ♦ +25.6dBm Input IP3
- ♦ 9.8dB Noise Figure
- ♦ 66dBc 2RF–2LO Spurious Rejection at P_{RF} = -10dBm
- ♦ Dual Channels Ideal for Diversity Receiver Applications
- ♦ Integrated LO Buffer
- ♦ Integrated RF and LO Baluns for Single-Ended Inputs
- ♦ Low -3dBm to +3dBm LO Drive
- ♦ Built-In SPDT LO Switch with 50dB LO1–LO2 Isolation and 50ns Switching Time
- ♦ 44dB Channel-to-Channel Isolation

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9995ETX	T_C** = -40°C to +85°C	36 Thin QFN-EP*
MAX9995ETX-T	T_C = -40°C to +85°C	36 Thin QFN-EP*
MAX9995ETX+D	T_C = -40°C to +85°C	36 Thin QFN-EP* lead free, bulk
MAX9995ETX+TD	T_C = -40°C to +85°C	36 Thin QFN-EP* lead free, T/R

*EP = Exposed pad.
**T_C = Case temperature.

ABSOLUTE MAXIMUM RATINGS

V_{CC} ....-0.3V to +5.5V
LO1, LO2 to GND ....±0.3V
IFM_, IFD_, IFM_SET, IFD_SET, LOSEL,
LO_ADJ_M, LO_ADJ_D to GND............-0.3V to (V_{CC} + 0.3V)
RFMAIN, RFDIV, and LO_ Input Power ....+20dBm
RFMAIN, RFDIV Current (RF is DC shorted to GND through balun)..50mA

Continuous Power Dissipation (T_A = +70°C)
36-Lead Thin QFN (derate 26mW/°C above +70°C)..2100mW
θ_{JA} ....+38°C/W
θ_{JC} ....+7.4°C/W
Operating Temperature Range (Note A) ....T_C = -40°C to +85°C
Maximum Junction Temperature Range..........................+150°C
Storage Temperature Range ....-65°C to +150°C
Lead Temperature (soldering, 10s) ....+300°C

Note A: T_C is the temperature on the exposed paddle of the package.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit*, no input RF or LO signals applied, V_{CC} = 4.75V to 5.25V, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, T_C = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	Total supply current		332	380	mA
		V_{CC} (pin 16)		82	90	
		V_{CC} (pin 30)		97	110	
		IFM+/IFM- (total of both)		70	90	
		IFD+/IFD- (total of both)		70	90	
LOSEL Input High Voltage	V_{IH}		2			V
LOSEL Input Low Voltage	V_{IL}				0.8	V
LOSEL Input Current	I_{IL} and I_{IH}		-10		+10	µA

AC ELECTRICAL CHARACTERISTICS

(*Typical Application Circuit,* V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{LO} = -3dBm to +3dBm, f_{RF} = 1700MHz to 2200MHz, f_{LO} = 1400MHz to 2000MHz, f_{IF} = 200MHz, with $f_{RF} > f_{LO}$, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, P_{LO} = 0dBm, f_{RF} = 1900MHz, f_{LO} = 1700MHz, f_{IF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RF Frequency	f_{RF}	(Note 7)	1700		2200	MHz
LO Frequency	f_{LO}	(Note 7)	1400		2000	MHz
		(Contact factory) (Note 7)	1900		2400	MHz
IF Frequency	f_{IF}	Meeting RF and LO frequency ranges; IF matching components affect the IF frequency range (Note 7)	40		350	MHz
Conversion Gain	G_C	f_{RF} = 1710MHz to 1875MHz		6		dB
		f_{RF} = 1850MHz to 1910MHz		6.2		
		f_{RF} = 2110MHz to 2170MHz		6.1		

AC ELECTRICAL CHARACTERISTICS (continued)

(*Typical Application Circuit,* V_{CC} = 4.75V to 5.25V, RF and LO ports are driven from 50Ω sources, P_{LO} = -3dBm to +3dBm, f_{RF} = 1700MHz to 2200MHz, f_{LO} = 1400MHz to 2000MHz, f_{IF} = 200MHz, with f_{RF} > f_{LO}, T_C = -40°C to +85°C. Typical values are at V_{CC} = 5.0V, P_{LO} = 0dBm, f_{RF} = 1900MHz, f_{LO} = 1700MHz, f_{IF} = 200MHz, and T_C = +25°C, unless otherwise noted.) (Notes 1, 2)

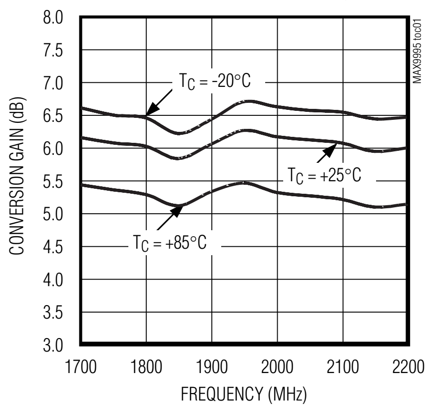
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Gain Variation from Nominal		V_{CC} = 5.0V, T_C = +25°C, P_{LO} = 0dBm, P_{RF} = -10dBm (Note 3)	f_{RF} = 1710MHz to 1875MHz		±0.5	±1	dB
			f_{RF} = 1850MHz to 1910MHz		±0.5	±1	
			f_{RF} = 2110MHz to 2170MHz		±0.5	±1	
Gain Variation with Temperature					±0.75		dB
Noise Figure	NF	No blockers present	f_{RF} = 1710MHz to 1875MHz		9.7		dB
			f_{RF} = 1850MHz to 1910MHz		9.8		
			f_{RF} = 2110MHz to 2170MHz		9.9		
Noise Figure (with Blocker)		8dBm blocker tone applied to RF port at 2000MHz, f_{RF} = 1900MHz, f_{LO} = 1710MHz, P_{LO} = -3dBm			22		dB
Input 1dB Compression Point	P_{1dB}	(Note 3)		9.5	12.6		dBm
Input Third-Order Intercept Point	IIP3	(Notes 3, 4)		23	25.6		dBm
2RF-2LO Spur Rejection	2 x 2	f_{RF} = 1900MHz, f_{LO} = 1700MHz, f_{SPUR} = 1800MHz (Note 3)	P_{RF} = -10dBm		66		dBc
			P_{RF} = -5dBm		61		
3RF-3LO Spur Rejection	3 x 3	f_{RF} = 1900MHz, f_{LO} = 1700MHz, f_{SPUR} = 1766.7MHz (Note 3)	P_{RF} = -10dBm	70	88		dBc
			P_{RF} = -5dBm	60	78		
Maximum LO Leakage at RF Port		f_{LO} = 1400MHz to 2000MHz			-29		dBm
Maximum 2LO Leakage at RF Port		f_{LO} = 1400MHz to 2000MHz			-17		dBm
Maximum LO Leakage at IF Port		f_{LO} = 1400MHz to 2000MHz			-25		dBm
Minimum RF to IF Isolation		f_{RF} = 1700MHz to 2200MHz, f_{IF} = 200MHz			37		dB
LO1-LO2 Isolation		P_{LO1} = 0dBm, P_{LO2} = 0dBm (Note 5)		40	50.5		dB
Minimum Channel-to-Channel Isolation		P_{RF} = -10dBm, RFMAIN (RFDIV) power measured at IFDIV (IFMAIN), relative to IFMAIN (IFDIV), all unused parts terminated at 50Ω		40	44		dB
LO Switching Time		50% of LOSEL to IF settled to within 2°			50		ns
RF Return Loss					14		dB
LO Return Loss		LO port selected			18		dB
		LO port unselected			21		
IF Return Loss		LO driven at 0dBm, RF terminated into 50Ω			21		dB

Note 1: Guaranteed by design and characterization.
Note 2: All limits reflect losses of external components. Output measurements taken at IF outputs of *Typical Application Circuit*.
Note 3: Production tested.
Note 4: Two tones 3MHz spacing, -5dBm per tone at RF port.
Note 5: Measured at IF port at IF frequency. f_{LO1} and f_{LO2} are offset by 1MHz.
Note 6: IF return loss can be optimized by external matching components.
Note 7: Operation outside this frequency band is possible but has not been characterized. See the *Typical Operating Characteristics*.

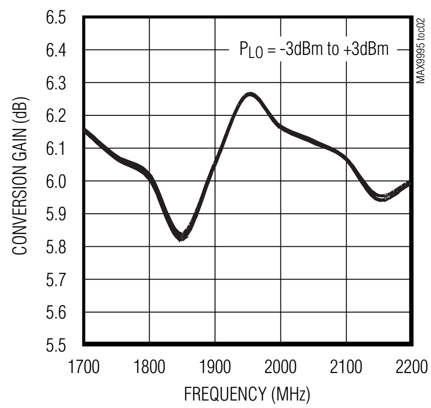
Typical Operating Characteristics

(*Typical Application Circuit*, V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, LO is low-side injected for a 200MHz IF, T_C = +25°C.)

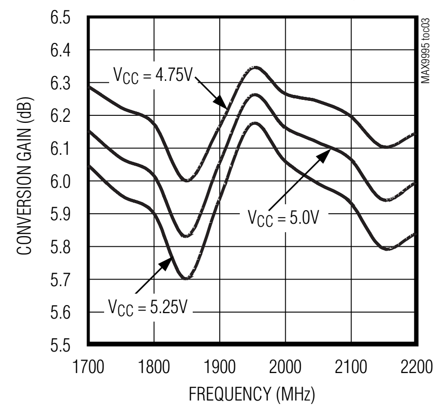
CONVERSION GAIN vs. RF FREQUENCY



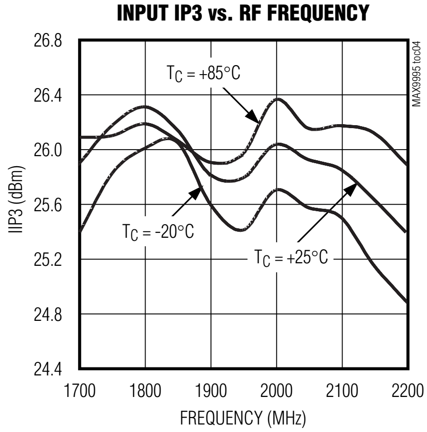
CONVERSION GAIN vs. RF FREQUENCY



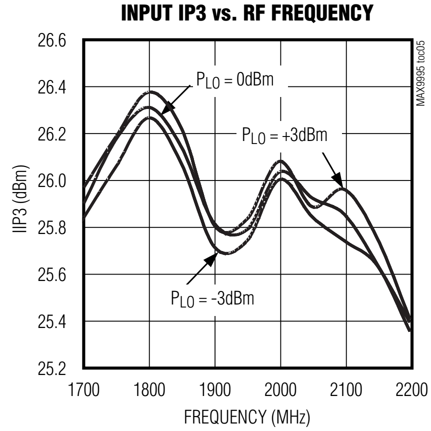
CONVERSION GAIN vs. RF FREQUENCY



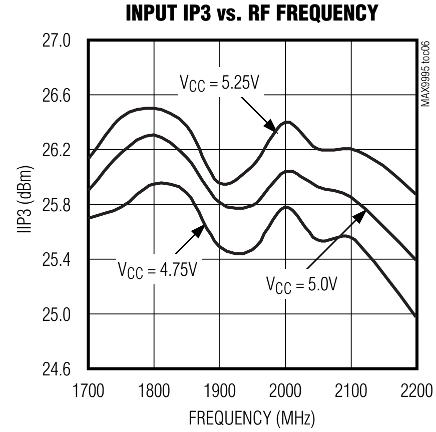
INPUT IP3 vs. RF FREQUENCY



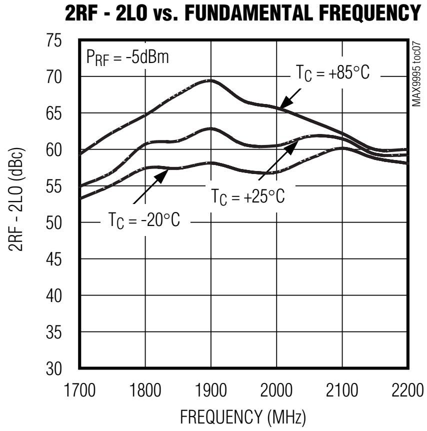
INPUT IP3 vs. RF FREQUENCY



INPUT IP3 vs. RF FREQUENCY



2RF - 2LO vs. FUNDAMENTAL FREQUENCY



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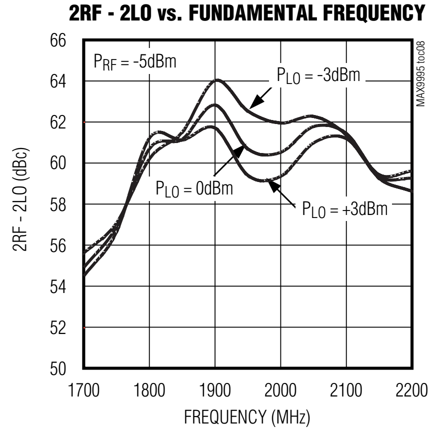

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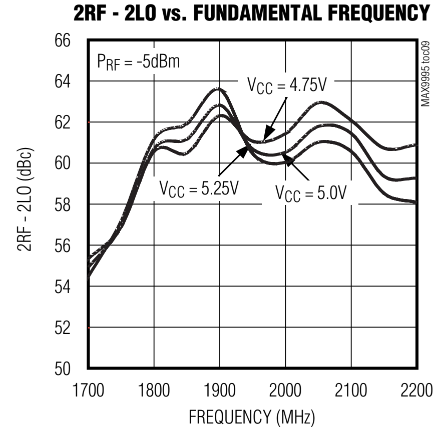
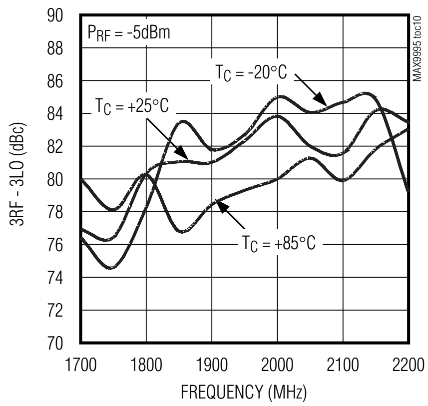


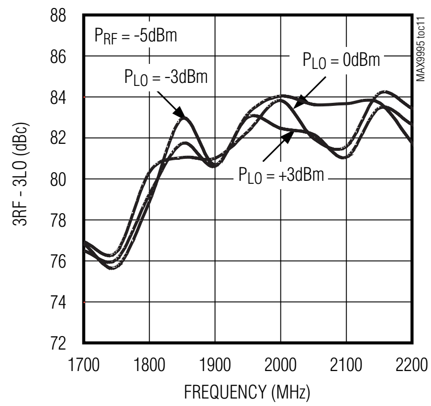
Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, LO is low-side injected for a 200MHz IF, T_C = +25°C.)

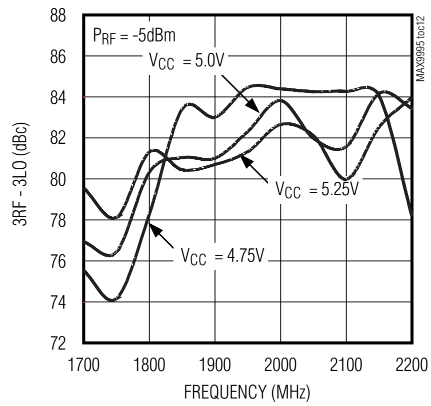
3RF - 3LO vs. FUNDAMENTAL FREQUENCY



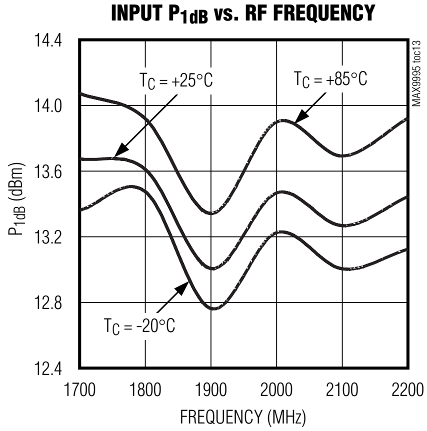
3RF - 3LO vs. FUNDAMENTAL FREQUENCY



3RF - 3LO vs. FUNDAMENTAL FREQUENCY



INPUT P_{1dB} vs. RF FREQUENCY



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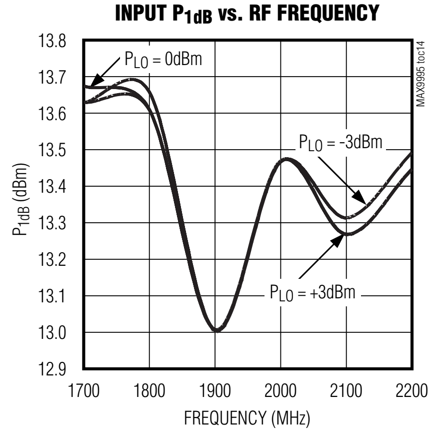

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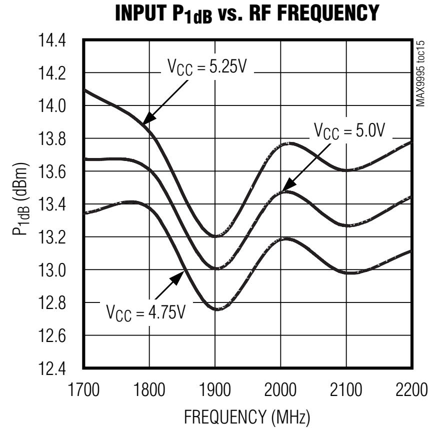
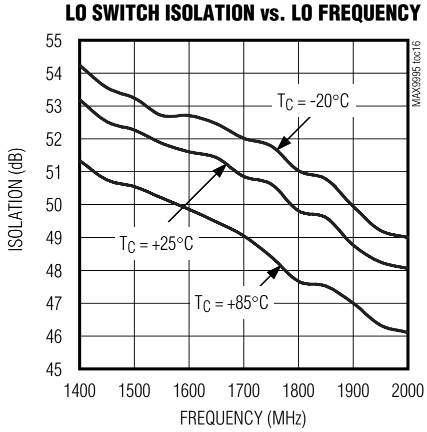


LO SWITCH ISOLATION vs. LO FREQUENCY



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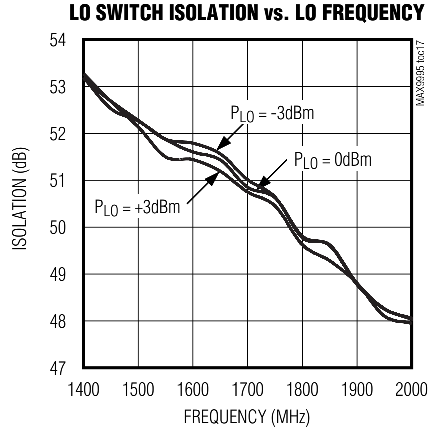

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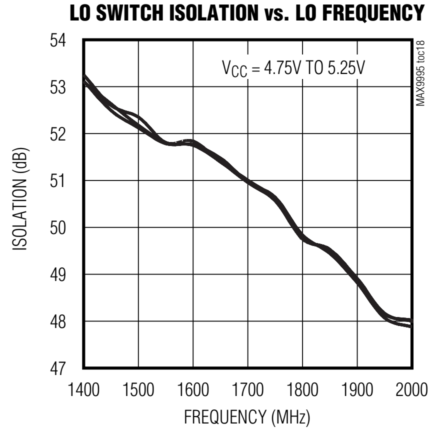
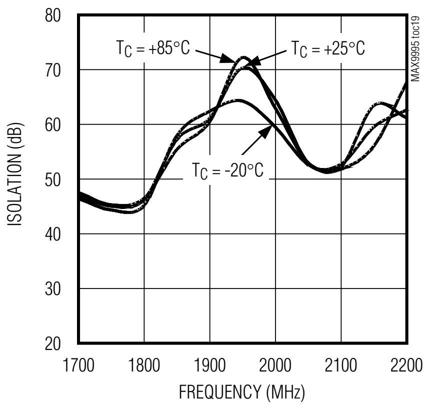


Dual, SiGe, High-Linearity, 1700MHz to 2200MHz Downconversion Mixer with LO Buffer/Switch

Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, LO is low-side injected for a 200MHz IF, T_C = +25°C.)

CHANNEL ISOLATION vs. RF FREQUENCY



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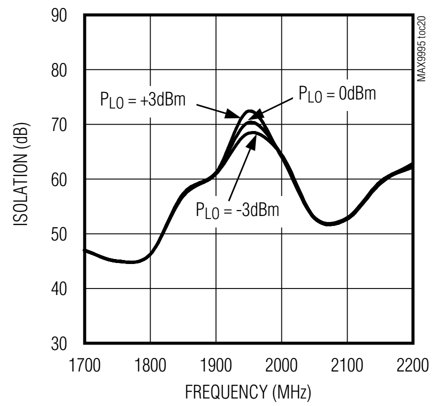

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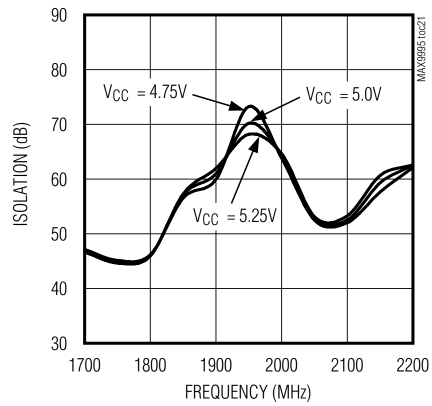
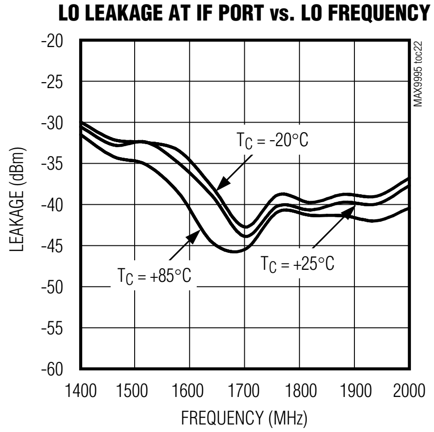
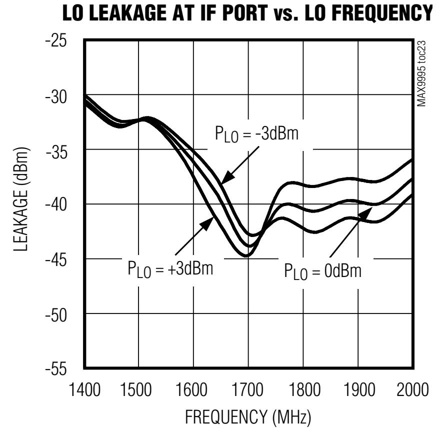


LO LEAKAGE AT IF PORT vs. LO FREQUENCY



LO LEAKAGE AT IF PORT vs. LO FREQUENCY



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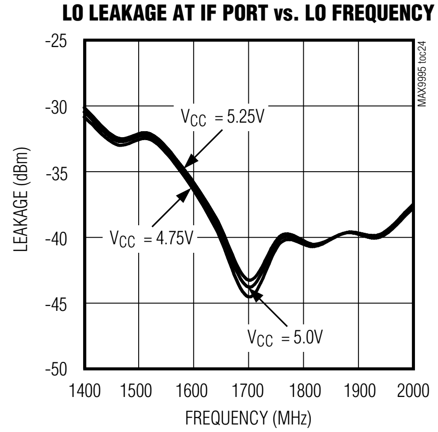

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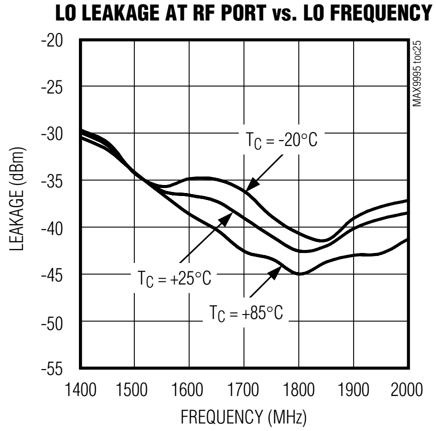

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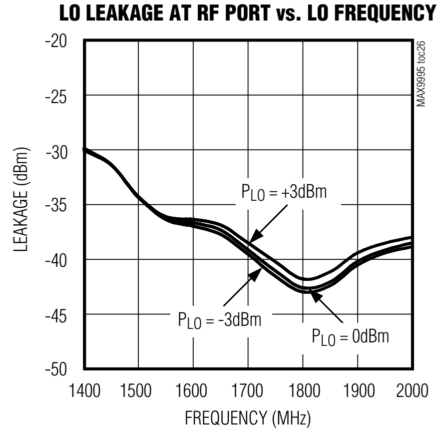

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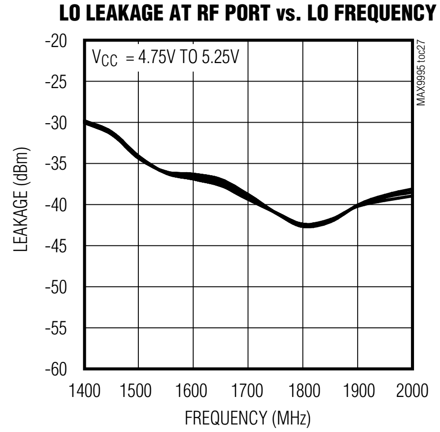
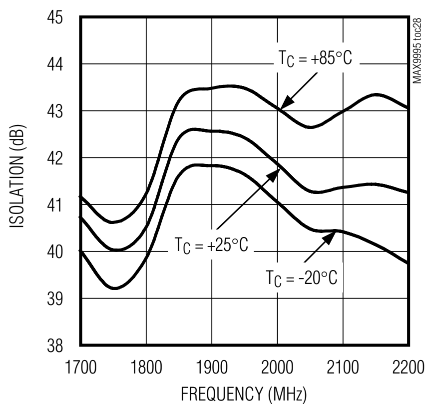


Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, LO is low-side injected for a 200MHz IF, T_C = +25°C.)

RF TO IF ISOLATION vs. RF FREQUENCY



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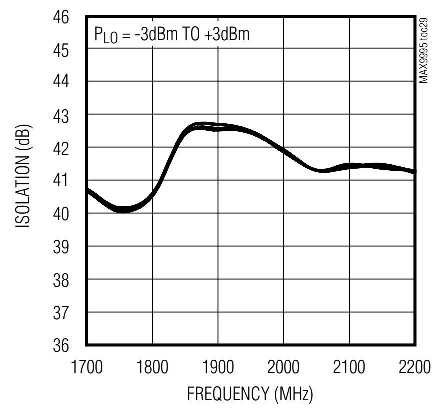

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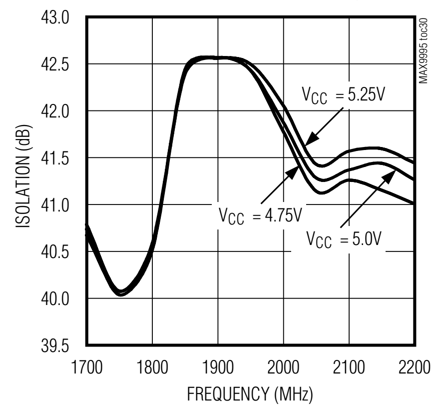
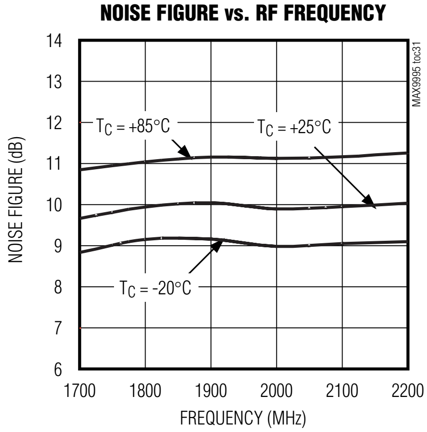


NOISE FIGURE vs. RF FREQUENCY



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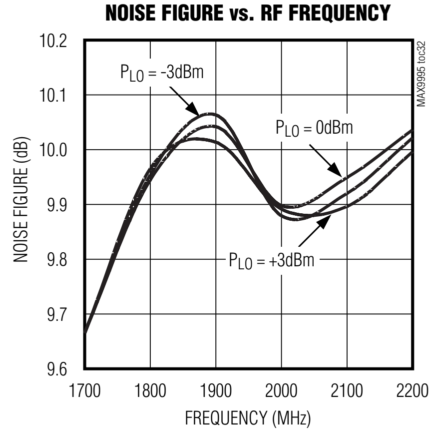

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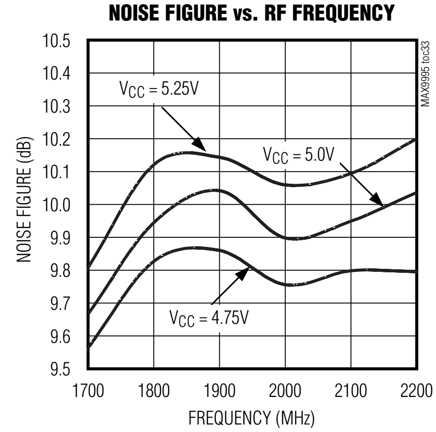
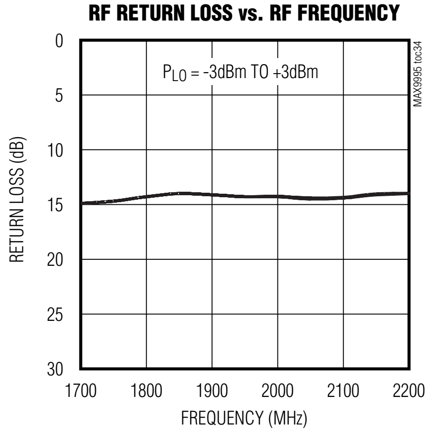
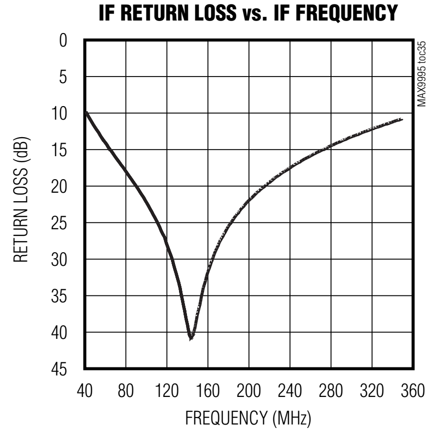


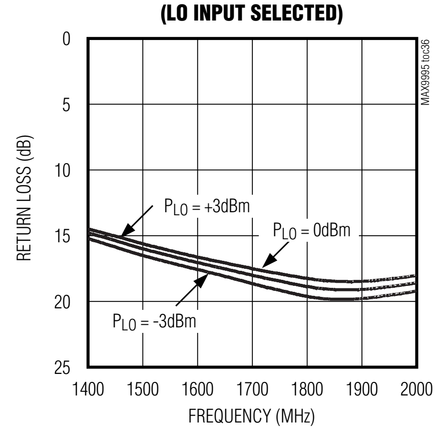
RF RETURN LOSS vs. RF FREQUENCY



IF RETURN LOSS vs. IF FREQUENCY



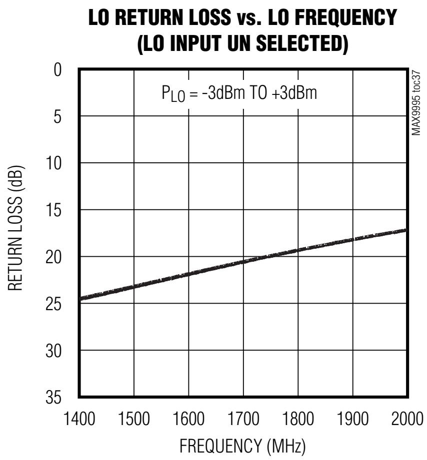
LO RETURN LOSS vs. LO FREQUENCY (LO INPUT SELECTED)

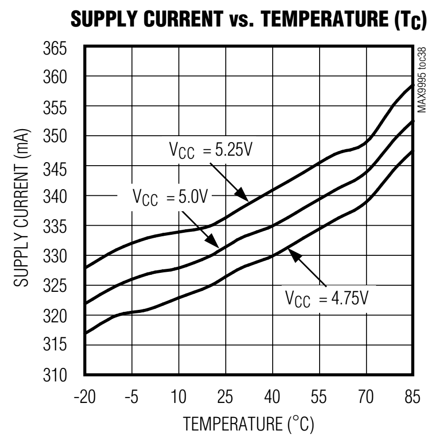


Dual, SiGe, High-Linearity, 1700MHz to 2200MHz Downconversion Mixer with LO Buffer/Switch

Typical Operating Characteristics (continued)

(*Typical Application Circuit*, V_{CC} = 5.0V, P_{RF} = -5dBm, P_{LO} = 0dBm, LO is low-side injected for a 200MHz IF, T_C = +25°C.)





Pin Description

PIN	NAME	FUNCTION
1	RFMAIN	Main Channel RF Input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
2	TAPMAIN	Main Channel Balun Center Tap. Connect a 0.033µF capacitor from this pin to the board ground.
3, 5, 7, 12, 20, 22, 24, 25, 26, 34	GND	Ground
4, 6, 10, 16, 21, 30, 36	V_{CC}	Power Supply. Connect bypass capacitors as close to the pin as possible (see the *Typical Application Circuit)*.
8	TAPDIV	Diversity Channel Balun Center Tap. Connect a 0.033µF capacitor from this pin to the ground.
9	RFDIV	Diversity Channel RF Input. Internally matched to 50Ω. Requires an input DC-blocking capacitor.
11	IFD_SET	IF Diversity Amplifier Bias Control. Connect a 1.2kΩ resistor from this pin to ground to set the bias current for the diversity IF amplifier.
13, 14	IFD+, IFD-	Diversity Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC} (see the *Typical Application Circuit*).
15	IND_EXTD	Connect a 10nH inductor from this pin to ground to increase the RF-IF and LO-IF isolation.
17	LO_ADJ_D	LO Diversity Amplifier Bias Control. Connect a 392Ω resistor from this pin to ground to set the bias current for the diversity LO amplifier.
18, 28	N.C.	No Connection. Not internally connected.
19	LO1	Local Oscillator 1 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
23	LOSEL	Local Oscillator Select. Set this pin to high to select LO1. Set to low to select LO2.

Pin Description (continued)

PIN	NAME	DESCRIPTION
27	LO2	Local Oscillator 2 Input. This input is internally matched to 50Ω. Requires an input DC-blocking capacitor.
29	LO_ADJ_M	LO Main Amplifier Bias Control. Connect a 392Ω resistor from this pin to ground to set the bias current for the main LO amplifier.
31	IND_EXTM	Connect a 10nH inductor from this pin to ground to increase the RF-IF and LO-IF isolation.
32, 33	IFM-, IFM+	Main Mixer Differential IF Output. Connect pullup inductors from each of these pins to V_{CC} (see the *Typical Application Circuit*).
35	IFM_SET	IF Main Amplifier Bias Control. Connect a 1.2kΩ resistor from this pin to ground to set the bias current for the main IF amplifier.
Exposed Paddle	GND	Exposed Ground Plane. This paddle affects RF performance and provides heat dissipation. The paddle must be connected to ground.

Detailed Description

The MAX9995 dual, high-linearity, downconversion mixer provides 6.1dB gain and +25.6dBm IIP3, with a 9.8dB noise figure. Integrated baluns and matching circuitry allow 50Ω single-ended interfaces to the RF and LO ports. A single-pole, double-throw (SPDT) LO switch provides 50ns switching time between LO inputs, with 50dB LO-to-LO isolation. Furthermore, the integrated LO buffer provides a high drive level to the mixer core, reducing the LO drive required at the MAX9995's inputs to -3dBm. The IF port incorporates a differential output, which is ideal for providing enhanced 2RF-2LO performance.

Table 1. Component Values

COMPONENT	VALUE	DESCRIPTION
C1, C8	4pF	Microwave capacitors (0402)
C2, C7	10pF	Microwave capacitors (0402)
C3, C6	0.033µF	Microwave capacitors (0603)
C4, C5, C14, C16	22pF	Microwave capacitors (0402)
C9, C13, C15, C17, C18	0.01µF	Microwave capacitors (0402)
C10, C11, C12, C19, C20, C21	150pF	Microwave capacitors (0603)
L1, L2, L4, L5	330nH	Wire-wound high-Q inductors (0805)
L3, L6	10nH	Wire-wound high-Q inductors (0603)
R1, R4	1.21kΩ	±1% resistors (0402)
R2, R5	392Ω	±1% resistors (0402)
R3, R6	10Ω	±1% resistors (1206)
T1, T2	4:1 (200:50)	IF baluns

Specifications are guaranteed over broad frequency ranges to allow for use in UMTS/WCDMA and 2G/2.5G/3G DCS1800, PCS1900, and cdma2000 base stations. The MAX9995 is specified to operate over an RF input range of 1700MHz to 2200MHz, an LO range of 1400MHz to 2000MHz, and an IF range of 40MHz to 350MHz. Operation beyond this is possible; however, performance is not characterized. This device can operate in high-side LO injection applications with an extended LO range, but performance degrades as f_{LO} continues to increase. For a device with better high-side performance, contact the factory. This device is available in a compact 6mm x 6mm, 36-pin thin QFN package with an exposed paddle.

RF Input and Balun

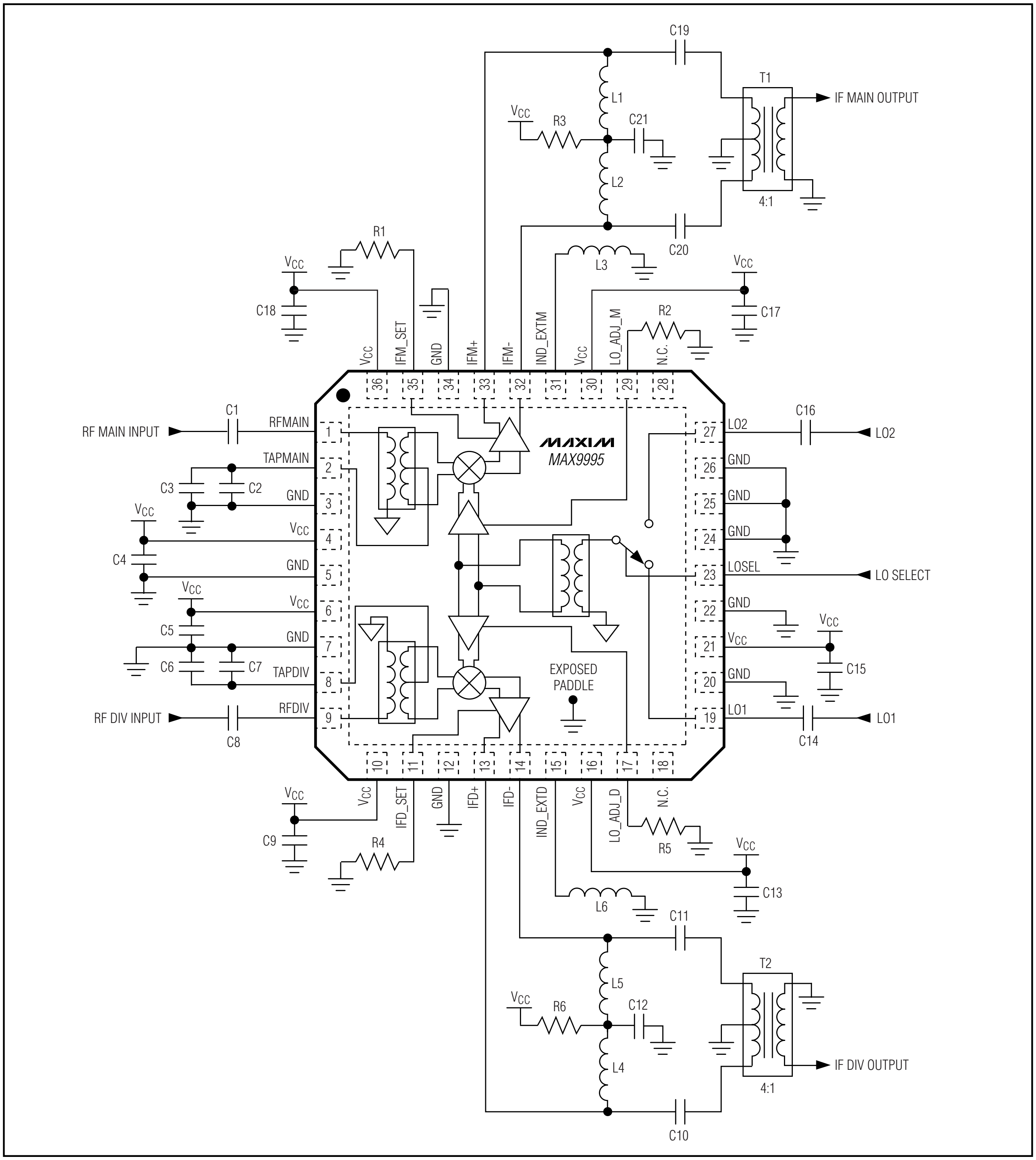
The MAX9995's two RF inputs (RFMAIN and RFDIV) are internally matched to 50Ω, requiring no external matching components. DC-blocking capacitors are required as the inputs are internally DC shorted to ground through the on-chip baluns. Input return loss is typically 14dB over the entire RF frequency range of 1700MHz to 2200MHz.

LO Input, Switch, Buffer, and Balun

The mixers can be used for either high-side or low-side injection applications with an LO frequency range of 1400MHz to 2000MHz. For a device with an LO frequency range of 1900MHz to 2400MHz, contact the factory. As an added feature, the MAX9995 includes an

Dual, SiGe, High-Linearity, 1700MHz to 2200MHz Downconversion Mixer with LO Buffer/Switch

Typical Application Circuit



internal LO SPDT switch that can be used for frequency-hopping applications. The switch selects one of the two single-ended LO ports, allowing the external oscillator to settle on a particular frequency before it is switched in. LO switching time is typically less than 50ns, which is more than adequate for virtually all GSM applications. If frequency hopping is not employed, set the switch to either of the LO inputs. The switch is controlled by a digital input (LOSEL): logic high selects LO1, and logic low selects LO2. LO1 and LO2 inputs are internally matched to 50Ω, requiring only a 22pF DC-blocking capacitor.

A two-stage internal LO buffer allows a wide input power range for the LO drive. All guaranteed specifications are for an LO signal power from -3dBm to +3dBm. The on-chip low-loss balun, along with an LO buffer, drives the double-balanced mixer. All interfacing and matching components from the LO inputs to the IF outputs are integrated on-chip.

High Linearity Mixers

The core of the MAX9995 is a pair of double-balanced, high-performance passive mixers. Exceptional linearity is provided by the large LO swing from the on-chip LO buffer. When combined with the integrated IF amplifiers, the cascaded IIP3, 2RF-2LO rejection, and NF performance is typically +25.6dBm, 66dBc, and 9.8dB, respectively.

Differential IF Output Amplifiers

The MAX9995 mixers have an IF frequency range of 40MHz to 350MHz. The differential, open-collector IF output ports require external pullup inductors to V_{CC}. Note that these differential outputs are ideal for providing enhanced 2RF-2LO rejection performance. Single-ended IF applications require a 4:1 balun to transform the 200Ω differential output impedance to a 50Ω single-ended output. After the balun, VSWR is typically 1.5:1.

Applications Information

Input and Output Matching

The RF and LO inputs are internally matched to 50Ω. No matching components are required. Return loss at each RF port is typically 14dB over the entire input range (1700MHz to 2200MHz), and return loss at the LO ports is typically 18dB (1400MHz to 2000MHz). RF and LO inputs require only DC-blocking capacitors for interfacing.

The IF output impedance is 200Ω (differential). For evaluation, an external low-loss 4:1 (impedance ratio) balun transforms this impedance down to a 50Ω single-ended output (see the *Typical Application Circuit*).

Bias Resistors

Bias currents for the LO buffer and the IF amplifier are optimized by fine tuning the resistors R1, R2, R4, and R5. If reduced current is required at the expense of performance, contact factory. If the ±1% bias resistor values are not readily available, substitute standard ±5% values.

Layout Considerations

A properly designed PC board is an essential part of any RF/microwave circuit. Keep RF signal lines as short as possible to reduce losses, radiation, and inductance. For the best performance, route the ground pin traces directly to the exposed pad under the package. The PC board exposed pad **MUST** be connected to the ground plane of the PC board. It is suggested that multiple vias be used to connect this pad to the lower-level ground planes. This method provides a good RF/thermal-conduction path for the device. Solder the exposed pad on the bottom of the device package to the PC board. The MAX9995 Evaluation Kit can be used as a reference for board layout. Gerber files are available upon request at www.maxim-ic.com.

Power-Supply Bypassing

Proper voltage-supply bypassing is essential for high-frequency circuit stability. Bypass each V_{CC} pin with a capacitor as close to the pin as possible (*Typical Application Circuit*).

Exposed Pad RF/Thermal Considerations

The exposed paddle (EP) of the MAX9995's 36-pin thin QFN-EP package provides a low thermal-resistance path to the die. It is important that the PC board on which the MAX9995 is mounted be designed to conduct heat from the EP. In addition, provide the EP with a low-inductance path to electrical ground. The EP **MUST** be soldered to a ground plane on the PC board, either directly or through an array of plated via holes.

Chip Information

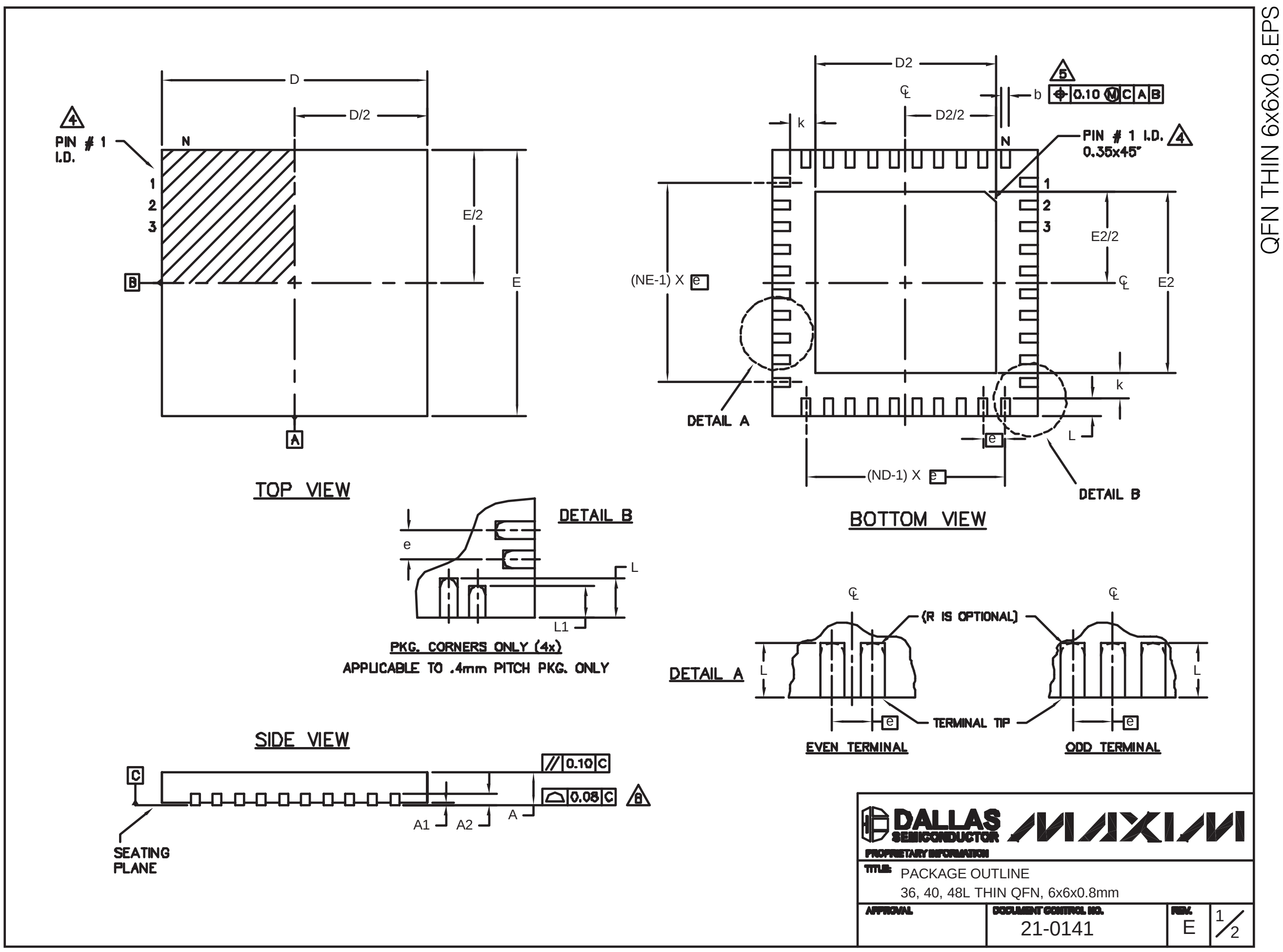
TRANSISTOR COUNT: 1414

PROCESS: SiGe BiCMOS

Dual, SiGe, High-Linearity, 1700MHz to 2200MHz Downconversion Mixer with LO Buffer/Switch

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS									
PKG.	36L 6x6			40L 6x6			48L 6x6		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	–	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.		
b	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
E	5.90	6.00	6.10	5.90	6.00	6.10	5.90	6.00	6.10
e	0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	–	–	0.25	–	–	0.25	0.35	0.45
L	0.45	0.55	0.65	0.30	0.40	0.50	0.40	0.50	0.60
L1	–	–	–	–	–	–	0.30	0.40	0.50
N	36			40			48		
ND	9			10			12		
NE	9			10			12		
JEDEC	WJJD-1			WJJD-2			–		

EXPOSED PAD VARIATIONS							DOWN BONDS ALLOWED
PKG. CODES	D2			E2			
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
T3666-1	3.60	3.70	3.80	3.60	3.70	3.80	NO
T3666-2	3.60	3.70	3.80	3.60	3.70	3.80	YES
T3666-3	3.60	3.70	3.80	3.60	3.70	3.80	NO
T4066-1	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-2	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-3	4.00	4.10	4.20	4.00	4.10	4.20	YES
T4066-4	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4066-5	4.00	4.10	4.20	4.00	4.10	4.20	NO
T4866-1	4.20	4.30	4.40	4.20	4.30	4.40	YES

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR 0.4mm LEAD PITCH PACKAGE T4866-1.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE
36, 40, 48L THIN QFN, 6x6x0.8mm

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