Preliminary

OKI Semiconductor

This version: Dec. 1998

MSM7654

NTSC/PAL Digital Video Encoder

GENERAL DESCRIPTION

The MSM7654, which is a digital video encoder supporting NTSC/PAL formats, converts digital image data to an analog video signal.
The encoder can receive the digital image or RGB digital image signals conforming to ITU-R BT601 as an input signal.
The encoder can output simultaneously the composite video and S-video signals, and it can also output the RGB analog signal by switching.
The encoder can control luminance (Y) signal output levels of the composite video and S-video signals.

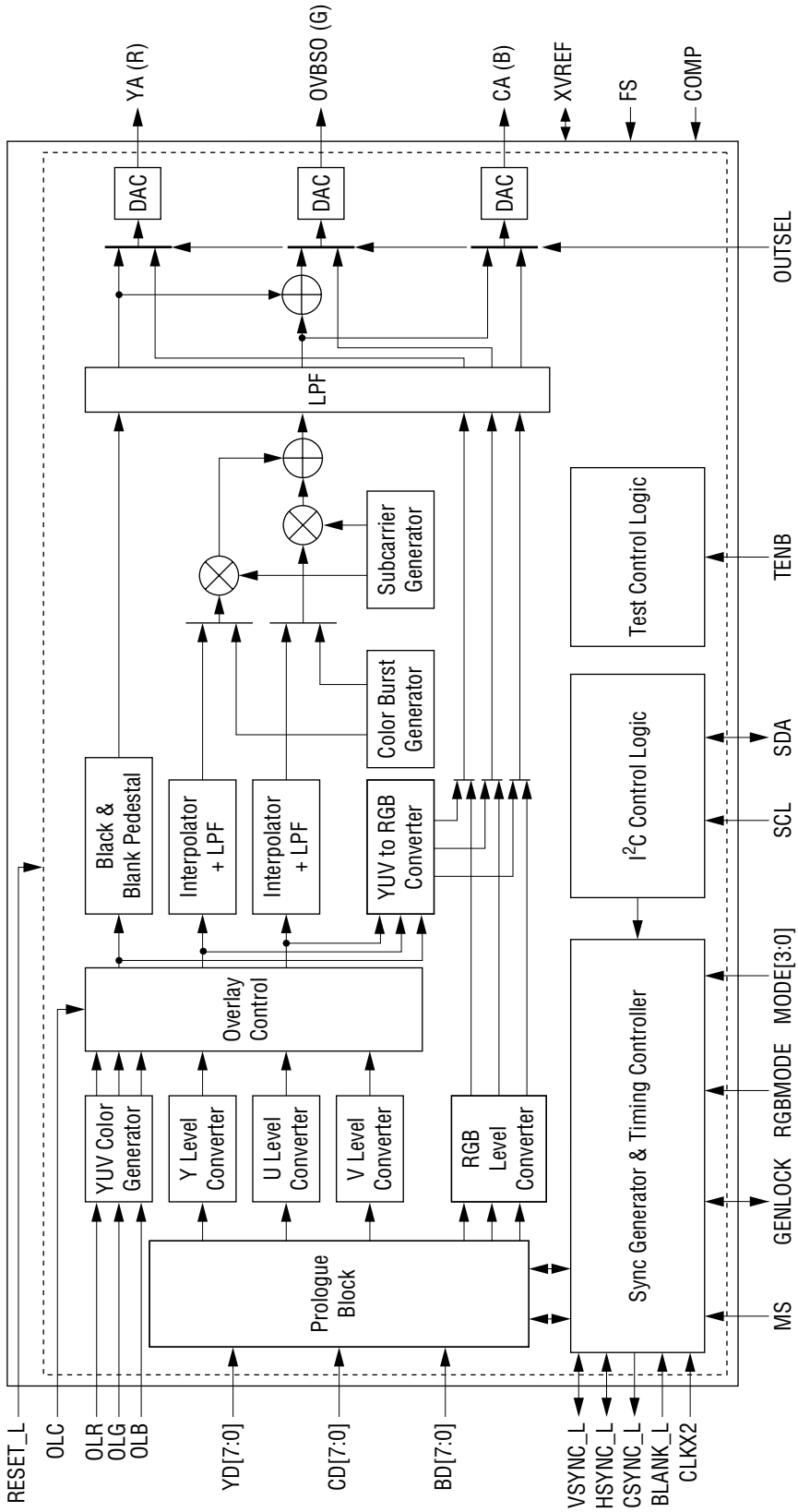
FEATURES

- Video signal system: NTSC/PAL
- Scanning system: interlaced/noninterlaced (NTSC : 262 lines/PAL : 312 lines)
- Input digital level: conforms to ITU-R601 (CCIR601)
- Input-output timing: conforms to ITU Rec. 656 or ITU-R BT624-4
- Input signal sampling ratio : Y:Cb:Cr = 4:2:2 or 4:1:1/R:G:B = 8:8:8
- Supported input interface
  - ITU Rec. 656
  - YCbCr format (8-bit input)
  - ITU-R601 (8-bit (Y) + 8-bit (CbCr) input)
  - RGB (24-bit input)
- Pixel frequency (Sampling frequency) :
  - 12.272727 MHz (24.54545 MHz) : NTSC Square Pixel
  - 13.5 MHz (27 MHz) : NTSC/PAL ITU-R BT601
  - 14.31818 MHz (28.63636 MHz) : NTSC 4Fsc
  - 14.75 MHz (29.5 MHz) : PAL Square Pixel
- Output format
  - Selectable composite & S-video or RGB
  - 37.5 Ω driving capability
- Master or slave operation (slave operation only in ITU Rec.656 mode)
- Internal 3ch 10-bit DAC
- 3-bit title graphics can be displayed (only for composite and S-video signals)
- Color bar function
- I^2C-bus host interface function
- Brightness level adjust of 100% to 68.75% (only for composite and S-video signals)
- CENLOCK control
- 3.3 V single power supply (each I/O pin is 5 V tolerable)
- Package
  64-pin plastic QFP (QFP64-P-1414-0.80-2K) (Product name: MSM7654GA)

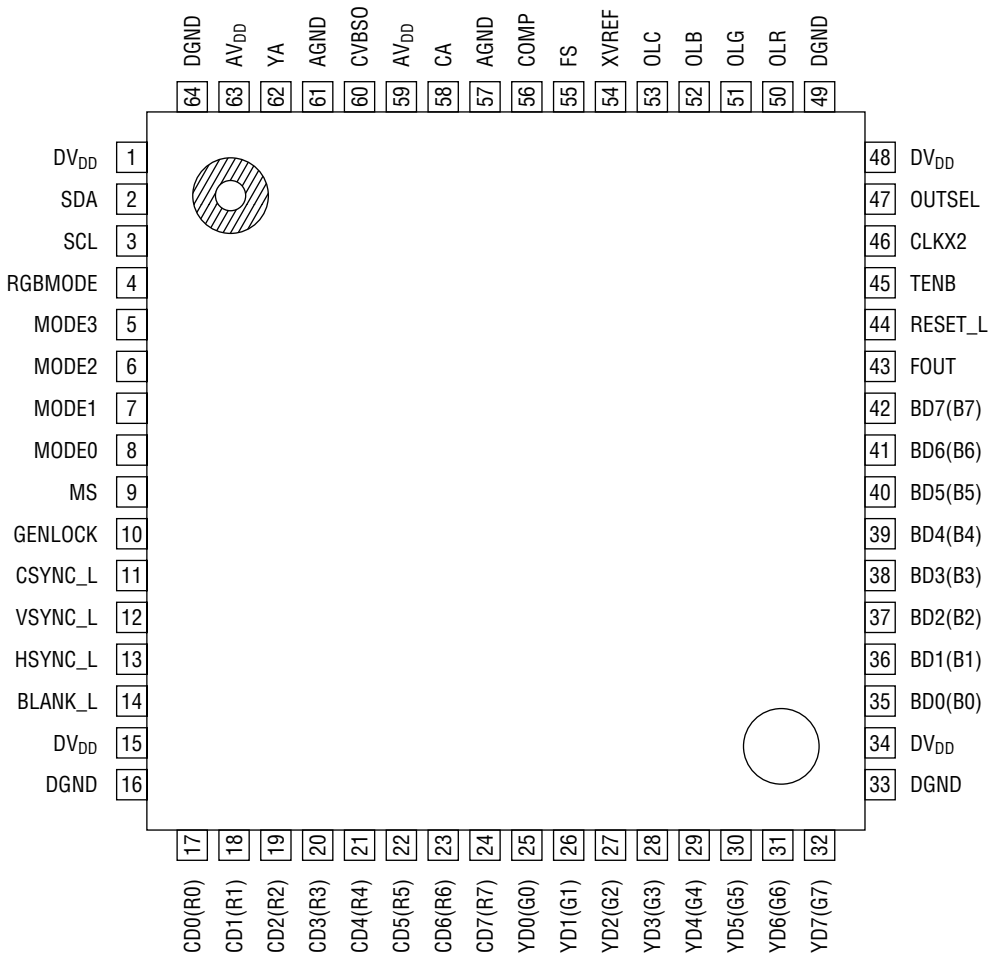
APPLICATIONS

- Video CD
- Video game equipment
- Electronic still cameras
- Video filing systems
- Video cameras
- Videophones
- Multimedia equipment
- Video printers
- Videoconferencing systems
- Scanners
- Video graphics boards
- Monitoring systems

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



64-Pin Plastic QFP

PIN DESCRIPTIONS

Pin	I/O	Symbol	Description
1		DV_{DD}	3.3 V digital power supply.
2	I/O	SDA	I^2C interface data bus.
3	I	SCL	I^2C interface clock bus.
4	I	RGBMODE	Input signal select pin. "0" : YCbCr / "1" : RGB, Internal pull-down.
5 to 8	I	MODE[3:0]	Operation mode select pin. However, sleepmode is valid while RGBMODE is "0". 0000 : NTSC ITU-R656 0001 : NTSC 27 MHz YCbCr 0010 : NTSC 24.52 MHz Square Pixel 0011 : NTSC 28.64 MHz 4Fsc 0101 : NTSC 13.5 MHz YCbCr 0110 : NTSC 12.27 MHz 0111 : NTSC 14.32 MHz 1000 : PAL ITU-R656 1001 : PAL 27 MHz YcbCr 1010 : PAL 29.5 MHz Square Pixel 1101 : PAL 13.5 MHz 1110 : PAL 14.75 MHz 1111 : Sleep Mode
9	I	MS	Master/slave operation selection in other modes than CCIR656. Internal pull-down. "1" : Master / "0" : Slave
10	I/O	GENLOCK	GENLOCK signal I/O pin.
11	O	CSYNC_L	Composite sync output pin.
12	I/O	VSYNC_L	Vertical sync input/output pin (ITU656: 0, others: I/O)
13	I/O	HSYNC_L	Horizontal signal input/output pin (ITU656: 0, others : I/O)
14	I	BLANK_L	Composite blank signal input pin.
15		DVDD	3.3 V digital power supply.
16	I	DGND	Digital GND.
17 to 24	I	CD0 to CD7	8-bit digital image chrominance signal data input pins at pixel rate operation. Level conforms to ITU-601. R signal input pins in RGB input mode. CD7 is MSB. Fixed to "0" when not used.
25 to 32	I	YD0 to YD7	8-bit digital image data input pins at double pixel rate operation. 8-bit digital luminance signal data input pinsat pixel rate operation. Level conforms to ITU-601. G signal input pins in RGB input mode. YD7 is MSB.
33		DGND	Digital GND
34		DVDD	3.3 V digital power supply
35 to 42	I	BD0 to BD7	B signal input pins in RGB input mode. Fixed to "0" when not used.
43	O	FOUT	Field information output pin (Odd Field : "1", Even Field : "0") (Polarity can be changed by the internal register.)
44	I	RESET_L	System reset pin.
45	I	TENB	Input pin for testing. Normally fixed to "0". Internal pull-down.
46	I	CLKX2	Clock input pin.
47	I	OUTSEL	Video output format select pin. "0" : S-Video & Composite / "1" RGB. Internal pull-down.
48		DV_{DD}	3.3 V digital power supply
49	I	DGND	Digital GND
50	I	OLR	Overlay text color (Red component).

PIN DESCRIPTIONS (continued)

Pin	I/O	Symbol	Description
51	I	OLG	Overlay text color (Green component).
52	I	OLB	Overlay text color (Blue component).
53	I	OLC	Transparent control signal. "1" indicates overlay signal.
54	I/O	XVREF	Reference voltage input pin for external DAC or internal reference voltage output pin. (Reference voltage for DAC)
55	I	FS	DAC full scale adjustment pin.
56	I	COMP	DAC phase correction pin.
57		AGND	Analog GND.
58	O	CA	Analog color chrominance signal output pin or B (Blue) signal output pin.
59		AV_{DD}	3.3 V analog power supply.
60	O	CVBSO	Analog composite signal output pin or G (Green) signal output pin.
61		AGND	Analog GND.
62	O	YA	Analog luminance signal output pin or R (Red) signal output pin.
63		AV_{DD}	3.3 V analog power supply.
64		DGND	Digital GND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	DV_{DD}	—	–0.3 to +4.5	V
	AV_{DD}	—	–0.3 to +4.5	
Digital Input Voltage	V_I	DV_{DD} = 3.3 V	–0.3 to +5.5	V
Analog Output Current	I_O	—	50	mA
Power Consumption	P_W	—	700	mW
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage (*1)	DV_{DD}	—	3.0	3.3	3.6	V
	AV_{DD}	—	3.0	3.3	3.6	
"H" Level Input Voltage	V_{IH}	—	2.2	—	—	V
"L" Level Input Voltage	V_{IL}	—	—	—	0.8	V
Operating Temperature 1	Ta1	DV_{DD} = AV_{DD} = 3.3 V	0	25	70	˚C
External Reference Voltage	Vrefex	DV_{DD} = AV_{DD} = 3.3 V, Ta = 25˚C	—	1.25	—	V
DA Current Setting Resistance	Riadj	(*2)	—	197.5	—	Ω
DA Output Load Resistance	R_L	(*3)	—	(75//75)	—	Ω

(*1) Supply an equal voltage to both DV_{DD} and AV_{DD}.

(*2) A volume control resistor of approx. 500 Ω is recommendable for adjusting the output current.

(*3) Indicates the value when Riadj = 197.5 Ω (typical value).

ELECTRICAL CHARACTERISTICS

DC Characteristics

(Ta = 0 to 70°C, DV_{DD} = 3.3 V ±0.3 V, AV_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H" Level Output Voltage	V_{OH}	I_{OH} = –4 mA (*1)	0.7V_{DD}	—	—	V
"L" Level Output Voltage	V_{OL}	I_{OL} = 4 mA (*1)	—	—	0.4	V
Input Leak Current	I_I	V_I = GND to DV_{DD}	–10	—	+10	µA
Output Leak Current	I_O	V_I = GND to DV_{DD} (*2)	–10	—	+10	µA
Power Supply Current (operating)	I_{DDO}	—	—	140	160	mA
Power Supply Current (standby)	I_{DDS}	RESET_L = "L" CLKX2 = 0 MHz	—	60	65	mA
Power Supply Current (Sleep mode)	I_{DDSM}	MODE [3:0] = 0000		0.5	5	mA
I^2 C-bus SDA Output Voltage	$SDAV_L$	Low level, I_{OL} = 3 mA	0	—	0.4	V
I^2C-bus SDA Output Current	$SDAI_O$	During Acknowledge	3	—	—	mA
Internal Reference Voltage	Vrefin	—	—	1.25	—	V
DA Output Load Resistance	R_L	75 Ω//75 Ω		37.5		Ω
Integral Linearity	SINL	—		±2		LSB
Differential Linearity	SDNL	—		±1		LSB

(*1) VSYNC_L, HSYNC_L, GENLOCK, CSYNC.L, FOUT
(*2) SDA

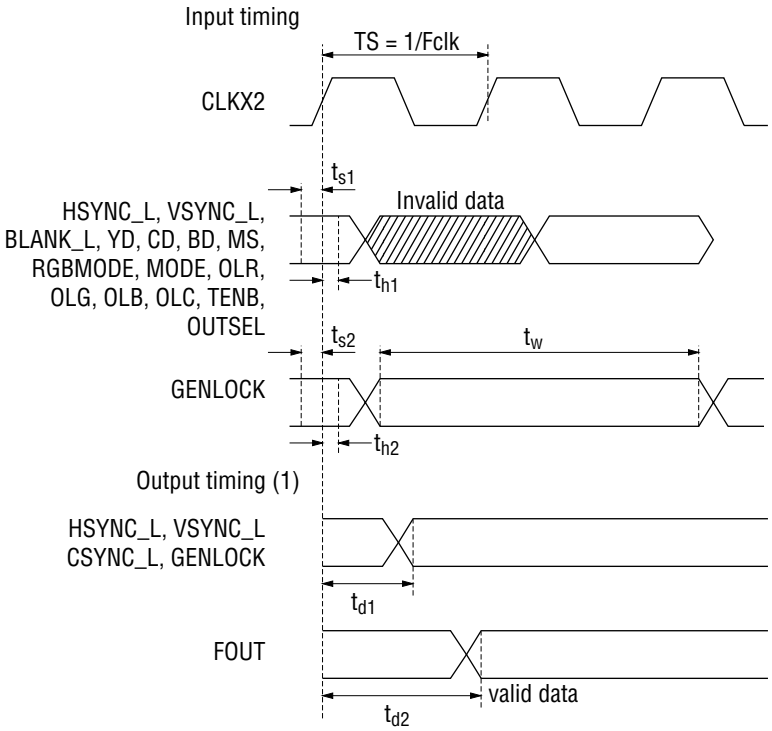
AC Characteristics

(Ta = 0 to 70°C, DV_{DD} = 3.3 V ±0.3 V, AV_{DD} = 3.3 V ±0.3 V)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
CLKX2 Frequency (*1)	Fclk	PAL Square Pixel	—	29.5	—	MHz
		NTSC 4Fsc	—	28.63636	—	MHz
		NTSC Square Pixel	—	24.54545	—	MHz
		ITU-R601/656	—	27.0	—	MHz
Input Data Setup Time	t_{s1}	—	7.0	—	—	ns
Input Data Setup Time	t_{s2}	—	0.0	—	—	ns
Input Data Hold Time	t_{h1}	—	5.0	—	—	ns
Input Data Hold Time	t_{h2}	—	11.08	—	—	ns
Pulse Width	t_w	—	93.0	—	—	ns
Output Delay Time	t_{d1}	—	5.0	—	15.0	ns
Output Delay Time2	t_{d2}	—	6.0	—	20.0	ns
I^2C-bus Clock Cycle Time	t_{C_SCL}	Rpull_up = 4.7 kΩ	200	—	—	ns
I^2C-bus High Level Cycle	t_{H_SCL}	Rpull_up = 4.7 kΩ	100	—	—	ns
I^2C-bus Low Level Cycle	t_{L_SCL}	Rpull_up = 4.7 kΩ	100	—	—	ns

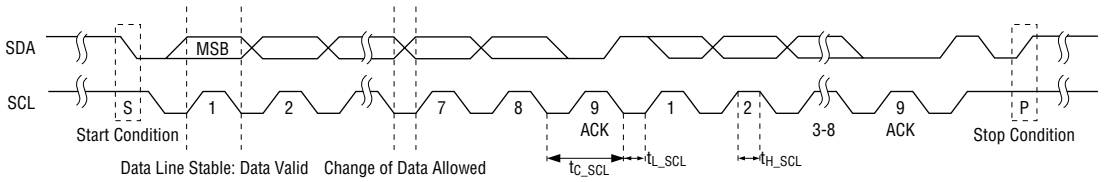
(*1) If high precision is needed for sub-carrier/synchronization signals, clocks within ±100 ppm(typ.) should be provided.

INPUT/OUTPUT TIMING



I²C-bus Interface Input/Output Timing

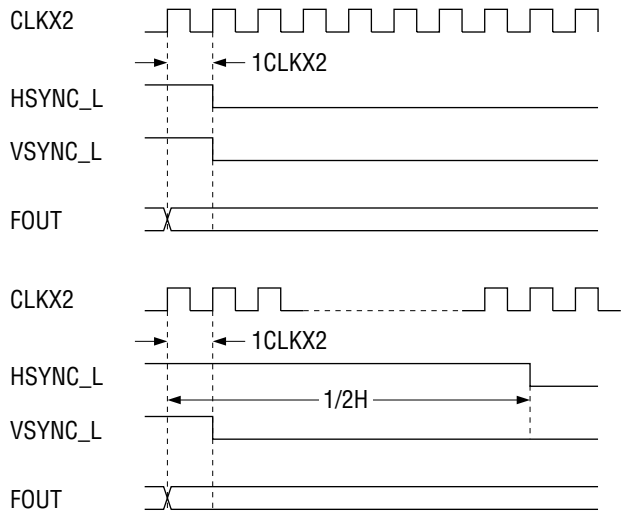
The following figure shows I²C-bus basic input/output timing.



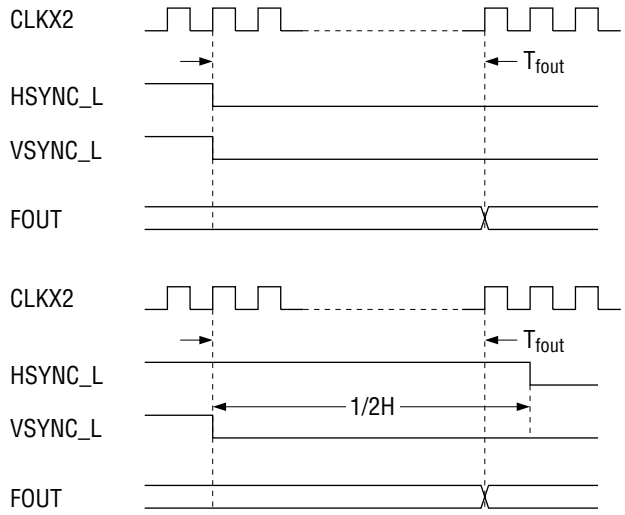
I²C-bus Basic Input/Output Timing

FOUT output timing

(1) In master mode



(2) In slave mode

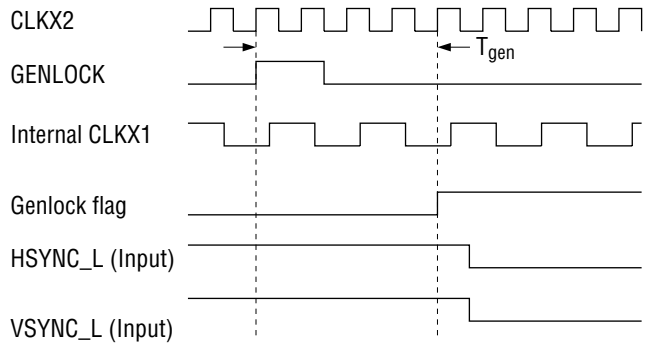


T_{fout} values in slave mode depend on pixel rates. The following table lists the T_{fout} value to each pixel rate.

Input interface	T_{fout}
CCIR Rec.656	5 clkx2
YCbCr (8bit)	9 clkx2
YCbCr (16bit)	9 clkx2 or 10 clkx2
RGB	9 clkx2 or 10 clkx2

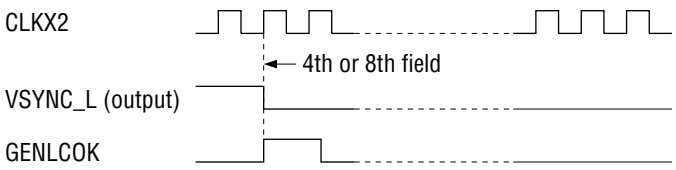
GENLOCK I/O timing

(1) Input timing



If the encoder is in the slave mode and the register MR1[0] is set to "0" (External pin Genlock control is valid), the subcarrier-phase reset signal can be input from the GENLOCK pin.
If the GENLOCK pulse is input to the encoder in the NTSC mode, the subcarrier is reset when the fourth field is shifted into the first. And if the GENLOCK pulse is input to the encoder in the PAL mode, the subcarrier is reset when the eighth field is shifted into the first.
The subcarrier-phase reset signal should be pulsed at the timing that meets the AC characteristics. 5 clkX2 pulses are required from the time the reset signal is input from the GENLOCK pin to when the internal GENLOCK flag is set.
Thus, the subcarrier-phase will be reset if the GENLOCK pulse is input 5 clkx2 pulses before HSYNC_L and VSYNC_L fall when the internal state of the encoder is the fourth field.
The subcarrier-phase, however, cannot be reset if the GENLOCK pin is fixed high.

(2) Output timing (master mode)



If the encoder is in the master mode, the register MR1[0] is set to "1" (Internal register control is valid) and the register MR1[1] is set to "0" (Genlock on), the subcarrier-phase reset signal can be output from the GENLOCK pin.
If the encoder is set to NTSC, the GENLOCK pulse will be output at the same timing as the HSYNC_L and VSYNC_L falling edges when the internal state of the encoder is the fourth field. And if the encoder is set to PAL, the GENLOCK pulse will be output at the same timing as the HSYNC_L and VSYNC_L falling edges when the internal state of the encoder is the eighth field.

BLOCK FUNCTIONAL DESCRIPTION

• Prologue Block

This block separates input data at the ITU Rec.656 format into a luminance signal (Y) and a chrominance signal (Cb & Cr), and also generates information concerning sync signals HSYNC_L, VSYNC_L, and BLANK_L.
This block separates input data at the 27 MHz YCbCr (8-bit input) format into a luminance signal (Y) and a chrominance signal (Cb & Cr).
This block separates input data at the 13.5 MHz YCbCr (16-bit input) format into a chrominance signal Cb and a chrominance signal Cr.
Of the processed input data, luminance and chrominance signals other than valid pixel data are replaced by 8'h10 and 8'h80 respectively.
RGB signals are converted into luminance (Y) and chrominance (Cb & Cr) signals.

• Y Limiter Block

This block limits the luminance input signal by clipping the lower limit of an input signal outside the ITU601 Standard

- Signals are limited to YD = 16 when YD < 16.
- Signals are limited to YD = 254 when YD (input during a valid pixel period) = 255.

In other cases, signals are fed as is to next processing.

• C Limiter Block

This block limits the chrominance signal by clipping the upper and lower limits of the input signal outside the ITU601 Standard.
CD = 1 when CD = 0 is input during a valid pixel period.
CD = 254 when CD = 255 is input during a valid pixel period.

• Y Level Converter

Converts ITU-601 standard luminance signal level to DAC digital input level.

• U Level Converter

Converts ITU-601 standard chrominance signal level to DAC digital input level.

• V Level Converter

Converts ITU-601 standard chrominance signal level to DAC digital input level.

• RGB Level Converter

Converts RGB signal level to DAC digital input level.

• YUV Color Generator

This block generates luminance and chrominance signals from overlay color signals OLR, OLG and OLB. Control signals (CR [2:0]) control the output content (overlay or color bar) and output level (100%, 75%, 50%, 25%).

- **Overlay Control**
  This block selects input image data or YUV Color Generator output signals.
  It is determined by the level of the control signal (OLC, CR [2]), as shown below: (x : don't care)
  CR [2] = 1, OLC = x: Selects color bar signal (YUV Color Generator output signal).
  CR [2] = 0, OLC = 1: Selects overlay signal (YUV Color Generator output signal).
  CR [2] = 0, OLC = 0: Selects input image data.

- **YUV to RGB Converter**
  This block converts YUV signals selected in the overlay control block into RGB signals.

- **Black & Blank Pedestal**
  This block adds sync signals at the luminance side to luminance signals.

- **Interpolator + LPF**
  This block executes data interpolation and the elimination of high frequency components by LPF for input chrominance signals.

- **I^2C Control Logic**
  This is the serial interface block based on I^2C standard of Phillips Corporation.
  Internal registers MR and CR can be set from the master side.
  When writing to the internal registers other than MR [1] (black level control) and CR [1:0] (overlay level), written contents are immediately set to them. It is during the vertical blanking period that written contents are set to MR [1] and CR [1:0].

- **Sync Generator & Timing Controller**
  This block generates sync signals and control signals.
  This block operates in slave mode, which performs external synchronization, and in master mode, which internally generates sync signals.

- **Color Burst Generator**
  Outputs U and V components of amplitude of burst signals.

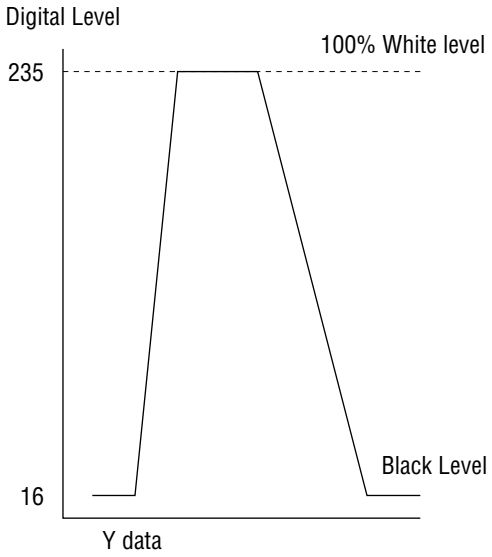
- **Subcarrier Generator**
  Executes color subcarrier generation.

- **Low Pass Filter (LPF)**
  This block performs upsampling at CLKX2 for luminance signals and chrominance signals modulated with CLKX1 divided from CLKX2. Interpolation processing is executed in this process.

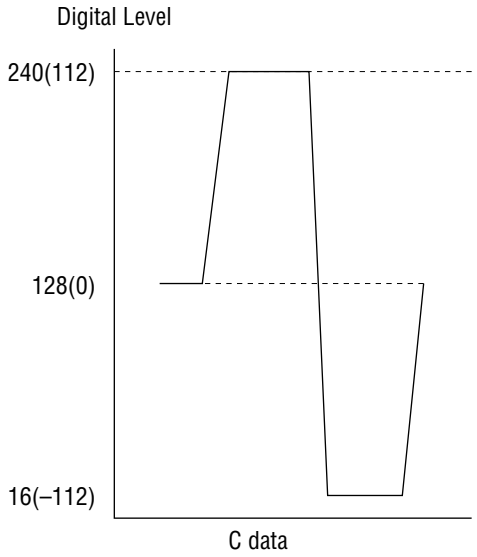
INPUT DATA FORMAT

• Input Level 1 (Y CbCr format)

The signal level specified by the ITU601 is input.
When other signal levels than specified by the ITU601 are input, the luminance signal level is clipped to 16 to 254 and the chrominance signal level to 1 to 254.
For chrominance signal input, the offset binary and 2's complement formats are available by setting of internal registers.



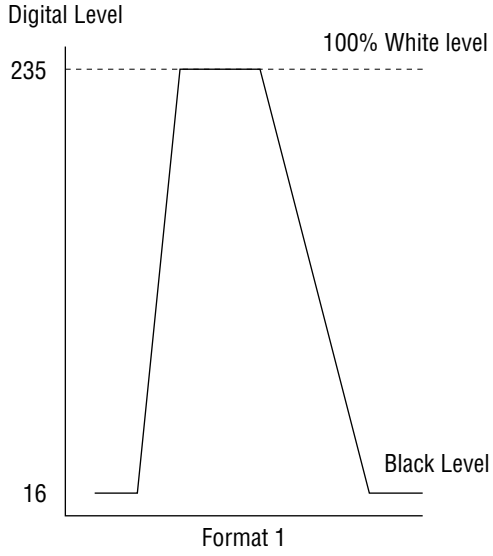
Input luminance signal level



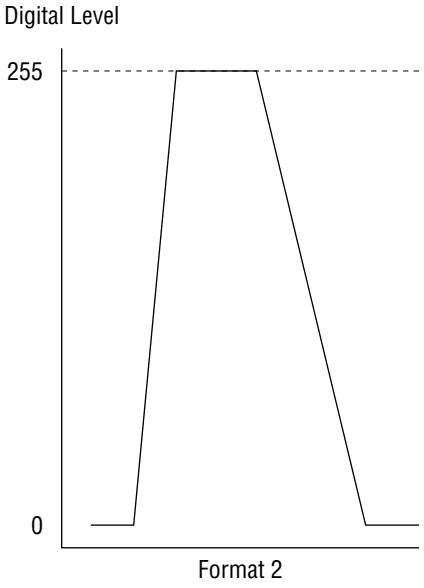
Input chrominance signal level

• Two Input Level 2 (RGB format)

Two types of input level are available by setting of internal registers.

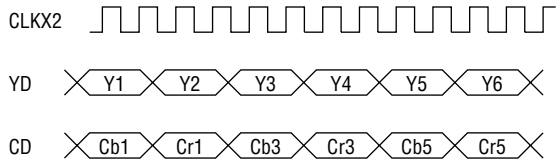


Input RGB signal level 1

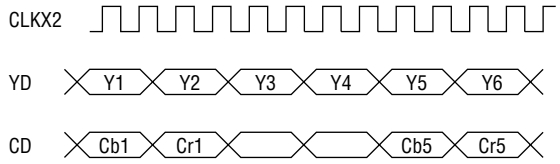


Input RGB signal level 2

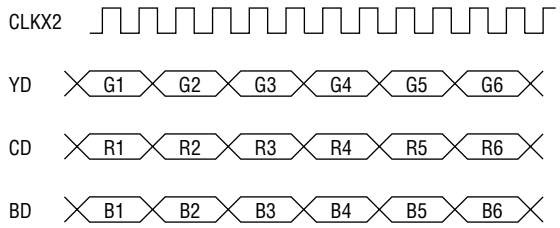
• **Basic Pixel Sampling Ratio**
4:2:2 or 4:1:1 is supported.



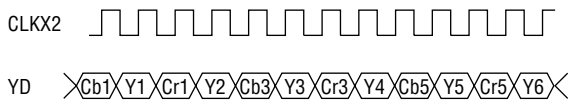
4:2:2 sampling
at 8bit Y/8bit CbCr input



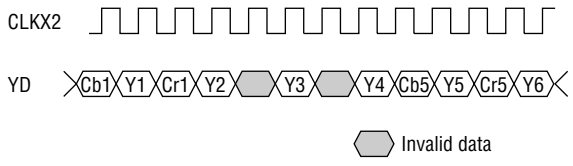
4:1:1 sampling
at 8bit Y/8bit CbCr input



At RGB input



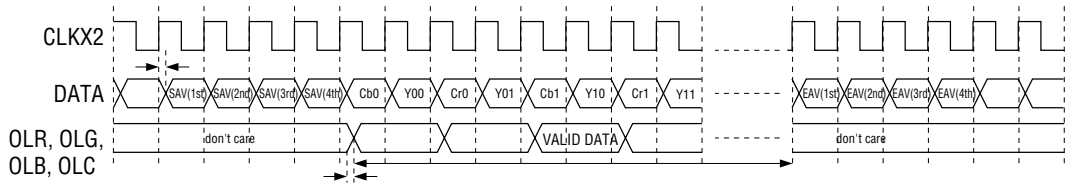
4:2:2 sampling
at 8bit YCbCr input



4:1:1 sampling
at 8bit YCbCr input

INPUT TIMING 1 (ITUR656 input)

The input data is fetched in the encoder at the rising edge of a clock pulse.



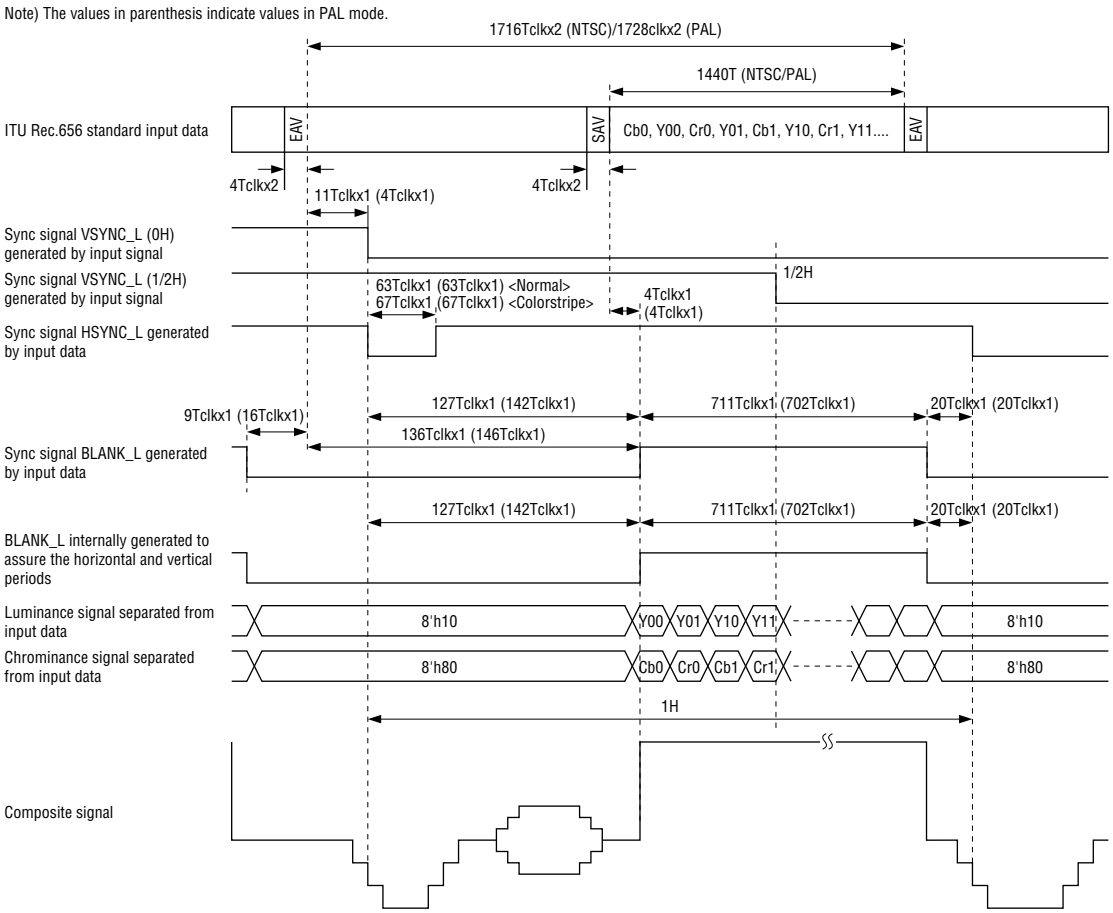
Input timing

RELATIONSHIP BETWEEN BLANK SIGNAL AND INPUT IMAGE DATA

The blank signal is generated by the ITU Rec.656 standard input data. The input image data is valid when the blank signal is "H".

VALID DATA RANGE

According to the ITU Rec.656 standard, the pixel data immediately from SAV (4th word) to a fixed value before EVA is valid.
The following figure shows the relationship between the input data at the CCIR Rec.656 format and the sync, luminance, chrominance signals which are processed inside the encoder.



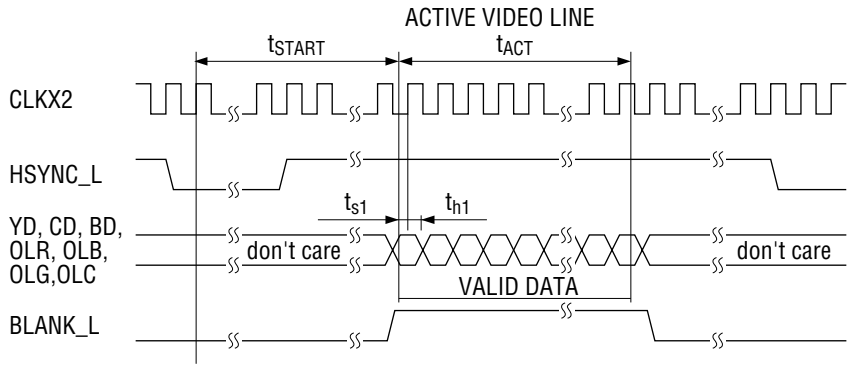
Relationship between input data and sync signal, luminance signal, chrominance signals

CLOCK TIMING2 (8bit Y/8bit CbCr input, 8bit YCbCr & RGB input)

Input Data Timing

Input data and sync signals are fed into the encoder at the rising edge of CLKX2.

Input data is handled as valid pixel data when t_{START} passes after the falling edge of HSYNC_L. Chrominance signal of input data at this time is regarded as Cb.



Video data input timing

Input data is recognized as valid pixel data when input signal BLANK_L is "H" in the t_{ACT} period. When BLANK_L is "H" during the blanking period, however, input data is not output as valid pixel data since processing to maintain blanking period is internally in-progress.

The values of t_{START} differ slightly between in master mode and in slave mode. The values of t_{START} are as follows.

In YCbCr format input mode, the values of t_{START} are the same, in 8 bit (Y) + 8 bit (CbCr) mode or in 8 bit (YCbCr) mode.

In master mode

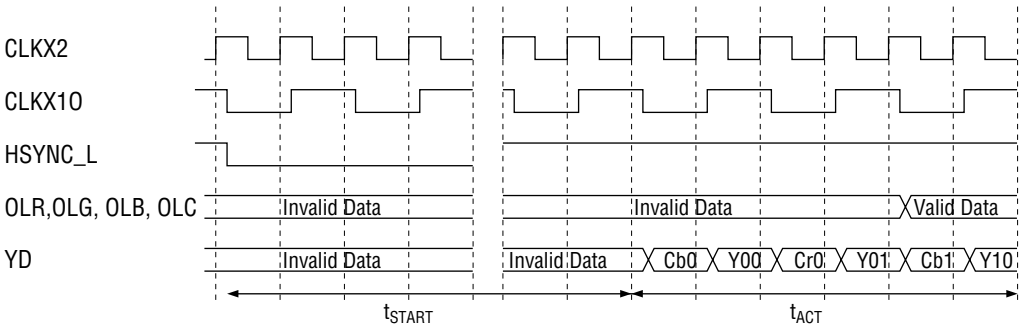
Operation mode	t_{STA}(Ts)
ITU 601 NTSC	250
ITU 601 PAL	280
4 Fsc NTSC	266
Square pixel NTSC	228
Square pixel PAL	306

In slave mode

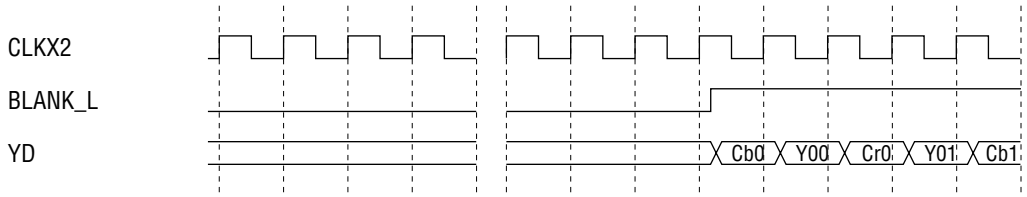
Operation mode	t_{STA}(Ts)
ITU 601 NTSC	260
ITU 601 PAL	290
4 Fsc NTSC	276
Square pixel NTSC	238
Square pixel PAL	316

$t_{STA} - t_{S1} = t_{START}$

Timing of Input Data to HSYNC_L

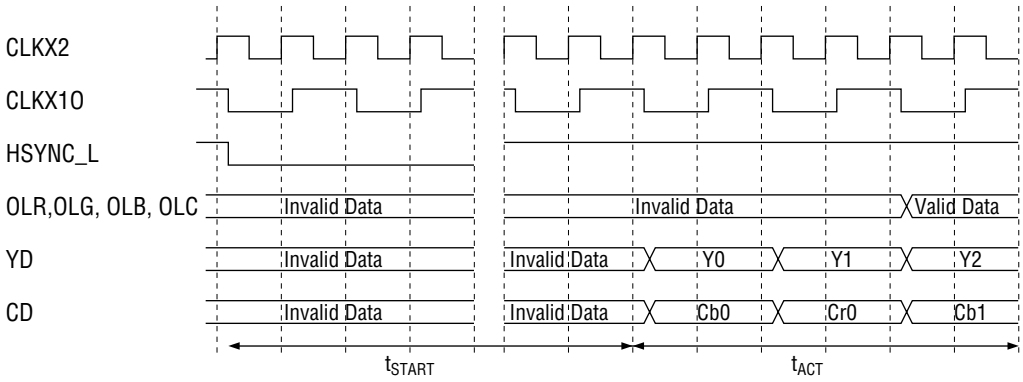


Input Timing when BLANK_L is Input

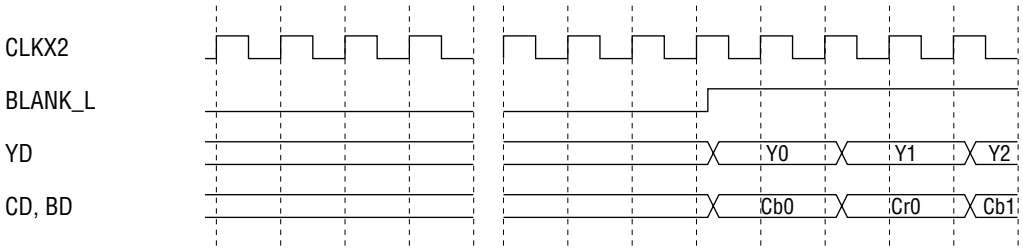


Input timing at double pixel rate YCbCr format

Timing of Input Data to HSYNC_L



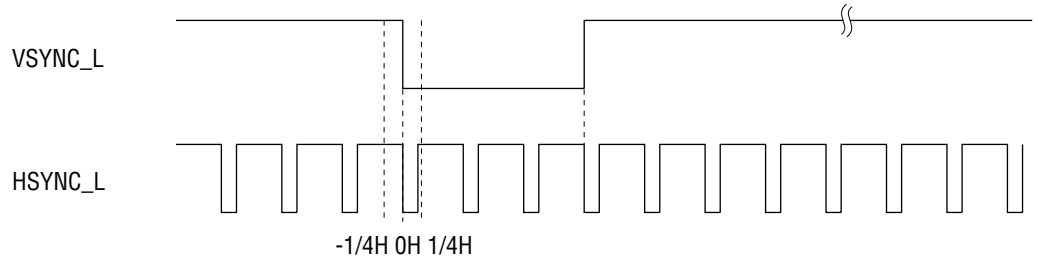
Input Timing when BLANK_L is Input



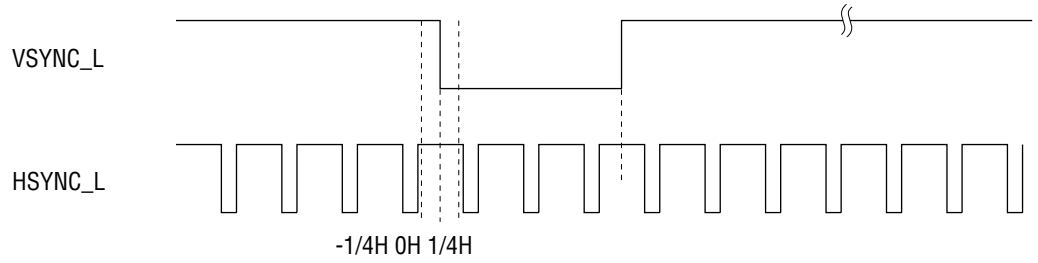
Input timing at pixel rate and RGB YCbCr format

• **VSYNC_L, HSYNC_L Input Timing**

Input timing of VSYNC_L and HSYNC_L in slave mode is as follows.



(1) If the encoder detects the VSYNC_L falling edge between -1/4H and 0H (not including 0H), it judges information with HSYNC_L and VSYNC_L as an odd field and normally operates.
(2) If the encoder detects the VSYNC_L falling edge between 0H and 1/4H (including 0H), it judges information with HSYNC_L and VSYNC_L as an odd field and mormally operates.

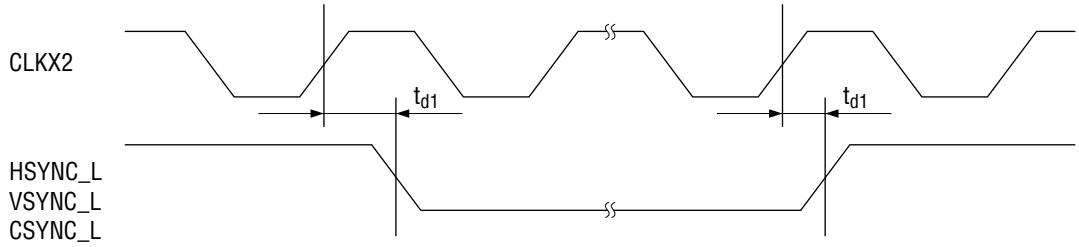


(3) If the encoder detects the VSYNC_L falling edge between 1/4H and 1/2H (not including 1/2H), it judges information with HSYNC_L and VSYNC_L as an even field and normally operates.
(4) If the encoder detects the VSYNC_L falling edge between 1/2H and 3/4H (including 1/2H), it judges information with HSYNC_L and VSYNC_L as an even field and normally operates.

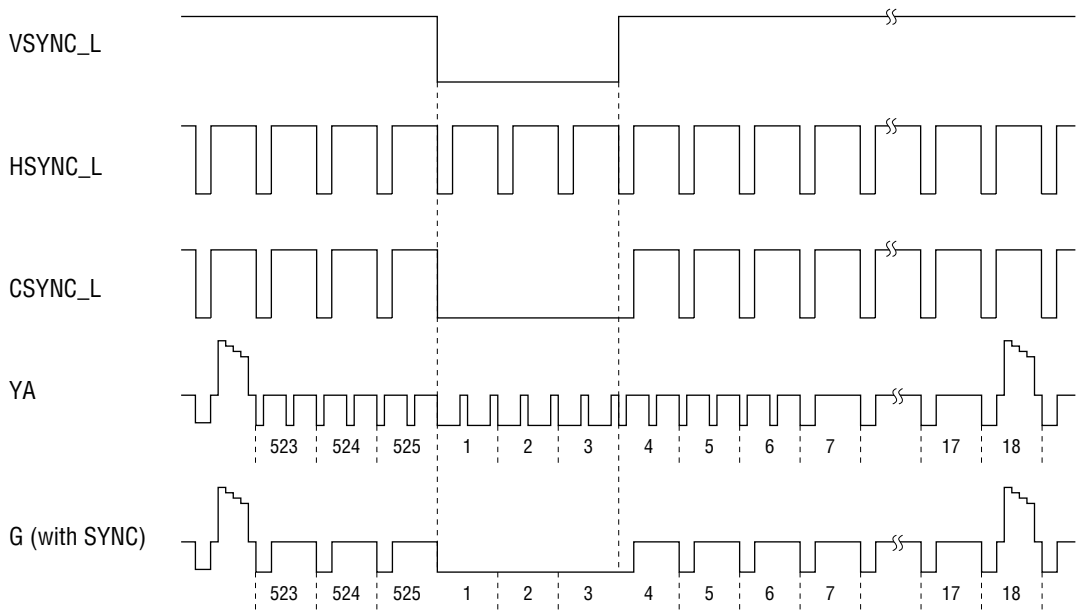
The normal vertical blanking periods cannot be obtained in the following cases:
(1) The HSYNC_L period is longer than the specification
(2) The HSYNC_L period is shorter than the specification
(3) The VSYNC_L period is longer than the specification
(4) The VSYNC_L period is shorter than the specification

Internal Synchronization Output Timing

Output timing of HSYNC_L and VSYNC_L in master mode is as follows.



Output timing 1 of internal synchronization, HSYNC_L, VSYNC_L, and CSYNC_L

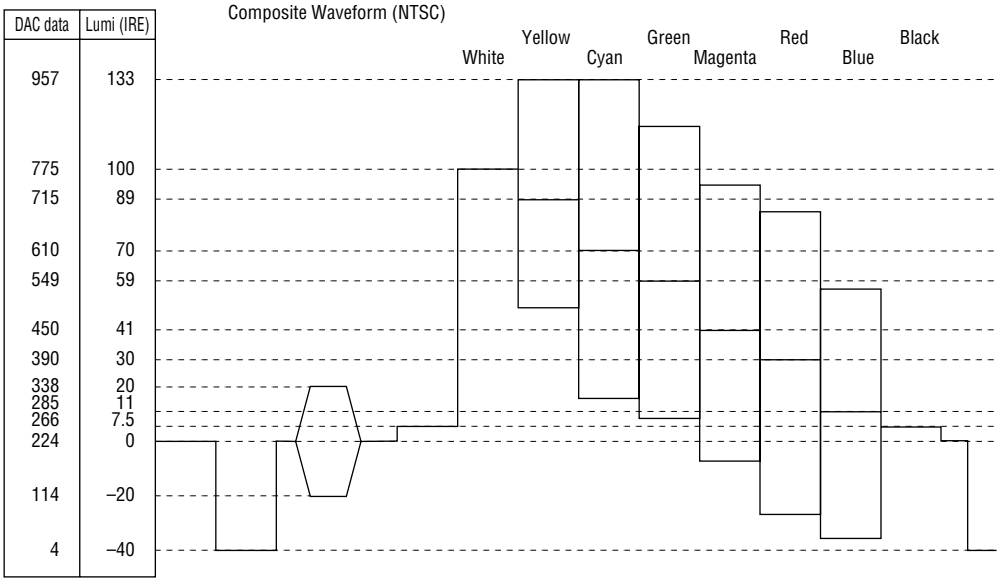


Output timing 2 of internal synchronization HSYNC_L, VSYNC_L, and CSYNC_L

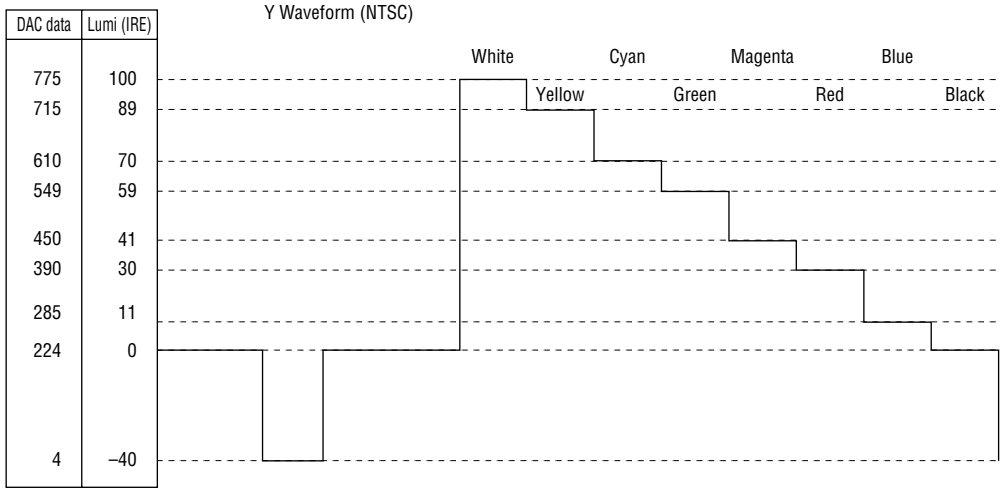
OUTPUT FORMAT

The timing conforms to the ITU624 standard.
In the NTSC operation mode, the existence/non-existence of setup level is selected by setting of internal regsiters.

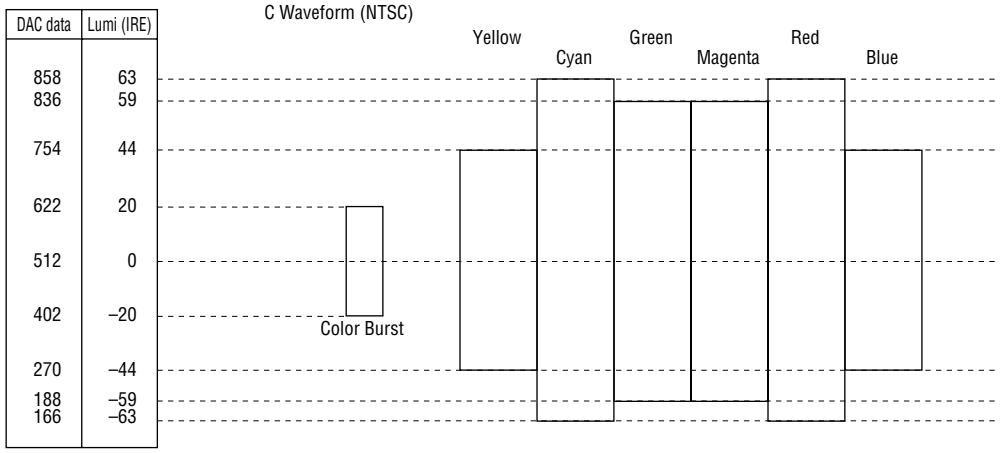
Data level on the DAC input terminal:
When the contents of 100% luminance order color bar are input into the encoder, the input level is as follows.



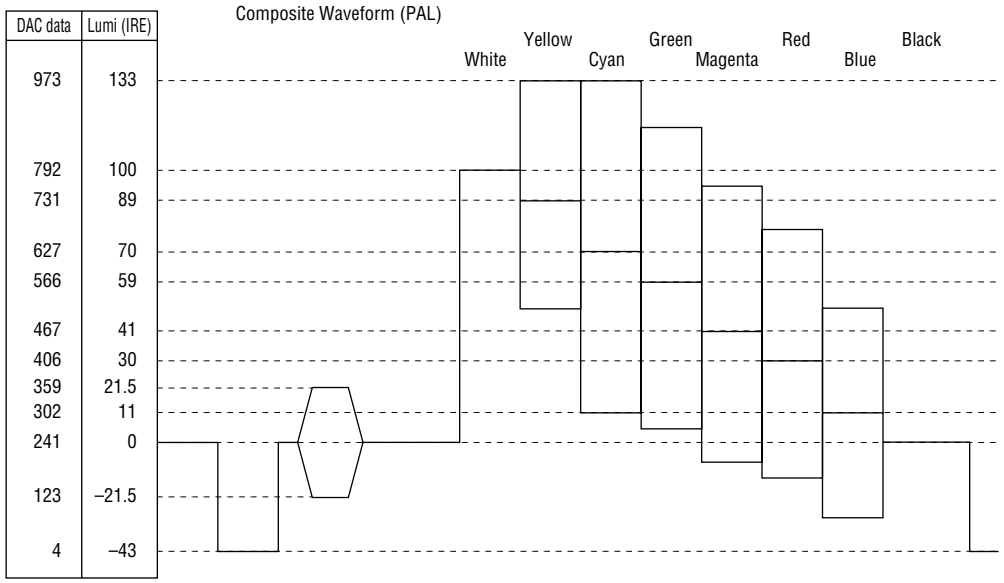
NTSC Composite Signal (Setup 7.5)



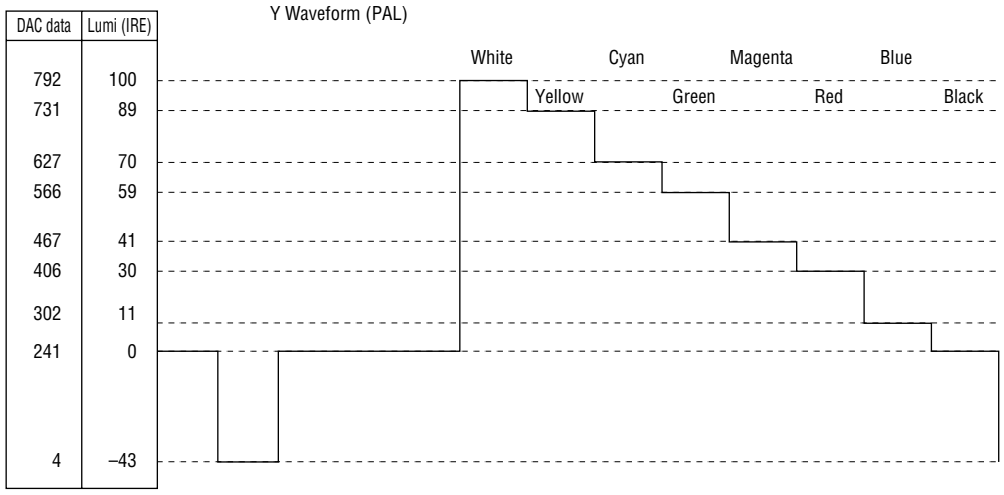
NTSC Y Signal Output (Setup 0)



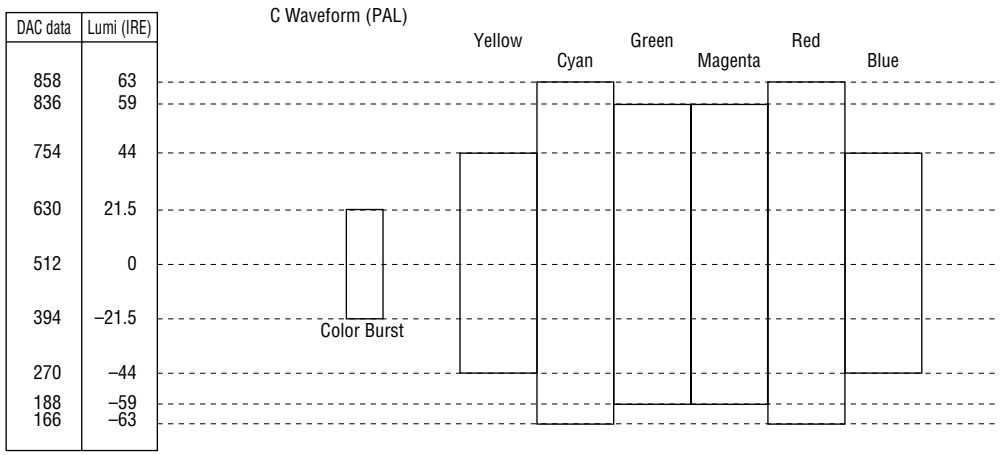
NTSC C Signal Output



PAL Composite Signal



PAL Y Signal Output

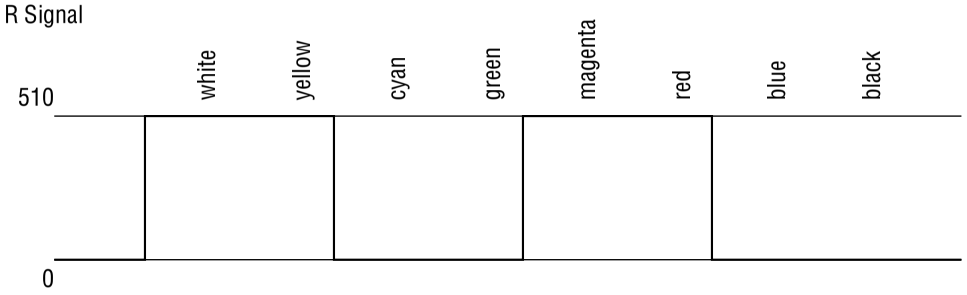


PAL C Signal Output

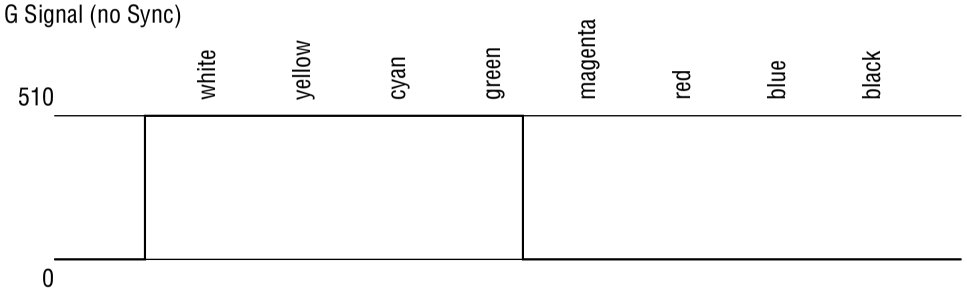
RGB Output Waveform

MR1[5] = 0

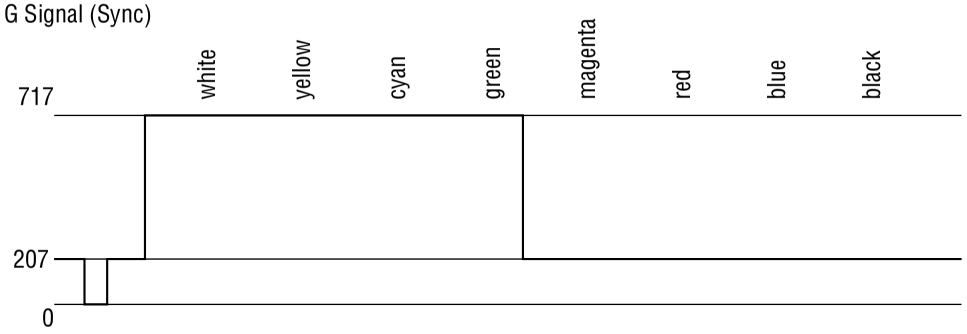
R Signal



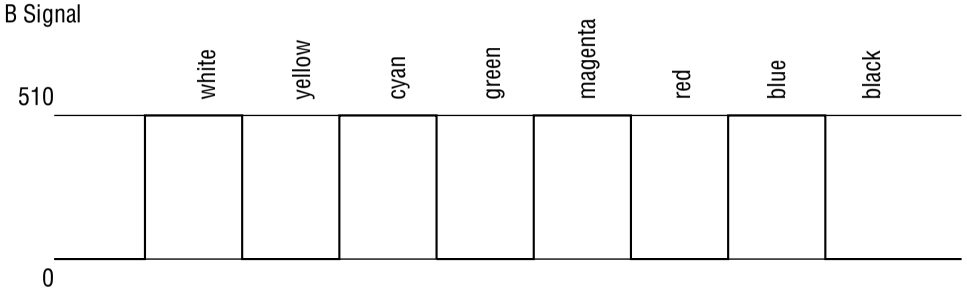
G Signal (no Sync)



G Signal (Sync)

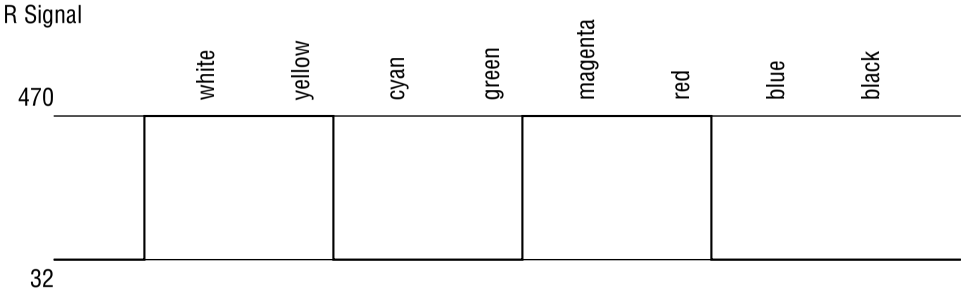


B Signal

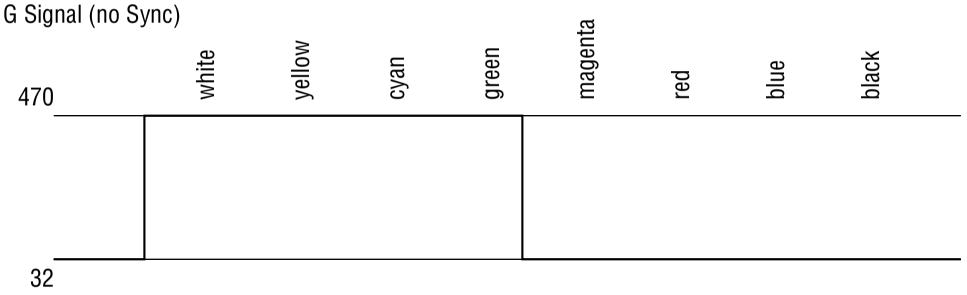


MR1[5] = 1

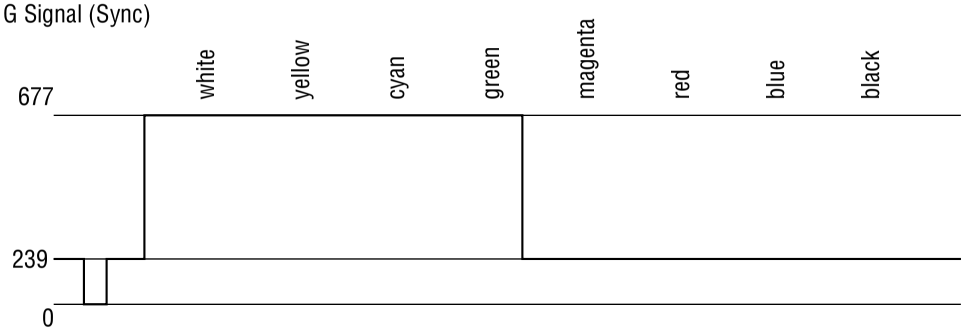
R Signal



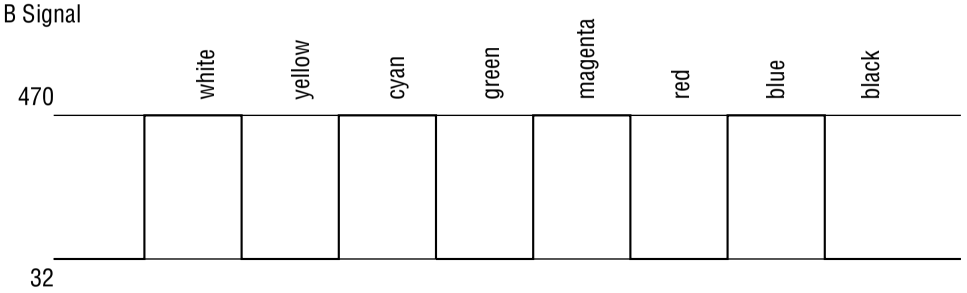
G Signal (no Sync)



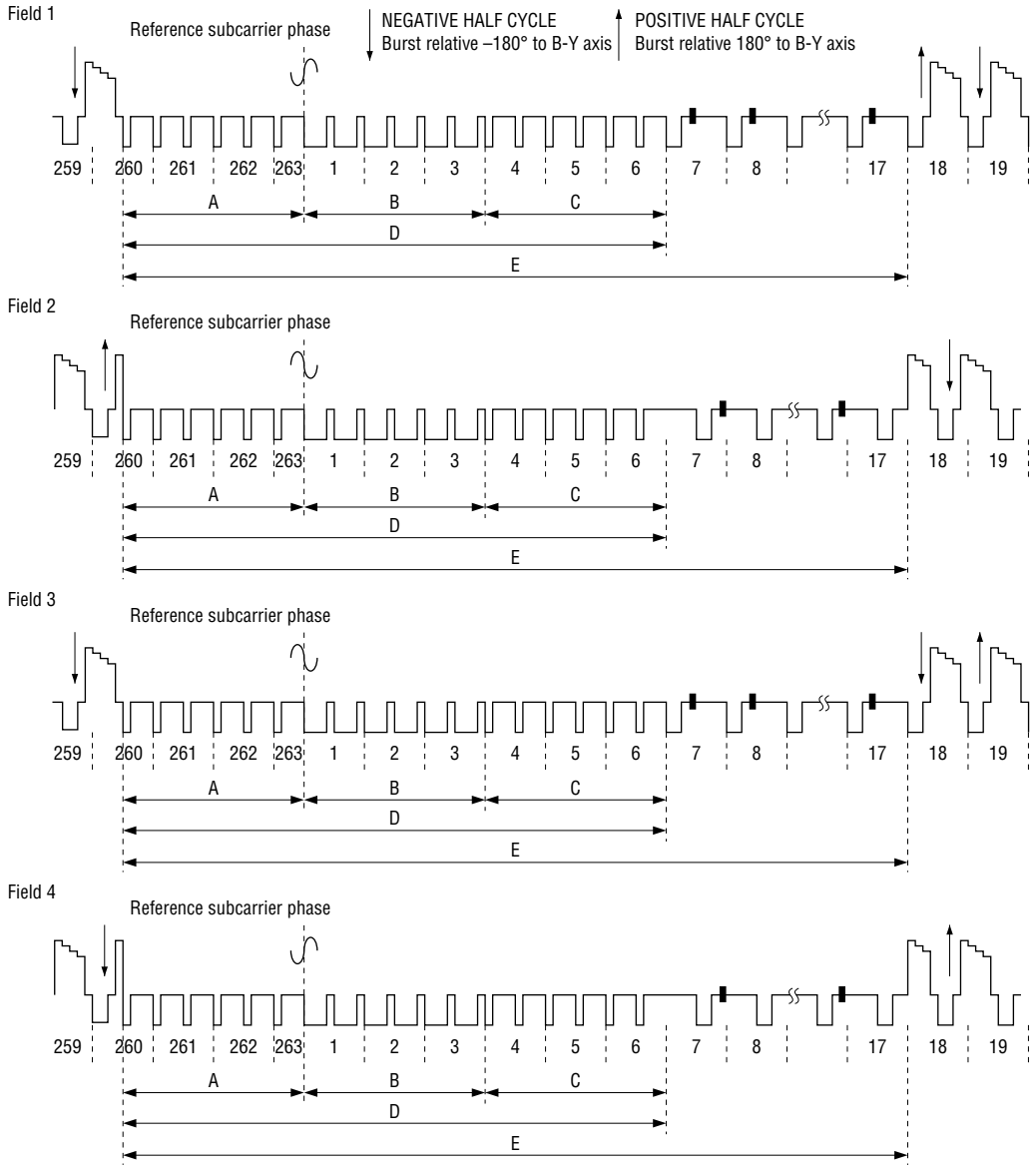
G Signal (Sync)



B Signal



NTSC (Interlaced)

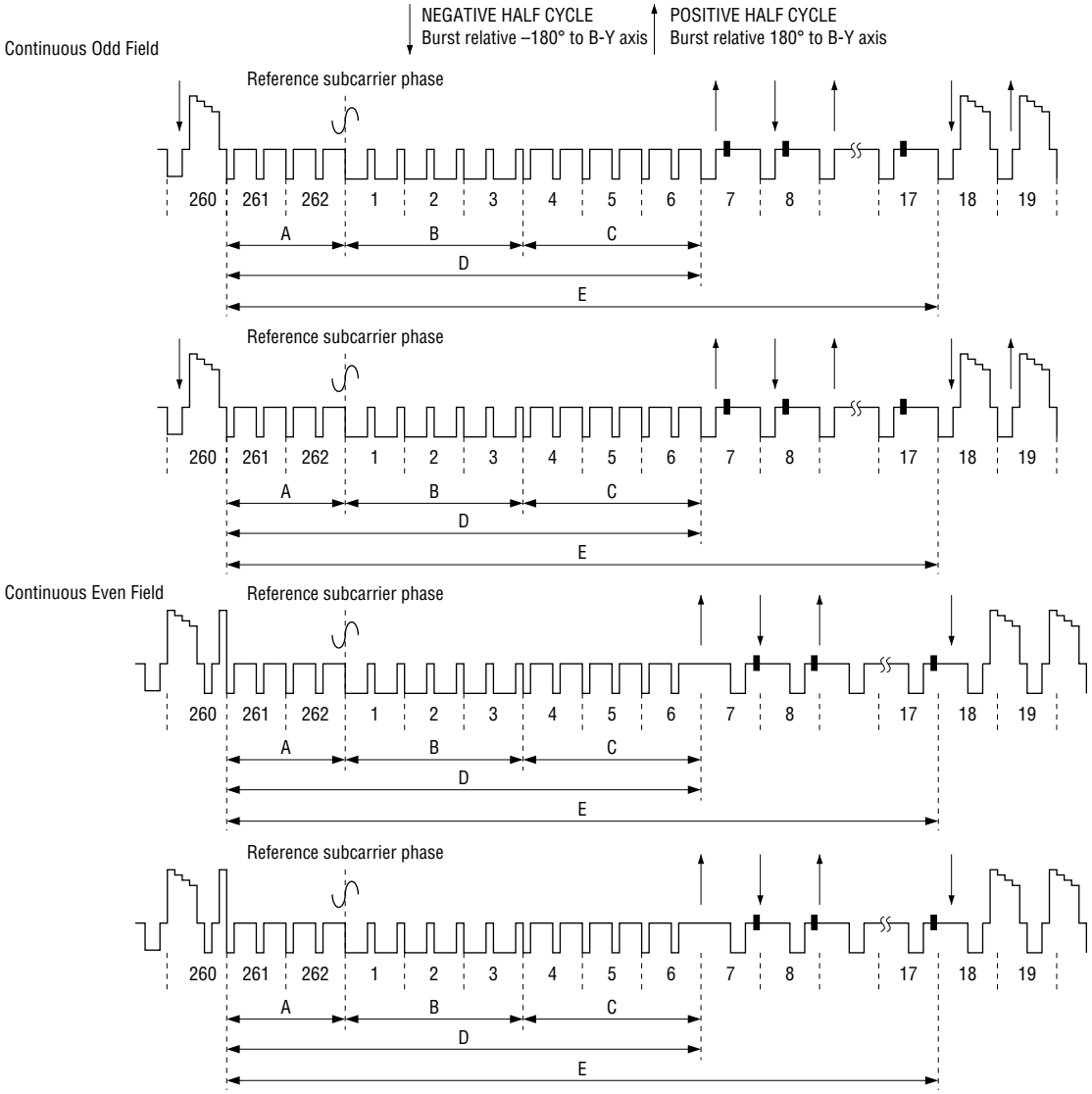


Output timing (Interlaced NTSC)

Symbol	Name	Period
		Odd field (Even field)
A	First equalizing pulse period (3H)	259.5 to 262.5H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (3H)	4 to 6H
D	Burst pause period	1 to 6,259.5 to 262.5H
E	Vertical blanking period (20H)	1 to 17,259.5 to 262.5H

Output timing (Interlaced NTSC)

NTSC (Non-interlaced)

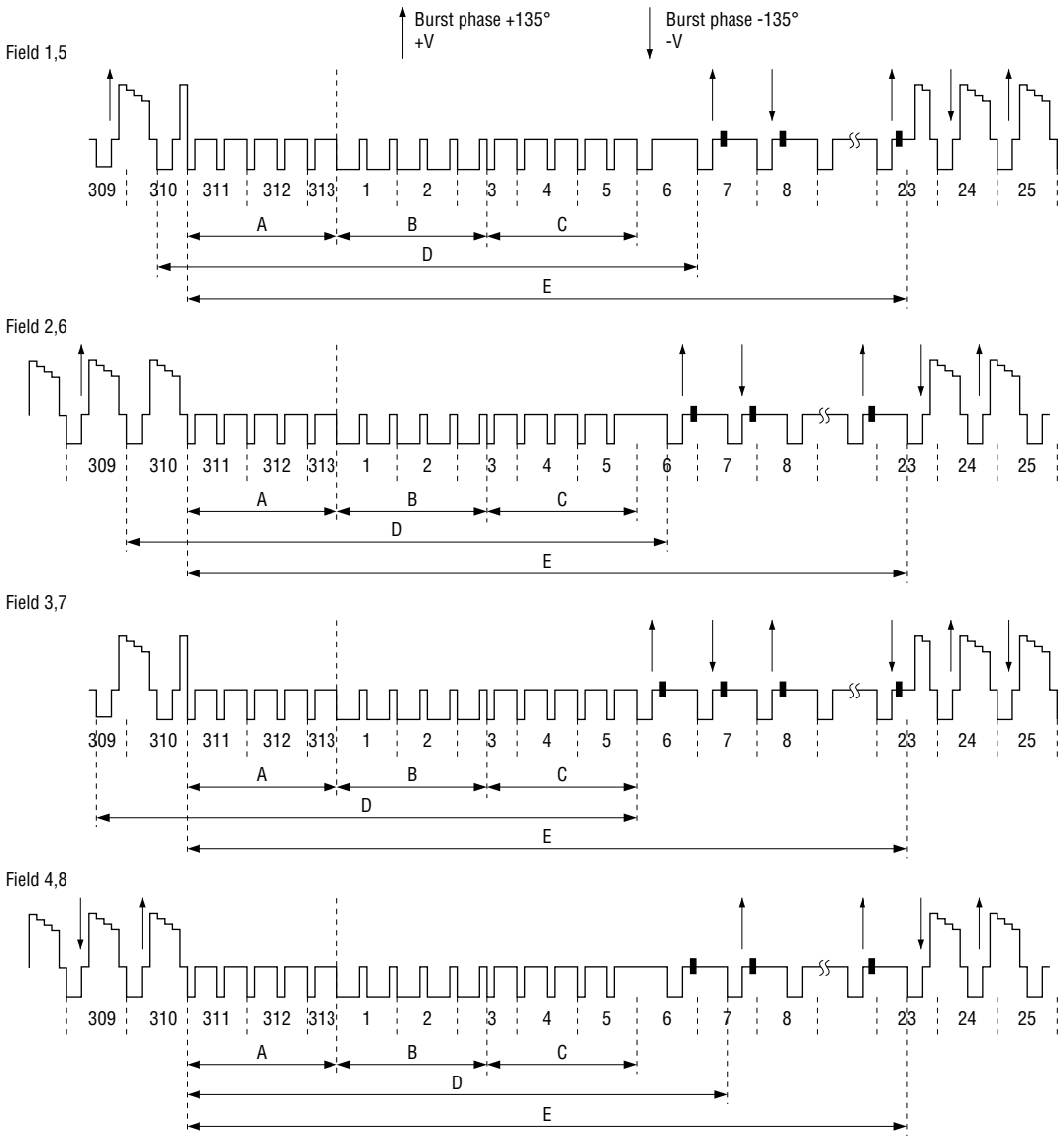


Output timing (Non-interlaced NTSC)

Symbol	Name	Period
		Continuous odd • even field
A	First equalizing pulse period (2H)	261 to 262H
B	Vertical synchronization period (3H)	1 to 3H
C	Second equalizing pulse period (2H)	4 to 6H
D	Burst pause period	261 to 6H
E	Vertical blanking period (19H)	261 to 17H

Output timing (Non-interlaced NTSC)

PAL (Interlaced)

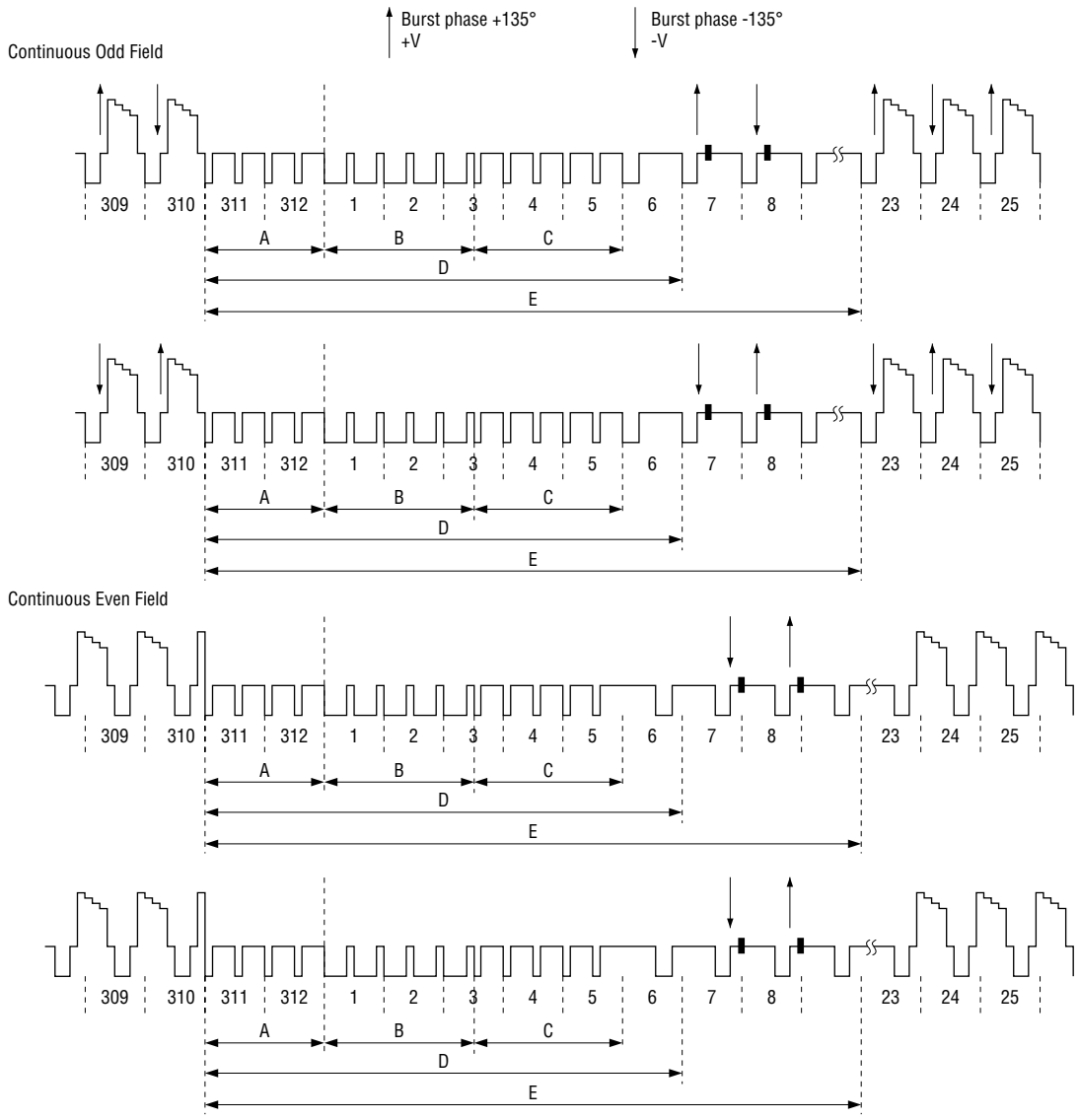


Output timing (Interlaced PAL)

Symbol	Name	Period			
		Field 1,5	Field 2,6	Field 3,7	Field 4,8
A	First equalizing pulse period (2.5H)	311 to 312.5H	311 to 312.5H	311 to 312.5H	311 to 312.5H
B	Vertical synchronization period (2.5H)	1 to 2.5H	1 to 2.5H	1 to 2.5H	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H	2.5 to 5H	2.5 to 5H	2.5 to 5H
D	Burst pause period	1 to 6,310 to 312.5H	1 to 5.5,308.5 to 312.5H	1 to 5,311 to 312.5H	1 to 6.5,309.5 to 312.5H
E	Vertical blanking period (25H)	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H	1 to 22.5,311 to 312.5H

Output timing (Interlaced PAL)

PAL (Non-interlaced)

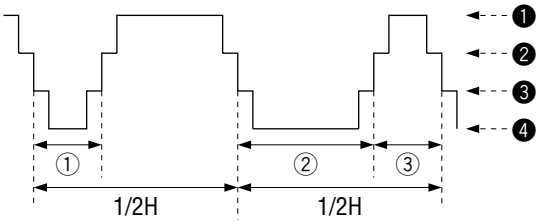


Output timing (Non-interlaced PAL)

Symbol	Name	Period
		Continuous odd • even field
A	First equalizing pulse period (2H)	311 to 312H
B	Vertical synchronization period (2.5H)	1 to 2.5H
C	Second equalizing pulse period (2.5H)	2.5 to 5H
D	Burst pause period	311 to 6H
E	Vertical blanking period (24H)	311 to 22H

Output timing (Non-interlaced PAL)

<Equalizing pulse, vertical synchronization period>

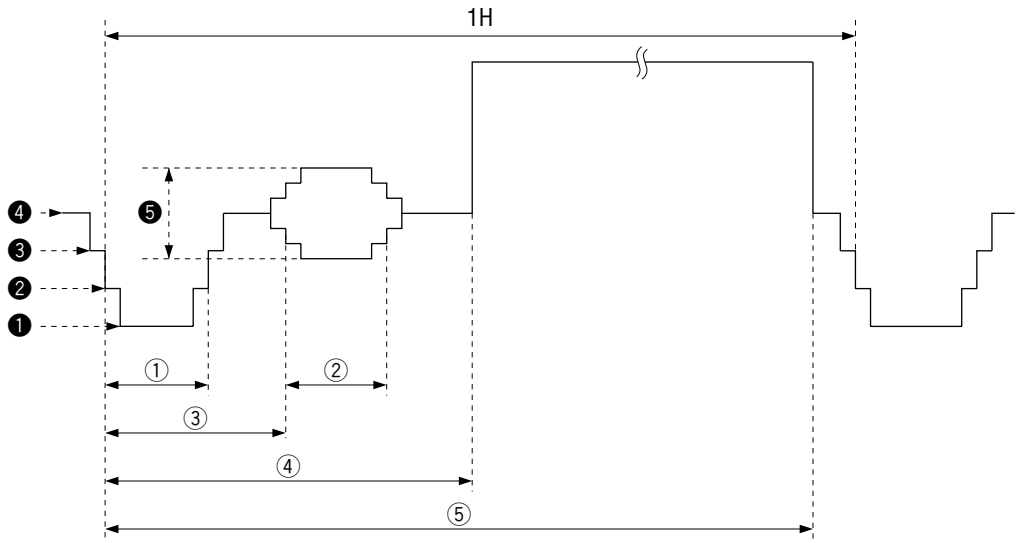


①Equalizing pulse width
②Vertical sync pulse width
③Serration
❶Blanking level
❷(synchronizing + blanking level) × (2/3)
❸(synchronizing + blanking level) × (1/3)
❹Synchronzing level

Setting content of equalizing pulse vertical synchronization period (Ts is sampling clock cycle in each mode)

	①	②	③	1/2H
ITU 601 NTSC	31Ts	365Ts	64Ts	429Ts
ITU 601 PAL	32Ts	369Ts	63Ts	432Ts
4Fsc NTSC	33Ts	387Ts	68Ts	455Ts
Square pixel NTSC	28Ts	332Ts	58Ts	390Ts
Square pixel PAL	35Ts	403Ts	69Ts	472Ts

<Horizontal blanking period>



①Horizontal sync pulse width
②Burst signal output period
③Burst signal start
④Horizontal blanking period (excluding front porch)
⑤Front porch start
❶Synchronzing level
❷(synchronizing + blanking level) × (1/3)
❸(synchronizing + blanking level) × (2/3)
❹Blanking level
❺Peak to peak value of burst

Horizontal blanking period

Setting content of horizontal blanking period (Ts is sampling clock cycle in each mode)

	①	②	③	④	⑤	Total dots/1H
ITU601 NTSC	63Ts	31Ts	71Ts	127Ts	838Ts	858
ITU601 PAL	63Ts	31Ts	75Ts	142Ts	844Ts	864
4Fsc NTSC	67Ts	36Ts	65Ts	135Ts	889Ts	910
Square pixel NTSC	58Ts	31Ts	65Ts	116Ts	762Ts	780
Square pixel PAL	69Ts	34Ts	82Ts	155Ts	922Ts	944

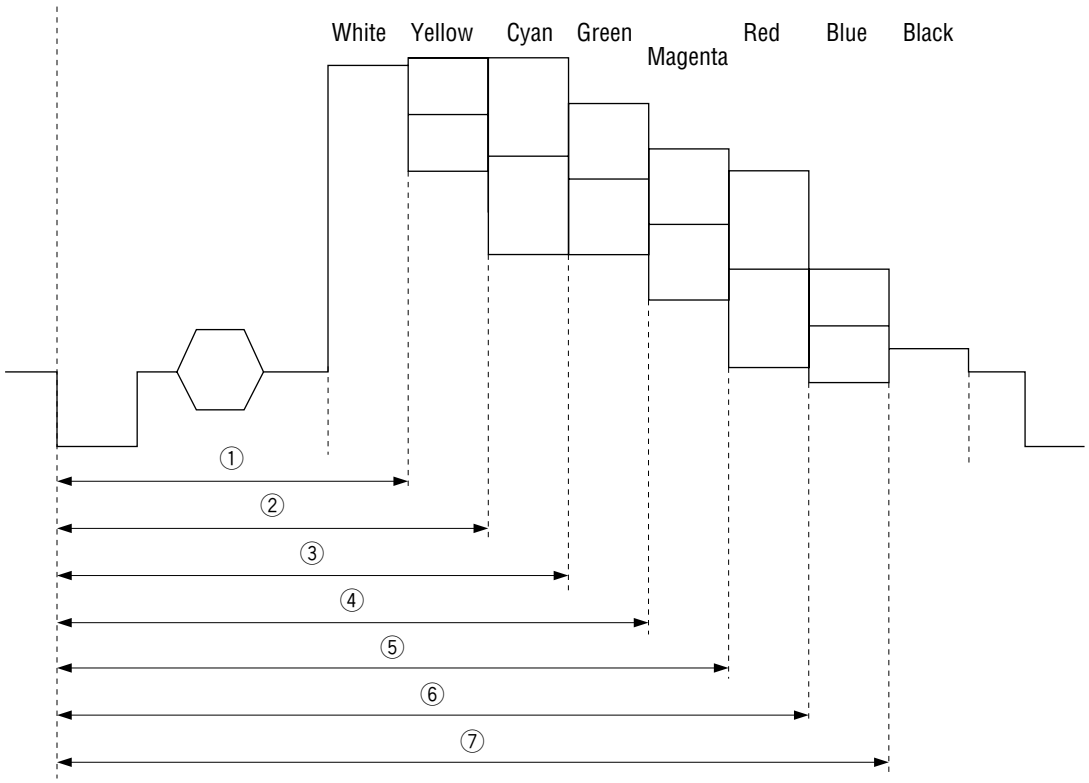
Setting content of horizontal blanking period

Setup Level Setting

When the NTSC operation mode is selected, one of the two kinds of setup level can be selected by setting of registers.
When the setup level 0 is selected, the Black-to-White is 100IRE.
When the setup level 7.5IRE is selected, the Black-to-White is 92.5IRE.
However, this setup function is valid only for the NTSC mode and invalid for the PAL mode.

Color Bar Generation Function

The 75% luminance order color bar or 100% luminance order color bar is output by setting internal registers. The output timings for each color bar color is as follows.



Output timing of each color bar color

Operation mode	hblank	①	②	③	④	⑤	⑥	⑦	1H
ITU601 NTSC	127Ts	216Ts	305Ts	394Ts	483Ts	572Ts	661Ts	750Ts	858Ts
ITU601 PAL	142Ts	230Ts	318Ts	406Ts	494Ts	582Ts	670Ts	757Ts	864Ts
4Fsc NTSC	135Ts	230Ts	325Ts	419Ts	513Ts	607Ts	701Ts	795Ts	910Ts
Square pixel NTSC	116Ts	197Ts	278Ts	395Ts	440Ts	521Ts	602Ts	682Ts	780Ts
Square pixel PAL	155Ts	251Ts	347Ts	443Ts	539Ts	635Ts	731Ts	827Ts	944Ts

(Ts : sampling clock period)

Contents of color bar output timing setting

I²C BUS FORMAT

Basic input format of I²C-bus interface is shown below.

S	Slave Address	A	Subaddress	A	Data 0	A	.....	Data n	A	P

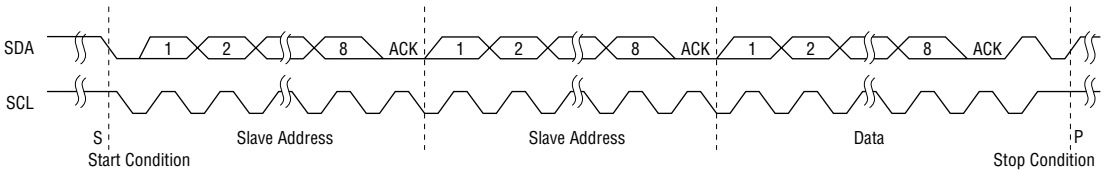
Symbol	Description
S	Start condition
Slave Address	Slave address 1000100X (ADRS pin : 0) the 8th bit is R (1)/W (0) signal.
A	Acknowledge. Generated by slave
Subaddress	Subaddress byte
Data n	Write to the address specified by the subaddress.
P	Stop condition

As described above, it is possible to write data from subaddress to subaddress continuously. Writing to discontinuous addresses is performed by repeating the Acknowledge and Stop condition formats after Data 0.

If one of the following matters occurs, the encoder will not return "A" (Acknowledge).

- The slave address does not match.
- A non-existent subaddress is specified.
- The write attribute of a register does not match "X" (write : 0 control bit).

The input timing is shown below.



I²C-bus Basic Input/Output Timing

INTERNAL REGISTERS

All registers can be written.
Details of the internal registers are described below.

Register name	R/W	Sub-address		Item to be set	Description
MR0 (Mode register)	Write Only	00	MR0 [7]	Override	Switching between the externalterminal and internal register settings(for the operation mode) *0 : External terminal setting enabled 1 : Internal register setting enabled
			MR0 [6]	Chroma format	Chrominance signal input format *0 : Offset binary 1 : 2's complement
			MR0 [5]	DAC sleep control	DAC sleep mode Control *0 : DAC active 1 : DAC sleep
			MR0 [4]	RGBMODE	Input signal switching *0 : YCbCr 1 : RGB Valid only in MODE [3:0] set as follows : (0101/0110/0111/1101/1110)
			MR0 [3:0]	Video mode select	Operation mode switching Corresponds to the external MODE [3:0] pin. The sleep mode is valid only when RGBMODE is "0". The sleep mode by the register isvalid for DAC only. *0000 : NTSC ITU-R656 0001 : NTSC 27 MHz YCbCr 0010 : NTSC 24.52 MHz Square Pixel 0011 : NTSC 28.64 MHz 4Fsc 0101 : NTSC 13.5 MHz YCbCr 0110 : NTSC 12.27 MHz 0111 : NTSC 14.32 MHz 1000 : PAL ITU-R656 1001 : PAL 27 MHz YcbCr 1010 : PAL 29.5 MHz Square Pixel 1101 : PAL 13.5 MHz 1110 : PAL 14.75 MHz 1111 : Sleep Mode

Register name	R/W	Sub-address		Item to be set	Description
MR1 (Mode register)	Write Only	01	MR1 [7]	Black level Control	Black level setup Note : Valid in NTSC mode only *0 : Black level 0IRE 1 : Black level 7.5IRE
			MR1 [6]	Counter Control	Non-standard signal input mode switching 0 : Coresonds to standard signal only 1 : Corresponds to standard and non-standard signals.
			MR1 [5]	RGB input Level	RGB input level switching RGB input level *0 : 0 to 255 1 : 16 to 235 RGB output level *0 : 0 to 510 1 : 32 to 470
			MR1 [4]	OUTSEL	Output signal switching *0 : S-video/composite 1 : RGB
			MR1 [3]	Master/Slave	Master/Slave operation switching *0 : Slave 1 : Master
			MR1 [2]	INTERLANCE	Scanning *0 : Interlace 1 : Non-interlace
			MR1 [1]	Genlock Control	Genlock function On/Off control *0 : Genlock On 1 : Genlock Off
			MR1 [0]	Genlock Select	Switching vetween Genlock control by the external pin and control by the internal register. *0 : External pin Genlock control is valid 1 : Internal register control is valid

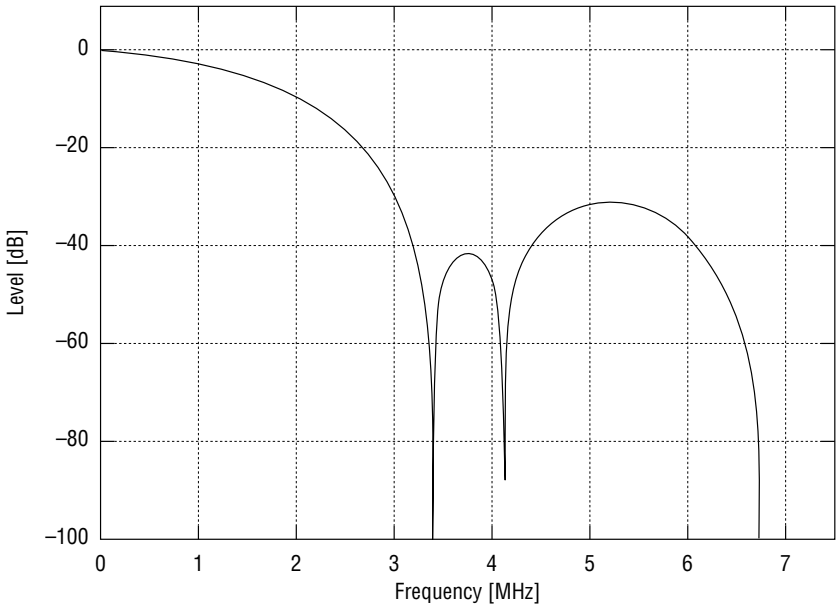
Register name	R/W	Sub-address		Item to be set	Description
CR0 (Command Register)	Write Only	02	CR0 [6]	CSYNC	Addition control of CSYNC_Lat RGB output *0 : Addition of CSYNC 1 : No addition of CSYNC to G signal
			CR0 [5]	FOUT	FOUT palarity change *0 : Odd field "L", Even field "H" 1 : Odd field "H", Even field "L"
			CR0 [4]	Trap Filter	TRAP filter On/Off control *0 : Trap filter Off 1 : Trap filter On
			CR0 [3]	Color Bar	Adjusting luminance ordercolor bar output control *0 : Input image data or overlay data 1 : Luminance order color bar
			CR0 [2:1]	Overlay level	Overlay signal/adjusting luminance order color bar output level control 11 : 25% 10 : 50% 01 : 75% *00 : 100%
			CR0 [0]	Sampling rate	Sampling rate control *0 : 4:2:2 1 : 4:1:1
CR1 (Command Register)	Write Only	03	CR1 [3:0]	Luminance Level	Adjusting luminance levelof input image data *0000 : 100.00% 0001 : 96.875% 0010 : 93.750% 0011 : 90.675% 0100 : 87.500% 0101 : 84.375% 0110 : 81.250% 0111 : 78.125% 1000 : 75.000% 1001 : 71.875% 1010 : 68.750%

FILTER CHARACTERISTICS

The characteristics of LPF used for color signal processing and interpolation filters used for upsampling processing are shown below.

LPF for 422 color signals

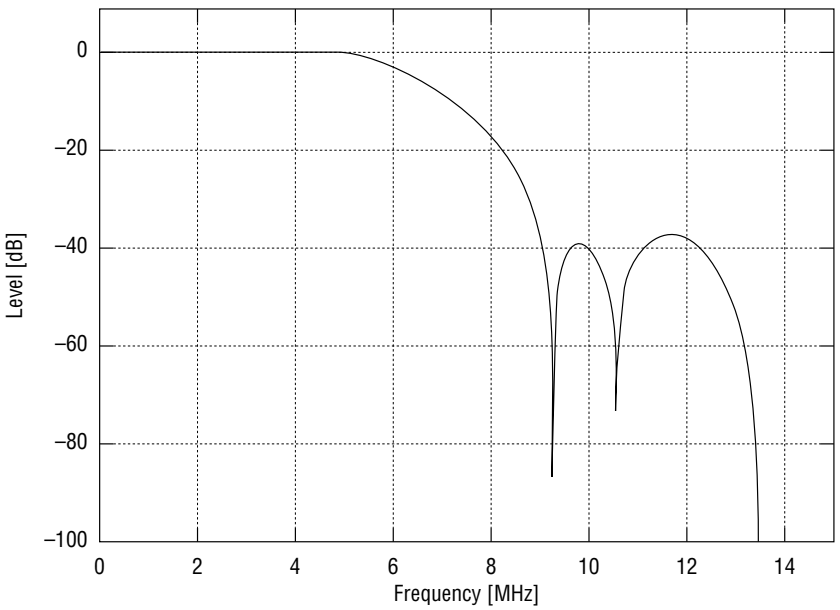
The following shows the characteristics when the clock frequency is 13.5 MHz.



422 Interpolation + LPF Frequency Characteristic

Interpolation

The following shows the characteristics when the clock frequency is 27 MHz.

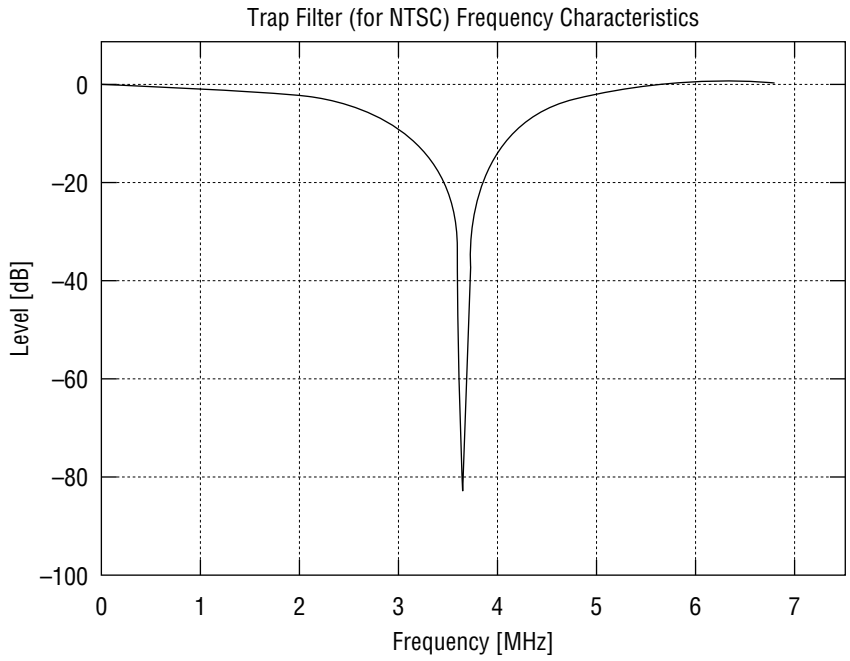


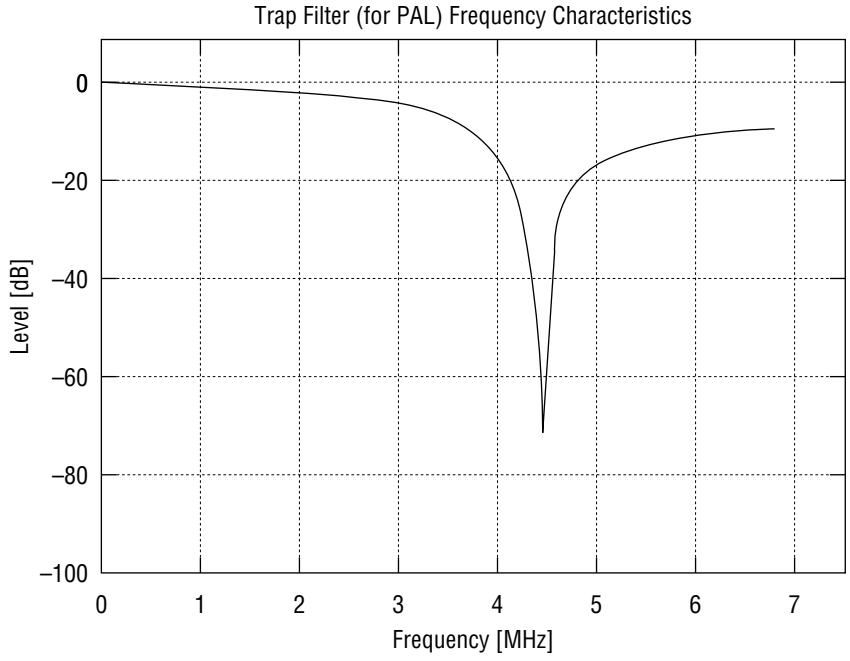
Up Sampling Filter Frequency Characteristic

(Note) The characteristics of these filters are based on design data.

Trap Filter

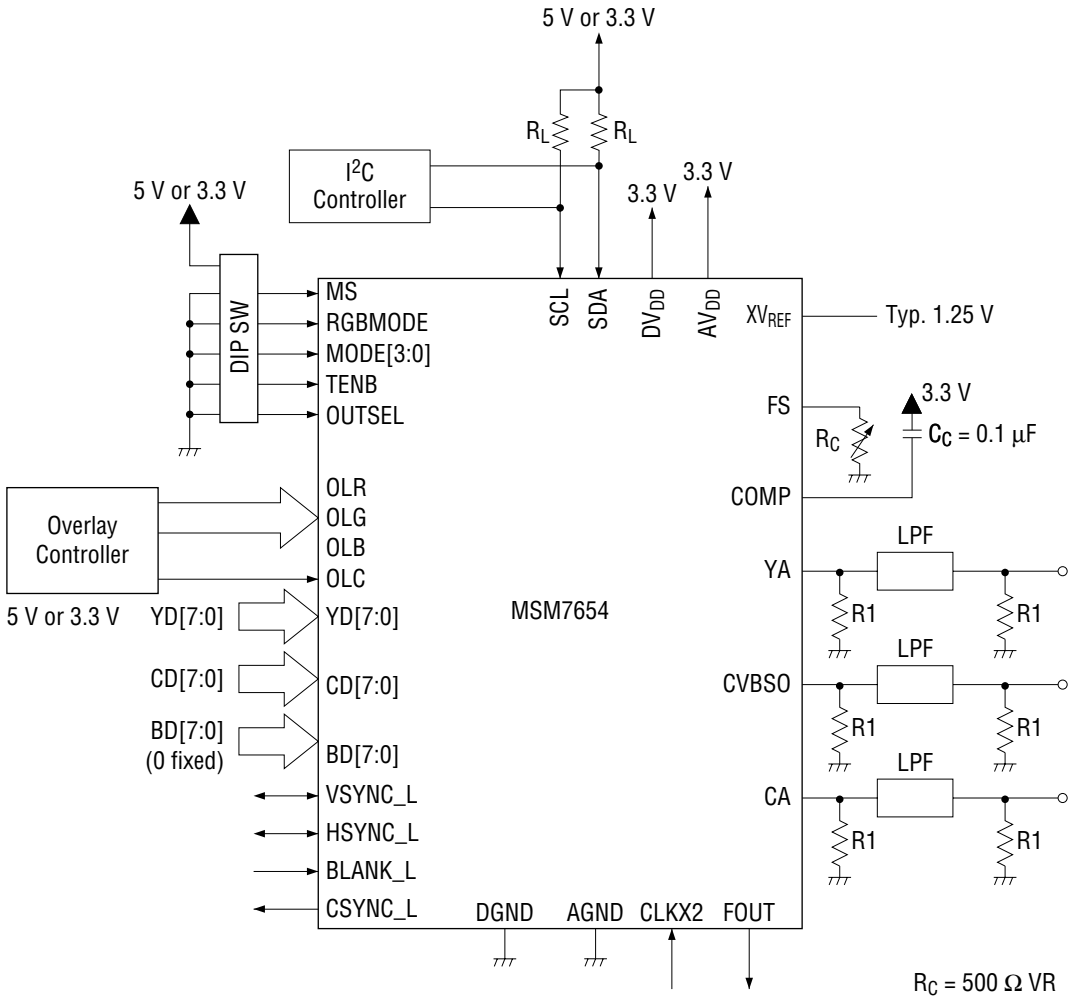
The following shows the characteristics when the clock frequency is 27 MHz.



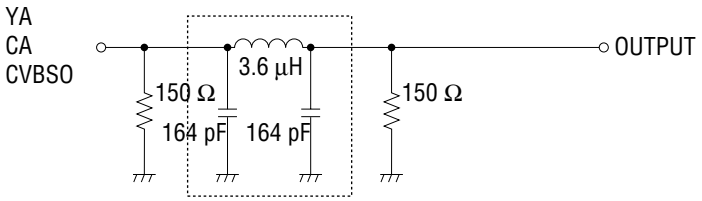


(Note) The characteristics of these filters are based on design data.

APPLICATION CIRCUIT EXAMPLE (YCbCr 16-bit input mode)



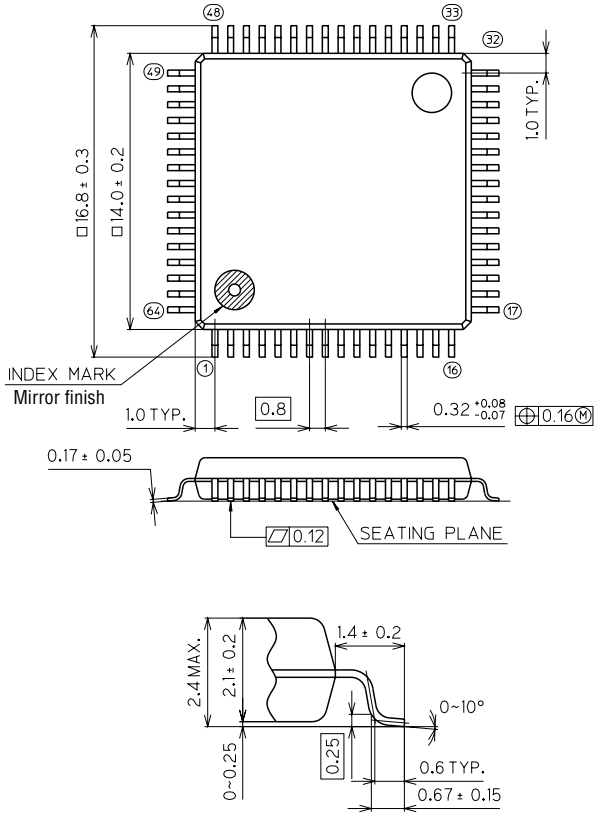
Sample of Analog Output Circuit



Note: The termination of a DA converter analog output with a 37.5 Ω load eliminates need for an AMP.

PACKAGE DIMENSIONS

(Unit : mm)



64-Pin Plastic QFP

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