

## Series PVY117

Microelectronic Power IC  
HEXFET® Power MOSFET Photovoltaic Relay  
Single-Pole, Normally-Open, 0-40V AC/DC, 470mA

### General Description

The PVY117 Series Photovoltaic Relay is a single-pole, normally-open solid-state relay that can replace dry and Mercury-wetted reed relays in many applications. It utilizes International Rectifier's proprietary HEXFET power MOSFET as the output switch, driven by an integrated circuit photovoltaic generator of novel construction. The output switch is controlled by radiation from a GaAlAs light emitting diode (LED), which is optically isolated from the photovoltaic generator.

The PVY117 is ideally suited for use as matrix relay in low voltage ATE applications and general instrumentation applications involving high frequency test signals. This can be accomplished thanks to the extremely low Figure Of Merit ( $FOM = Coff * Ron$ ), which is the product of the relay's off-state output capacitance and on-state resistance.

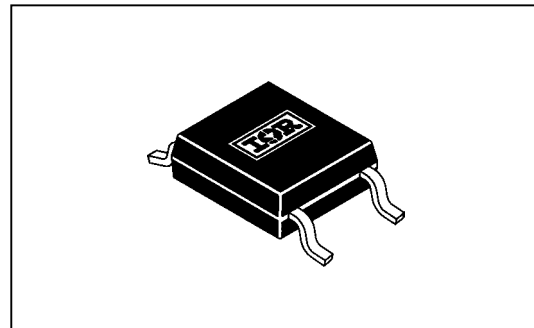
The PVY117 is packaged in a 4-pin, molded small outline package (SOP-4) with surface mount (gull wing) terminals. It is available in plastic shipping tubes or on tape-and-reel. Please refer to Part Identification information.

### Applications

- Automated Test Equipment
- Instrumentation
- Data Acquisition

### Features

- Low signal distortion at high frequencies
- Low  $Coff * Ron$  Figure Of Merit
- High off-state resistance
- 1,500 V<sub>RMS</sub> I/O isolation
- Long operational life
- Solid-State Reliability
- ESD Tolerance 2000V Human Body Model



### Part Identification

PVY117	surface-mount
PVY117-T	surface-mount, tape-and-reel



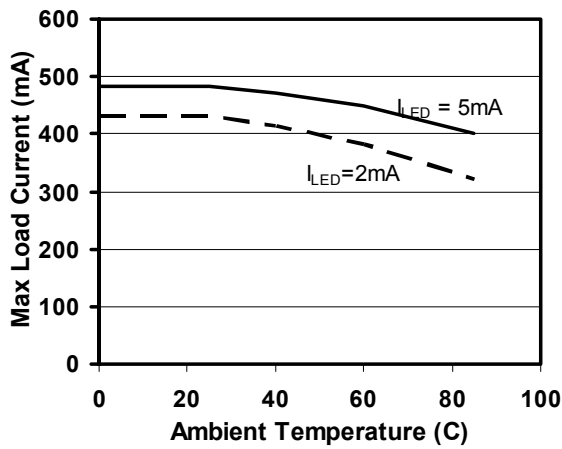


Figure 1. Current Derating Curves

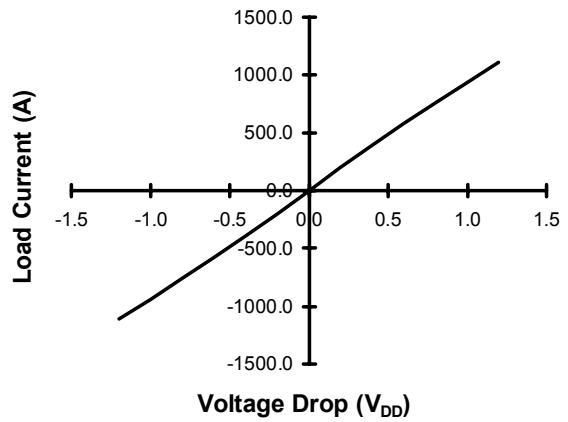


Figure 2. Typical On Characteristics

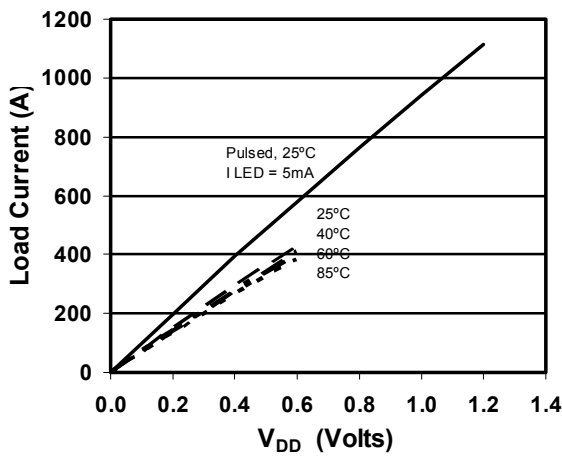


Figure 3. Typical On Characteristics

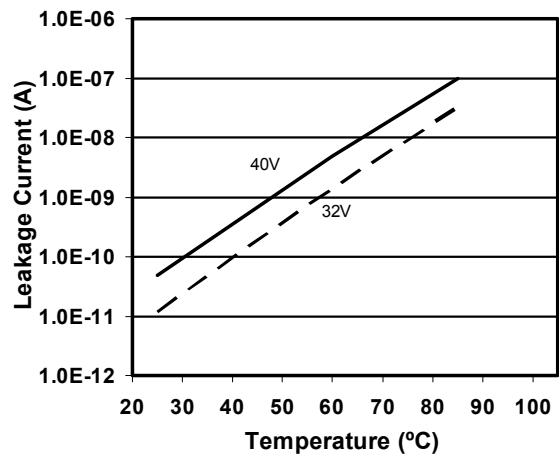


Figure 4. Typical Leakage Characteristics

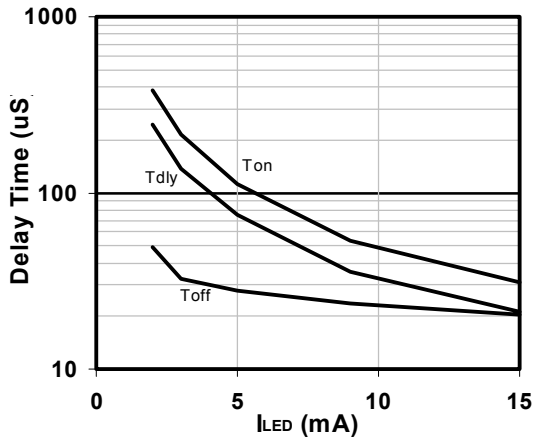


Figure 5. Typical Delay Times

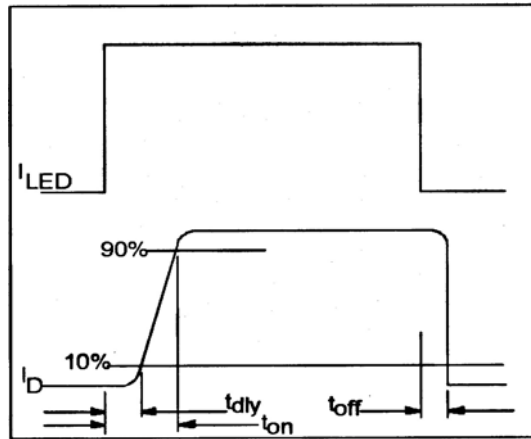


Figure 6. Delay Time Definitions

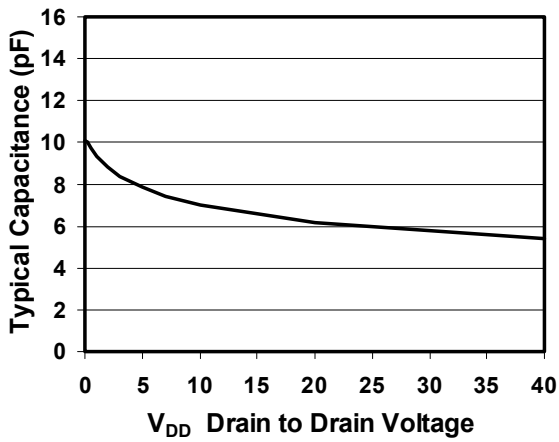


Figure 7. Output Capacitance

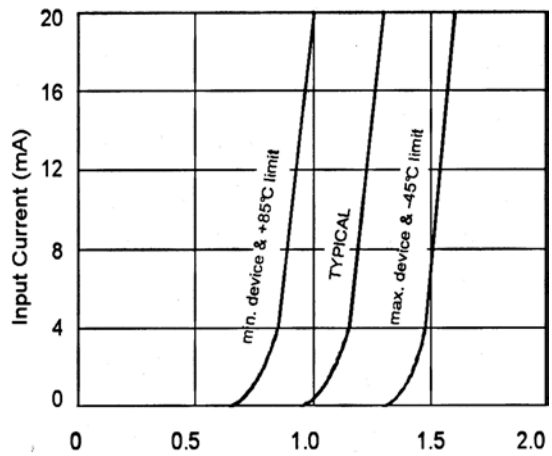


Figure 8. Input Characteristics (Current Controlled)

**Case Outlines - 4 Lead SOP**

