

FEATURES

- Normally ON Configuration
- Low Interelectrode Capacitances
- High-Speed Switching
- Wide Dynamic Range

APPLICATIONS

- High-Speed Analog Switches
- Wide-Band Dual Differential Amplifiers
- Dual Cascode Amplifiers
- High Intercept Point Double Balanced Mixers

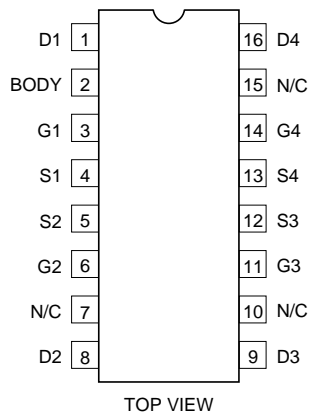
DESCRIPTION

The SD5501 is manufactured utilizing Calogic's proprietary high speed, low capacitance DMOS process featuring an N-Channel depletion-mode design. This "normally-ON" device is well suited for high speed instrumentation and communication systems where multiple channels are required for fast switching or dual amplification. Available in a 16-pin plastic dual in-line plastic package or chip form.

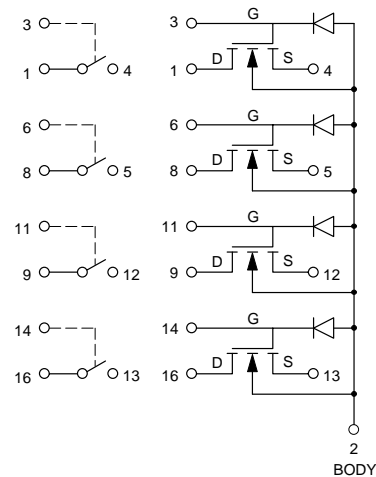
ORDERING INFORMATION

Part	Package	Temperature Range
SD5501N	Plastic	-55°C to +125°C
XSD5501	Sorted Chips in Carriers	-55°C to +125°C

PIN CONFIGURATION



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

V_{DS} Drain-Source Voltage	+30 Vdc	P_D Total Package Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	640 mW
V_{SD} Source-Drain Voltage	+0.5 Vdc	Linear Derating Factor	10.7 mW/ $^\circ\text{C}$
V_{DB} Drain-Body Voltage	+30 Vdc	P_D Single Device Power Dissipation (at or below $T_A = +25^\circ\text{C}$)	300 mW
V_{SB} Source-Body Voltage	+15 Vdc	Linear Derating Factor	5.0 mW/ $^\circ\text{C}$
V_{GS} Gate-Source Voltage	+25 Vdc	T_j Operating Junction Temperature Range . .	-55 to +85 $^\circ\text{C}$
V_{GB} Gate-Body Voltage	+25 Vdc	T_s Storage Temperature Range	-55 to +150 $^\circ\text{C}$
Gate-Body Voltage	-0.3 Vdc		
V_{GD} Gate-Drain Voltage	+25 Vdc		
I_D Continuous Drain Current	50 mA		

ELECTRICAL CHARACTERISTICS ($T_A = +25^\circ\text{C}$ unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	TEST CONDITIONS
STATIC						
B_{VDS}	Drain-Source Breakdown Voltage	20			V	$I_D = 10 \text{ nA}, V_{GS} = V_{BS} = -5.6\text{V}$
B_{VSD}	Source-Drain Breakdown Voltage	10				$I_S = 10 \text{ nA}, V_{GD} = V_{BD} = -5.6\text{V}$
B_{VDB}	Drain-Body Breakdown Voltage	25				$I_D = 10 \text{ nA}, V_{GB} = 0, \text{Source Open}$
B_{VSB}	Source-Body Breakdown Voltage	15				$I_S = 10 \mu\text{A}, V_{GB} = 0, \text{Drain Open}$
$I_{GSS(fwd)}$	Forward Gate Leakage Current			1.0	nA	$V_{GS} = 25\text{V}, V_{DS} = V_{BS} = 0$
I_G	Gate Operating Current		-3.0	-100	pA	$V_{DG} = 15\text{V}, I_D = 5.0 \text{ mA}, V_{BS} = -5.6\text{V}$
			-0.7	-10	nA	
$V_{GS(off)}$	Gate - Source Cutoff Voltage	-1.0		-5.0	V	$V_{DS} = 10\text{V}, I_D = 1.0 \mu\text{A}, V_{BS} = 5.6\text{V}$
$V_{GS(on)}$	Gate-Source On Voltage	-0.3		-3.0		$V_{DG} = 10\text{V}, I_D = 5\text{mA}, V_{SB} = -5.6\text{V}$
I_{DSX}	Zero Gate Voltage Drain Current	7.0		40	mA	$V_{DS} = 10\text{V}, V_{GS} = 0, V_{BS} = -5.6\text{V}$
		5.0				
$r_{DS(ON)}$	Drain-Source On Resistance		100	150	ohms	$I_D = 1.0\text{mA}, V_{GS} = 0, V_{BS} = -5.6\text{V}$
DYNAMIC						
g_{fs}	Common-Source Forward Transconductance ⁽¹⁾	6.0	7.5	12	mS	$V_{DG} = 10\text{V}, I_D = 5.0\text{mA}, V_{BS} = -5.6\text{V}$
g_{os}	Common-Source Output Conductance		200	350	μS	
C_{iss}	Common-Source Input Capacitance		3.5		pF	f = 1 MHz
C_{oss}	Common-Source Output Capacitance		1.2			
C_{rss}	Common-Source Reverse Transfer Capacitance		0.3			
$C_{(gs+sb)}$	Source Node Capacitance		4.5			
MATCHING						
V_{GSM}	Gate Source Voltage Match			50	mV	$V_{DG} = 10\text{V}, I_D = 5.0\text{mA}, V_{BS} = -5.6\text{V}$
$r_{DS(on)}$	Drain-Source On Resistance Match			10%		$I_D = 1.0 \text{ mA}, V_{GS} = 0, V_{BS} = 5.6\text{V}$
I_{DXSM}	Zero Gate Voltage Drain Current Match			10%		$V_{DG} = 10\text{V}, I_D = 5.0 \text{ mA}, V_{BS} = -5.6\text{V}$
g_{fsm}	Transconductance Match ^{(1), (2)}			10%		f = 1 KHz

Note 1: Pulse Test, 80 sec, 1% Duty Cycle

Note 2: Match of 4 channels