



PCI 9080

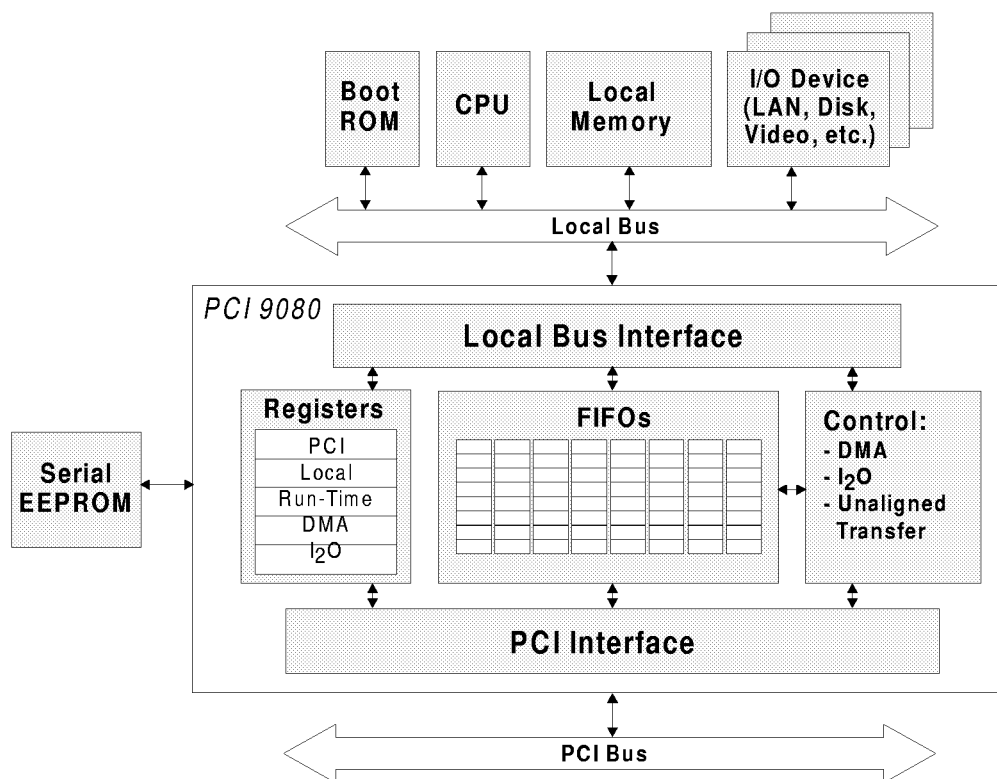
PCI I/O ACCELERATOR

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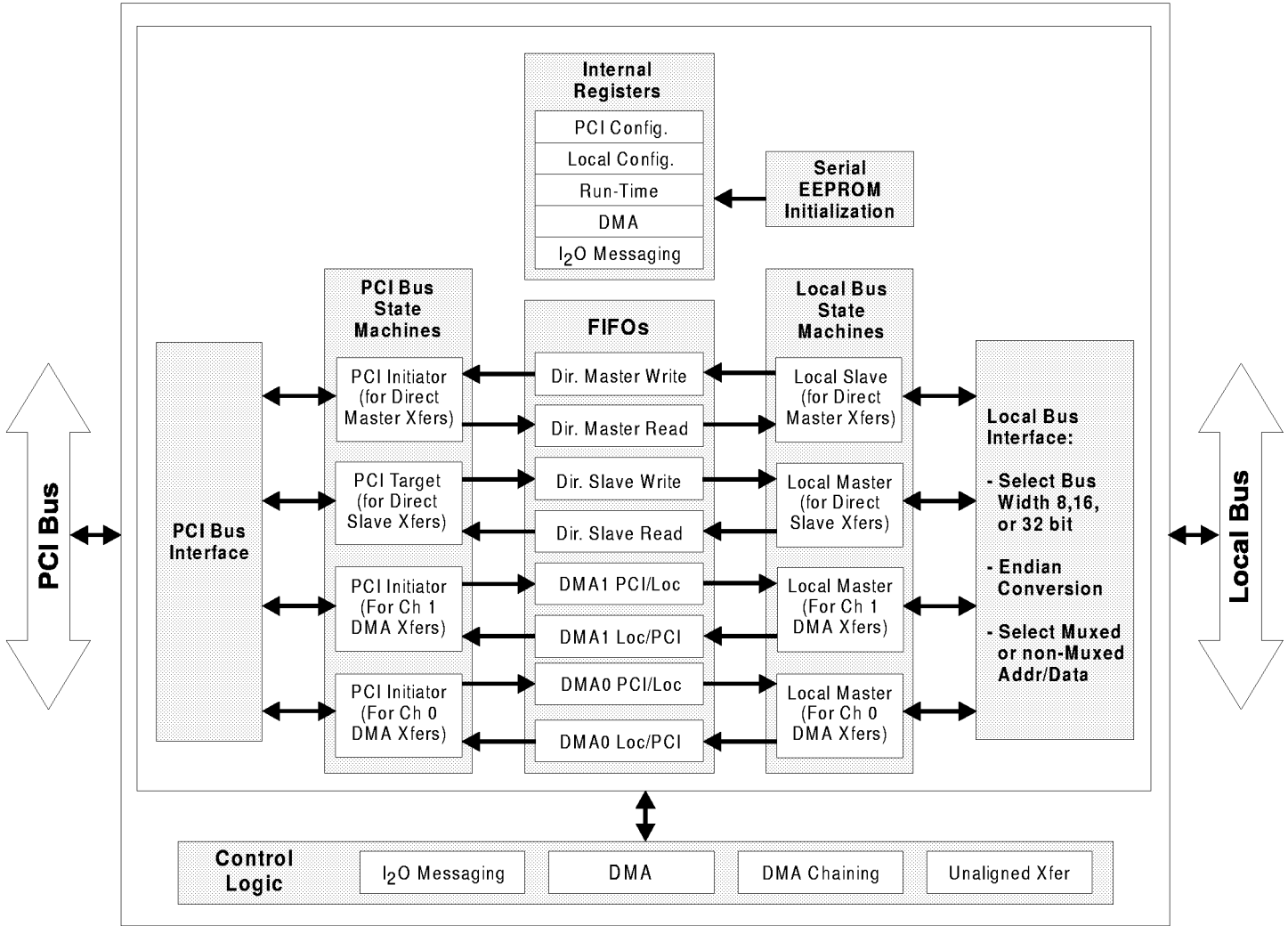
I₂O COMPATIBLE PCI BUS MASTER INTERFACE CHIP
FOR ADAPTERS AND EMBEDDED SYSTEMS

FEATURES

- PCI Specification 2.1 (v2.1) compliant Bus Master Interface chip for adapters and embedded systems
- I₂O Compatible Messaging Unit
- 3.3 or 5 volt PCI signaling, 5 volt core, low-power CMOS in a 208-pin PQFP
- Two independent DMA channels for Local Bus memory to and from PCI Host Bus Data transfers
- Eight programmable FIFOs for zero wait state burst operation
- PCI ↔ Local Data transfers up to 132 MB/sec
- Programmable Local Bus supports nonmultiplexed 32-bit address/data, multiplexed 32- or 16-bit, and Slave accesses of 32-, 16-, or 8-bit Local Bus devices
- Local Bus runs asynchronously to the PCI Bus
- Eight 32-bit Mailbox and two 32-bit Doorbell registers
- Performs Big Endian/Little Endian conversion
- Upward compatibility with the PCI 9060, PCI 9060ES, and PCI 9060SD



Typical Adapter Block Diagram



PCI 9080 Internal Block Diagram

1. GENERAL DESCRIPTION

1.1 Company and Product Background

PLX Technology, Inc., the world leader in PCI-to-Local Bus I/O accelerator chips, supports more than 500 OEM customers in a wide variety of PCI applications. Customer applications include PC workstations and servers, PCI add-in boards, embedded PCI communication systems such as routers and switches, and industrial PCI implementations such as CompactPCI, PMC, and Passive Backplane PCI.

PLX Technology, Inc., is an active participant in industry standard committees, including the PCI SIG[®], I₂O SIG[®], and PICMG[®], and maintains active developer technology and cross-marketing partnerships with industry leaders, such as Intel, IBM, Hewlett-Packard, Motorola, Integrated Systems, WindRiver and others.

Focused on providing complete solutions for PCI implementations, PLX provides design assistance to customers in the form of Reference Design and Software Development kits. Depending upon the application, these kits may include reference boards, API libraries, software debug tools, and sample device drivers with source, enabling customers to quickly bring new designs to production. New tools, application notes, FAQs, and information updates are constantly added to the website for the convenience of PLX customers. Our expertise and total solutions for the PCI interface allow customers to focus on adding value in their designs without worrying about the complexities of implementing PCI, I₂O, and CompactPCI.

1.2 PCI 9080 Applications

1.2.1 PCI Adapter Cards

Major PCI adapter card applications for the PCI 9080 include high performance communications, networking, disk control, multimedia, and video adapters. The PCI 9080 moves data between the host PCI Bus and adapter Local Bus in several ways. First, the local CPU or host processor may program the DMA controller of the PCI 9080 to move data between the adapter memory and host PCI Bus. Second, the PCI 9080 can perform Direct Master Transfers, whereby a local CPU or controller accesses the PCI Bus directly through a PCI Master transfer. The PCI 9080 also supports Slave transfers in which another PCI device is the Master. Finally, the PCI 9080 contains a complete messaging unit with mailbox registers, doorbell registers, and queue

management pointers that can be used for message passing under the I₂O protocol or a custom protocol.

1.2.2 Embedded Systems

Another application for the PCI 9080 is in embedded systems, such as network hubs and routers, printer engines, and industrial equipment. In this configuration, all four of the above-mentioned Data Transfer modes are used. In addition, the PCI 9080 supports Type 0 and Type 1 PCI Configuration cycles, which allows embedded CPU to act as the embedded system host and to configure other PCI devices in the system.

1.3 Major Features

PCI 2.1 Compliant. The PCI 9080 is compliant with all aspects of PCI Specification v2.1.

I₂O Messaging Unit. The PCI 9080 incorporates an I₂O messaging unit. This enables the adapter or embedded system to communicate with other I₂O-supported devices. The I₂O messaging unit is fully compatible with the PCI extension of the I₂O specification v1.5.

Dual Independent Programmable DMA Controllers with Programmable FIFOs. The PCI 9080 provides two independently programmable DMA controllers with programmable FIFOs for each channel. Each channel supports Non-chaining and Chaining DMA modes, Demand mode DMA, and End of Transfer (EOT) mode.

Direct Bus Master. The PCI 9080 supports Memory-Mapped bursts, Transfer accesses, and I/O-Mapped Single-Transfer accesses to the PCI Bus from the Local Bus Master. The PCI 9080 also supports PCI Bus Interlock (LOCK#) cycles. The Read and Write FIFOs enable high-performance bursting.

PCI Host Capability. In Direct Master mode, the PCI 9080 can generate Type 0 or Type 1 PCI Configuration cycles.

Direct Slave. The PCI 9080 supports Burst Memory-Mapped and single I/O-Mapped accesses to the Local Bus. The Read and Write FIFOs enable high-performance bursting.

Programmable Local Bus Modes. The PCI 9080 is a PCI Bus Master interface chip that connects a PCI Bus to one of three Local Bus types, selected through mode pins. The PCI 9080 may be connected to any Local Bus with a similar design with little or no glue logic. Table 1-1 lists the three modes.

Table 1-1. Programmable Local Bus Modes

Mode	Description
C	32-bit address/32-bit data, nonmultiplexed
J	32-bit address/32-bit data, multiplexed
S	32-bit address/16-bit data, multiplexed

Interrupt Generator. The PCI 9080 can generate PCI and Local interrupts from several sources.

Clock. The PCI 9080 Local Bus interface runs from a local TTL clock and generates the necessary internal clocks. This clock runs asynchronously to the PCI clock. There is a buffered PCI clock (BPCLKo) for the Local Bus to use. BPCLKo may be connected to LCLK.

3.3 Volt and 5 Volt Operation. The PCI 9080 core requires 5V Vcc. The PCI 9080 provides 3.3V or 5V signaling on the PCI Bus. The Local Bus operates at a 5V signaling level.

Serial EEPROM Interface. The PCI 9080 contains an optional serial EEPROM interface that can be used to load configuration information. This is useful for loading information unique to a particular adapter (such as Network ID or Vendor ID).

Mailbox registers. The PCI 9080 contains eight 32-bit mailbox registers that may be accessed from the PCI or Local Bus.

Doorbell registers. The PCI 9080 includes two 32-bit doorbell registers. One generates interrupts from the PCI Bus to Local Bus. The other generates interrupts from the Local Bus to the PCI Bus.

Unaligned DMA Transfer Support. The PCI 9080 can transfer data on any byte boundary.

Big/Little Endian Conversion. The PCI 9080 supports dynamic switching between Big Endian and Little Endian operations for Direct Slave, Direct Master, DMA, and the Internal register accesses on the Local Bus.

The PCI 9080 supports on-the-fly Endian conversion for Space 0, Space 1, and Expansion ROM space. The Local Bus can be Big/Little Endian by using the BIGEND# input pin or programmable internal register configuration. When BIGEND# is asserted, it overrides the internal register configuration.

Note: *The PCI Bus is always Little Endian.*

Read Ahead Mode. The PCI 9080 supports Read Ahead mode, where prefetched data can be read from the PCI 9080 internal FIFO instead of from the Local Bus. Address must be subsequent to previous address and 32-bit aligned (next address = current address + 4).

Programmable Bus Wait States. The PCI 9080 can be programmed to keep the PCI Bus by generating a wait state(s), thereby de-asserting TRDY#, if the Write FIFO becomes full. The PCI 9080 can also be programmed to keep the Local Bus. LHOLD is asserted if the Direct Slave Write FIFO becomes empty or the Direct Slave Read FIFO becomes full. The Local Bus is dropped in either case when the Local Bus Latency Timer is enabled and expires.

1.4 Compatibility of PCI 9080 with PCI 9060, PCI 9060ES, and PCI 9060SD

The PCI 9080 is upward compatible with the PCI 9060, PCI 9060ES and PCI 9060SD, except as noted in Table 1-2 and Section 4.1, "New Register Definitions Summary."

1.4.1 Pin Compatibility

When upgrading from the PCI 9060, 9060ES or 9060SD, observe the following new pin definitions listed in Table 1-2.

Table 1-2. Pin Compatibility

Pin #	PCI 9060/9060ES/9060SD		PCI 9080	
	Pin Name	Description	Pin Name	Description
170	CLKSEL	Serial EEPROM Clock Select	NC	—
175	EE1MC	Optional Serial EEPROM Clock Source	EESEL	Serial EEPROM Select 1=93CS46 (1K bit) 0=93CS56 (2K bit)

1.4.2 Register Compatibility

All registers implemented in the PCI 9060, PCI 9060ES, and PCI 9060SD are implemented in the PCI 9080. There are a limited number of new bit definitions and several new registers. Refer to Section 4.1, "New Register Definitions Summary."

1.5 Comparison of PCI 9060, PCI 9060ES, PCI 9060SD, and PCI 9080

Table 1-3. Comparison of the PCI 9060, PCI 9060ES, PCI 9060SD, and PCI 9080

Feature	PCI 9060	PCI 9060ES	PCI 9060SD	PCI 9080
Number of DMA Channel(s)	2	0	1	2
Local Address Spaces	2	2	3	3
Direct Master Mode	Yes	Yes	No	Yes
Mailbox Registers	Eight 32-bit	Four 32-bit	Four 32-bit	Eight 32-bit
Doorbell Registers	Two 32-bit	Two 8-bit	Two 8-bit	Two 32-bit
FIFOs	8	4	4	8
FIFO Depth—Direct Slave Write, Direct Master Write, DMA 0 Read and DMA 0 Write	8 Lwords (32 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)	32 Lwords (128 bytes)
FIFO Depth—Direct Slave Read, Direct Master Read, DMA 1 Read and DMA 1 Write	8 Lwords (32 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)	16 Lwords (64 bytes)
LLOCKo# Pin for Lock Cycles	No	Yes	Yes	Yes
WAITI# Pin for Wait State Generation	No	Yes	Yes	Yes
BPCLKo Pin; Buffered PCI Clock	No	Yes	Yes	Yes
DREQ# and DACK# Pins for Demand Mode DMA Support	Yes	No	Yes (Channel 1 only)	Yes
Register Addresses	—	Identical except 9060ES has no DMA registers and Tables 25, 26, and 43 were added	Identical, except 9060SD has one DMA register and Tables 4-29 and 4-30 were added	Identical except PCI 9080 has additional I ₂ O related registers and 30h, 34h, 40h, and 44h were remapped
Pin Out <i>Note: The PCI 9080 includes all changes made for PCI 9060, PCI 9060ES, and PCI 9060SD.</i>	—	Signals deleted: DREQ0# (pin 29) DACK0# (pin 30) Input signals added: WAITI# (pin 6) BIGEND# (pin 48) Output signals added: BPCLKo (pin 168) LLOCKo# (pin 7)	Signals deleted: BREQ (pin 21) DMPAF# (pin 8) DREQ0# (pin 29) DACK0# (pin 30) BTERMo# (pin 28) Input signals added: WAITI# (pin 6) BIGEND# (pin 48) EOTO# (pin 164 in C mode, Pin 5 in J and S modes) Output signals added: BPCLKo (pin 168) LLOCKo# (pin 7)	Input signal added: EOT1# (pin 163) Signal changed: EESEL (pin 175)
Big/Little Endian Conversion	No	Yes	Yes	Yes
PCI Specification v2.1 Deferred Reads	No	Yes	Yes	Yes
Programmable Prefetch Counter	No	Yes	Yes	Yes
Write and Invalidate Cycle	No	Yes	Yes	Yes
Additional Device and Vendor ID Register	No	Yes	Yes	Yes
I ₂ O Messaging Unit	No	No	No	Yes
3.3V PCI Bus Signaling	No	No	No	Yes

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2. BUS OPERATION

2.1 PCI Bus Cycles

The PCI 9080 is compliant with PCI Specification v2.1. Refer to the PCI 2.1 spec for any specific features of the PCI Bus.

2.1.1 PCI Target Command Codes

As a Target, the PCI 9080 allows access to its Internal registers and the Local Bus, using the commands listed in Table 2-1.

Table 2-1. PCI Target Command Codes

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)
Configuration Read	1010 (Ah)
Configuration Write	1011 (Bh)

All Read or Write accesses to the PCI 9080 can be Byte, Word, or Longword (Lword) accesses. All memory commands are aliased to the basic memory commands. All I/O accesses to the PCI 9080 are decoded to an Lword boundary. The byte enables are used to determine which bytes are read or written. An I/O access with illegal byte enable combinations is terminated with a Target Abort.

2.1.2 PCI Master Command Codes

The PCI 9080 can access the PCI Bus to perform DMA transfers or Direct Master Local-to-PCI Bus transfers. During the Direct Master or DMA transfer, the command code assigned to the PCI 9080 Internal register location, (CNTRL[15:0], is used as the PCI command code. Table 2-2 through Table 2-5 lists the various PCI Master Command codes.

Notes: Programmable Internal registers determine PCI command codes when the PCI 9080 is Master.

DMA cannot perform I/O or Configuration accesses.

2.1.2.1 DMA Master Command Codes

DMA controllers of the PCI 9080 can generate the Memory cycles listed in Table 2-2.

Table 2-2. DMA Master Command Codes

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)
Memory Write and Invalidate	1111 (Fh)

2.1.2.2 Direct Local-to-PCI Command Codes

For direct Local-to-PCI Bus accesses, the PCI 9080 generates the cycles listed in Table 2-3 through Table 2-5.

Table 2-3. Local-to-PCI Memory Access

Command Type	Code (C/BE[3:0]#)
Memory Read	0110 (6h)
Memory Write	0111 (7h)
Memory Read Multiple	1100 (Ch)
Memory Read Line	1110 (Eh)

Table 2-4. Local-to-PCI I/O Access

Command Type	Code (C/BE[3:0]#)
I/O Read	0010 (2h)
I/O Write	0011 (3h)

Table 2-5. Local-to-PCI Configuration Access

Command Type	Code (C/BE[3:0]#)
Configuration Memory Read	1010 (Ah)
Configuration Memory Write	1011 (Bh)

2.1.3 PCI Arbitration

The PCI 9080 asserts output REQ# to request the PCI Bus. The PCI 9080 can be programmed using MARBR[23] to de-assert REQ# when it asserts FRAME# during a Bus Master cycle, or to keep REQ# asserted for the entire Bus Master cycle. The PCI 9080 always de-asserts REQ# for a minimum of two PCI clocks between Bus Master ownership that includes a Target disconnect.

The Direct Master Write Delay bits (DMPBAM[15:14]) can be programmed to delay assertion of the PCI 9080 PCI REQ# signal during a Direct Master Write cycle.

This register can be programmed to wait 0, 4, 8, or 16 PCI Bus clocks after the PCI 9080 has received its first Write data from the Local Master and is ready to begin the PCI Write transaction. This feature is useful in applications where the Local Master is bursting and the Local Bus clock is slower than the PCI Bus clock. This allows Write data to accumulate in the Direct Master Write FIFO of the PCI 9080, which provides for better utilization of the PCI Bus.

2.2 LOCAL BUS CYCLES

The PCI 9080 connects a PCI Host bus to several Local processor bus types, as listed in Table 2-6. It operates in one of three modes, selected through mode pins 9 and 10, corresponding to three bus types—C, J, and S.

Table 2-6. Local Processor Bus Types

Bit 9	Bit 10	Mode	Bus Type
0	0	C	32-bit nonmultiplexed
0	1	J	32-bit multiplexed
1	0	S	16-bit multiplexed
1	1	Reserved	—

2.2.1 Local Bus Arbitration

When the PCI 9080 owns the Local Bus, both its L_HOLD output and L_HOLD_A input are asserted. When the PCI 9080 samples that BREQ is asserted during a DMA transfer or Direct Slave Write transfer, it gives up the Local Bus within two L_word transfers by de-asserting L_HOLD and floating its Local Bus outputs if:

- BREQ is gated or disabled; or
- Gating is enabled and the Local Bus Latency Timer expires

The Local Arbiter can now grant the Local Bus to another Local Master. After the PCI 9080 samples that its L_HOLD_A is de-asserted and its Local Pause Timer is zero, it re-asserts L_HOLD to request the Local Bus. When the PCI 9080 receives L_HOLD_A, it drives the bus and continues from where it left off.

2.2.2 Local Bus Direct Master

Local Bus cycles can be Continuous Single or Burst cycles (programmable by way of the PCI 9080 Internal registers). As a Local Bus Target, the PCI 9080 allows access to its Internal registers and the PCI Bus.

In C and J modes, Local Bus Direct Master accesses to the PCI 9080 must be for a 32-bit nonpipelined bus.

In S mode, Local Bus Direct Master accesses to the PCI 9080 must be for a 16-bit nonpipelined bus.

2.2.3 Local Bus Direct Slave

PCI Bus Master Read/Write to Local Bus (the PCI 9080 is a PCI Bus Target and Local Bus Master).

2.2.3.1 Ready/Wait State Control

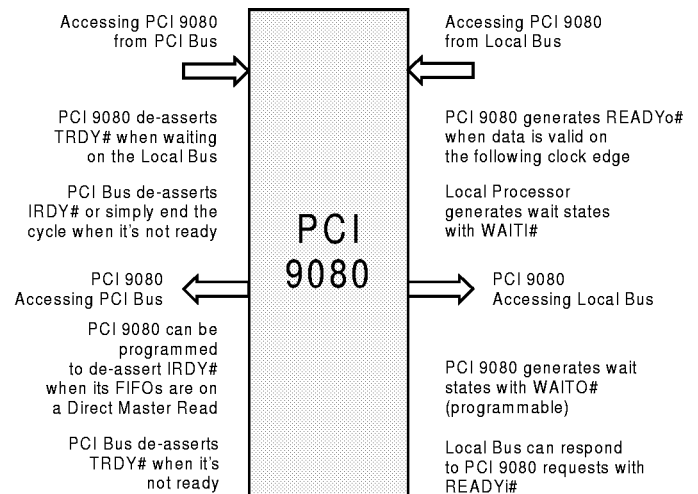


Figure 2-1. Wait States

Note: The figure represents a sequence of Bus cycles.

If READYi# input is disabled, the external READYi# input has no effect on wait states for a local access. Wait states between Data cycles are generated internally by a wait state counter. Wait state counter is initialized with its Configuration register value at the start of each data access.

If READYi# is enabled, READYi# has no effect until the wait state counter is 0. READYi# then controls the number of additional wait states.

BTERM# input is not sampled until the wait state counter is 0. BTERM# overrides READYi# when BTERM# is asserted.

2.2.3.1.1 Wait State—Local Bus

With Direct Master mode and accessing the PCI 9080 registers (PCI 9080 local as Slave):

- PCI 9080 generates wait states with READYo#
- Local processor generates wait states with WAITI#

With Direct Slave and DMA modes (PCI 9080 Local Bus as Master):

- The PCI 9080 generates wait states with WAITO#
- Local processor generates wait states with READYi#
- Use LBRD0[21:18, 5:2], DMAMODE0[5:2], and DMAMODE1[5:2] to program the number of wait states

2.2.3.1.2 Wait State—PCI Bus

When the wait state occurs on the PCI Bus, Master throttles IRDY# and Slave throttles TRDY#.

2.2.3.2 Burst Mode and Continuous Burst Mode (Bterm “Burst Terminate” Mode)

Table 2-7. Burst and Bterm on the Local Bus

Mode	Burst	Bterm	Result
Single Cycle	0	0	One ADS# per data (default)
Single Cycle	0	1	Still one ADS# per data
Burst-4	1	0	One ADS# per four data (use this mode for i960)
Burst Forever	1	1	One ADS# per BTERM#

On the Local Bus, BLAST# and BTERM# perform the following:

- If burst is enabled (LBRD0[26,24] for non-DMA, DMAMODE0[8] and DMAMODE1[8] for DMA), but Bterm mode is disabled (LBRD0[7], DMAMODE0[7] and DMAMODE1[7]), then the PCI 9080 bursts four Lwords. BLAST# is generated at the fourth Lword (LA[3:2]=11), new ADS# at the first Lword (LA[3:2]=00) of the next burst.
- If BTERM# sampling is enabled and BTERM# is low, the PCI 9080 forces a new ADS#, but does not generate a new BLAST# signal.
- BTERM# input is valid only when the PCI 9080 is the Master of the Local Bus (Direct Slave or DMA modes).
- BTERM# is generated by external logic. It is input to the PCI 9080 (and i960) and used to tell the PCI 9080 (and i960) to break up a Burst cycle.
- BTERM# is used, *for example*, to signal that a Memory access is crossing the page boundary.

On the PCI Bus, burst is always enabled.

Notes: If Bterm is disabled, the PCI 9080 performs the following:

- 32-bit Local Bus—Burst up to four Lwords
- 16-bit Local Bus—Burst up to two Lwords
- 8-bit Local Bus—Burst up to one Lword

In every case, it performs four transactions.

In the following sections, Bterm refers to the PCI 9080 Internal register bit. BTERM# refers to the PCI 9080 external signal.

2.2.3.2.1 Burst Mode

If bursting is enabled and BTERM# input is not enabled, bursting can start on any boundary and continue up to an address boundary, as described in Table 2-8. After the data at the boundary is transferred, the PCI 9080 generates a new Address cycle (ADS#).

Table 2-8. Burst Mode

Bus Mode	Burst
C, J	32-bit bus—Four Lwords or up to a quad Lword boundary (LA3, LA2 = 11)
C, J	16-bit bus—Four words or up to a quad word boundary (LA2, LA1 = 11)
C, J	8-bit bus—Four bytes or up to a quad byte boundary (LA1, LA0 = 11)
S	16-bit bus—Eight words or up to a quad Lword boundary (LA3, LA2 = 11)

2.2.3.2.2 Continuous Burst Mode (Bterm “Burst Terminate” Mode)

Bterm mode enables the PCI 9080 to perform long bursts to devices that can accept longer than four Lword bursts. The PCI 9080 generates one Address cycle and continues to burst data. If a device requires a new Address cycle after a certain address boundary, it can assert BTERM# input to cause the PCI 9080 to generate a new Address cycle. BTERM# input acknowledges the current Data transfer and requests that a new Address cycle be generated (ADS#). This address is used for the next Data transfer. If Bterm mode is enabled, the PCI 9080 asserts BLAST# only if its FIFOs become full or empty, or if a transfer is complete.

Note: If BTERM# is asserted, BLAST# does not assert until the previously described conditions are met.

2.2.3.2.3 Partial Lword Accesses

Lword accesses in which not all byte enables are asserted are broken into Single Address and Data cycles, as listed in Table 2-9.

Table 2-9. Partial Lword Accesses

Register Value for LBRD0		Result (Number of Transfers)
Burst Enable	Bterm Enable	
0	0	Single Cycle (Default)
0	1	Single Cycle
1	0	Burst four Lwords at a time
1	1	Continuous Burst Mode

2.2.3.3 Recovery States

In J and S modes, the PCI 9080 inserts one recovery state between the last Data transfer and next Address cycle.

The PCI 9080 does not support the 80960J feature of using READYi# input to add recovery states. No additional recovery states are added if READYi# input remains asserted during the last Data cycle.

2.2.3.4 Local Bus Read Accesses

For all Single Cycle Local Bus Read accesses, the PCI 9080 reads only bytes corresponding to byte enables requested by the PCI initiator. For all Burst Cycle Bus Read accesses, the PCI 9080 reads only Lwords.

2.2.3.5 Local Bus Write Accesses

For Local Bus writes, only the bytes specified by a PCI Bus Master or the PCI 9080 DMA controller are written. Access to an 8- or 16-bit bus results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each transfer, the byte enables are encoded as in the 80960C to provide Local Address bits LA[1:0].

2.2.3.6 Direct Slave Write Accesses—8- and 16-Bit Buses

A Direct PCI access to an 8- or 16-bit bus results in the PCI Bus Lword being broken into multiple Local Bus transfers. For each transfer, the byte enables are encoded as in the 80960C to provide Local Address bits LA[1:0].

2.2.3.7 Local Bus Data Parity

There is one data parity pin for each byte lane of the PCI 9080 data bus (DP[3:0]). Even data parity is generated for each lane during Local Bus reads from the PCI 9080 and during PCI 9080 Master writes to the Local Bus.

Even data parity is checked during Local Bus writes to the PCI 9080 and during PCI 9080 reads from the Local Bus. Parity is checked for each byte lane with an asserted byte enable. PCHK# is asserted in the Clock cycle following the data being checked if a parity error is detected.

Generation or use of Local Bus data parity is optional. Signals on data parity pins do not affect operation of the PCI 9080. PCI Bus parity checking and generation is independent of Local Bus parity checking and generation.

2.2.3.8 Local Bus Big/Little Endian

PCI Bus is a Little Endian bus (*that is*, data is Lword aligned to the lowermost byte lane). Byte 0 (address 0) appears in AD[7:0], Byte 1 appears in AD[15:8], Byte 2 appears in AD[23:16] and Byte 3 appears in AD[31:24].

The PCI 9080 Local Bus can be programmed to operate in Big or Little Endian mode, as listed in Table 2-10.

Table 2-10. Big/Little Endian Program Mode

BIGEND# Pin	Register 1=Big, 0=Little	Endian
0	0	Big
0	1	Big
1	0	Little
1	1	Big

For Configuration cycles, refer to BIGEND[0]. For Direct Master, Memory, and I/O cycles, refer to BIGEND[1]. For Direct Slave cycles, refer to BIGEND[2], Space 0, and BIGEND[3], Expansion ROM.

In Big Endian mode, the PCI 9080 transposes data byte lanes. Data is transferred as listed in Table 2-11 through Table 2-15.

2.2.3.8.1 32-Bit Local Bus—Big Endian Mode

Data is Lword aligned to the uppermost byte lane. Byte lanes and burst orders are listed in Table 2-11 and illustrated in Figure 2-2.

Table 2-11. Upper Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

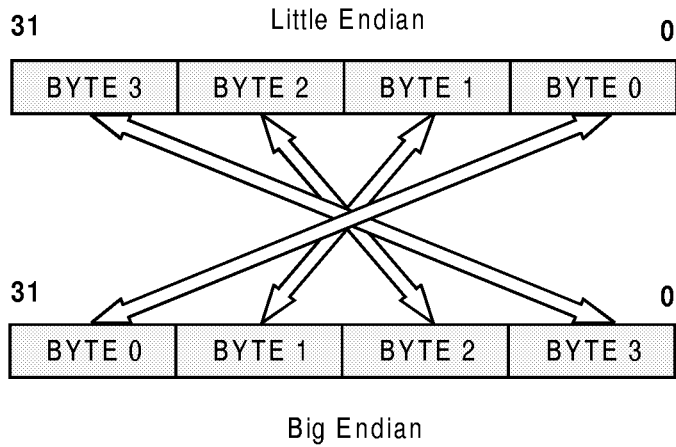


Figure 2-2. Big/Little Endian—32-Bit Local Bus

2.2.3.8.2 16-Bit Local Bus—Big Endian Mode

For a 16-bit Local Bus, the PCI9080 can be programmed to use the upper or lower word lane. Byte lanes and burst order are listed in Table 2-12 and Table 2-13 and illustrated in Figure 2-3.

Table 2-12. Upper Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [31:24]
	Byte 1 appears on Local Data [23:16]
Second Transfer	Byte 2 appears on Local Data [31:24]
	Byte 3 appears on Local Data [23:16]

Table 2-13. Lower Word Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [15:8]
	Byte 1 appears on Local Data [7:0]
Second Transfer	Byte 2 appears on Local Data [15:8]
	Byte 3 appears on Local Data [7:0]

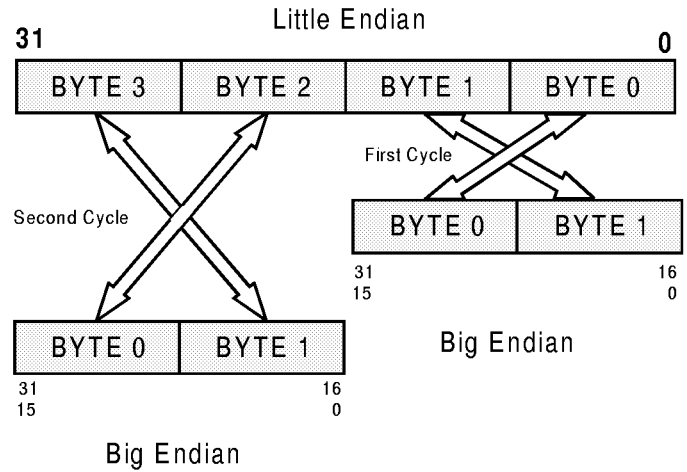


Figure 2-3. Big/Little Endian—16-Bit Local Bus

2.2.3.8.3 8-Bit Local Bus—Big Endian Mode

For an 8-bit Local Bus, the PCI9080 can be programmed to use the upper or lower byte lane. Byte lanes and burst order are listed in Table 2-14 and Table 2-15 and illustrated in Figure 2-4.

Table 2-14. Upper Byte Lane Transfer

Burst Order	Byte Lane
First transfer	Byte 0 appears on Local Data [31:24]
Second transfer	Byte 1 appears on Local Data [31:24]
Third transfer	Byte 2 appears on Local Data [31:24]
Fourth transfer	Byte 3 appears on Local Data [31:24]

Table 2-15. Lower Byte Lane Transfer

Burst Order	Byte Lane
First Transfer	Byte 0 appears on Local Data [7:0]
Second Transfer	Byte 1 appears on Local Data [7:0]
Third Transfer	Byte 2 appears on Local Data [7:0]
Fourth Transfer	Byte 3 appears on Local Data [7:0]

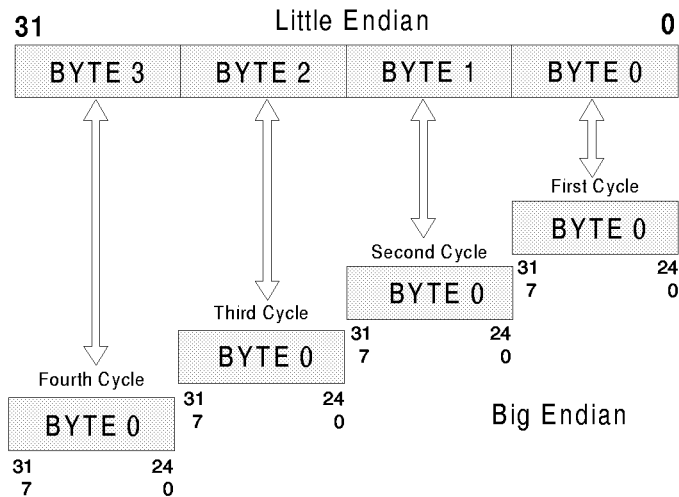


Figure 2-4. Big/Little Endian—8-Bit Local Bus

For each of the following transfer types, the PCI 9080 Local Bus can be independently programmed to operate in Little Endian or Big Endian mode:

- Local Bus accesses to the PCI 9080 Configuration registers
- Direct Slave PCI accesses to Local Address Space 0
- Direct Slave PCI accesses to Local Address Space 1
- Direct Slave PCI accesses to Expansion ROM
- DMA Channel 0 accesses to the Local Bus
- DMA Channel 1 accesses to the Local Bus
- Direct Master accesses to PCI Bus

For Local Bus Configuration accesses, an input pin can be used to dynamically change the Endian mode.

Notes: The PCI Bus is always Little Endian mode.

Only byte lanes are swapped, not individual bits.

3. FUNCTIONAL DESCRIPTION

Functional operation described can be changed or modified, depending on the register configuration.

3.1 RESET

3.1.1 PCI Bus Input RST#

PCI Bus RST# input pin is a PCI Host reset. It causes all PCI Bus outputs to float, resets the entire PCI 9080 and causes the local reset output, LRESETo#, to be asserted. If you have a PCI Host (PCICR[2:0]), Master Enable, Memory Space, I/O Space is programmed by the host after initialization is complete (CNTRL[31]=1). (Refer to Figure 3-1.)

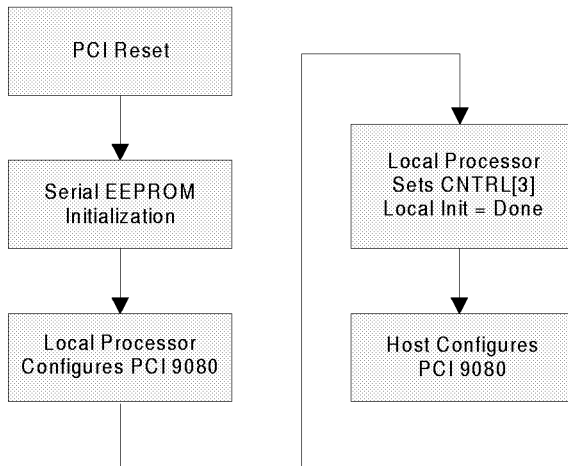


Figure 3-1. Reset and Initialization Process

3.1.2 Software Reset LRESETo#

When asserted, the LRESETo# Software Reset CNTRL[30] resets the PCI 9080 Local Configuration and Local DMA registers. However, it does not reset the PCI Configuration and Shared Runtime registers. When the bit is set, the PCI 9080 responds to PCI accesses, but not to local accesses. The PCI 9080 remains in this condition until PCI Host clears the bit. The serial EEPROM is reloaded if CNTRL[29] is set.

3.1.3 Local Bus Input LRESETi#

When asserted, the LRESETi# input resets the Local Bus portion of the PCI 9080, clears all local configuration and DMA registers and causes LRESETo# output to be asserted.

3.1.4 Local Bus Output LRESETo#

LRESETo# is asserted when PCI Bus RST# input is asserted, the LRESETi# input is asserted, or the Software Reset bit in the Init Control register is set to 1.

3.1.5 Software Reset

A host on the PCI Bus can set the software Software Reset bit in the Init Control register to reset the PCI 9080 and assert the LRESETo# output. All Local Configuration and DMA registers reset. PCI Configuration registers do not reset. When the Software Reset bit is set, the PCI 9080 responds to PCI accesses, but not to Local accesses. The PCI 9080 remains in this reset condition until the PCI Host clears the bit.

Note: The Local Bus cannot clear this reset bit because the Local Bus is in a reset state.

3.2 PCI 9080 Initialization

The PCI 9080 Configuration registers can be programmed by an optional serial EEPROM and/or by a Local processor, as listed in Table 3-1. The serial EEPROM can be reloaded by setting CNTRL[29].

In general, the PCI 9080 retries all PCI cycles until the Local Init Done bit is set or until NB# is low.

Note: The PCI Host processor can also access the internal Configuration register after power-on.

Table 3-1. NB# and Serial EEPROM Guidelines

NB#	Serial EEPROM	System Boot Condition
Low	No	Boot with PCI 9080 default values.
	Programmed	Boot with serial EEPROM values.
	Blank	Not recommended (uses default values).
High	No	Local processor programs the PCI 9080 registers, then sets Local Init Status (CNTRL[31] = done). <i>Note:</i> Some systems hang if Direct Slave reads and writes take too long (during initialization, the PCI Host also performs Direct Slave accesses). Value of PCI Target Retry Delay Clocks (LBRD0[31:28]) may resolve this problem.
	Programmed	Load serial EEPROM, but Local processor can reprogram the PCI 9080.
	Blank	Load serial EEPROM (default values), but Local processor can reprogram the PCI 9080. The system can boot. <i>Note:</i> The serial EEPROM can be programmed through the PCI 9080 after system boots in this condition.

3.2.1 Serial EEPROM Initialization

During serial EEPROM initialization, the PCI 9080 response to PCI Target accesses is Retry. During serial EEPROM initialization, the PCI 9080 response to a Local processor is to hold off READYo#.

3.2.2 Local Initialization

The PCI 9080 issues a Retry to all PCI accesses until the Local Init Done bit in the Init Control register is set. The Init Done bit is programmable through Local Bus Configuration accesses. If this bit is not going to be set by a Local processor, then NB# input should be tied low. Holding NB# input low externally forces the Local Init Done bit to 1.

The PCI 9080 default values are used if a serial EEPROM is not present and Local Init Status bit is set to 1 by holding the NB# input low or set by the Local processor.

3.3 SERIAL EEPROM

After reset, the PCI 9080 attempts to read the serial EEPROM to determine its presence. An active low start bit indicates the serial EEPROM is present (the PCI 9080 supports 93CS46 (1K) or 93CS56 (2K), selectable by way of the ESEL pin). (Refer to manufacturer's data sheet for particular serial EEPROM being used.) The first word is then checked to verify the serial EEPROM is programmed. If the first word (16 bit) is all ones, a blank serial EEPROM the PCI 9080 uses default values instead.

The 5V serial EEPROM clock (EESK, pin 173) is derived from the PCI clock. The PCI 9080 generates the serial EEPROM clock by internally dividing the PCI clock by 32.

The serial EEPROM can be read or programmed from the PCI or Local Bus. Bits [27:24] of the Serial EEPROM Control register (CNTRL[27:24]) control the PCI 9080 pins that enable the reading or writing of serial EEPROM data bits. (Refer to manufacturer's data sheet for particular serial EEPROM being used.)

The PCI 9080 has three serial EEPROM load options:

- **Short Load Mode**—SHORT# input pin is pulled down and the PCI 9080 loads five Lwords from the serial EEPROM
- **Long Load Mode**—SHORT# input pin is pulled up, bit 25 of the Local Bus Region Descriptor Register is set to 0, and the PCI 9080 loads 17 Lwords from the serial EEPROM (LBRD0[25])
- **Extra Long Load Mode**—SHORT# input pin is pulled up, bit 25 of the Local Bus Region Descriptor Register is set to 1 during Long Load from the serial EEPROM, and the PCI 9080 loads 21 Lwords from the serial EEPROM (LBRD0[25])

3.3.1 Short Serial EEPROM Load

The registers listed in Table 3-2 are loaded from serial EEPROM after reset is de-asserted if SHORT# pin is low. The serial EEPROM is organized in 16-bit words. The PCI 9080 first loads MSW (Most Significant Word; bits [31:16]), starting from the most significant bit [31]. The PCI 9080 then loads LSW (Least Significant Word; bits [15:0]), starting again from the most significant bit [15]. Therefore, the PCI 9080 loads Device ID, Vendor ID, class code, and so forth. The five 32-bit words are stored sequentially in the serial EEPROM.

Table 3-2. Short Serial EEPROM Load Registers

Serial EEPROM Offset	Description	Sample Serial EEPROM Value
0	Device ID	9080
2	Vendor ID	10B5
4	Class Code	0680
6	Class Code, Revision	0002
8	Maximum Latency, Minimum Grant	0000
A	Interrupt Pin, Interrupt Line Routing	0100
C	MSW of Mailbox 0 (User Defined)	xxxx
E	LSW of Mailbox 0 (User Defined)	xxxx
10	MSW of Mailbox 1 (User Defined)	xxxx
12	LSW of Mailbox 1 (User Defined)	xxxx

3.3.2 Long Serial EEPROM Load

The registers listed in LBRD0 are loaded from serial EEPROM after reset is de-asserted if SHORT# pin is high. The serial EEPROM is organized in 16-bit words. The PCI 9080 first loads MSW (Most Significant Word; bits [31:16]), starting from the most significant bit [31]. The PCI 9080 then loads LSW (Least Significant Word; bits [15:0]), starting again from the most significant bit [15]. Therefore, the PCI 9080 loads Device ID, Vendor ID, class code, and so forth.

The serial EEPROM value can be entered into a DATA I/O programmer in the order shown below. The values shown are examples and must be modified for each particular application. The 34 16-bit words listed in the table are stored sequentially in the serial EEPROM.

Table 3-3. Long Serial EEPROM Load Registers

Serial EEPROM Offset	Description
0	Device ID
2	Vendor ID
4	Class Code
6	Class Code, Revision
8	Maximum Latency, Minimum Grant
A	Interrupt Pin, Interrupt Line Routing
C	MSW of Mailbox 0 (User Defined)
E	LSW of Mailbox 0 (User Defined)
10	MSW of Mailbox 1 (User Defined)
12	LSW of Mailbox 1 (User Defined)
14	MSW of Range for PCI-to-Local Address Space 0
16	LSW of Range for PCI-to-Local Address Space 0
18	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 0
1A	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 0
1C	MSW of Local Arbitration Register
1E	LSW of Local Arbitration Register
20	MSW of Local Bus Big/Little Endian Descriptor Register
22	LSW of Local Bus Big/Little Endian Descriptor Register
24	MSW of Range for PCI-to-Local Expansion ROM
26	LSW of Range for PCI-to-Local Expansion ROM
28	MSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM
2A	LSW of Local Base Address (Remap) for PCI-to-Local Expansion ROM
2C	MSW of Bus Region Descriptors for PCI-to-Local Accesses
2E	LSW of Bus Region Descriptors for PCI-to-Local Accesses
30	MSW of range for Direct Master to PCI
32	LSW of range for Direct Master to PCI
34	MSW of Local Base Address for Direct Master to PCI Memory
36	LSW of Local Base Address for Direct Master to PCI Memory
38	MSW of Local Bus Address for Direct Master to PCI IO/CFG
3A	LSW of Local Bus Address for Direct Master to PCI IO/CFG
3C	MSW of PCI Base Address (Remap) for Direct Master to PCI
3E	LSW of PCI Base Address (Remap) for Direct Master to PCI
40	MSW of PCI Configuration Address Register for Direct Master to PCI IO/CFG
42	LSW of PCI Configuration Address Register for Direct Master to PCI IO/CFG

3.3.3 Extra Long Serial EEPROM Load

An Extra Long Load mode is provided in the PCI 9080 (LBRDO) to load an additional five Lwords from the serial EEPROM. If bit 25 is set to 1 in the Local Bus Region Descriptor register (LBRDO), the following five Lword registers are loaded in addition to normal Long Load process (refer to Section 3.3.2, "Long Serial EEPROM Load"). Bit 25 must be set to 1 during the Long Load Process. (Refer to Table 3-4.)

Table 3-4. Extra Long Serial EEPROM Load Registers

Serial EEPROM Offset	Description
44	Subsystem ID
46	Subsystem Vendor ID
48	MSW of Range for PCI-to-Local Address Space 1 (1 MB)
4A	LSW of Range for PCI-to-Local Address Space 1 (1 MB)
4C	MSW of Local Base Address (Remap) for PCI-to-Local Address Space 1
4E	LSW of Local Base Address (Remap) for PCI-to-Local Address Space 1
50	MSW of Bus Region Descriptors (Space 1) for PCI-to-Local accesses
52	LSW of Bus Region Descriptors (Space 1) for PCI-to-Local accesses
54	MSW of PCI Base Address for Local Expansion ROM
56	LSW of PCI Base Address for Local Expansion ROM

3.3.4 Recommended Serial EEPROMs

A 1K-bit (National NM93CS46 or compatible) or 2K-bit (National NM93CS56 or compatible) device can be used. Table 3-5 lists the recommended serial EEPROM loads. Refer also to Table 5-2 in Section 5, "Pin Description."

Table 3-5. Recommended Serial EEPROM Loads

Load	Unused Bytes for CS46 (1K bit)	Unused Bytes for CS56 (2K bit)
Short	108	236
Long	60	188
Extra Long	40	168

Note: The PCI 9080 does not support serial EEPROMs that do not support sequential read and write (such as the NM93C46 or NM93C56).

3.3.5 Programming the Serial EEPROM

The serial EEPROM can be written or read, using bits [28:24] of the Serial EEPROM Control register (CNTRL[28:24]).

3.4 Internal Register Access

The PCI 9080 chip provides several Internal registers, allowing for maximum flexibility in bus interface design and performance. The register types are accessible from both the PCI and Local Buses, including the following:

- PCI Configuration registers
- Local Configuration registers
- Mailbox registers
- Doorbell registers
- DMA registers
- Messaging queue registers (I₂O)

Figure 3-2 illustrates how these registers are accessed.

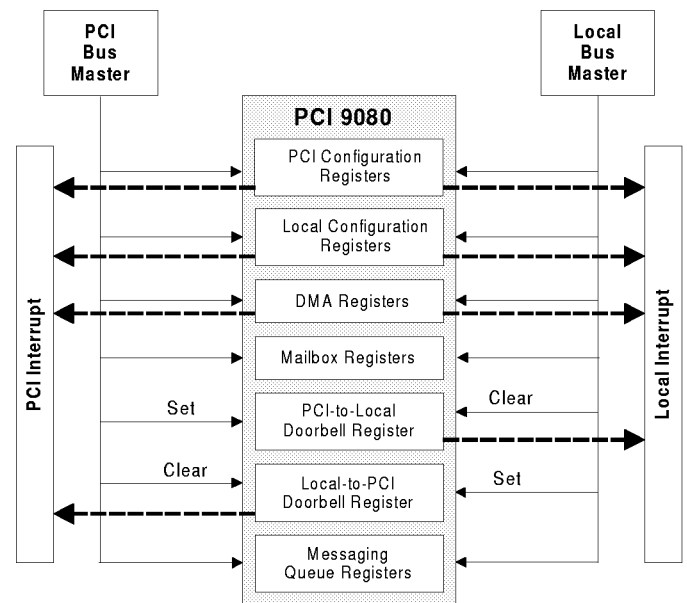


Figure 3-2. PCI 9080 Internal Register Access

3.4.1 PCI Bus Access to Internal Registers

The PCI 9080 PCI Configuration registers can be accessed from the PCI Bus with a Type 0 Configuration cycle.

The PCI 9080 Internal registers can be accessed by a Memory cycle, with the PCI Bus address that matches

the base address specified in the PCI Base Address 0 for Memory-Mapped Configuration register of the PCI 9080. They can also be accessed by an I/O cycle, with the PCI Bus address matching the base address specified in the PCI Base Address 1 for the I/O-Mapped Configuration register of the PCI 9080.

All PCI Read or Write accesses to the PCI 9080 registers can be Byte, Word, or Lword accesses. All PCI Memory accesses to the PCI 9080 registers can be Burst or Non-burst. The PCI 9080 responds with a PCI Disconnect for all Burst I/O accesses to the PCI 9080 registers.

3.4.2 Local Bus Access to Internal Registers

The Local processor can access all the Internal registers of the PCI 9080 through either internal or external address decode logic. The PCI 9080 provides an Address Decode Mode Pin (ADMODE) that selects whether the internal address decode logic is used or the designer supplies an external chip select from an external address decoder. Figure 3-3 illustrates how dual address decode logic works.

If the Address Decode Mode pin is set to 1, internal PCI 9080 address decode logic is enabled. In this mode, the PCI 9080 Internal registers are selected when Local Address bits LA[31:29] match input address select pins S[2:0]. If the Address Decode Mode pin is set to 0, the PCI 9080 responds to Local Bus access when S0 is asserted low through external chip select logic.

Notes: S0 must be decoded while ADS# is low.

If ADMODE is 1 LA[31:29], specify 512 MB of Local Memory space allocated for accessing Internal registers.

All Local Read or Write accesses to the PCI 9080 registers can be Byte, Word, or Lword accesses. All Local accesses to the PCI 9080 registers can be Burst or Non-burst.

For C and J modes, accesses must be for a 32-bit nonpipelined bus. The PCI 9080 READY# indicates a Data transfer is complete.

For S mode, accesses must be for a 16-bit nonpipelined bus. The PCI 9080 READY# indicates a Data transfer is complete.

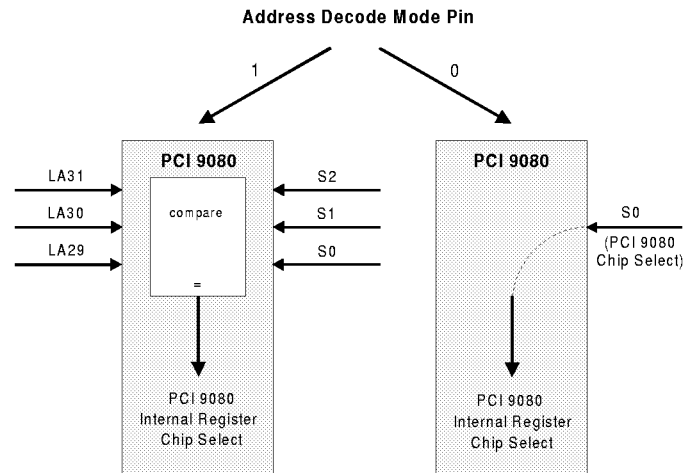


Figure 3-3. Dual Address Decode Mode

3.5 Response to Full and Empty FIFOs

Table 3-6 lists the response of the PCI 9080 to full and empty FIFOs.

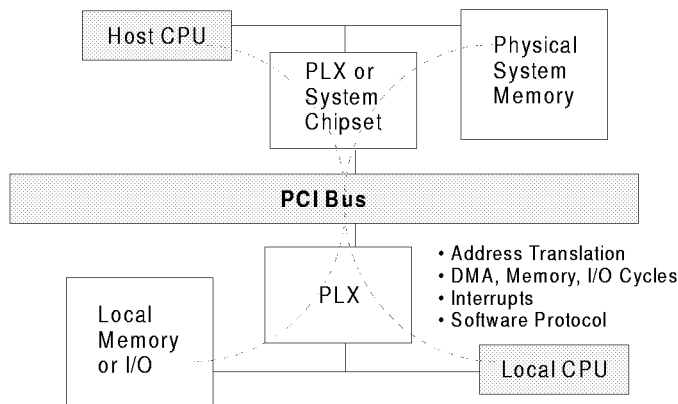
Table 3-6. Response to Full and Empty FIFOs

Mode	Direction	FIFO	PCI Bus	Local Bus
Direct Master Write	Local-to-PCI	Full	No action	Negate READY#
		Empty	Negate REQ# (off PCI Bus)	No action
Direct Master Read	PCI-to-Local	Full	Negate REQ# or throttle IRDY#	No action
		Empty	No action	Negate READY#
Direct Slave Write	PCI-to-Local	Full	Disconnect or throttle TRDY#	No action
		Empty	No action	Negate LHOLD, assert BLAST# (see Note)
Direct Slave Read	Local-to-PCI	Full	No action	Negate LHOLD, assert BLAST# (see Note)
		Empty	Throttle TRDY#	No action
DMA	Local-to-PCI	Full	No action	Negate LHOLD, assert BLAST#
		Empty	Negate REQ#	No action
	PCI-to-Local	Full	Negate REQ#	No action
		Empty	No action	Negate LHOLD, assert BLAST#

Note: De-assertion of LHOLD depends on MARBR[21].

3.6 Direct Data Transfer Modes

Figure 3-4 and Figure 3-5 illustrate the direct Data Transfer modes. Refer also to Table 3-6 for responses to full and empty FIFOs.



Host CPU accesses Local Memory or I/O = Direct Slave read/write
 Local CPU accesses System Memory = Direct Master read/write
 PCI 9080 read/write from System Memory and write/read to Local memory = DMA read/write

Figure 3-4. Direct Master, Direct Slave, and DMA

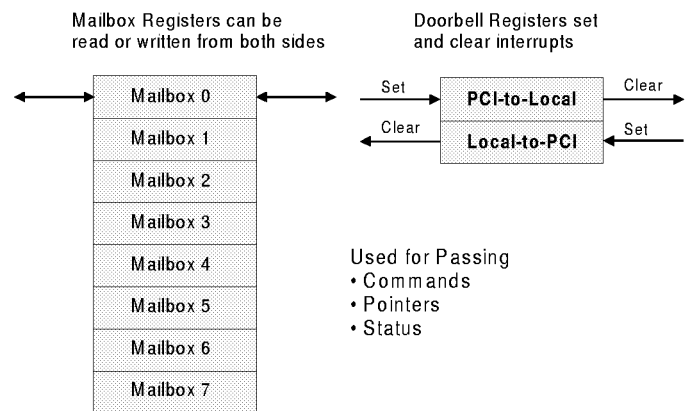


Figure 3-5. Mailbox/Doorbell Message Passing

3.6.1 Direct Master Operation (Local Master to PCI Target)

The PCI 9080 supports direct access of the PCI Bus by the Local processor or an intelligent controller. Master mode must be enabled in the PCI Command register. Five registers are used to define Local-to-PCI access:

- Range
- Local Base Address for Direct Master to PCI Memory Register

- Local Base Address for Direct Master to PCI IO/CFG Register
- PCI Configuration Address Register for Direct Master to PCI IO/CFG
- PCI Base Address

3.6.1.1 Decode

The Range register specifies the Local Address bits to use for decoding a Local-to-PCI access. The Local processor can perform only Memory cycles. Therefore, the Local Base Address for Direct Master to PCI Memory register is used to decode an access to PCI memory space. The Local Base Address for Direct Master to PCI IO/CFG register is used to decode an access to PCI I/O space or PCI Bus Configuration cycle access.

3.6.1.2 FIFOs

For Direct Master Memory access to the PCI Bus, the PCI 9080 has a 32-Lword (128 byte) Write FIFO and a 16-Lword (64 byte) Read FIFO. The FIFOs enable the Local Bus to operate independently of the PCI Bus and allows high-performance bursting on the Local and PCI Buses. In a Direct Master Write, the Local processor (Master) writes data to the PCI (Slave). In a Direct Master Read, the Local processor (Master) reads data from the PCI (Slave). Figure 3-6 and Figure 3-7 illustrate the FIFOs during a Direct Master Write and Read.

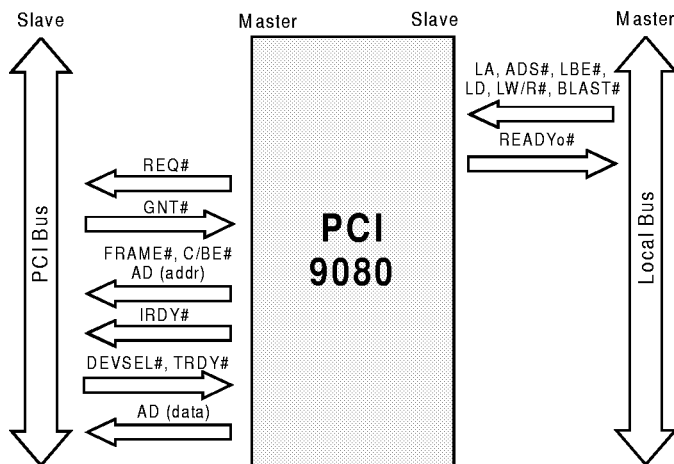


Figure 3-6. Direct Master Write

Note: The figure represents a sequence of Bus cycles.

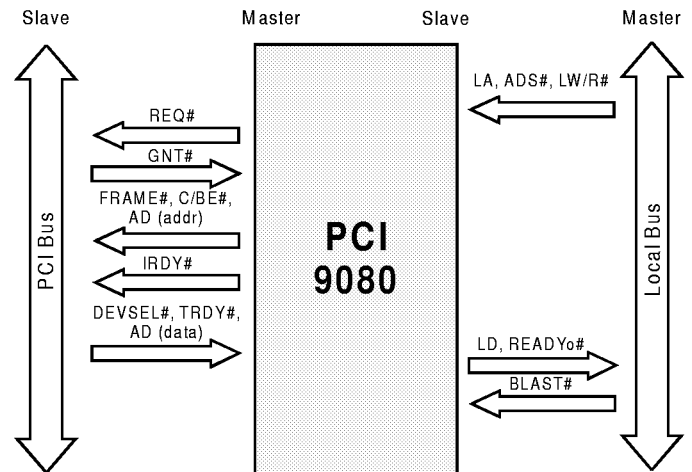


Figure 3-7. Direct Master Read

Note: The figure represents a sequence of Bus cycles.

3.6.1.3 Memory Access

The Local processor can read or write to the PCI memory. The PCI 9080 converts the Local Read/Write access. The Local Address space starts from the Direct Master Local Base Address up to the range. Remap (PCI Base Address) defines the PCI starting address.

Writes—The PCI 9080 continues to accept writes and returns READYo# until the Write FIFO is full. It then holds off READYo# until space becomes available in the Write FIFO. A programmable Direct Master FIFO “almost full” status output is provided (DMPAF#).

Reads—The PCI 9080 holds off READYo# while gathering an Lword from the PCI Bus. Programmable Prefetch modes are available if prefetch is enabled: prefetch, 4, 8, 16, or continuous until the Direct Master cycle ends. The Read cycle is terminated when the Local BLAST# input is asserted. Unused Read data is then flushed from the FIFO.

The PCI 9080 does not prefetch Read data for Single Cycle Direct Master reads (Local BLAST# input asserted during first Data phase). In this case, the PCI 9080 reads a single PCI Lword.

For Direct Master Single Cycle reads, the PCI 9080 asserts the same PCI Bus byte enables as asserted on the Local Bus.

For Multiple Cycle reads, the PCI 9080 reads entire Lwords (all PCI byte enables are asserted), regardless of local byte enables.

If the Prefetch Limit bit DMPBAM[11] is enabled, the PCI 9080 does not prefetch past a 4 KB boundary. Also, the Local Bus must not cross a 4 KB boundary during a Burst read.

The PCI 9080 never prefetches beyond the region specified for Direct Master accesses.

3.6.1.4 IO/CFG Access

When a Local Direct Master I/O access to the PCI Bus is made, the Configuration Enable bit of the PCI Configuration Address register determines if I/O or Configuration access is to be made to the PCI Bus.

Local Burst accesses are broken into Single PCI I/O Address/Data cycles. The PCI 9080 does not prefetch Read data for I/O and CFG reads.

For Direct Master I/O or Configuration cycles, the PCI 9080 asserts the same PCI Bus byte enables as asserted on the Local Bus.

3.6.1.5 I/O

If the Configuration Enable bit is clear, a single I/O access is made to the PCI Bus. The Local Address, remapped decode address bits and the local byte enables are encoded to provide the address and is output with an I/O Read or Write command during the PCI Address cycle.

For writes, data is loaded into the Write FIFO and READYo# returned to the Local Bus. For reads, the PCI 9080 holds off READYo# while gathering an Lword from the PCI Bus.

When the I/O Remap Select bit is set to a value of 1, these PCI Address bits [31:16] are forced to a value of 0 (DMPBAM[13]).

3.6.1.6 CFG (PCI Configuration Type 0 or Type 1 Cycles)

If the Configuration Enable bit is set, a CFG access is made to the PCI Bus. In addition to enabling the Configuration bit of DMCFGGA[31], the user must provide all register information. The register number (bits [7:2]) or the device number (bits [15:11]) must be modified and a new CFG Read/Write cycle must be performed before other registers or devices can be accessed.

If the PCI Configuration Address register selects a Type 0 command, bits [10:0] from the register are copied to address bits [10:0]. Bits [15:11] (device number) are translated into a single bit being set in PCI Address bits [31:11]. PCI Address bits [31:11] can be used as a device select. For a Type 1 command, bits [23:0] are

copied from the register to bits [23:0] of the PCI Address. PCI Address bits [31:24] are 0. A Configuration Read or Write command code is output with the address during the PCI Address cycle (DMCFGGA).

For writes, Local data is loaded into the Write FIFO and READYo# is returned. For reads, the PCI 9080 holds off READYo# while gathering an Lword from the PCI Bus.

Example 1—To perform a Type 0 Configuration cycle to PCI device on AD[21]:

- The PCI 9080 must be configured to allow Direct Master access to the PCI Bus. The PCI 9080 must also be set to respond to I/O Space accesses. Set PCICR[2,0] as follows:
 - Bit 0 = I/O Space = 1
 - Bit 2 = Master Enable = 1
- The board designer selects the Direct Master range. For this example, use a range of 1 MB:
 - 1 MB = 2^{20} = 000FFFFFh

The value to program into the range register is the inverse of 000FFFFFh, which is FFF00000h:

 - DMRR = FFF00000h
- The board designer determines local Base Address for Direct Master to PCI IO/CFG. For this example, use 40000000h:
 - DMLBAI = 40000000h
- The PCI Address (Remap) for Direct Master to PCI Memory register must enable Direct Master I/O access. Set DMPBAM[1] as follows:
 - Bit 1 = Direct Master I/O Access Enable = 1
- The PCI Bus must know which PCI device and PCI Configuration register the PCI Configuration cycle is accessing. For this example, access the PCI device on AD[21], as well as PCIBAR0, the PCI Base Address 0 for Memory-Mapped Configuration register (the fourth register, counting from 0—use Table 4-5, “PCI Configuration Registers,” for reference). Set DMCFGGA[31, 23:0] as follows:
 - Bits 1:0 = Configuration Type 0 = 00b
 - Bits 7:2 = Register Number = The fourth register, and therefore must program a 4 into this bit, beginning with bit 2 = 000100b
 - Bits 10:8 = Function Number = 000b
 - Bits 15:11 = Device Number = $n-11$, where n is the value in AD[n]=21-11 = 10 = 01010b

- Bits 23:16 = Bus Number = 00000000b
- Bit 31 = Configuration Enable = 1

The Register Number (bits [7:2]) or Device Number (bits [15:11]) must be modified and a new CFG Read/Write cycle must be performed before other registers or devices can be accessed.

3.6.1.7 Direct Bus Master Lock

The PCI 9080 supports direct Local-to-PCI Bus exclusive accesses (locked atomic operations). A locked operation must start with the Local Bus input LLOCK# being asserted during a Direct Master Bus Read cycle. Refer to the timing in Section 8, "Timing Diagrams."

3.6.1.8 Master/Target Abort

The PCI 9080 Master/Target abort logic enables a Local Bus Master to perform a Direct Master Bus poll of devices to determine whether the devices exist (typically when the Local Bus performs Configuration cycles to the PCI Bus).

If a PCI Master, Target Abort, or Retry Time-out is encountered during a transfer, the PCI 9080 asserts LSERR# if enabled (INTCSR[1:0]) (can be used as an NMI). If the Local Bus Master is waiting for a READY#, it is asserted along with BTERMo#. The Local Master's interrupt handler can take the appropriate application specific action. It can then clear the Abort bits in the PCI Status Configuration register (PCISR) to clear the LSERR# interrupt and re-enable Direct Master transfers.

If a Local Bus Master is attempting a Burst read from a nonresponding PCI device (Master/Target abort), it receives the READY# and BTERMo# for the first cycle only. If the Local processor cannot terminate its Burst cycle, it may cause the Local processor to hang. The Local Bus must then be reset from the PCI Bus or by a local watchdog timer asserting RESETi#. If the Local Bus Master cannot terminate its cycle with BTERMo#, it should not perform Burst cycles when attempting to determine whether a PCI device exists.

3.6.1.9 Write and Invalidate

The PCI 9080 can be programmed to perform Write and Invalidate cycles to the PCI for DMA and Direct Master transfers. The PCI 9080 supports Write and Invalidate transfers for cache line sizes of 8 or 16 Lwords. The size is specified in the PCI Cache Line Size register. If a size other than 8 or 16 is specified, the PCI 9080 performs Write transfers rather than Write and Invalidate transfers.

3.6.1.9.1 DMA Write and Invalidate

DMA Write and Invalidate transfers are enabled when the Write and Invalidate Enable bit of a DMA controller is set in its Mode register and the Memory Write and Invalidate Enable bit is set in the PCI Command register.

In Write and Invalidate mode, the PCI 9080 waits until the number of Lwords required for the specified cache line size have been read from the Local Bus before starting the PCI access. This ensures that a complete cache line write can be completed in one PCI Bus ownership. If a Target disconnects before a cache line is completed, the PCI 9080 completes the remainder of that cache line using normal writes before resuming Write and Invalidate transfers. If a Write and Invalidate cycle is in progress, the PCI 9080 continues to burst if another cache line has been read from the Local Bus before the cycle completes. Otherwise, the PCI 9080 terminates the burst and waits for the next cache line to be read from the Local Bus. If the final transfer is not a complete cache line, the PCI 9080 completes the DMA transfer, using normal writes.

3.6.1.9.2 Direct Master Write and Invalidate

Direct Master Write and Invalidate transfers are enabled when the Invalidate Enable bit is set in the PCI Base Address (Remap) register for Direct Master to PCI Memory and the Memory Write and Invalidate Enable bit is set in the PCI Command register (PCICR).

In Write and Invalidate mode, if the start address of the Direct Master transfer is on a cache line boundary, the PCI 9080 waits until the number of Lwords required for specified cache line size have been written from the Local Bus before starting PCI Write and Invalidate access. This ensures that a complete cache line write can be completed in one PCI Bus ownership. If the start address is not on a cache line boundary, the PCI 9080 starts a normal PCI Write access. The PCI 9080 terminates a cycle at a cache line boundary if it is performing a normal write or if it is performing a Write and Invalidate cycle and another cache line of data is not available. If an entire cache line is available by the time the PCI 9080 regains use of the PCI Bus, the PCI 9080 resumes Write and Invalidate cycles. Otherwise, it continues with a normal write. If a Target disconnects before a cache line is completed, the PCI 9080 completes the remainder of that cache line using normal writes.

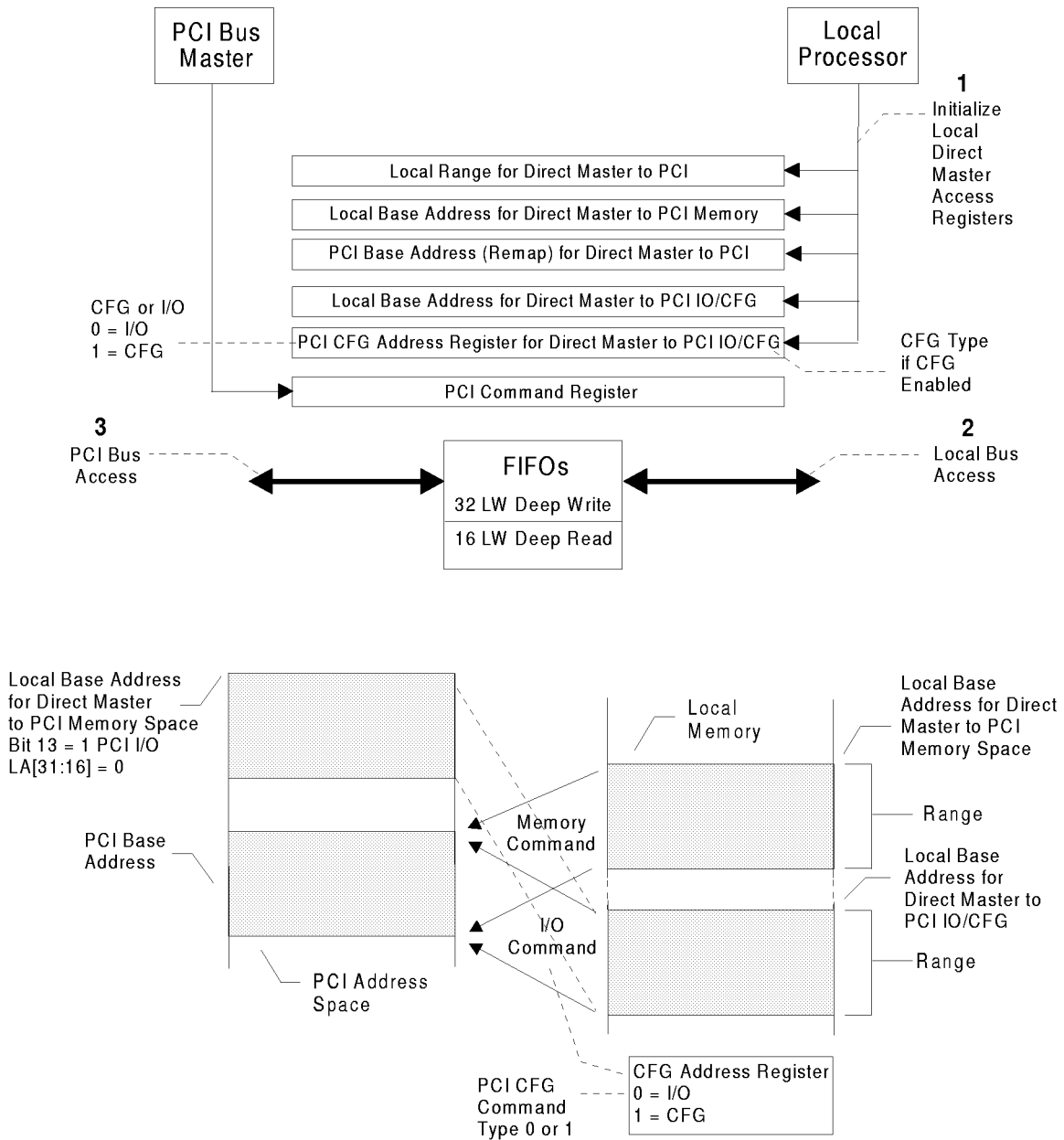


Figure 3-8. Local Master Direct Master Access of PCI Bus

3.6.2 Direct Slave Operation (PCI Master to Local Bus Access)

The PCI 9080 supports both Burst Memory-Mapped Transfer accesses and I/O-Mapped, Single-Transfer accesses to the Local Bus from the PCI Bus. PCI Base Address registers are provided to set up the location of the adapter in PCI memory and I/O space. In addition, local mapping registers allow address translation from PCI Address space to Local Address Space. Three spaces are available:

- Space 0
- Space 1
- Expansion ROM space

Expansion ROM space is intended to support a bootable ROM device for the host. Each Local space can be programmed to operate 8-, 16, or 32-bit Local Bus width. The PCI 9080 has an internal wait state generator and external wait state input, $READY\#$, which can be disabled or enabled with the Internal Configuration register. The Local Bus, independent of the PCI Bus, can:

- Burst as long as data is available
Continuous Burst (mode)
- Burst four Lwords at a time
- Perform continuous single cycle, with or without wait state(s)

For Single Cycle Direct Slave reads, the PCI 9080 reads a single Local Bus Lword or partial Lword. The PCI 9080 disconnects after one transfer for all Direct Slave I/O accesses.

For the highest Data transfer rate, the PCI 9080 supports posted writes and can be programmed to prefetch data during PCI Burst reads. The prefetch size, when enabled, can be from one to 16 Lwords, or until the PCI stops requesting. The PCI 9080 prefetches, if enabled, and drops the Local Bus after the Prefetch Counter is reached. In Continuous Prefetch mode, the PCI 9080 prefetches as long as any FIFO space is available and terminates the prefetch when the PCI terminates the request. If Read prefetching is disabled, the PCI 9080 disconnects after one Read transfer.

3.6.2.1 PCI 2.1 Mode

The PCI 9080 can be programmed through the Local Arbitration and PCI Mode register to perform delayed reads, as specified in PCI Specification v2.1.

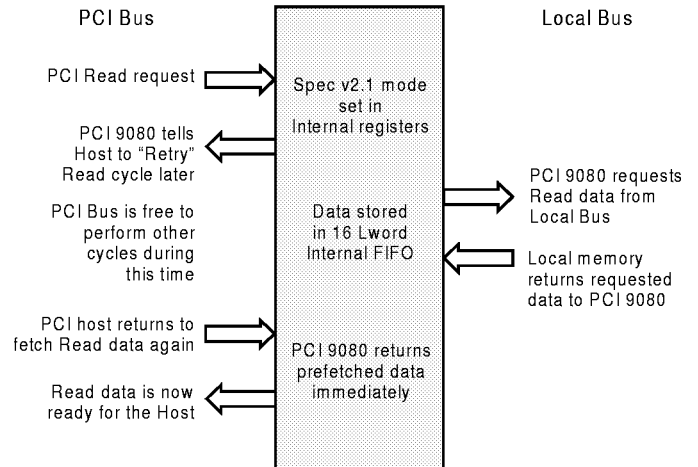


Figure 3-9. PCI Specification v2.1 Delayed Reads

Note: The figure represents a sequence of Bus cycles.

In addition to delayed read, the PCI 9080 supports the following PCI Specification v2.1 features:

- No write while read is pending (Retry for reads)
- Write and flush pending read

The PCI 9080 also supports Read Ahead mode (refer to Figure 3-10), where prefetched data can be read from the internal PCI 9080 FIFO instead of from the Local Bus. The address must be subsequent to the previous address and must be 32-bit aligned (next address = current address + 4).

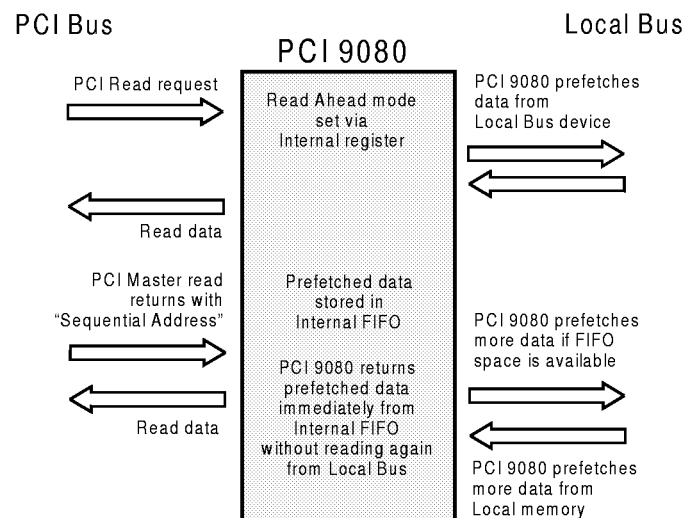


Figure 3-10. PCI 9080 Read Ahead Mode

Note: The figure represents a sequence of Bus cycles.

The PCI 9080 can be programmed to keep the PCI Bus by generating a wait state(s), thereby de-asserting TRDY#, if the Write FIFO becomes full. The PCI 9080 can also be programmed to keep the Local Bus, thereby asserting LHOLD, if the Direct Slave Write FIFO becomes empty or the Direct Slave Read FIFO becomes full. The Local Bus is dropped in either case when the Local Bus Latency Timer is enabled and expires. (Refer to Figure 3-11 and Figure 3-12.)

For Direct Slave writes, the PCI (Master) writes data to the Local Bus (Slave). Direct Slave is the “Command from the PCI Host,” which has the highest priority. Direct Slave or Direct Master pre-empts DMA; however, Direct Slave does not pre-empt Direct Master (refer to Section 3.6.2.3.1, “Backoff”).

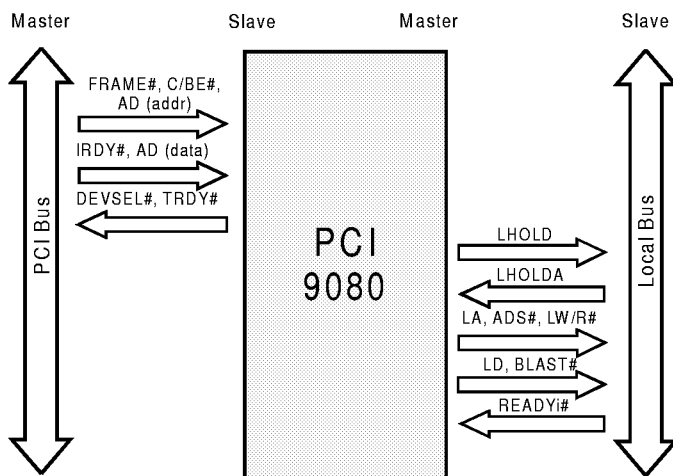


Figure 3-11. Direct Slave Write

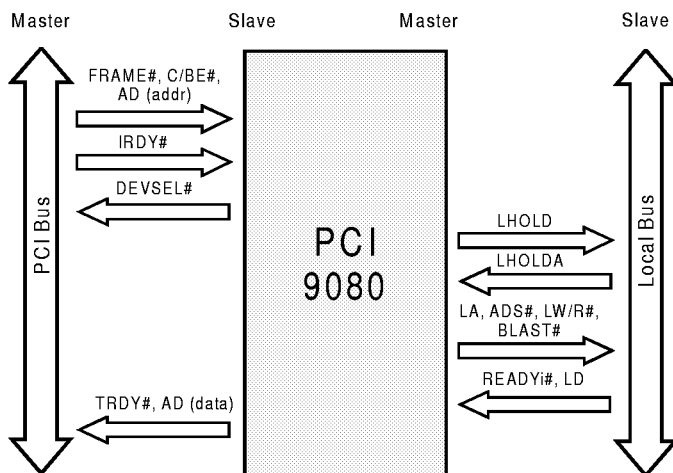


Figure 3-12. Direct Slave Read

Note: The figures represent a sequence of Bus cycles.

For Direct Slave reads, the PCI (Master) reads data from the Local Bus (Slave).

The PCI 9080 supports on-the-fly Endian conversion for Space 0, Space 1, and Expansion ROM space. The Local Bus can be Big/Little Endian by either using the BIGEND# input pin or the programmable internal register configuration. When BIGEND# is asserted, it overrides the internal register configuration.

Note: The PCI Bus is always Little Endian.

3.6.2.2 PCI-to-Local Address Mapping

Note: Not applicable if I₂O mode.

Three Local Address spaces—Space 0, Space 1, and Expansion ROM—are accessible from the PCI Bus. Each is defined by a set of three registers:

- Local Address Range
- Local Base Address
- PCI Base Address

A fourth register, Bus Region Descriptor for PCI-to-Local Accesses, defines the Local Bus characteristics for both regions (refer to Figure 3-13).

3.6.2.2.1 Byte Enables

LBE[3:0]# (pins 139-142) are encoded based on the configured bus width, as follows:

32-Bit Bus—For a 32-bit bus, the four byte enables indicate which of the four bytes are active during a Data cycle.

- BE3# Byte Enable 3—LD[31:24]
- BE2# Byte Enable 2—LD[23:16]
- BE1# Byte Enable 1—LD[15:8]
- BE0# Byte Enable 0—LD[7:0]

16-Bit Bus—For a 16-bit bus, BE3#, BE1# and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively.

- BE3# Byte High Enable (BHE#)—LD[15:8]
- BE2# not used
- BE1# Address bit 1 (LA1)
- BE0# Byte Low Enable (BLE#)—LD[7:0]

8-Bit Bus—For an 8-bit bus, BE1# and BE0# are encoded to provide LA1 and LA0, respectively.

- BE3# not used
- BE2# not used
- BE1# Address bit 1 (LA1)
- BE0# Address bit 0 (LA0)

Each PCI-to-Local Address space is defined as part of reset initialization as described in the next section.

3.6.2.2.2 Local Bus Initialization Software

Range—Specifies which PCI Address bits to use for decoding a PCI access to Local Bus space. Each Prefetch Limit bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others.

Remap PCI-to-Local Addresses into a Local Address Space—Bits in this register remap (replace) the PCI Address bits used in decode as the Local Address bits.

Local Bus Region Descriptor—Specifies the Local Bus characteristics.

3.6.2.2.3 PCI Initialization Software

PCI reset software determines how much address space is required by writing a value of all ones (1) to a PCI Base Address register and then reading back the value. The PCI 9080 return zeroes in Don't Care Address bits, effectively specifying the address space required. The PCI software then maps the Local Address space into the PCI Address space by programming the PCI Base Address register. (Refer to Figure 3-13.)

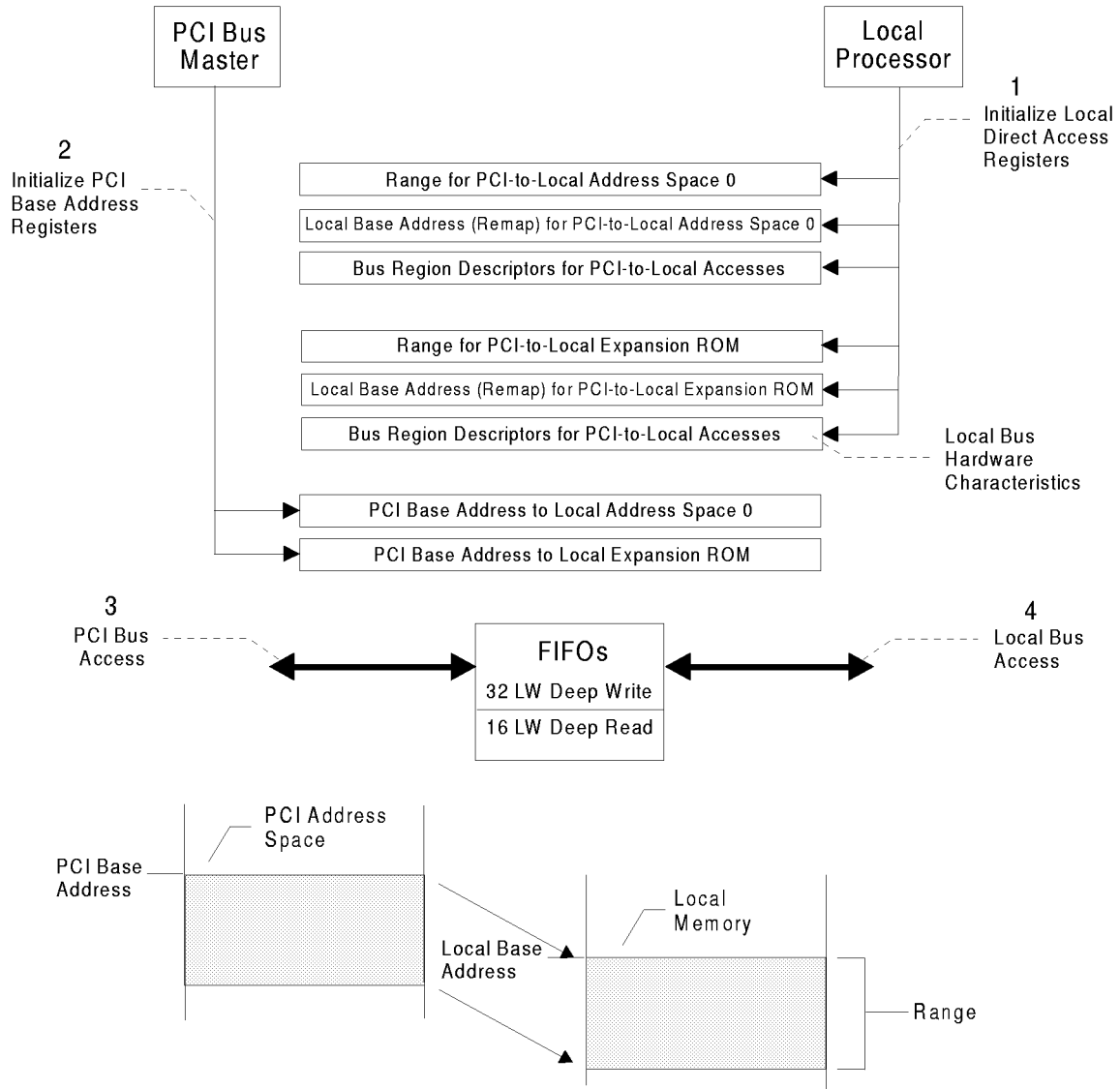


Figure 3-13. Direct Slave Access of Local Bus

Example 2—A 1 MB Local Address Space 12300000h through 123FFFFFFh is accessible from the PCI Bus at PCI Addresses 78900000h through 789FFFFFFh.

- a. Local initialization software sets the Range and Local Base Address registers, as follows:
 - **Range**—FFF00000h (1 MB, decode the upper 12 PCI Address bits)
 - **Local Base Address (remap)**—123XXXXXh (Local Base Address for PCI-to-Local accesses) (bit 0, the Space Enable bit, must be set to 1 to be recognized by the Host)
- b. PCI Initialization software writes all ones to the PCI Base Address, then reads it back again.
 - The PCI 9080 returns a value FFF00000h. The PCI software then writes to PCI Base Address register
 - **PCI Base Address**—789XXXXXh (PCI Base Address for access to Local Address Space)

For PCI direct access to the Local Bus, the PCI 9080 has a 32-Lword (128 byte) Write FIFO and a 16-Lword (64 byte) Read FIFO. The FIFOs enable the Local Bus to operate independently of the PCI Bus. The PCI 9080 can be programmed to return a Retry response or to throttle TRDY# for any PCI Bus transaction attempting to write to the PCI 9080 Local Bus when the FIFO is full.

For PCI Read transactions from the PCI 9080 Local Bus, the PCI 9080 holds off TRDY# while gathering the Local Bus Lword to be returned. For Read accesses mapped to the PCI memory space, the PCI 9080 prefetches up to 16 Lwords (has Continuous Prefetch mode) from the Local Bus. Unused Read data is flushed from the FIFO. For Read accesses mapped to the PCI I/O space, the PCI 9080 does not prefetch Read data. Rather, it breaks each read of the Burst cycle into a Single Address/Data cycle on the Local Bus.

The period of time the PCI 9080 holds off TRDY# can be programmed (the Target Retry Timer) in the Local Bus Region Descriptor register (LBRD0). The PCI 9080 issues a Retry to the PCI Bus transaction Master when the programmed time period expires. This occurs when the PCI 9080 cannot gain control of the Local Bus and return TRDY# within the programmed time period.

3.6.2.3 Deadlock and BREQo

Deadlock can occur when a Master on the PCI Bus wants to access the PCI 9080 Local Bus at the same time a Master on the PCI 9080 Local Bus requires access to the PCI Bus. Two types of deadlock situations can occur:

- **Partial Deadlock**—Master on Local Bus is performing a direct Bus Master access to a PCI Bus device other than the PCI Bus device concurrently trying to access the Local Bus.
- **Full Deadlock**—Master on Local Bus is performing a direct Bus Master access to the same PCI Bus device concurrently trying to access the Local Bus.

This applies only to Direct (“pass through”) Master and Slave accesses through the PCI 9080. Deadlock does not occur in transfers through the PCI 9080 DMA controller or the mailboxes.

For partial deadlock, the PCI access to the Local Bus times out (the Target Retry Timer, which is programmable through the Local Bus Region Descriptor register for PCI-to-Local accesses) and the PCI 9080 responds with a PCI Retry. PCI specification requires that a PCI Master release its request for the PCI Bus (de-asserts REQ#) for a minimum of two PCI clocks after receiving a Retry. This allows the PCI Bus arbiter to grant the PCI Bus to the PCI 9080 so that it can complete its Direct Master access and free up the Local Bus. Possible solutions are described below for cases in which the PCI Bus arbiter does not function as described (PCI Bus architecture dependent), waiting for a time-out is undesirable, or a full deadlock condition exists.

For full deadlock, the only solution is to back off the Local Master.

3.6.2.3.1 Backoff

The PCI 9080 contains a pin (BREQo) that indicates a possible deadlock condition exists. The PCI 9080 starts the BREQo timer (programmable through registers) when it detects the following conditions:

- A Master on the PCI Bus is trying to access memory or an I/O device on the Local Bus and is not gaining access (*for example*, LHOLDA not received).
- A Master on the Local Bus is performing a direct Bus Master Read access to the PCI Bus or a Master on the Local Bus is performing a direct Bus Master Write access to the PCI Bus and the PCI 9080 Direct Master Write FIFO cannot accept another Write cycle.

If the timer expires and the PCI 9080 has not received the LHOLDA signal, the PCI 9080 asserts BREQo. External bus logic can use this as a signal to perform Backoff.

A Backoff cycle is device/bus architecture dependent. External logic (arbiter) can assert the necessary signals to cause the Local Master to release the Local Bus (Backoff). After backing off the Local Master, it can grant the bus to the PCI 9080 (by asserting LHOLDA).

Once BREQo is asserted, READYo# for the current Data cycle is never asserted (the Local Bus Master must perform Backoff). When the PCI 9080 detects LHOLDA, it proceeds with the PCI Master to Local Bus access. When this access is complete and the PCI 9080 releases the Local Bus, the external logic can release Backoff and the Local Master can resume the cycle interrupted by the Backoff cycle. The Write FIFO of the PCI 9080 retains all the data it has acknowledged (*that is*, the last data for which READYo# was asserted).

After the Backoff condition ends, the Local Master restarts the last cycle with ADS#. For writes, the data following this ADS# should be the data that was not acknowledged by the PCI 9080 prior to the Backoff cycle (for instance, the last data for which there was no READYo# asserted).

If a PCI Read cycle is completed when the Local Bus is backed off, the Local Bus Master receives that data if Local Master restarts the same last cycle (data is not read twice). A new read is performed, if the resumed Local Bus cycle is not the same as the backed-off cycle.

3.6.2.3.2 Software/Hardware Solution for Systems without Backoff Capability

For adapters that do not support Backoff, a possible deadlock solution is as follows.

PCI Host software, external Local Bus hardware, general purpose output USERO and general purpose input (USERI) can be used by PCI Host software to prevent deadlock. USERO can be set to request that the external arbiter not grant the bus to any Local Bus Master except the PCI 9080. A status output from the local arbiter can be connected to general-purpose input USERI to indicate that no Local Bus Master owns the Local Bus. The PCI Host to determine that no Local Bus Master currently owns the Local Bus can read the input. PCI Host can then perform a Direct Slave access. When the host is done, it clears USERO. For devices that support pre-empt, USERO can be used to pre-empt the current Bus Master device. The current Local Bus Master device completes its current cycle and gives up the Local Bus (de-asserts LHOLD).

3.6.2.3.3 Software Solutions to Deadlock

PCI Host software and Local Bus software can use a combination of mailbox registers, doorbell registers, interrupts, direct Local-to-PCI accesses and direct PCI-to-Local accesses to avoid deadlock.

3.6.2.4 Direct Slave Lock

The PCI 9080 supports direct PCI-to-Local Bus exclusive accesses (locked atomic operations). A PCI locked operation to Local Bus results in the entire address Space 0, Space 1 and Expansion ROM space being locked until they are released by the PCI Bus Master. The PCI 9080 asserts LLOCKo# during the first clock of an atomic operation (Address cycle) and de-asserts it a minimum of one clock, following the last Bus access for the atomic operation. LLOCKo# is de-asserted after the PCI 9080 detects PCI FRAME# and PCI LOCK# de-asserted at the same time. Refer to the timing diagrams in Section 8, "Timing Diagrams." Locked operations are enabled or disabled with the Local Bus Region Descriptor register for PCI-to-Local accesses.

It is the responsibility of external arbitration logic to monitor the LLOCKo# pin and enforce the meaning for an atomic operation. *For example*, if a Local Master initiates a locked operation, the local arbiter may choose to not grant use of the Local Bus to other Masters until the locked operation is complete.

3.6.3 Direct Slave Priority

Direct Slave accesses have higher priority than DMA accesses.

Direct Slave accesses pre-empt DMA transfers. When the PCI 9080 DMA controller owns the Local Bus, its LHOLD output and LHOLDA input are asserted and its LDSHOLD output is de-asserted. When a Direct Slave access occurs, the PCI 9080 gives up the Local Bus within two Lword transfers by de-asserting LHOLD and floating its Local Bus outputs. After the PCI 9080 samples its LHOLDA input de-asserted, it requests the Local Bus for a Direct Slave transfer by asserting LHOLD and LDSHOLD. When the PCI 9080 receives LHOLDA, it drives the bus and performs the Direct Slave transfer. Upon completion of the Direct Slave transfer, the PCI 9080 gives up the Local Bus by de-asserting both LHOLD and LDSHOLD and floating its Local Bus outputs. After the PCI 9080 samples its LHOLDA de-asserted and its local pause timer is zero, it requests the Local Bus for a DMA transfer by re-asserting LHOLD. When it receives LHOLDA, it drives the bus and continues with the DMA transfer.

3.7 DMA Operation

The PCI 9080 supports two independent DMA channels capable of transferring data from the Local Bus to the PCI Bus or from the PCI Bus to the Local Bus. Each channel consists of a DMA controller and a programmable FIFO. Both channels support Chaining and Non-chaining transfers, Demand mode DMA, and End of Transfer (EOT) pins. Master mode must be enabled in the PCI Command register.

3.7.1 Non-Chaining Mode DMA

The host processor or the Local processor sets the Local Address, PCI Address, transfer count and transfer direction. The host or Local processor then sets a control bit to initiate the transfer. The PCI 9080 arbitrates the PCI and Local Buses and transfer data. Once the transfer is complete, the PCI 9080 sets the Channel Done bit to a value of 1 and generates an interrupt to the Local processor or the PCI Host (programmable). DMA Done bit in the internal DMA register can be pooled to indicate the status of DMA transfer.

DMA registers are accessible from the PCI Bus and Local Bus. (Refer to Figure 3-14.)

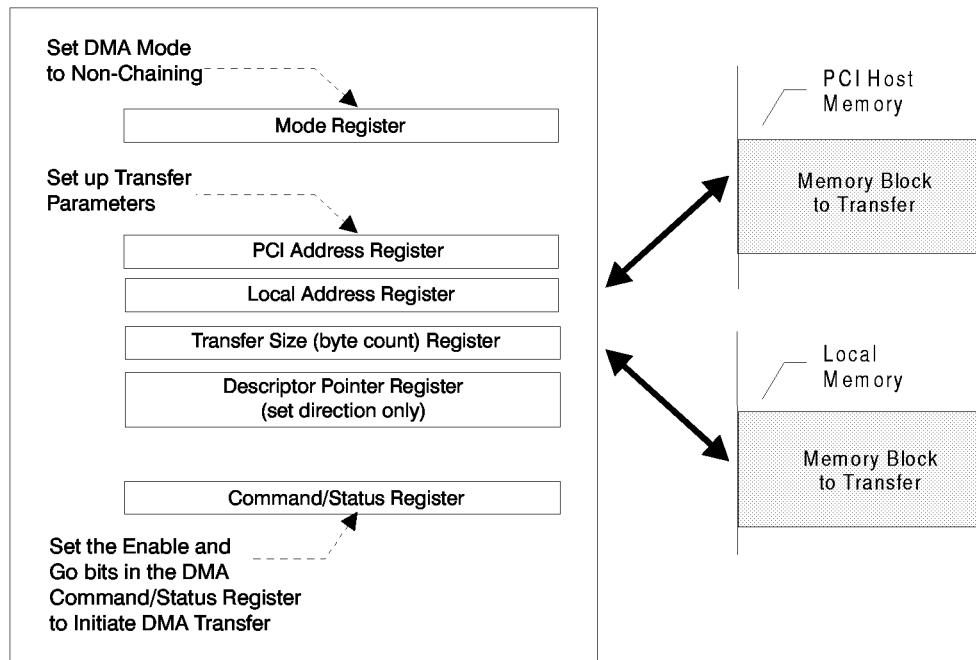


Figure 3-14. Non-Chaining DMA Initialization

The Local processor or PCI requires DMA. The PCI 9080 is Master on both the PCI and Local Buses. Direct Slave or Direct Master pre-empts DMA.

The PCI 9080 releases the PCI Bus if one of the following occurs (refer to Figure 3-15):

- FIFO is full
- Terminal count is reached
- PCI Latency Timer (PCILTR[7:0]) expires—normally programmed by the Host PCI BIOS—and PCI GNT# de-asserts
- PCI Host asserts STOP
- Direct Master request pending

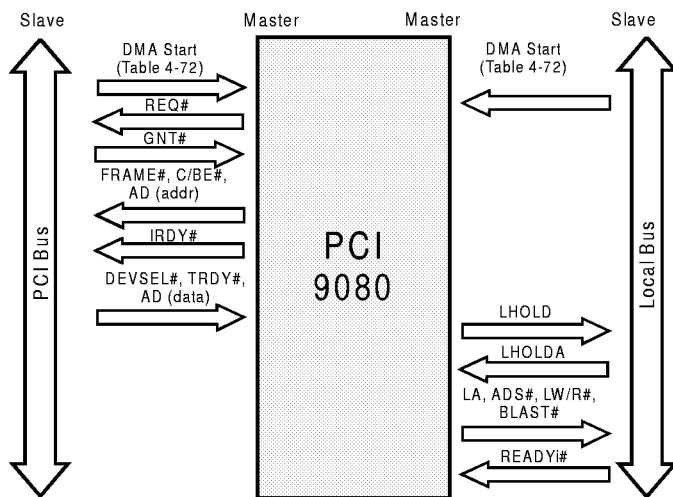


Figure 3-15. DMA, PCI-to-Local

Note: The figure represents a sequence of Bus cycles.

The PCI 9080 releases the Local Bus if one of the following occurs (refer to Figure 3-16):

- FIFO is empty
- Terminal count is reached
- Local Bus Latency Timer (MARBR[7:0]) expires
- BREQ# input is asserted
- Direct Slave request is pending

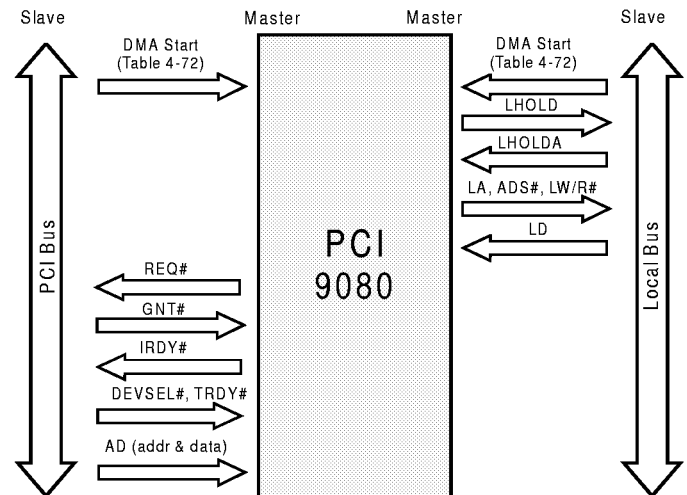


Figure 3-16. DMA, Local-to-PCI

Note: The figure represents a sequence of Bus cycles.

3.7.2 Chaining Mode DMA

In Chaining mode DMA, the Host Processor or the Local Processor sets up descriptor blocks in local or host memory that are composed of a PCI Address, Local Address, transfer count, transfer direction, and address of the next descriptor block (refer to Figure 3-18). Host or Local Processor then sets up the address of the initial descriptor block in the Descriptor Pointer register of the PCI 9080 and initiates the transfer by setting a control bit. The PCI 9080 loads the first descriptor block and initiates the Data transfer. The PCI 9080 continues to load descriptor blocks and transfer data until it detects the End of Chain bit is set in the Next Descriptor Pointer register. The PCI 9080 can be programmed to interrupt the Local processor by setting the Interrupt after Terminal Count bit or PCI Host upon completion of each block transfer and after all block transfers are complete (done) (refer to Figure 3-17). If chaining descriptors are located in Local memory, the DMA controller can be programmed to clear the transfer size at the completion of each DMA (DMAMODE0[16] and DMAMODE1[16]).

Notes: In Chaining mode DMA, the descriptor includes PCI Address, Local Address, Transfer Size and the Next Descriptor Pointer (DMAPADR0-DMADPR0). The Descriptor Pointer register contains the End of Chain bit, Direction of Transfer, Next Descriptor Address, and Next Descriptor Location.

The DMA descriptor can be on Local or PCI memory, or both (first descriptor on Local memory, and second descriptor on PCI memory).

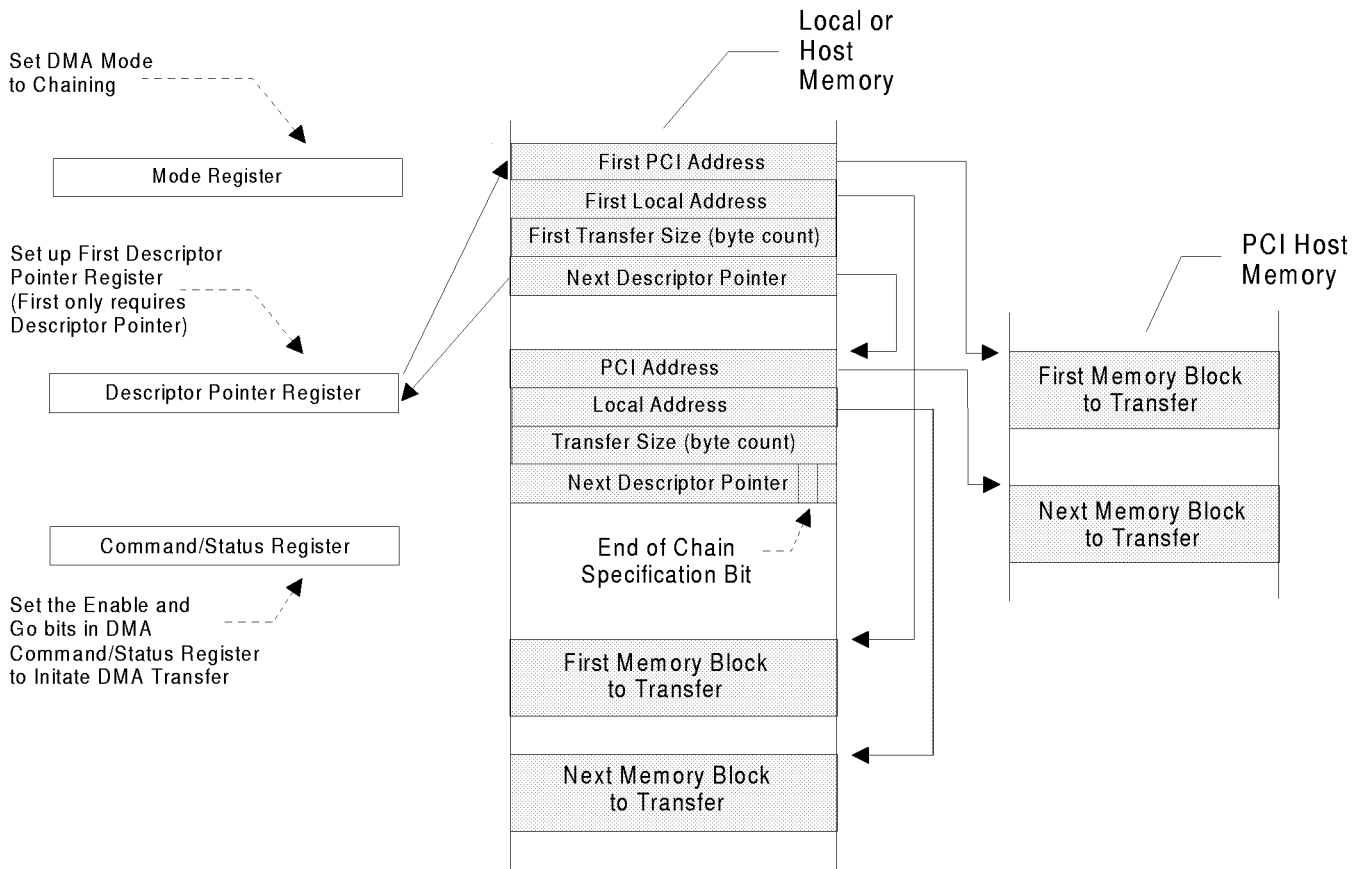


Figure 3-17. Chaining DMA Initialization

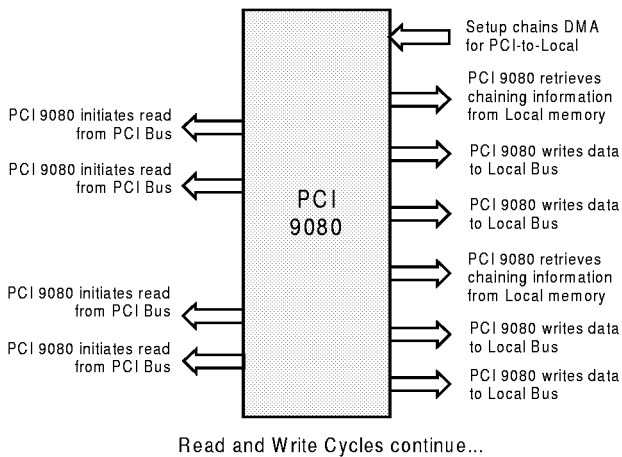


Figure 3-18. Chaining Mode DMA from PCI-to-Local

Note: The figure represents a sequence of Bus cycles.

3.7.3 DMA Data Transfers

The PCI 9080 DMA controller can be programmed to transfer data from the Local Bus side to the PCI Bus side or from the PCI Bus side to the Local Bus side. Refer to Figure 3-19 and Figure 3-20 for a description of the operation.

3.7.3.1 Local-to-PCI Bus DMA Transfer

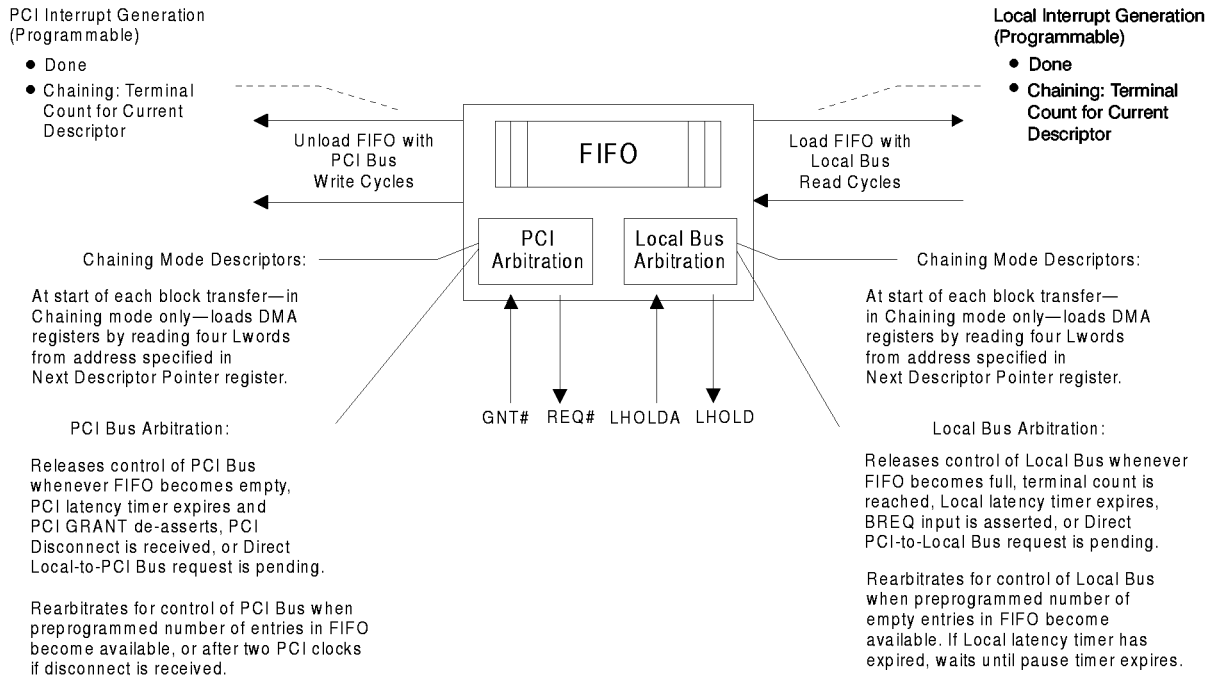


Figure 3-19. Local-to-PCI Bus DMA Data Transfer Operation

3.7.3.2 PCI-to-Local Bus DMA Transfer

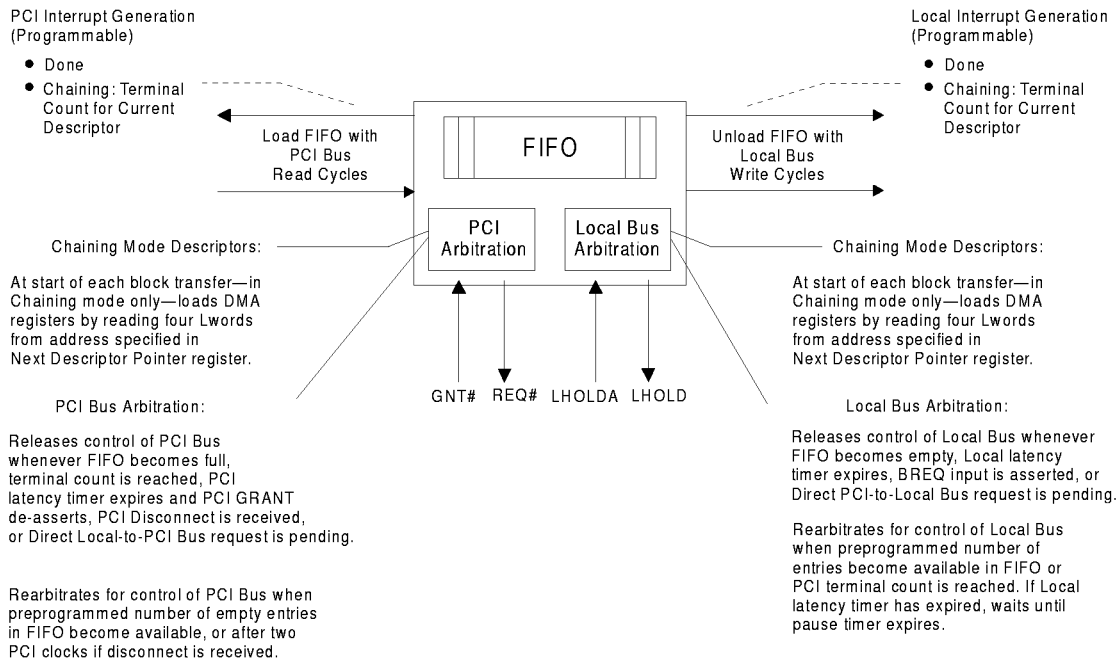


Figure 3-20. PCI-to-Local Bus DMA Data Transfer Operation

3.7.3.3 Unaligned Transfers

For unaligned Local-to-PCI transfers, the PCI 9080 reads a partial Lword from the Local Bus. It continues to read Lwords from the Local Bus. Lwords are assembled, aligned to the PCI Bus address and loaded into the FIFO.

For PCI-to-Local transfers, Lwords are read from the PCI Bus and loaded into the FIFO. On the Local Bus, the Lwords are assembled from the FIFO, aligned to the Local Bus address and written to the Local Bus. On both the Local and PCI Buses, the byte enables for writes determine LA[1:0] for the start of a transfer. For the last transfer, the byte enables specify the bytes to be written. All reads are Lwords.

3.7.4 Demand Mode DMA

DMA Mode register bit 15 (BLAST mode for Demand mode DMA), determines the number of Lwords transferred after a DMA controller's DREQ[1:0]# input is de-asserted.

If BLAST# output is not required for the last Lword of the DMA transfer (bit 15 = 1), the DMA controller releases the data bus after it receives an external READYi# or the internal wait state counter decrements to a value of 0 for the current Lword. If DMA controller is currently bursting data, which is not the last Data phase for the burst, BLAST# output is not asserted.

If BLAST# output is required for the last Lword of the DMA transfer (bit 15 = 0), the DMA controller transfers one or two Lwords. If DREQ[1:0]# is de-asserted during the Address phase of the first transfer in a PCI 9080 Local Bus ownership (ADS#, LHOLDA asserted), the DMA controller completes the current Lword. If DREQ[1:0]# is de-asserted during any phase other than the Address phase of the first transfer in a PCI 9080 Local Bus ownership, the DMA controller completes the current Lword, and one additional Lword (this allows BLAST# output to be asserted during the final Lword). If the DMA FIFO is full or empty after the Data phase in which DREQ[1:0]# is de-asserted, the second Lword is not transferred. DREQ[1:0]# controls only the number of Lword transfers. For an 8-bit bus, the PCI 9080 gives up the bus after the last byte for the Lword is transferred. For a 16-bit bus, the PCI 9080 gives up the bus after the last word for the Lword is transferred.

3.7.5 DMA Priority

DMA Channel 0 priority, DMA Channel 1 priority, or rotating priority can be specified in the DMA Arbitration register.

3.7.6 DMA Arbitration

The PCI 9080 DMA controller releases control of the Local Bus (de-asserts LHOLD) when one of the following occurs:

- FIFOs are full in a Local-to-PCI transfer
- FIFOs are empty in a PCI-to-Local transfer
- Local Bus Latency Timer expires (if enabled)
- BREQ input is asserted (BREQ can be enabled or disabled, or gated with a latency timer before the PCI 9080 gives up the Local Bus)
- Direct Slave access is pending
- EOT input is received (if enabled)

The DMA controller releases control of the PCI Bus when one of the following occurs:

- FIFOs are full or empty
- PCI Latency Timer expires and loses the PCI GNT# signal
- Target Disconnect response is received

DMA controller de-asserts its PCI Bus request (REQ#) for a minimum of two PCI clocks.

3.7.6.1 End of Transfer (EOT0# or EOT1#) Input

DMA Mode register bit 15 (BLAST mode for EOT), determines the number of Lwords transferred after a DMA controller EOT[1:0]# input is asserted.

If BLAST# output is not required for the last Lword of the DMA transfer (bit 15 = 1), the DMA controller releases the data bus and terminates DMA after it receives an external READYi# or the internal wait state counter decrements to a value of 0 for the current Lword. If the DMA controller is currently bursting data, which is not the last Data phase for the burst, BLAST# output is not asserted.

If BLAST# output is required for the last Lword of the DMA transfer (bit 14 = 0), the DMA controller transfers one or two Lwords. If EOT[1:0]# is asserted, the DMA controller completes the current Lword, and one additional Lword (this allows BLAST# output to be asserted during the final Lword). If the DMA FIFO is full or empty after the Data phase in which EOT[1:0]# is asserted, the second Lword is not transferred.

The DMA controller terminates a transfer on an Lword boundary after EOT[1:0]# is asserted. For an 8-bit bus, the PCI 9080 terminates after the last byte for the Lword is transferred. For a 16-bit bus, the PCI 9080 terminates after the last word for the Lword is transferred.

3.7.6.2 DMA Abort

A DMA transfer can be aborted. The abort process is as follows:

1. DMA Channel must be enabled (DMACSR0[0]=1).
2. DMA Channel must be started (DMACSR0[1]=1).
3. Wait for the Channel Done bit to be set to zero (DMACSR0[4]=0).
4. Disable the DMA Channel (DMACSR0[0] =0).
5. Abort DMA by programming the Channel Abort bit (DMACSR0[2]=1).
6. Wait until the Channel Done bit is set (DMACSR0[4]=1).

Note: One to two Data transfers occur after the Abort bit is set. Aborting when no DMA cycles are in progress causes the next DMA to abort.

3.7.6.3 Local Latency and Pause Timers

A Local Bus Latency Timer and Local Bus Pause Timer are programmable with the DMA Arbitration register. If the Local Latency Timer expires, the PCI 9080 completes the current Lword transfer and releases LHOLD. After its programmable Pause Timer expires, it reasserts LHOLD. When it receives LHOLDA, it continues the transfer. The PCI Bus transfer continues until the FIFO is empty for a Local-to-PCI transfer or until it is full for a PCI-to-Local transfer.

3.8 Vendor and Device ID Registers

Three Vendor and Device ID registers are supported:

- PCIIDR, which contains the normal Device and Vendor IDs. This register can be loaded from the serial EEPROM or from Local processors.

- PCISVID, which contains the Subsystem and Subvendor IDs. This register can be loaded from the serial EEPROM or from Local processors.
- PCIHIDR, which contains the hardcoded PLX Vendor and Device IDs.

3.9 Doorbell Registers

There are two 32-bit doorbell interrupt/status registers in the PCI 9080. One is assigned to the PCI Bus interface and the other is assigned to the Local Bus interface.

The Local processor can generate a PCI Bus interrupt by writing any number other than all zeroes to the PCI-to-Local Doorbell register (P2LDBELL).

A PCI Host can generate a Local Bus interrupt by writing any number other than all zeroes to the Local-to-PCI Doorbell register (L2PDBELL).

3.10 Mailbox Registers

There are eight 32-bit mailbox registers in the PCI 9080 that can be written to and read from both buses. These registers can be used to pass command and status information directly between Local and PCI Bus devices.

A Local interrupt can be generated, if enabled, when the PCI Host writes to one of the first four mailbox registers.

3.11 User Input and Output

The PCI 9080 supports user input and output pins, USERI[31] and USERO[27], respectively. User output data can be logged by writing to CNTRL[16]. User input data can be read from CNTRL[17].

3.12 Interrupts

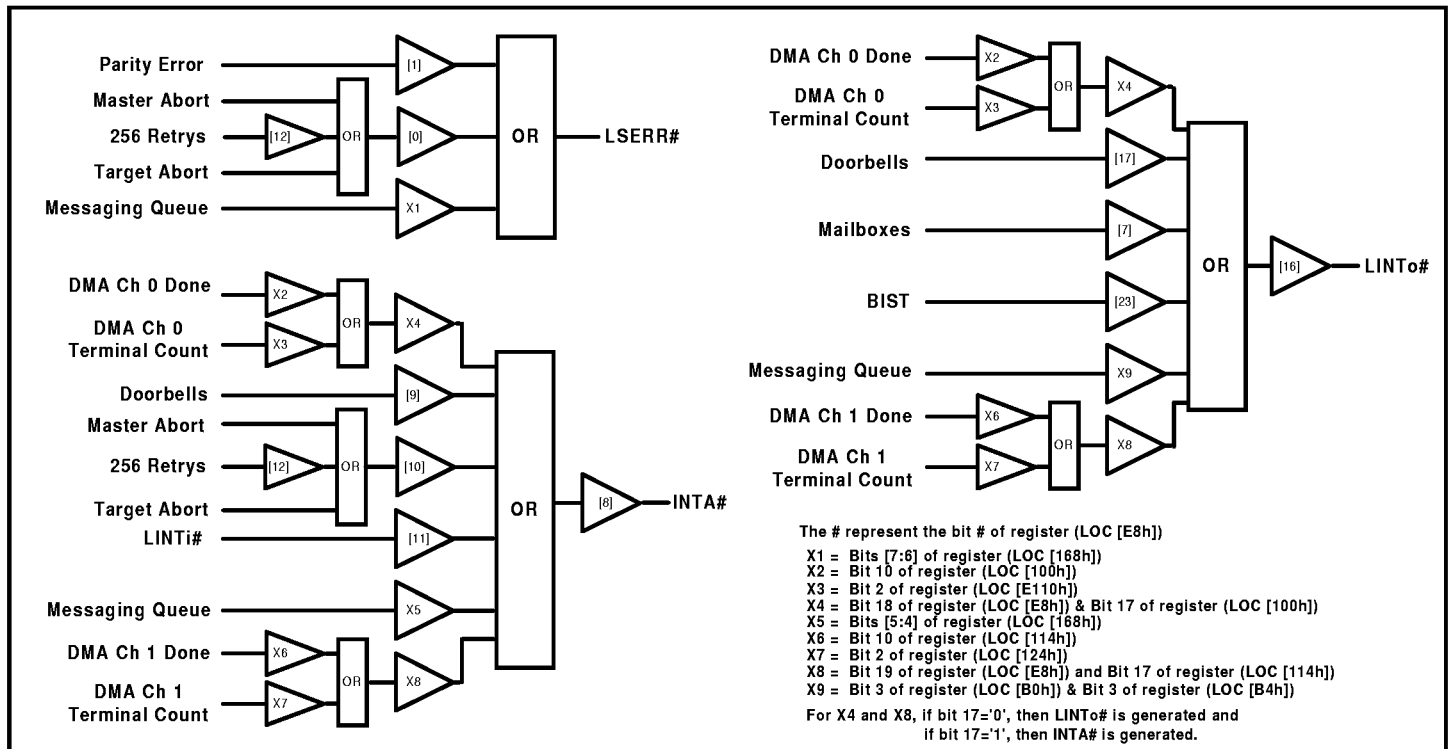


Figure 3-21. Interrupt and Error Sources

3.12.1 PCI Interrupts (INTA#)

A PCI 9080 PCI Interrupt (INTA#) can be generated by one of the following:

- Local-to-PCI Doorbell register
- Local interrupt input
- Master/Target abort status condition
- DMA Ch 0/Ch 1 Done
- DMA Ch 0/Ch 1 Terminal Count reached
- Messaging Outbound Post Queue is not empty

INTA#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9080 Interrupt Control/Status register (INTCSR). This register also provides interrupt status for each interrupt source.

The PCI 9080 PCI Bus interrupt is level output. Disabling an Interrupt Enable bit or clearing the cause(s) of the interrupt can clear an interrupt.

3.12.1.1 Local Interrupt Input

Asserting Local Bus input pin LINTi# can generate a PCI Bus interrupt. PCI Host processor can read the PCI 9080 Interrupt Control/Status register to determine that an interrupt is pending due to the LINTi# pin being asserted.

The interrupt remains asserted as long as the LINTi# pin is asserted and the Local interrupt input is enabled. Adapter specific action can be taken by the PCI Host processor to cause the Local Bus to release LINTi#.

3.12.1.2 Master/Target Abort Interrupt

The PCI 9080 sets the Master Abort or Target Abort Status bit in the PCI Configuration register when it detects a Master or Target abort. These status bits cause PCI INTA# to be asserted if interrupts are enabled.

The interrupt remains asserted as long as the Master or Target Abort bits remain set in the PCI Status Configuration register (PCISR) and Master/Target Abort

Interrupt is enabled. Use a PCI Type 0 Configuration access or a Local access to clear the Master Abort and Target Abort Interrupt bits in the PCI Status Configuration register.

Interrupt Control/Status register Bits (INTCSR[26:24]) are latched at the time of a Target abort interrupt or Master abort interrupt. They provide information as to who was Master when an abort occurred. The PCI 9080 updates these bits whenever an abort occurs.

3.12.2 Local interrupts (LINTo#)

A PCI 9080 Local interrupt (LINTo#) can be generated by one of the following:

- PCI-to-Local Doorbell/Mailboxes Register access
- PCI BIST interrupt, the DMA done interrupt
- DMA terminal count is reached
- DMA abort interrupt or the Messaging Outbound Post Queue is not empty

LINTo#, or individual sources of an interrupt, can be enabled or disabled with the PCI 9080 Interrupt Control/Status register (INTCSR). The Interrupt Control/Status register also provides interrupt status for each source of the interrupt.

The PCI 9080 Local interrupt is a level output. An interrupt can be cleared by disabling the Interrupt Enable bit of a source or by clearing the cause of an interrupt.

3.12.2.1 Local-to-PCI Doorbell Interrupt

A Local Bus Master can generate a PCI Bus interrupt by writing to the Local-to-PCI Doorbell register (L2PDBELL). PCI Host processor can then read the PCI 9080 Interrupt Control/Status register (INTCSR) to determine that a doorbell interrupt is pending. It can then read the PCI 9080 Local-to-PCI Doorbell register.

Each bit in the Local-to-PCI Doorbell register is individually controlled. The Local Bus can only set bits in the Doorbell register. From the Local Bus, writing 1 to any bit position sets that bit and writing 0 to a bit position has no effect. Bits in the Local-to-PCI Doorbell register can only be cleared from the PCI Bus. From the PCI Bus, writing 1 to any bit position clears that bit and writing 0 to a bit position has no effect.

The interrupt remains asserted as long as any of the Local-to-PCI Doorbell register bits are set and PCI Doorbell Interrupt is enabled.

To prevent race conditions when the PCI Bus is accessing the Doorbell register (or any Configuration

register), the PCI 9080 automatically de-asserts READYo# to prevent Local Bus accesses.

3.12.2.2 PCI-to-Local Doorbell Interrupt

A PCI Bus Master can generate a Local Bus interrupt by writing to the PCI-to-Local Doorbell register (P2LDBELL). Local processor can then read the PCI 9080 Interrupt Control/Status register (INTCSR) to determine that a doorbell interrupt is pending. It can then read the PCI 9080 PCI-to-Local Doorbell register.

Each bit in the PCI-to-Local Doorbell register is individually controlled. The PCI Bus can only set bits in the Doorbell register. From the PCI Bus, writing 1 to any bit position sets that bit and writing 0 to a bit position has no effect. Bits in the PCI-to-Local Doorbell register can only be cleared from the Local Bus. From the Local Bus, writing 1 to any bit position clears that bit and writing 0 to a bit position has no effect.

Note: *If Local Bus cannot clear Doorbell Interrupt, do not use the PCI-to-Local Doorbell register.*

The interrupt remains asserted as long any of the PCI-to-Local Doorbell register bits are set and the Local Doorbell Interrupt is enabled.

To prevent race conditions when the Local Bus is accessing the Doorbell register (or any Configuration register), the PCI 9080 automatically issues a Retry to the PCI Bus.

3.12.2.3 Built-In Self Test Interrupt (BIST)

A PCI Bus Master can generate a Local Bus interrupt by performing a PCI Type 0 Configuration write to a bit in the PCI BIST register. The Local processor can then read the PCI 9080 Interrupt Control/Status register (INTCSR) to determine that a BIST interrupt is pending.

The interrupt remains asserted as long as the bit is set and the BIST interrupt is enabled. The Local Bus then resets the bit when BIST is complete. PCI Host software may fail the device if the bit is not reset after two seconds.

Note: *The PCI 9080 does not have an internal BIST.*

3.12.2.4 DMA Channel 0/1 Interrupts

A DMA channel can generate a PCI or Local Bus interrupt when done (transfer complete) or after a transfer is complete for a descriptor in Chaining mode. A bit in the DMA mode register determines whether to generate a PCI or Local interrupt. The local or PCI processor can then read the PCI 9080 Interrupt

Control/Status register (INTCSR) to determine whether a DMA channel interrupt is pending.

A Done Status Bit in the Control/Status register can be used to determine whether the interrupt is

- A done interrupt
- The result of a transfer for a descriptor in a chain that is not yet complete

The mode register of a channel enables a Done Interrupt. In Chaining mode, a bit in the Next Descriptor Pointer register of the channel (loaded from Local memory) specifies whether to generate an interrupt at the end of the transfer for the current descriptor.

A DMA channel interrupt is cleared by writing a 1 to the Clear Interrupt bit in the DMA Command/Status register (DMACSR0[3] and DMACSR1[3]).

3.12.3 PCI SERR# (PCI NMI)

The PCI 9080 generates an SERR# pulse if parity checking is enabled in the PCI Command register and it detects an address parity error or the Generate SERR# bit in the Interrupt Control/Status register (INTCSR) is 0 and a 1 is written.

SERR# output can be enabled or disabled with the PCI Command register.

3.12.4 Local LSERR# (Local NMI)

LSERR# interrupt output is asserted if the following occurs:

- PCI Bus Target Abort or Master Abort Status bit is set in the PCI Status Configuration register
- Parity Error Status bit is set in the PCI Status Configuration register
- Messaging Outbound Free Queue overflows

If parity error checking is enabled in the PCI Command register, the PCI 9080 sets the Master Detected Parity Error Status bit in the PCI Status Configuration register (PCISR) if it detects one of the following:

- Parity error during a PCI 9080 Master Read
- PCI Bus signal PERR# being asserted during a PCI 9080 Master Write

The PCI 9080 sets a Parity Error bit in the PCI Status Configuration register (PCISR) if it detects one of the following:

- Data parity error during a PCI 9080 Master Read

- Data parity error during a Slave Write access to the PCI 9080
- Address parity error

The PCI 9080 Interrupt Control/Status register (INTCSR) can be used to individually enable or disable LSERR# for an abort or parity error. LSERR# is a level output that remains asserted as long as the Abort or Parity Error Status bits are set.

3.13 I₂O Compatible Message Unit

The Messaging Unit supplies two paths for messages, two inbound FIFOs to receive messages from the primary PCI Bus and two outbound FIFOs to pass messages to the primary PCI Bus. Refer to *I₂O Architecture Specification v1.5* for details.

Figure 3-22 and Figure 3-23 illustrate information about the I₂O architecture.

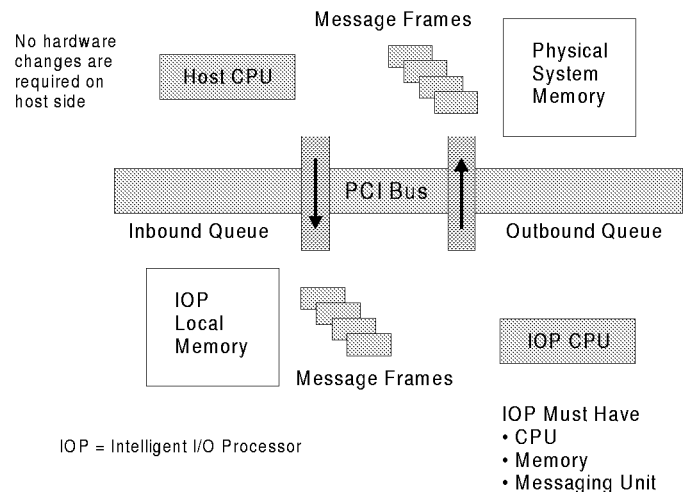


Figure 3-22. I₂O System Architecture

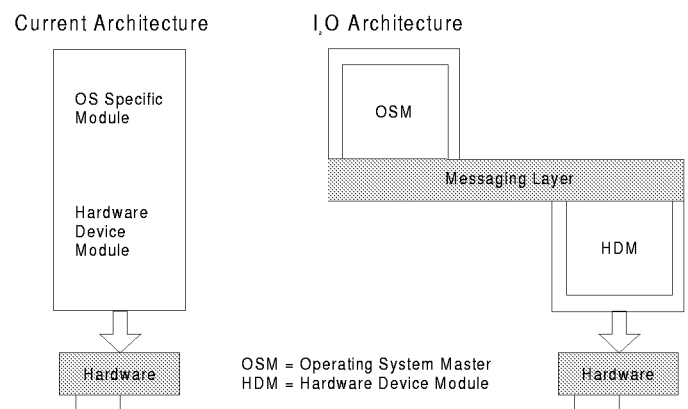


Figure 3-23. I₂O Software Architecture

3.13.1 Inbound Messages

Inbound messages reside in a pool of message frames (minimum of 64-byte frames) allocated in shared Local Bus (IOP) memory. The Inbound Message Queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Inbound Free List FIFO holds the message frame addresses (MFA) of available message frames in Local memory. The Inbound Post List FIFO holds the message frame addresses (MFA) of all currently posted messages.

The inbound circular FIFOs are accessed by external PCI agents through the Inbound Queue Port location in the PCI Address space. The Inbound Queue Port, when read by an external PCI agent, returns the Inbound Free List FIFO MFA. An external PCI agent places a message frame into the Inbound Post List FIFO by writing its MFA to the Inbound Queue Port location.

3.13.2 Outbound Messages

Outbound messages reside in a pool of message frames (minimum 64-byte frames) allocated in shared PCI Bus (Host System) memory. The Outbound Message Queue is comprised of a pair of rotating FIFOs implemented in Local memory. The Outbound Free List FIFO holds the message frame addresses (MFA) of available message frames in system memory. The Outbound Post List FIFO holds the MFA of all currently posted messages.

The outbound circular FIFOs are accessed by external PCI agents through the Outbound Queue Port location in the PCI Address space. The Outbound Queue Port, when read by an external PCI agent, returns the Outbound Post List FIFO MFA. An external PCI agent places free message frames into the Outbound Free List FIFO by writing the free MFA into the Outbound Queue Port location.

Memory for the circular FIFOs must be allocated in Local Bus (IOP) memory. The base address of the queues is contained in the Queue Base Address register (QBAR). Each FIFO entry is a 32-bit data value. Each read and write of the queue must be a single 32-bit access.

The circular FIFOs range in size from 4 KB entries to 64 KB entries. All four FIFOs must be contiguous and of the same size. Therefore, the total amount of Local memory needed for circular FIFOs ranges from 64 KB to 1 MB. The FIFO size is specified in the Messaging Queue Configuration register (MQCR).

The starting address of each FIFO is based on the Queue Base Address and the FIFO size, as listed in Table 3-7.

Table 3-7. Queue Starting Address

FIFO	Starting Address
Inbound Free List	QBAR
Inbound Post List	QBAR + (1 * FIFO Size)
Outbound Post List	QBAR + (2 * FIFO Size)
Outbound Free List	QBAR + (3 * FIFO Size)

3.13.3 I₂O Pointer Management

The FIFOs always reside in shared Local Bus (IOP) memory and are allocated and initialized by the IOP. Before enabling I₂O (Messaging Queue Configuration register bit 0 set to 1), the Local processor must initialize the following registers with the initial offset, according to the configured FIFO size:

- Inbound Post and Free Head Pointer registers
- Inbound Post and Free Tail Pointer registers
- Outbound Post and Free Head Pointer registers
- Outbound Post and Free Tail Pointer registers

The Messaging Unit (MU) automatically adds the Queue Base Address to the offset in each head and tail pointer register. The software can then enable I₂O. After initialization, the local software should not write to the pointers managed by the MU hardware.

The empty flags are set if the queues are disabled (MQCR[0] = 0) and head and tail pointers are equal. This occurs independently of how the head and tail pointers are set.

An empty flag is cleared, signifying not empty, only if the queues are enabled and the pointers become not equal.

If an empty flag is cleared and the queues are enabled, the empty flag is set only if the tail pointer is incremented and the head and tail pointers become equal.

Full flags are always cleared when the queues are disabled or the head and tail pointers are not equal.

A full flag is set when the queues are enabled, the head pointer is incremented, and the head and tail pointers become equal.

Each circular FIFO has a head pointer and a tail pointer, which are offsets from the Queue Base Address. Writes to a FIFO occur at the head of the FIFO and reads occur from the tail. The head and tail pointers are incremented by either the Local processor or the MU hardware. The unit that writes to the FIFO also maintains the pointer. The pointers are incremented after a FIFO access. Both pointers wrap around to the first address of the circular FIFO when they reach the FIFO size, so that the head and tail pointers “chase” each other around and around

in the circular FIFO. MU wraps the pointers automatically for the pointers that it maintains. IOP software must wrap the pointers that it maintains. Whenever they are equal, the FIFO is empty. To prevent overflow conditions, I₂O specifies that the number of message frames allocated should be less than or equal to the number of entries in a FIFO. (Refer to Figure 3-24 for additional information.)

Each inbound MFA is specified by I₂O as the offset from the start of shared Local Bus (IOP) memory region 0 to the start of the message frame. Each outbound MFA is specified as the offset from the Host memory location 0x00000000h to the start of the message frame in the shared Host memory. Since the MFA is an actual address, the message frames need not be contiguous. The IOP allocates and initializes inbound message frames in shared IOP memory using any suitable memory allocation technique. The Host allocates and initializes outbound message frames in shared Host memory using any suitable memory allocation technique. Message frames are a minimum of 64 bytes in length.

I₂O uses a “push” (write-preferred) memory model. That means that the IOP writes messages and data to the shared Host memory, and the Host writes messages and data to shared IOP memory. Software should make use of Burst and DMA transfers whenever possible to ensure efficient use of the PCI Bus for message passing.

Additional information on message passing implementation may be found in the *I₂O Architecture Specification v1.5*.

3.13.4 Inbound Free List FIFO

The Local processor allocates inbound message frames in its shared memory and can place the address of a free (available) message frame into the Inbound Free List FIFO by writing its MFA into the FIFO location pointed to by the Queue Base register + Inbound Free Head Pointer register. The Local processor must then increment the Inbound Free Head Pointer register.

A PCI Master (Host or another IOP) can obtain the MFA of a free message frame by reading the Inbound Queue Port Address (40h of the first PCI Memory Base Address register). If the FIFO is empty (*that is*, no free inbound message frames are currently available, and the head and tail pointers are equal), the MU returns a value of -1 (FFFFFFFFh). If the FIFO is not empty (*that is*, the head and tail pointers are not equal), the MU reads the MFA pointed to by the Queue Base register + Inbound Free Tail Pointer register, returns its value and increments the Inbound Free Tail Pointer register. If the Inbound Free Queue is not empty, and queue prefetching is enabled (QSR[3], the next entry in the FIFO is read from the Local Bus into a prefetch register. The prefetch register then provides the data for the next PCI read from this queue, thus reducing the number of PCI wait states.

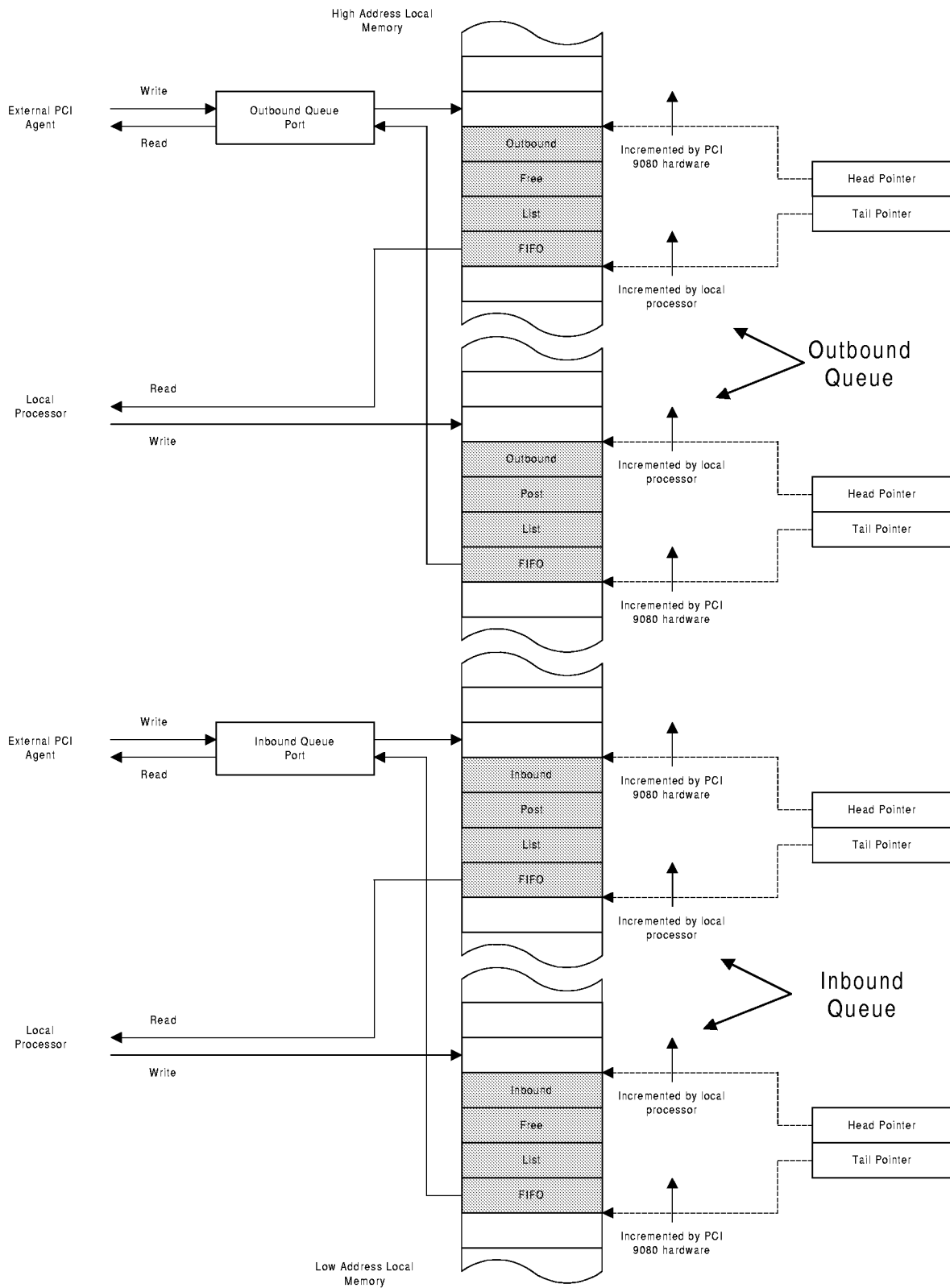


Figure 3-24. Circular FIFO Operation

3.13.5 Inbound Post List FIFO

A PCI Master (Host or another IOP) can write a message into an available message frame in shared Local Bus (IOP) memory. It can then post that message by writing the message frame address (MFA) to the Inbound Queue Port Address (40h of the first PCI Memory Base Address register). When the port is written, the MU writes the MFA to the Inbound Post List FIFO location pointed to by the Queue Base register + FIFO Size + Inbound Post Head Pointer register. After the MU writes the MFA to the Inbound Post List FIFO, it increments the Inbound Post Head Pointer register.

The Inbound Post Tail Pointer register points to the Inbound Post List FIFO location which holds the MFA of the oldest posted message. The Local processor maintains the tail pointer. After a Local processor reads the oldest MFA, it can remove the MFA from the Inbound Post List FIFO by incrementing the Inbound Post Tail Pointer register.

The PCI 9080 generates a Local interrupt when the Inbound Post List FIFO is not empty. The Inbound Post List FIFO Interrupt bit in the Queue Status/Control register (QSR) indicates the interrupt status. The interrupt clears when the Inbound Post List FIFO is empty. The interrupt can be masked by the Inbound Post List FIFO Interrupt Mask bit (QSR[4]).

To prevent race conditions from the time the PCI Write transaction is received until the data is written in Local memory and the Inbound Post Head Pointer register is incremented, any PCI Direct Slave access to the PCI 9080 is issued a Retry.

3.13.6 Outbound Post List FIFO

A Local Master (IOP) can write a message into an available message frame in shared Host memory. It can then post that message by writing the message frame address (MFA) to the Outbound Post List FIFO location pointed to by the Queue Base register + Outbound Post Head Pointer register + (2 * FIFO Size). The Local processor should then increment the Outbound Post Head Pointer register.

A PCI Master can obtain the MFA of the oldest posted message by reading the Outbound Queue Port Address (44h of the first PCI Memory Base Address register). If the FIFO is empty (*that is*, no more outbound messages are posted, and the head and tail pointers are equal), the MU returns a value of -1 (FFFFFFFFh). If the Outbound Post List FIFO is not empty (*that is*, the head and tail pointers are not equal), the MU reads the MFA pointed to by the Queue Base register + (2 * FIFO Size) +

Outbound Post Tail Pointer register, returns its value and increments the Outbound Post Tail Pointer register.

The PCI 9080 generates a PCI Interrupt when the Outbound Post Head Pointer register is not equal to the Outbound Post Tail Pointer register. The Outbound Post List FIFO Interrupt bit of the Outbound Post List FIFO Interrupt Status (OPLFIS) register indicates the interrupt status. When the pointers become equal, both the interrupt and the Outbound Post List FIFO Interrupt bit are automatically cleared. The pointers become equal when a PCI Master (Host or another IOP) reads enough FIFO entries to empty the FIFO. The Outbound Post List FIFO Interrupt Mask (OPLFIM) register can mask the interrupt.

3.13.7 Outbound Post Queue

To reduce read latency, prefetching from the tail of the queue occurs whenever the queue is not empty and the tail pointer is incremented (queue has been read from), or when the queue is empty and the head pointer is incremented (queue has been written to). When the host CPU reads the Outbound Post Queue, the data is immediately available.

3.13.8 Inbound Free Queue

To reduce read latency, prefetching from the tail of the queue occurs whenever the queue is not empty and the tail pointer is incremented (queue has been read from), or when the queue is empty and the head pointer is incremented (queue has been written to). When the host CPU reads the Inbound Free Queue, the data is immediately available.

3.13.9 Outbound Free List FIFO

A PCI Master (Host or other IOP) allocates outbound message frames in its shared memory and can place the address of a free (available) message frame into the Outbound Free List FIFO by writing the message frame address (MFA) to the Outbound Queue Port Address (44h of the first PCI Memory Base Address register). When the port is written, the MU writes the MFA to the Outbound Free List FIFO location pointed to by the Queue Base register + (3 * FIFO Size) + Outbound Free Head Pointer register. After the MU writes the MFA to the Outbound Free List FIFO, it increments the Outbound Free Head Pointer register.

When the IOP needs a free outbound message frame, it must first check whether any free frames are available. If the Outbound Free List FIFO is empty (*that is*, the outbound free head and tail pointers are equal), the IOP must wait for the Host to place additional outbound free

message frames in the Outbound Free List FIFO. If the Outbound Free List FIFO is not empty (*that is*, the head and tail pointers are not equal), the IOP can obtain the MFA of the oldest free outbound message frame by reading the location pointed to by the Queue Base register + (3 * FIFO Size) + Outbound Free Tail Pointer register. After the IOP reads the MFA, it must increment the Outbound Free Tail Pointer register. To prevent overflow conditions, I₂O specifies that the number of message frames allocated should be less than or equal to the number of entries in a FIFO. MU also checks for overflows of the Outbound Free List FIFO. When the

head pointer is incremented and becomes equal to the tail pointer, the Outbound Free List FIFO is full, and the MU generates a local LSERR (NMI) interrupt. The interrupt is recorded in the Queue Status Control (QSR) register.

From the time that the PCI Write transaction is received until the data is written into Local memory and the Outbound Free Head Pointer register is incremented, any PCI Direct Slave access to the PCI 9080 is issued a Retry.

Table 3-8. Circular FIFO Summary

FIFO Name	PCI Port	Generate PCI Interrupt?	Generate Local Interrupt	Head Pointer Maintained by	Tail Pointer Maintained by
Inbound Free List FIFO	Inbound Queue Port (Host Read)	No	No	Local processor	MU hardware
Inbound Post List FIFO	Inbound Queue Port (Host Write)	No	Yes, when the Port is written	MU hardware	Local processor
Outbound Post List FIFO	Outbound Queue Port (Host Read)	Yes, when the FIFO is not empty	No	Local processor	MU hardware
Outbound Free List FIFO	Outbound Queue Port (Host Write)	No	Yes, (LSERR) when the FIFO is full	MU hardware	Local processor

3.13.10 I₂O Enable Sequence

To enable I₂O, the Local processor should perform the following:

- Initialize Space 1 address and range
- Initialize all FIFOs and message frame memory
- Set the PCI class code in PCICCR to be an I₂O device with programming interface 01h
- Set the I₂O Enable bit
- Set the Local Init Done bit

Note: NB# must be pulled up so the PCI 9080 issues retries to all PCI accesses until the Local Init Done bit is set in CNTRL by the Local processor.

The I₂O Enable bit in the Queue Status register (QSR) causes remapping of resources for use in I₂O mode. When this bit is set, all Memory-Mapped Configuration registers (such as queue ports 40h and 44h) and Space 1 share PCIBAR0. PCI accesses to offset 00h-FFh of PCIBAR0 result in accesses to the internal Configuration registers of the PCI 9080. Accesses above offset FFh of PCIBAR0 result in Local Space accesses, beginning at offset 100h from the Local Space 1 Remap register (LAS1BA). Therefore space located at offset 00h-FFh from LAS1BA is not addressable by way of PCIBAR0.

Programmer's Note: Because PCI accesses to offset 00h-FFh of PCIBAR0 result in internal Configuration accesses, Inbound Free MFAs must be greater than FFh.

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4. REGISTERS

4.1 New Register Definitions Summary

Refer to descriptions in the following sections for a full explanation.

Table 4-1. New Registers Definitions Summary

PCI Offset	Local Offset	Register	Bits	Description
08h or ACh	88h or 12Ch	MARBR	23	Add PCIREQMODE output.
			28	Read Ahead mode.
18h	98h	LBRD0	15	Single Read mode removed.
28h	A8h	DMPBAM	10	Extend almost full flag to five bits (fifth bit not contiguous).
			11	Add CDMPFLIMIT output; do not prefetch past 4 KB boundary for Direct Master.
			12, 3	Direct Master Read prefetch size control.
			13	I/O Remap select.
			15:14	Direct Master write delay.
30h	B0h	OPLFIS	all	New Outbound Post List FIFO Interrupt Status register.
34h	B4h	OPLFIM	all	New Outbound Post List FIFO Interrupt Mask register.
40h	N/A	IQP	all	New Inbound Queue Port register.
44h	N/A	OQP	all	New Outbound Queue Port register.
68h	E8h	INTCSR	4	Move DMA0INTSEL output to DMAMODE0. Change to Reserved.
			5	Move DMA1INTSEL output to DMAMODE1. Change to Reserved.
			3	Mailbox interrupt enable on F, not on PCI 9060.
			31:28	Mailbox interrupts on SD, not on PCI 9060.
80h	100h	DMAMODE0	16	Clear byte count in chaining descriptor.
			17	Add C0_INTSEL output. 0=Local int., 1=PCI int.
94h	114h	DMAMODE1	16	Clear byte count in chaining descriptor.
			17	Add C1_INTSEL output. 0=Local int., 1=PCI int.
C0h	140h	MQCR	all	New Messaging Queue Configuration register.
C4h	144h	QBAR	all	New Queue Base Address register.
C8h	148h	IFHPR	all	New Inbound Free Head Pointer.
CCh	14Ch	IFTPR	all	New Inbound Free Tail Pointer.
D0h	150h	IPHPR	all	New Inbound Post Head Pointer.
D4h	154h	IPTPR	all	New Inbound Post Tail Pointer.
D8h	158h	OFHPR	all	New Outbound Free Head Pointer.
DCh	15Ch	OFTPR	all	New Outbound Free Tail Pointer.
E0h	160h	OPHPR	all	New Outbound Post Head Pointer.
E4h	164h	OPTPR	all	New Outbound Post Tail Pointer.
E8h	168h	QSR	all	New I ₂ O Queue Status register.
F0h	170h	LAS1RR	all	New Local Address Space 1 Range Register for PCI-to-Local.
F4h	174h	LAS1BA	all	New Local Address Space 1 Local Base Address (Remap).
F8h	178h	LBRD1	all	New Local Address Space 1 Bus Region Descriptor.

4.1.1 Register Differences between PCI 9080 and PCI 9060, PCI 9060ES, and PCI 9060SD

Table 4-2. Register Differences between PCI 9080 and PCI 9060

Register	PCI/Local Offset	Bits	Description
PCIIDR	00/00	31:16	Default changed from PCI 9060 to PCI 9080
PCICR	04/04	4	Memory Write and Invalidate now supported
PCISR	06/06	6	User-definable bit added
PCICLSR	0C/0C	7:0	Cache line size is now used for Memory Write and Invalidate
PCIBAR0	10/10	8:6	Register Bank size changed from 128 to 256
PCIBAR1	14/14	8:6	Register Bank size changed from 128 to 256
PCIBAR3	1C/1C	31:0	Base address register for Local Address Space 1
PCISVID	2C/2C	15:0	Subsystem Vendor ID register
PCISID	2E/2E	15:0	Subsystem ID register
MARBR	08, AC/88, 12C	31:0	Mode/Arbitration register now accessible from the PCI Bus
		21	Local Bus Direct Slave Give up Bus Mode
		22	Direct Slave Lock Enable
		23	PCI Request Mode
		24	PCI Specification v2.1 Mode
		25	PCI Read/No Write Mode
		26	PCI Read with Write Flush Mode
		27	Get Local Bus Latency Timer with BREQ
		28	PCI Read/No Flush Mode
BIGEND	0C/8C	7:0	Big/Little Endian Descriptor register
EROMBA	14/94	5	BREQo Timer Resolution control
LBRD0	18/98	1:0	Local Bus width now programmable in S mode
		10	Read Prefetch Count Enable
		14:11	Read Prefetch Count
		17:16	Local Bus width now programmable in S mode
		25	Extra Long Serial EEPROM Load
DMPBAM	28/A8	12, 3	Direct Master Read Prefetch Size Control
		10, 8:5	Programmable Almost Full Flag increased by two bits
		11	Direct Master Prefetch Limit
		13	I/O Remap select
		15:14	Direct Master Write Delay
LAS1RR	F0/170	31:0	Local Address Space 1 Range register
LAS1BA	F4/174	31:0	Local Address Space 1 Local Base Address register (Remap)
LBRD1	F8/178	31:0	Local Address Space 1 Bus Region Descriptor register
MBOX0	40, 78/C0	31:0	MBOX0 moved to PCI Address 78 when Messaging Queue is enabled
MBOX1	44, 7C/C4	31:0	MBOX1 moved to PCI Address 7C when Messaging Queue is enabled

Table 4-2. Register Differences between PCI 9080 and PCI 9060 (continued)

Register	PCI/Local Offset	Bits	Description
INTCSR	68/E8	3	Mailbox Interrupt Enable
		28	Mailbox 0 Interrupt Status
		29	Mailbox 1 Interrupt Status
		30	Mailbox 2 Interrupt Status
		31	Mailbox 3 Interrupt Status
PCIHIDR	70/F0	31:0	PCI Permanent Configuration ID register
PCIHREV	74/F4	7:0	PCI Permanent Revision ID register
DMAMODE0	80/100	13	Write and Invalidate Mode for DMA Channel 0 transfers
		13	DMA Write and Invalidate Mode
		14	DMA EOT[1:0]# (End of Transfer) Input Pin Enable
		15	DMA Stop Data Transfer Mode
		16	DMA Clear Count Mode
		17	DMA Interrupt Select
DMADPR0	90/110	0	DMA Descriptor Location Selector (PCI or Local)
DMAMODE1	94/114	13	DMA Write and Invalidate Mode
		14	DMA EOT[1:0]# (End of Transfer) Input Pin Enable
		15	DMA Stop Data Transfer Mode
		16	DMA Clear Count Mode
		17	DMA Interrupt Select
DMADPR1	A4/124	0	DMA Descriptor Location Selector (PCI or Local)
DMACSR0	A8/128	4	DMA Channel 0 Done
DMACSR1	A9/129	4	DMA Channel 1 Done
DMATHR	B0/130	15:0	Changed thresholds to accommodate 32-word Write FIFOs
OPQIS	30/B0	31:0	Outbound Post Queue Interrupt Status register
OPQIM	34/B4	31:0	Outbound Post Queue Interrupt Mask register
IQP	40	31:0	Inbound Queue Port
OQP	44	31:0	Outbound Queue Port
MQCR	C0/140	31:0	Messaging Queue Configuration register
QBAR	C4/144	31:0	Queue Base Address register
IFHPR	C8/148	31:0	Inbound Free Head Pointer register
IFTPR	CC/14C	31:0	Inbound Free Tail Pointer register
IPHPR	D0/150	31:0	Inbound Post Head Pointer register
IPTPR	D4/154	31:0	Inbound Post Tail Pointer register
OFHPR	D8/158	31:0	Outbound Free Head Pointer register
OFTPR	DC/15C	31:0	Outbound Free Tail Pointer register
OFHPR	E0/160	31:0	Outbound Post Head Pointer register
OPTPR	E4/164	31:0	Outbound Post Tail Pointer register
QSR	E8/168	7:0	Queue Status/Control register

Table 4-3. Register Differences between PCI 9080 and PCI 9060ES

Register	PCI/Local Offset	Bits	Description
PCIIDR	00/00	31:16	Default changed from PCI 906E to PCI 9080
PCISR	06/06	6	User-definable bit added
PCICLSR	0C/0C	7:0	Cache line size is now used for Memory Write and Invalidate
PCIBAR0	10/10	8:6	Register Bank size changed from 128 to 256
PCIBAR1	14/14	8:6	Register Bank size changed from 128 to 256
PCIBAR3	1C/1C	31:0	Base address register for Local Address Space 1
PCISVID	2C/2C	15:0	Subsystem Vendor ID register
PCISID	2E/2E	15:0	Subsystem ID register
MARBR	08, AC/88, 12C	20:19	DMA Channel Priority
		23	PCI Request Mode
		25	PCI Read/No Write Mode
		26	PCI Read with Write Flush Mode
		27	Get Local Bus Latency Timer with BREQ
BIGEND	0C/8C	28	PCI Read/No Flush Mode
		5	Direct Slave Big Endian Mode
		6	DMA Channel 1 Big Endian Mode
EROMBA	14/94	7	DMA Channel 0 Big Endian Mode
		5	BREQo Timer Resolution control
		LBRD0	18/98
15	Single Read Access Mode removed		
17:16	Local Bus width now programmable in S mode		
25	Extra Long Serial EEPROM Load		
DMPBAM	28/A8	12, 3	Direct Master Read Prefetch Size Control
		10, 8:5	Programmable Almost Full Flag increased by one bit
		11	Direct Master Prefetch Limit
		13	I/O Remap Slect
		15:14	Direct Master Write Delay
LAS1RR	F0/170	31:0	Local Address Space 1 Range register
LAS1BA	F4/174	31:0	Local Address Space 1 Local Base Address register (Remap)
LBRD1	F8/178	31:0	Local Address Space 1 Bus Region Descriptor register
MBOX0	40, 78/C0	31:0	MBOX0 moved to PCI Address 78 when the Messaging Queue is enabled
MBOX1	44, 7C/C4	31:0	MBOX1 moved to PCI Address 7C when the Messaging Queue is enabled
MBOX4	50/D0	31:0	MBOX4 added
MBOX5	54/D4	31:0	MBOX5 added
MBOX6	58/D8	31:0	MBOX6 added
MBOX7	5C/DC	31:0	MBOX7 added
P2LDBELL	60/E0	31:8	24 more Doorbell bits added to PCI-to-Local Doorbell register
L2PDBELL	64/E4	31:8	24 more Doorbell bits added to Local-to-PCI Doorbell register
INTCSR	68/E8	3	Mailbox Interrupt Enable

Table 4-3. Register Differences between PCI 9080 and PCI 9060ES (continued)

Register	PCI/Local Offset	Bits	Description
INTCSR	68/E8	18	DMA Channel 0 Interrupt Enable
		19	DMA Channel 1 Interrupt Enable
		21	DMA Channel 0 Interrupt Status
		22	DMA Channel 1 Interrupt Status
		25	DMA Channel 0 active during abort
		26	DMA Channel 1 active during abort
		28	Mailbox 0 Interrupt Status
		29	Mailbox 1 Interrupt Status
		30	Mailbox 2 Interrupt Status
		31	Mailbox 3 Interrupt Status
CNTRL	6C/EC	3:0	Read command for DMA
		7:4	Write command for DMA
PCIHREV	74/F4	7:0	PCI Permanent Revision ID register
DMAMODE0	80/100	31:0	DMA Channel 0 Mode register
DMAPADR0	84/104	31:0	DMA Channel 0 PCI Address register
DMALADR0	88/108	31:0	DMA Channel 0 Local Address register
DMASIZ0	8C/10C	31:0	DMA Channel 0 Size register
DMADPR0	90/110	31:0	DMA Channel 0 Descriptor Pointer register
DMAMODE1	94/114	31:0	DMA Channel 1 Mode register
DMAPADR1	98/108	31:0	DMA Channel 1 PCI Address register
DMALADR1	9C/11C	31:0	DMA Channel 1 Local Address register
DMASIZ1	A0/120	31:0	DMA Channel 1 Size register
DMADPR1	A4/124	31:0	DMA Channel 1 Descriptor Pointer register
DMACSR0	A8/128	7:0	DMA Channel 0 Command/Status
DMACSR1	A9/129	7:0	DMA Channel 1 Command/Status
DMATHR	B0/130	31:0	DMA Threshold register
OPQIS	30/B0	31:0	Outbound Post Queue Interrupt Status register
OPQIM	34/B4	31:0	Outbound Post Queue Interrupt Mask register
IQP	40	31:0	Inbound Queue Port
OQP	44	31:0	Outbound Queue Port
MQCR	C0/140	31:0	Messaging Queue Configuration register
QBAR	C4/144	31:0	Queue Base Address register
IFHPR	C8/148	31:0	Inbound Free Head Pointer register
IFTPR	CC/14C	31:0	Inbound Free Tail Pointer register
IPHPR	D0/150	31:0	Inbound Post Head Pointer register
IPTPR	D4/154	31:0	Inbound Post Tail Pointer register
OFHPR	D8/158	31:0	Outbound Free Head Pointer register
OFTPR	DC/15C	31:0	Outbound Free Tail Pointer register
OFHPR	E0/160	31:0	Outbound Post Head Pointer register
OPTPR	E4/164	31:0	Outbound Post Tail Pointer register
QSR	E8/168	7:0	Queue Status/Control register

Table 4-4. Register Differences between PCI 9080 and PCI 9060SD

Register	PCI/Local Offset	Bits	Description
PCIIDR	00/00	31:16	Default changed from PCI 906D to PCI 9080
PCISR	06/06	6	User-definable bit added
PCIBAR0	10/10	8:6	Register Bank size changed from 128 to 256
PCIBAR1	14/14	8:6	Register Bank size changed from 128 to 256
PCISVID	2C/2C	15:0	Subsystem Vendor ID register
PCISID	2E/2E	15:0	Subsystem ID register
MARBR	08, AC/88, 12C	31:0	Mode/Arbitration register now accessible from the PCI Bus
		23	PCI Request Mode
		28	PCI Read/No Flush Mode
BIGEND	0C/8C	1	Direct Master Big Endian Mode
		7	DMA Channel 0 Big Endian Mode
EROMBA	14/94	3:0	Direct Slave BREQo Delay Clocks
		4	Local Bus BREQo Enable
		5	BREQo Timer Resolution control
LBRD0	18/98	1:0	Local Bus width now programmable in S mode
		15	Single Read Access Mode removed
		17:16	Local Bus width now programmable in S mode
DMRR	1C/9C	31:16	Local Range register for Direct Master to PCI
DMLBAM	20/A0	31:0	Local Bus Base Address register for Direct Master to PCI Memory
DMLBAI	24/A4	31:0	Local Bus Base Address register for Direct Master to PCI IO/CFG
DMPBAM	28/A8	31:0	PCI Base Address (Remap) register for Direct Master to PCI Memory
LAS1RR	F0/170	31:0	Local Address Space 1 Range register was at 30/B0 in PCI 9060SD
LAS1BA	F4/174	31:0	Local Address Space 1 Local Base Address register (Remap) was at 34/B4 in PCI 9060SD
LBRD1	F8/178	31:0	Local Address Space 1 Bus Region Descriptor register was at 38/B8 in PCI 9060SD
LBRD1	F8/178	15	Single Read Access Mode removed
MBOX0	40,78/C0	31:0	MBOX0 moved to PCI Address 78 when the Messaging Queue is enabled
MBOX1	44, 7C/C4	31:0	MBOX1 moved to PCI Address 7C when the Messaging Queue is enabled
MBOX4	50/D0	31:0	MBOX4 added
MBOX5	54/D4	31:0	MBOX5 added
MBOX6	58/D8	31:0	MBOX6 added
MBOX7	5C/DC	31:0	MBOX7 added
INTCSR	68/E8	18	DMA Channel 0 Interrupt Enable
		21	DMA Channel 0 Interrupt Active
		24	Direct Master active during abort
		25	DMA Channel 0 active during abort
PCIHREV	74/F4	7:0	PCI Permanent Revision ID register

Table 4-4. Register Differences between PCI 9080 and PCI 9060SD (continued)

Register	PCI/Local Offset	Bits	Description
DMAMODE0	80/100	31:0	DMA Channel 0 Mode register
DMAADDR0	84/104	31:0	DMA Channel 0 PCI Address register
DMALADDR0	88/108	31:0	DMA Channel 0 Local Address register
DMASIZ0	8C/10C	31:0	DMA Channel 0 Transfer Size register
DMADPR0	90/110	31:0	DMA Channel 0 Descriptor Pointer register
DMACSR0	A8/128	7:0	DMA Channel 0 Command/Status register
DMATHR	B0/130	15:0	DMA Channel 0 Thresholds
OPQIS	30/B0	31:0	Outbound Post Queue Interrupt Status register
OPQIM	34/B4	31:0	Outbound Post Queue Interrupt Mask register
IQP	40	31:0	Inbound Queue Port
OQP	44	31:0	Outbound Queue Port
MQCR	C0/140	31:0	Messaging Queue Configuration register
QBAR	C4/144	31:0	Queue Base Address register
IFHPR	C8/148	31:0	Inbound Free Head Pointer register
IFTPR	CC/14C	31:0	Inbound Free Tail Pointer register
IPHPR	D0/150	31:0	Inbound Post Head Pointer register
IPTPR	D4/154	31:0	Inbound Post Tail Pointer register
OFHPR	D8/158	31:0	Outbound Free Head Pointer register
OFTPR	DC/15C	31:0	Outbound Free Tail Pointer register
OFHPR	E0/160	31:0	Outbound Post Head Pointer register
OPTPR	E4/164	31:0	Outbound Post Tail Pointer register
QSR	E8/168	7:0	Queue Status/Control register

4.2 Register Address Mapping

4.2.1 PCI Configuration Registers

Table 4-5. PCI Configuration Registers Description

PCI CFG Register Address	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.								PCI/Local Writable	Serial EEPROM Writable
		31	24	23	16	15	8	7	0		
00h	00h	Device ID				Vendor ID				Local	Y
04h	04h	Status				Command				Y	N
08h	08h	Class Code					Revision ID			Local	Y
0Ch	0Ch	BIST	Header Type		PCI Latency Timer		Cache Line Size		Y [15:0], Local	N	
10h	10h	PCI Base Address 0 for Memory-Mapped Configuration Registers (PCIBAR0)								Y	N
14h	14h	PCI Base Address 1 for I/O Mapped Configuration Registers (PCIBAR1)								Y	N
18h	18h	PCI Base Address 2 for Local Address Space 0 (PCIBAR2)								Y	N
1Ch	1Ch	PCI Base Address 3 for Local Address Space 1 (PCIBAR3)								Y	N
20h	20h	Unused Base Address (PCIBAR4)								N	N
24h	24h	Unused Base Address (PCIBAR5)								N	N
28h	28h	Cardbus CIS Pointer (Not Supported)								N	N
2Ch	2Ch	Subsystem ID				Subsystem Vendor ID				Local	Y
30h	30h	PCI Base Address for Local Expansion ROM								Y	Y
34h	34h	Reserved								N	N
38h	38h	Reserved								N	N
3Ch	3Ch	Max_Lat	Min_Gnt		Interrupt Pin		Interrupt Line		Y [7:0], Local	Y	

Note: Refer to PCI Specification v2.1 for definitions of these registers.

4.2.2 Local Configuration Registers

Table 4-6. Local Configuration Registers Description

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.		PCI/Local Writable	Serial EEPROM Writable
		31	0		
00h	80h	Range for PCI-to-Local Address Space 0		Y	Y
04h	84h	Local Base Address (Remap) for PCI-to-Local Address Space 0		Y	Y
08h	88h	Mode/Arbitration Register		Y	Y
0Ch	8Ch	Big/Little Endian Descriptor Register		Y	Y
10h	90h	Range for PCI-to-Local Expansion ROM		Y	Y
14h	94h	Local Base Address (Remap) for PCI-to-Local Expansion ROM and BREQo control		Y	Y
18h	98h	Local Bus Region Descriptors (Space 0 and Expansion ROM) for PCI-to-Local Accesses		Y	Y
1Ch	9Ch	Range for Direct Master to PCI		Y	Y
20h	A0h	Local Base Address for Direct Master to PCI Memory		Y	Y
24h	A4h	Local Base Address for Direct Master to PCI IO/CFG		Y	Y
28h	A8h	PCI Base Address (Remap) for Direct Master to PCI		Y	Y
2Ch	ACh	PCI Configuration Address Register for Direct Master to PCI IO/CFG		Y	Y
F0h	170h	Range for PCI-to-Local Address Space 1		Y	Y
F4h	174h	Local Base Address (Remap) for PCI-to-Local Address Space 1		Y	Y
F8h	178h	Local Bus Region Descriptor (Space 1) for PCI-to-Local Accesses		Y	Y

4.2.3 Runtime Registers

Table 4-7. Runtime Registers Description

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.		PCI/Local Writable	Serial EEPROM Writable
		31	0		
40h	C0h	Mailbox Register 0 (see Note)		Y	Y
44h	C4h	Mailbox Register 1 (see Note)		Y	Y
48h	C8h	Mailbox Register 2		Y	N
4Ch	CCh	Mailbox Register 3		Y	N
50h	D0h	Mailbox Register 4		Y	N
54h	D4h	Mailbox Register 5		Y	N
58h	D8h	Mailbox Register 6		Y	N
5Ch	DCh	Mailbox Register 7		Y	N
60h	E0h	PCI-to-Local Doorbell Register		Y	N
64h	E4h	Local-to-PCI Doorbell Register		Y	N
68h	E8h	Interrupt Control / Status		Y	N
6Ch	ECh	Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control		Y	N
70h	F0h	Device ID	Vendor ID	N	N
74h	F4h	Unused	Revision ID	N	N
78h	C0h	Mailbox Register 0 (see Note)		Y	N
7Ch	C4h	Mailbox Register (see Note)		Y	N

Note: Mailbox registers 0 and 1 are always accessible at addresses 78h/C0h and 7Ch/C4. When the I₂O feature is disabled (QSR[0]=0), Mailbox registers 0 and 1 are also accessible at PCI Addresses 40h and 44h for PCI 9060 compatibility. When the I₂O feature is enabled, the Inbound and Outbound Queue pointers are accessed at addresses 40h and 44h, replacing the Mailbox registers in PCI Address space.

4.2.4 DMA Registers

Table 4-8. DMA Registers Description

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.			PCI/Local Writable	Serial EEPROM Writable
		31		0		
80h	100h	DMA Ch 0 Mode			Y	N
84h	104h	DMA Ch 0 PCI Address			Y	N
88h	108h	DMA Ch 0 Local Address			Y	N
8Ch	10Ch	DMA Ch 0 Transfer Byte Count			Y	N
90h	110h	DMA Ch 0 Descriptor Pointer			Y	N
94h	114h	DMA Ch 1 Mode			Y	N
98h	118h	DMA Ch 1 PCI Address			Y	N
9Ch	11Ch	DMA Ch 1 Local Address			Y	N
A0h	120h	DMA Ch 1 Transfer Byte Count			Y	N
A4h	124h	DMA Ch 1 Descriptor Pointer			Y	N
A8h	128h	Reserved	DMA Channel 1 Command/Status Register	DMA Channel 0 Command/Status Register	Y	N
ACh	12Ch	Mode/Arbitration Register			Y	N
B0h	130h	DMA Threshold Register			Y	N

4.2.5 Messaging Queue Registers

Table 4-9. Messaging Queue Registers Description

PCI (Offset from Base Address)	Local Access (Offset from Chip Select Address)	To ensure software compatibility with other versions of the PCI 9080 family and to ensure compatibility with future enhancements, write 0 to all unused bits.		PCI/Local Writable	Serial EEPROM Writable
		31	0		
30h	B0h	Outbound Post Queue Interrupt Status		N	N
34h	B4h	Outbound Post Queue Interrupt Mask		Y	N
40h	—	Inbound Queue Port		PCI	N
44h	—	Outbound Queue Port		PCI	N
C0h	140h	Messaging Unit Configuration Register		Y	N
C4h	144h	Queue Base Address Register		Y	N
C8h	148h	Inbound Free Head Pointer Register		Y	N
CCh	14Ch	Inbound Free Tail Pointer Register		Y	N
D0h	150h	Inbound Post Head Pointer Register		Y	N
D4h	154h	Inbound Post Tail Pointer Register		Y	N
D8h	158h	Outbound Free Head Pointer Register		Y	N
DCh	15Ch	Outbound Free Tail Pointer Register		Y	N
E0h	160h	Outbound Post Head Pointer Register		Y	N
E4h	164h	Outbound Post Tail Pointer Register		Y	N
E8h	168h	Queue Status/Control Register		Y	N

Notes: When I_2O messaging is enabled ($QSR[0]=1$), the PCI Master (Host or another IOP) uses the Inbound Queue Port to read Message Frame Addresses (MFAs) from the Inbound Free List FIFO and to write MFAs to the Inbound Post List FIFO. The PCI Master (Host or another IOP) uses the Outbound Queue Port to read MFAs from the Outbound Post List FIFO and to write MFAs to the Outbound Free List FIFO.

Each Inbound MFA is specified by I_2O as offset from PCI Base Address 0 (programmed in register PCIBAR0 at offset 10h) to start of message frame. This means that all inbound message frames should reside in PCI Base Address 0 memory space.

Each Outbound Message Frame Address (MFA) is specified by I_2O as offset from system address 0x00000000h. The Outbound MFA is the physical 32-bit address of a frame in shared PCI system memory.

The Inbound and Outbound Queues may reside in Local Address Space 0 or 1 by programming the QSR register. The queues need not be in shared memory.

4.3 PCI Configuration Registers

All registers may be written to or read from in Byte, Word, or Lword accesses.

4.3.1 (PCIIDR; PCI:00h, LOC:00h) PCI Configuration ID Register

Table 4-10. (PCIIDR; PCI:00h, LOC:00h) PCI Configuration ID Register Description

Bit	Description	Read	Write	Value after Reset
15:0	Vendor ID. Identifies device manufacturer. Defaults to PCI SIG issued vendor ID of PLX (10B5h) if no serial EEPROM is present and pin NB# (no Local Bus initialization) is asserted low.	Yes	Local/ Serial EEPROM	10B5h or 0
31:16	Device ID. Identifies particular device. Defaults to PLX part number for PCI interface chip (PCI 9080) if no serial EEPROM is present and pin NB# (no Local Bus initialization) is asserted low.	Yes	Local/ Serial EEPROM	9080h or 0

4.3.2 (PCICR; PCI:04h, LOC:04h) PCI Command Register

Table 4-11. (PCICR; PCI:04h, LOC:04h) PCI Command Register Description

Bit	Description	Read	Write	Value after Reset
0	I/O Space. Value of 1 allows device to respond to I/O Space accesses. Value of 0 disables device from responding to I/O Space accesses.	Yes	Yes	0
1	Memory Space. Value of 1 allows device to respond to Memory Space accesses. Value of 0 disables device from responding to Memory Space accesses.	Yes	Yes	0
2	Master Enable. Value of 1 allows device to behave as Bus Master. Value of 0 disables device from generating Bus Master accesses. This bit must be set for the PCI 9080 to perform Direct Master or DMA cycles.	Yes	Yes	0
3	Special Cycle. Not supported.	Yes	No	0
4	Memory Write and Invalidate. Value of 1 enables Memory Write and Invalidate. Value of 0 disables Memory Write and Invalidate. (Refer to DMA Mode Registers for Direct Master, DMAMODE0, and DMAMODE1[13], as well as (DMPBAM[13], DMAMODE0[13], and DMAMODE1[13], respectively).	Yes	Yes	0
5	VGA Palette Snoop. Not supported.	Yes	No	0
6	Parity Error Response. Value of 0 indicates parity error is ignored and operation continues. Value of 1 indicates parity checking is enabled.	Yes	Yes	0
7	Wait Cycle Control. Controls whether device performs address/data stepping. Value of 0 indicates device never does stepping. Value of 1 indicates device always does stepping. Note: <i>Hardcoded to 0.</i>	Yes	No	0
8	SERR# Enable. Value of 1 enables SERR# driver. Value of 0 disables SERR# driver.	Yes	Yes	0
9	Fast Back-to-Back Enable. Indicates type of fast back-to-back transfers Master can perform on bus. Value of 1 indicates fast back-to-back transfers can occur to any agent on bus. Value of 0 indicates fast back-to-back transfers can only occur to same agent as previous cycle.	Yes	No	0
15:10	Reserved.	Yes	No	0

4.3.3 (PCISR; PCI:06h, LOC:06h) PCI Status Register

Table 4-12. (PCISR; PCI:06h, LOC:06h) PCI Status Register Description

Bit	Description	Read	Write	Value after Reset
5:0	Reserved.	Yes	No	0
6	If high, supports User Definable Features. This bit can only be written from the Local Bus. Read-only from the PCI Bus.	Yes	Local	0
7	Fast Back-to-Back Capable. When set to 1, indicates adapter can accept fast back-to-back transactions. Value of 0 indicates adapter cannot.	Yes	No	1
8	Master Data Parity Error Detected. This bit is set to 1 when three conditions are met: 1) The PCI 9080 asserted PERR# itself or observed PERR# asserted; 2) The PCI 9080 was Bus Master for operation in which error occurred; 3) Parity Error Response bit in Command Register is set. Writing 1 clears the bit (0).	Yes	Yes/Clr	0
10:9	DEVSEL Timing. Indicates timing for DEVSEL# assertion. Value of 01 indicates medium decode. <i>Note: Hardcoded to 01.</i>	Yes	No	01
11	Target Abort. When set to 1, indicates the PCI 9080 has signaled a Target abort. Writing a 1 clears the bit (0).	Yes	Yes/Clr	0
12	Received Target Abort. When set to 1, indicates the PCI 9080 has received Target abort signal. Writing a 1 clears the bit (0).	Yes	Yes/Clr	0
13	Master Abort. When set to 1, indicates the PCI 9080 has generated Master abort signal. Writing a 1 clears the bit (0).	Yes	Yes/Clr	0
14	Signaled System Error. When set to 1, indicates the PCI 9080 has reported a system error on SERR# signal. Writing a 1 clears the bit (0).	Yes	Yes/Clr	0
15	Detected Parity Error. When set to 1, indicates the PCI 9080 has detected a PCI Bus parity error, even if parity error handling is disabled (Parity Error Response bit in Command register is clear). One of three conditions can cause this bit to be set. 1) The PCI 9080 detected parity error during PCI Address phase; 2) The PCI 9080 detected a data parity error when it was Target of a write; 3) The PCI 9080 detected a data parity error when performing Master Read operation. Writing a 1 clears the bit (0).	Yes	Yes/Clr	0

4.3.4 (PCIREV; PCI:08h, LOC:08h) PCI Revision ID Register

Table 4-13. (PCIREV; PCI:08h, LOC:08h) PCI Revision ID Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Revision ID. Silicon revision of the PCI 9080.	Yes	Local/ Serial EEPROM	Current Rev #

4.3.5 (PCICCR; PCI:09-0Bh, LOC:09-0Bh) PCI Class Code Register

Table 4-14. (PCICCR; PCI:09-0Bh, LOC:09-0Bh) PCI Class Code Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Register Level Programming Interface. 00h = Queue Ports at 40h and 44h. 01h = Queue Ports at 40h and 44h, and Int Status and Int Mask at 30h and 34h, respectively.	Yes	Local/ Serial EEPROM	00
15:8	Subclass Code. 80h = Other Bridge Device, 00h = I ₂ O Device.	Yes	Local/ Serial EEPROM	80h
23:16	Base Class Code. 06h = Bridge Device, 0Eh = I ₂ O controller.	Yes	Local/ Serial EEPROM	06h

4.3.6 (PCICLSR; PCI:0Ch, LOC:0Ch) PCI Cache Line Size Register

Table 4-15. (PCICLSR; PCI:0Ch, LOC:0Ch) PCI Cache Line Size Register Description

Bit	Description	Read	Write	Value after Reset
7:0	System cache line size in units of 32-bit words.	Yes	Yes	0

4.3.7 (PCILTR; PCI:0Dh, LOC:0Dh) PCI Latency Timer Register

Table 4-16. (PCILTR; PCI:0Dh, LOC:0Dh) PCI Latency Timer Register Description

Bit	Description	Read	Write	Value after Reset
7:0	PCI Latency Timer. Units of PCI Bus clocks that specify amount of time the PCI 9080, as a Bus Master, can burst data on the PCI Bus.	Yes	Yes	0

4.3.8 (PCIHTR; PCI:0Eh, LOC:0Eh) PCI Header Type Register

Table 4-17. (PCIHTR; PCI:0Eh, LOC:0Eh) PCI Header Type Register Description

Bit	Description	Read	Write	Value after Reset
6:0	Configuration Layout Type. Specifies layout of bits 10h through 3Fh in configuration space. Only one encoding 0 is defined. All other encodings are reserved.	Yes	Local	0
7	Header Type. Value of 1 indicates multiple functions. Value of 0 indicates single function.	Yes	Local	0

4.3.9 (PCIBISTR; PCI:0Fh, LOC:0Fh) PCI Built-In Self Test (BIST) Register

Table 4-18. (PCIBISTR; PCI:0Fh, LOC:0Fh) PCI Built-In Self Test (BIST) Register Description

Bit	Description	Read	Write	Value after Reset
3:0	Value of 0 indicates device passed its test. Nonzero values indicate device failed. Device specific failure codes can be encoded in nonzero value.	Yes	Local	0
5:4	Reserved. Device returns 0.	Yes	No	0
6	PCI writes 1 to invoke BIST. Generates interrupt to Local Bus. Local Bus resets the bit when BIST is complete. Software should fail device if BIST is not complete after two seconds. Refer to Runtime registers for interrupt control/status.	Yes	Yes	0
7	Returns 1 if device supports BIST. Returns 0 if device is not BIST compatible.	Yes	Local	0

4.3.10 (PCIBAR0; PCI:10h, LOC:10h) PCI Base Address Register for Memory Accesses to Local, Runtime, and DMA Registers

Table 4-19. (PCIBAR0; PCI:10h, LOC:10h) PCI Base Address Register for Memory Accesses to Local, Runtime, and DMA Registers Description

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into memory space. Value of 1 indicates register maps into I/O space. Note: <i>Hardcoded to 0.</i>	Yes	No	0
2:1	Location of Register. Location values: 00—Locate anywhere in 32-bit memory address space 01—Locate below 1 MB memory address space 10—Locate anywhere in 64-bit memory address space 11—Reserved Note: <i>Hardcoded to 0.</i>	Yes	No	0
3	Prefetchable. Value of 1 indicates there are no side effects on reads. Does not affect operation of the PCI 9080. Note: <i>Hardcoded to 0.</i>	Yes	No	0
7:4	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers (default is 256 bytes). Note: <i>Hardcoded to 0.</i>	Yes	No	0
31:8	Memory Base Address. Memory base address for access to Local, Runtime, and DMA registers.	Yes	Yes	0

Note: For I₂O, Inbound message frame pool must reside in address space pointed to by PCIBAR0. Message Frame Address (MFA) is defined by I₂O as offset from this base address to start of message frame.

4.3.11 (PCIBAR1; PCI:14h, LOC:14h) PCI Base Address Register for I/O Accesses to Local, Runtime, and DMA Registers

Table 4-20. (PCIBAR1; PCI:14h, LOC:14h) PCI Base Address Register for I/O Accesses to Local, Runtime, and DMA Registers Description

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into memory space. Value of 1 indicates register maps into I/O space. <i>Note:</i> Hardcoded to 1.	Yes	No	1
1	Reserved.	Yes	No	0
7:2	I/O Base Address. Base Address for I/O access to Local, Runtime, and DMA registers. (Default is 256 bytes) <i>Note:</i> Hardcoded to 0.	Yes	No	0
31:8	I/O Base Address. Base Address for I/O access to Local, Runtime, and DMA registers.	Yes	Yes	0

4.3.12 (PCIBAR2; PCI:18h, LOC:18h) PCI Base Address Register for Memory Accesses to Local Address Space 0

Table 4-21. (PCIBAR2; PCI:18h, LOC:18h) PCI Base Address Register for Memory Accesses to Local Address Space 0 Description

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into memory space. Value of 1 indicates register maps into I/O space. (Specified in LASORR register.)	Yes	No	0
2:1	Location of Register (If Memory Space). Location values: 00—Locate anywhere in 32-bit memory address space 01—Locate below 1-MB memory address space 10—Locate anywhere in 64-bit memory address space 11—Reserved (Specified in LASORR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: No for bit 1, Yes for bit 2	0
3	Prefetchable (If Memory Space). Value of 1 indicates there are no side effects on reads. Reflects value of LASORR[3] and provides only status to system. Does not affect operation of the PCI 9080. The prefetching features of this address space are controlled by the associated Bus Region Descriptor register. (Specified in LASORR register.) If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Memory Base Address. Memory base address for access to Local Address Space 0.	Yes	Yes	0

Note: PCIBAR2 can be enabled or disabled by setting or clearing LAS0BA[0].

4.3.13 (PCIBAR3; PCI:1Ch, LOC:1Ch) PCI Base Address Register for Memory Accesses to Local Address Space 1

Table 4-22. (PCIBAR3; PCI:1Ch, LOC:1Ch) PCI Base Address Register for Memory Accesses to Local Address Space 1 Description

Bit	Description	Read	Write	Value after Reset
0	Memory Space Indicator. Value of 0 indicates register maps into memory space. Value of 1 indicates register maps into I/O space. (Specified in LAS1RR register.)	Yes	No	0
2:1	Location of register. Location values: 00—Locate anywhere in 32-bit memory address space 01—Locate below 1-MB memory address space 10—Locate anywhere in 64-bit memory address space 11—Reserved (Specified in LAS1RR register.) If I/O Space, bit 1 is always 0 and bit 2 is included in the base address.	Yes	Mem: No I/O: No for bit 1, Yes for bit 2	0
3	Prefetchable (If Memory Space). Value of 1 indicates there are no side effects on reads. Reflects value of LAS1RR[3] and only provides status to the system. Does not affect operation of the PCI 9080. The prefetching features of this address space are controlled by the associated Bus Region Descriptor register. (Specified in LAS1RR register.) If I/O Space, bit 3 is included in the base address.	Yes	Mem: No I/O: Yes	0
31:4	Memory Base Address. Memory base address for access to Local Address Space 1.	Yes	Yes	0

Note: PCIBAR3 can be enabled or disabled by setting or clearing LAS1BA[0]. If QSR[0] is set, PCIBAR3 returns 0.

4.3.14 (PCIBAR4; PCI:20h, LOC:20h) PCI Base Address Register

Table 4-23. (PCIBAR4; PCI:20h, LOC:20h) PCI Base Address Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Reserved.	Yes	No	0

4.3.15 (PCIBAR5; PCI:24h, LOC:24h) PCI Base Address Register

Table 4-24. (PCIBAR5; PCI:24h, LOC:24h) PCI Base Address Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Reserved.	Yes	No	0

4.3.16 (PCICIS; PCI:28h, LOC:28h) PCI Cardbus CIS Pointer Register

Table 4-25. (PCICIS; PCI:28h, LOC:28h) PCI Cardbus CIS Pointer Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Cardbus Information Structure Pointer for PCMCIA. Not supported.	Yes	No	0

4.3.17 (PCISVID; PCI:2Ch, LOC:2Ch) PCI Subsystem Vendor ID Register

Table 4-26. (PCISVID; PCI:2Ch, LOC:2Ch) PCI Subsystem Vendor ID Register Description

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem Vendor ID (unique add-in board Vendor ID).	Yes	Local/ Serial EEPROM	10B5

4.3.18 (PCISID; PCI:2Eh, LOC:2Eh) PCI Subsystem ID Register

Table 4-27. (PCISID; PCI:2Eh, LOC:2Eh) PCI Subsystem ID Register Description

Bit	Description	Read	Write	Value after Reset
15:0	Subsystem ID (unique add-in board Device ID).	Yes	Local/ Serial EEPROM	9080h

4.3.19 (PCIERBAR; PCI:30h, LOC:30h) PCI Expansion ROM Base Register

Table 4-28. (PCIERBAR; PCI:30h, LOC:30h) PCI Expansion ROM Base Register Description

Bit	Description	Read	Write	Value after Reset
0	Address Decode Enable. Value of 1 indicates device accepts accesses to Expansion ROM address. Value of 0 indicates device does not accept accesses to Expansion ROM space. Should be set to 1 by PCI Host if Expansion ROM is present.	Yes	Yes	0
10:1	Reserved.	Yes	No	0
31:11	Expansion ROM Base Address (upper 21 bits).	Yes	Yes	0

4.3.20 (PCIILR; PCI:3Ch, LOC:3Ch) PCI Interrupt Line Register

Table 4-29. (PCIILR; PCI:3Ch, LOC:3Ch) PCI Interrupt Line Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Line Routing Value. Indicates which input of system interrupt controller(s) to which the interrupt line of device is connected.	Yes	Yes	0

4.3.21 (PCIIPR; PCI:3Dh, LOC:3Dh) PCI Interrupt Pin Register

Table 4-30. (PCIIPR; PCI:3Dh, LOC:3Dh) PCI Interrupt Pin Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Interrupt Pin Register. Indicates which interrupt pin device uses. The following values are decoded: 0 = No Interrupt Pin 1 = INTA# 2 = INTB# 3 = INTC# 4 = INTD# Note: The PCI 9080 supports only one PCI interrupt pin (INTA#).	Yes	Local/ Serial EEPROM	1

4.3.22 (PCIMGR; PCI:3Eh, LOC:3Eh) PCI Min_Gnt Register

Table 4-31. (PCIMGR; PCI:3Eh, LOC:3Eh) PCI Min_Gnt Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Min_Gnt. Specifies how long a burst period device needs, assuming clock rate of 33 MHz. Value is multiple of 1/4 μ s increments.	Yes	Local/ Serial EEPROM	0

4.3.23 (PCIMLR; PCI:3Fh, LOC:3Fh) PCI Max_Lat Register

Table 4-32. (PCIMLR; PCI:3Fh, LOC:3Fh) PCI Max_Lat Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Max_Lat. Specifies how often device must gain access to PCI Bus. Value is multiple of 1/4 μ s increments.	Yes	Local/ Serial EEPROM	0

4.4 Local Configuration Registers

4.4.1 (LAS0RR; PCI:00h, LOC:80h) Local Address Space 0 Range Register for PCI-to-Local Bus

Table 4-33. (LAS0RR; PCI:00h, LOC:80h) Local Address Space 0 Range Register for PCI-to-Local Bus Description

Bit	Description	Read	Write	Value after Reset										
0	Memory Space Indicator. Value of 0 indicates Local address Space 0 maps into PCI memory space. Value of 1 indicates address Space 0 maps into PCI I/O space.	Yes	Yes	0										
2:1	If mapped into memory space, encoding is as follows: <table border="1"> <thead> <tr> <th>2/1</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>Locate anywhere in 32-bit PCI Address space</td> </tr> <tr> <td>0 1</td> <td>Locate below 1 MB in PCI Address space</td> </tr> <tr> <td>1 0</td> <td>Locate anywhere in 64-bit PCI Address space</td> </tr> <tr> <td>1 1</td> <td>Reserved</td> </tr> </tbody> </table> If mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [31:3] to indicate decoding range.	2/1	Meaning	0 0	Locate anywhere in 32-bit PCI Address space	0 1	Locate below 1 MB in PCI Address space	1 0	Locate anywhere in 64-bit PCI Address space	1 1	Reserved	Yes	Yes	0
2/1	Meaning													
0 0	Locate anywhere in 32-bit PCI Address space													
0 1	Locate below 1 MB in PCI Address space													
1 0	Locate anywhere in 64-bit PCI Address space													
1 1	Reserved													
3	If mapped into memory space, value of 1 indicates reads are prefetchable (does not affect operation of the PCI 9080, but is used for system status). If mapped into I/O space, included with bits [31:2] to indicate decoding range.	Yes	Yes	0										
31:4	Specifies which PCI Address bits to use for decoding PCI access to Local Bus Space 0. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits to be included in decode and 0 to all others (used in conjunction with PCI Configuration register 18h). Default is 1 MB.	Yes	Yes	FFF0000h										

Notes: Range (*not* Range register) must be power of 2. "Range register value" is inverse of range.

User should limit all I/O spaces to 256 bytes per PCI Specification v2.1.

4.4.2 (LAS0BA; PCI:04h, LOC:84h) Local Address Space 0 Local Base Address (Remap) Register

Table 4-34. (LAS0BA; PCI:04h, LOC:84h) Local Address Space 0 Local Base Address (Remap) Register Description

Bit	Description	Read	Write	Value after Reset
0	Space 0 Enable. Value of 1 enables decoding of PCI Addresses for Direct Slave access to Local Space 0. Value of 0 disables decoding. If set to 0, PCI BIOS may not allocate (assign) base address for Space 0. Note: Must be set to 1 for any Direct Slave access to Space 0.	Yes	Yes	0
1	Reserved.	Yes	No	0
3:2	If Local Space 0 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits [31:4] for remapping.	Yes	Yes	0
31:4	Remap of PCI Address to Local Address Space 0 into a Local Address Space. Remap (replace) PCI Address bits used in decode as Local Address bits.	Yes	Yes	0

Note: Remap Address value must be multiple of Range (*not* Range register).

4.4.3 (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/Arbitration Register

Table 4-35. (MARBR; PCI:08h or ACh, LOC:88h or 12Ch) Mode/Arbitration Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Local Bus Latency Timer. Number of Local Bus Clock cycles before de-asserting HOLD and releasing the Local Bus. Also used with bit 27 to delay BREQ input to give up the Local Bus only when this timer expires.	Yes	Yes	00
15:8	Local Bus Pause Timer. Number of Local Bus Clock cycles before reasserting HOLD after releasing the Local Bus. <i>Note:</i> Applicable only to DMA operation.	Yes	Yes	00
16	Local Bus Latency Timer Enable. Value of 1 enables latency timer.	Yes	Yes	0
17	Local Bus Pause Timer Enable. Value of 1 enables pause timer.	Yes	Yes	0
18	Local Bus BREQ Enable. Value of 1 enables Local Bus BREQ input. When BREQ input is active, the PCI 9080 de-asserts HOLD and releases Local Bus.	Yes	Yes	0
20:19	DMA Channel Priority. Value of 00 indicates rotational priority scheme. Value of 01 indicates Channel 0 has priority. Value of 10 indicates Channel 1 has priority. Value of 11 is reserved.	Yes	Yes	0
21	Local Bus Direct Slave Give up Bus Mode. When set to 1, the PCI 9080 de-asserts HOLD and releases the Local Bus when the Direct Slave Write FIFO becomes empty during a Direct Slave Write or when the Direct Slave Read FIFO becomes full during a Direct Slave Read.	Yes	Yes	1
22	Direct Slave LLOCKo# Enable. Value of 1 enables PCI Direct Slave locked sequences. Value of 0 disables Direct Slave locked sequences.	Yes	Yes	0
23	PCI Request Mode. Value of 1 causes the PCI 9080 to de-assert REQ when it asserts FRAME during a Master cycle. Value of 0 causes the PCI 9080 to leave REQ asserted for the entire Bus Master cycle.	Yes	Yes	0
24	PCI Specification v2.1 Mode. When set to 1, the PCI 9080 operates in Delayed Transaction mode for Direct Slave Reads. The PCI 9080 issues a Retry and prefetches Read data.	Yes	Yes	0
25	PCI Read No Write Mode. Value of 1 forces Retry on Writes if Read is pending. Value of 0 allows Writes to occur while Read is pending.	Yes	Yes	0
26	PCI Read with Write Flush Mode. Value of 1 submits request to flush pending a Read cycle if a Write cycle is detected. Value of 0 submits request to not effect pending Reads when a Write cycle occurs (PCI Specification v2.1 compatible).	Yes	Yes	0
27	Gate Local Bus Latency Timer with BREQ. If set to 0, the PCI 9080 gives up the Local Bus during Direct Slave or DMA transfer after the current cycle (if enabled and BREQ is sampled). If set to 1, the PCI 9080 gives up the Local Bus only if BREQ is sampled and the Local Bus Latency Timer is enabled and expired during a Direct Slave or DMA transfer.	Yes	Yes	0
28	PCI Read No Flush Mode. Value of 1 submits a request to not flush the Read FIFO if a PCI Read cycle completes (Read Ahead mode). Value of 0 submits a request to flush the Read FIFO if a PCI Read cycle completes.	Yes	Yes	0
29	If set to 0, reads from PCI Configuration register address 00h and returns Device ID and Vendor ID. If set to 1, reads from PCI Configuration Register address 00h and returns Subsystem ID and Subsystem Vendor ID.	Yes	Yes	0
31:30	Reserved.	Yes	No	0

4.4.4 (BIGEND; PCI:0Ch, LOC:8Ch) Big/Little Endian Descriptor Register

Table 4-36. (BIGEND; PCI:0Ch, LOC:8Ch) Big/Little Endian Descriptor Register Description

Bit	Description	Read	Write	Value after Reset
0	Configuration Register Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Local accesses to the Configuration registers. Value of 0 specifies Little Endian ordering. Big Endian mode can be specified for Configuration Register accesses by asserting BIGEND# pin during Address phase of access.	Yes	Yes	0
1	Direct Master Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Master accesses. Value of 0 specifies Little Endian ordering. Big Endian mode can be specified for Direct Master accesses by asserting the BIGEND# input pin during Address phase of access.	Yes	Yes	0
2	Direct Slave Address Space 0 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 0. Value of 0 specifies Little Endian ordering.	Yes	Yes	0
3	Direct Slave Address Expansion ROM 0 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Expansion ROM. Value of 0 specifies Little Endian ordering.	Yes	Yes	0
4	Big Endian Byte Lane Mode. Value of 1 specifies that in Big Endian mode, use byte lanes [31:16] for 16-bit Local Bus and byte lanes [31:24] for 8-bit Local Bus. Value of 0 specifies that in Big Endian mode, byte lanes [15:0] be used for 16-bit Local Bus and byte lanes [7:0] for 8-bit Local Bus.	Yes	Yes	0
5	Direct Slave Address Space 1 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for Direct Slave accesses to Local Address Space 1. Value of 0 specifies Little Endian ordering.	Yes	Yes	0
6	DMA Channel 1 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for DMA Channel 1 accesses to the Local Address Space. Value of 0 specifies Little Endian ordering.	Yes	Yes	0
7	DMA Channel 0 Big Endian Mode. Value of 1 specifies use of Big Endian data ordering for DMA Channel 0 accesses to the Local Address Space. Value of 0 specifies Little Endian ordering.	Yes	Yes	0
31:8	Reserved.	Yes	No	0

4.4.5 (EROMRR; PCI:10h, LOC:90h) Expansion ROM Range Register

Table 4-37. (EROMRR; PCI:10h, LOC:90h) Expansion ROM Range Register Description

Bit	Description	Read	Write	Value after Reset
10:0	Reserved.	Yes	No	0
31:11	Specifies which PCI Address bits to use for decoding PCI-to-Local Bus Expansion ROM. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits to be included in decode and 0 to all others (used in conjunction with PCI Configuration register 30h). Default is 64 KB.	Yes	Yes	FFFF00h

Note: Range (*not* Range register) must be power of 2. "Range register value" is inverse of range.

4.4.6 (EROMBA; PCI:14h, LOC:94h) Expansion ROM Local Base Address (Remap) Register and BREQo Control

Table 4-38. (EROMBA; PCI:14h, LOC:94h) Expansion ROM Local Base Address (Remap) Register and BREQo Control Description

Bit	Description	Read	Write	Value after Reset
3:0	Direct Slave BREQo (Backoff Request Out) Delay Clocks. Number of Local Bus clocks in which Direct Slave HOLD request is pending and a Local Direct Master access is in progress and not being granted the bus (LHOLDA) before asserting BREQo. Once asserted, BREQo remains asserted until the PCI 9080 receives LHOLDA (LSB = 8 or 64 clocks).	Yes	Yes	0
4	Local Bus BREQo Enable. Value of 1 enables the PCI 9080 to assert BREQo output.	Yes	Yes	0
5	BREQo Timer-Resolution. Value of 1 changes LSB of the BREQo timer from 8 to 64 clocks.	Yes	Yes	0
10:6	Reserved.	Yes	No	0
31:11	Remap of PCI Expansion ROM Space into a Local Address Space. Remap (replace) PCI Address bits used in decode as Local Address bits.	Yes	Yes	0

Note: Remap Address value must be multiple of Range (*not* Range register).

4.4.7 (LBRD0; PCI:18h, LOC:98h) Local Address Space 0/Expansion ROM Bus Region Descriptor Register

Table 4-39. (LBRD0; PCI:18h, LOC:98h) Local Address Space 0/Expansion ROM Bus Region Descriptor Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Memory Space 0 Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11
5:2	Memory Space 0 Internal Wait States (data to data; 0-15 wait states).	Yes	Yes	0
6	Memory Space 0 Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0
7	Memory Space 0 BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI 9080 bursts four Lword maximum at a time.	Yes	Yes	0
8	Memory Space 0 Prefetch Disable. If mapped into memory space, value of 0 enables Read prefetching. Value of 1 disables prefetching. If prefetching is disabled, the PCI 9080 disconnects after each memory read.	Yes	Yes	0
9	Expansion ROM Space Prefetch Disable. Value of 0 enables Read prefetching. Value of 1 disables prefetching. If prefetching is disabled, the PCI 9080 disconnects after each memory read.	Yes	Yes	0
10	Read Prefetch Count Enable. When set to 1 and memory prefetching is enabled, the PCI 9080 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9080 ignores the count and continues prefetching until terminated by PCI Bus.	Yes	Yes	0
14:11	Prefetch Counter. Number of Lwords to prefetch during Memory Read cycles (0-15). Count of zero selects prefetch of 16 Lwords.	Yes	Yes	0
15	Reserved.	Yes	No	0
17:16	Expansion ROM Space Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11
21:18	Expansion ROM Space Internal Wait States (data to data; 0-15 wait states).	Yes	Yes	0
22	Expansion ROM Space Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0
23	Expansion ROM Space Bterm Input Enable. Value of 1 enables BTERM# input. Value of 0 disables Bterm input. If set to 0, the PCI 9080 bursts four Lword maximum at a time.	Yes	Yes	0
24	Memory Space 0 Burst Enable. Value of 1 enables bursting. Value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0
25	Extra Long Load from Serial EEPROM. Value of 1 loads Subsystem ID and Local Address Space 1 registers. Value of 0 indicates not to load them.	Yes	No	0
26	Expansion ROM Space Burst Enable. Value of 1 enables bursting. Value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0
27	Direct Slave PCI Write Mode. Value of 0 indicates the PCI 9080 should disconnect when the Direct Slave Write FIFO is full. Value of 1 indicates the PCI 9080 should de-assert TRDY# when the Write FIFO is full.	Yes	Yes	0
31:28	PCI Target Retry Delay Clocks. Contains value (multiplied by 8) of the number of PCI Bus clocks after receiving PCI -to-Local Read or Write access and not successfully completing a transfer. Only pertains to Direct Slave Writes when bit 27 is set to 1.	Yes	Yes	4 (32 clocks)

4.4.8 (DMRR; PCI:1Ch, LOC:9Ch) Local Range Register for Direct Master to PCI

Table 4-40. (DMRR; PCI:1Ch, LOC:9Ch) Local Range Register for Direct Master to PCI Description

Bit	Description	Read	Write	Value after Reset
15:0	Reserved (64 KB increments).	Yes	No	0
31:16	Specifies which Local Address bits to use for decoding Local-to-PCI Bus access. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others. Used for Direct Master Memory, I/O, or Configuration accesses.	Yes	Yes	0

Note: Range (*not* Range register) must be power of 2. "Range register value" is inverse of range.

4.4.9 (DMLBAM; PCI:20h, LOC:A0h) Local Bus Base Address Register for Direct Master to PCI Memory

Table 4-41. (DMLBAM; PCI:20h, LOC:A0h) Local Bus Base Address Register for Direct Master to PCI Memory Description

Bit	Description	Read	Write	Value after Reset
15:0	Reserved.	Yes	No	0
31:16	Assigns value to bits to use for decoding Local-to-PCI Memory access.	Yes	Yes	0

Note: Local Base Address value must be multiple of Range (*not* Range register).

4.4.10 (DMLBAI; PCI:24h, LOC:A4h) Local Base Address Register for Direct Master to PCI IO/CFG

Table 4-42. (DMLBAI; PCI:24h, LOC:A4h) Local Base Address Register for Direct Master to PCI IO/CFG Description

Bit	Description	Read	Write	Value after Reset
15:0	Reserved.	Yes	No	0
31:16	Assigns value to bits to use for decoding Local-to-PCI I/O or Configuration access. Used for Direct Master I/O and Configuration accesses.	Yes	Yes	0

Notes: Local Base Address value must be multiple of Range (*not* Range register).

Refer to DMPBAM[13] for I/O Remap Address option.

4.4.11 (DMPBAM; PCI:28h, LOC:A8h) PCI Base Address (Remap) Register for Direct Master to PCI Memory

Table 4-43. (DMPBAM; PCI:28h, LOC:A8h) PCI Base Address (Remap) Register for Direct Master to PCI Memory Description

Bit	Description	Read	Write	Value after Reset
0	Direct Master Memory Access Enable. Value of 1 enables decode of Direct Master Memory accesses. Value of 0 disables decode of Direct Master Memory accesses.	Yes	Yes	0
1	Direct Master I/O Access Enable. Value of 1 enables decode of Direct Master I/O accesses. Value of 0 disables decode of Direct Master I/O accesses.	Yes	Yes	0
2	LLOCK# Input Enable. Value of 1 enables LLOCK# input, enabling PCI-locked sequences. Value of 0 disables LLOCK# input.	Yes	Yes	0
12, 3	Direct Master Read Prefetch Size control. Values: 00 = The PCI 9080 continues to prefetch Read data from the PCI Bus until the Direct Master access is finished. May result in additional four unneeded Lwords being prefetched from the PCI Bus. 01 = Prefetch up to four Lwords from the PCI Bus 10 = Prefetch up to eight Lwords from the PCI Bus 11 = Prefetch up to 16 Lwords from the PCI Bus If PCI memory prefetch is not wanted, performs Direct Master Single cycle. Direct Master Burst reads must not exceed programmed limit.	Yes	Yes	00
4	Direct Master PCI Read Mode. Value of 0 indicates the PCI 9080 should release PCI Bus when the Read FIFO becomes full. Value of 1 indicates the PCI 9080 should keep PCI Bus and de-assert IRDY when the Read FIFO becomes full.	Yes	Yes	0
10, 8:5	Programmable Almost Full Flag. When the number of entries in the 32-word Direct Master Write FIFO exceeds this value, output pin DMPAF# is asserted low.	Yes	Yes	000
9	Write and Invalidate Mode. When set to 1, the PCI 9080 waits for 8 or 16 Lwords to be written from the Local Bus before starting PCI access. When set, all Local Direct Master to PCI Write accesses must be 8- or 16-Lword bursts. Use in conjunction with PCICR[4] and Section 3.6.1.9.2, "Direct Master Write and Invalidate").	Yes	Yes	0
11	Direct Master Prefetch Limit. If set to 1, don't prefetch past 4 KB (4098 bytes) boundaries.	Yes	Yes	0
13	I/O Remap Select. When set to 1, forces PCI Address bits [31:16] to all zeros. When set to 0, uses bits [31:16] of this register as PCI Address bits [31:16].	Yes	Yes	0
15:14	Direct Master Write Delay. Used to delay PCI Bus request after Direct Master Burst Write cycle has started. Values: 00 = No delay; start cycle immediately 01 = Delay 4 PCI clocks 10 = Delay 8 PCI clocks 11 = Delay 16 PCI clocks	Yes	Yes	00
31:16	Remap of Local-to-PCI Space into PCI Address Space. Remap (replace) Local Address bits used in decode as PCI Address bits. Used for Direct Master Memory and I/O accesses.	Yes	Yes	0

Note: Remap Address value must be multiple of Range (**not** Range register).

4.4.12 (DMCFG_A; PCI:2Ch, LOC:ACH) PCI Configuration Address Register for Direct Master to PCI IO/CFG

Table 4-44. (DMCFG_A; PCI:2Ch, LOC:ACH) PCI Configuration Address Register for Direct Master to PCI IO/CFG Description

Bit	Description	Read	Write	Value after Reset
1:0	Configuration Type (00=Type 0, 01=Type 1).	Yes	Yes	0
7:2	Register Number. If different register Read/Write is needed, value must be programmed and new PCI Configuration cycle must be generated.	Yes	Yes	0
10:8	Function Number.	Yes	Yes	0
15:11	Device Number.	Yes	Yes	0
23:16	Bus Number.	Yes	Yes	0
30:24	Reserved.	Yes	No	0
31	Configuration Enable. Value of 1 allows Local-to-PCI I/O accesses to be converted to a PCI Configuration cycle. Parameters in this table are used to generate PCI configuration address.	Yes	Yes	0

Note: Refer to Configuration Cycle Generation example in Section 3.6.1.6, "CFG (PCI Configuration Type 0 or Type 1 Cycles)."

4.4.13 (LAS1RR; PCI:F0h, LOC:170h) Local Address Space 1 Range Register for PCI-to-Local Bus

Table 4-45. (LAS1RR; PCI:F0h, LOC:170h) Local Address Space 1 Range Register for PCI-to-Local Bus Description

Bit	Description	Read	Write	Value after Reset										
0	Memory Space Indicator. Value of 0 indicates Local Address Space 1 maps into PCI memory space. Value of 1 indicates Address Space 1 maps into PCI I/O space.	Yes	Yes	0										
2:1	If mapped into memory space, encoding is as follows: <table border="1" style="margin-left: 20px;"> <thead> <tr> <th>2/1</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>Locate anywhere in 32-bit PCI Address space</td> </tr> <tr> <td>0 1</td> <td>Locate below 1 MB in PCI Address space</td> </tr> <tr> <td>1 0</td> <td>Locate anywhere in 64-bit PCI Address space</td> </tr> <tr> <td>1 1</td> <td>Reserved</td> </tr> </tbody> </table> If mapped into I/O space, bit 1 must be set to 0. Bit 2 is included with bits [31:3] to indicate decoding range.	2/1	Meaning	0 0	Locate anywhere in 32-bit PCI Address space	0 1	Locate below 1 MB in PCI Address space	1 0	Locate anywhere in 64-bit PCI Address space	1 1	Reserved	Yes	Yes	0
2/1	Meaning													
0 0	Locate anywhere in 32-bit PCI Address space													
0 1	Locate below 1 MB in PCI Address space													
1 0	Locate anywhere in 64-bit PCI Address space													
1 1	Reserved													
3	If mapped into memory space, value of 1 indicates reads are prefetchable (does not affect operation of the PCI 9080, but is used for system status). If mapped into I/O space, bit is included with bits [31:2] to indicate decoding range.	Yes	Yes	0										
31:4	Specifies which PCI Address bits to use for decoding PCI access to Local Bus Space 1. Each bit corresponds to a PCI Address bit. Bit 31 corresponds to Address bit 31. Write 1 to all bits that must be included in decode and 0 to all others (used in conjunction with PCI Configuration Register Ch 1). Default is 1 MB.	Yes	Yes	FFF0000h										

Notes: Range (**not** Range register) must be power of 2. "Range register value" is inverse of range.

User should limit all I/O spaces to 256 bytes per PCI Specification v2.1.

If QSR bit 0 is set, defines PCI Base Address 0.

4.4.14 (LAS1BA; PCI:F4h, LOC:174h) Local Address Space 1 Local Base Address (Remap) Register

Table 4-46. (LAS1BA; PCI:F4h, LOC:174h) Local Address Space 1 Local Base Address (Remap) Register Description

Bit	Description	Read	Write	Value after Reset
0	Space 1 Enable. Value of 1 enables decoding of PCI Addresses for Direct Slave access to Local Space 1. Value of 0 disables decoding. If set to 0, PCI BIOS may not allocate (assign) base address for Space 1. <i>Note: Must be set to 1 for any Direct Slave access to Space 1.</i>	Yes	Yes	0
1	Reserved.	Yes	No	0
3:2	If Local Space 1 is mapped into memory space, bits are not used. If mapped into I/O space, bit is included with bits [31:4] for remapping.	Yes	Yes	0
31:4	Remap of PCI Address to Local Address Space 1 into a Local Address Space. Remap (replace) PCI Address bits used in decode as Local Address bits.	Yes	Yes	0

Note: Remap Address value must be multiple of Range (not Range register).

4.4.15 (LBRD1; PCI:F8h, LOC:178h) Local Address Space 1 Bus Region Descriptor Register

Table 4-47. (LBRD1; PCI:F8h, LOC:178h) Local Address Space 1 Bus Region Descriptor Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Memory Space 1 Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11
5:2	Memory Space 1 Internal Wait States (data to data; 0-15 wait states).	Yes	Yes	0
6	Memory Space 1 Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0
7	Memory Space 1 BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI 9080 bursts four Lword maximum at a time.	Yes	Yes	0
8	Memory Space 1 Burst Enable. Value of 1 enables bursting. Value of 0 disables bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0
9	Memory Space 1 Prefetch Disable. If mapped into memory space, value of 0 enables Read prefetching. Value of 1 disables prefetching. If prefetching is disabled, the PCI 9080 disconnects after each memory read.	Yes	Yes	0
10	Read Prefetch Count Enable. When set to 1 and memory prefetching is enabled, the PCI 9080 prefetches up to the number of Lwords specified in prefetch count. When set to 0, the PCI 9080 ignores the count and continues prefetching until terminated by PCI Bus.	Yes	Yes	0
14:11	Prefetch Counter. Number of Lwords to prefetch during memory Read cycles (0-15).	Yes	Yes	0
31:15	Reserved.	Yes	No	0

4.5 Runtime Registers

4.5.1 (MBOX0; PCI:40h or 78h, LOC:C0h) Mailbox Register 0

Table 4-48. (MBOX0; PCI:40h or 78h, LOC:C0h) Mailbox Register 0 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

Note: Mailbox register 0 is replaced by the Inbound Queue Port when the I₂O feature is enabled (QSR[0] is set). Mailbox register 0 is always accessible at PCI Address 78h and Local Address C0h.

4.5.2 (MBOX1; PCI:44h or 7Ch, LOC:C4h) Mailbox Register 1

Table 4-49. (MBOX1; PCI:44h or 7Ch, LOC:C4h) Mailbox Register 1 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

Note: Mailbox register 1 is replaced by Outbound Queue Port when I₂O feature is enabled (QSR[0] is set). Mailbox register 1 is always accessible at PCI Address 7Ch and Local Address C4h.

4.5.3 (MBOX2; PCI:48h, LOC:C8h) Mailbox Register 2

Table 4-50. (MBOX2; PCI:48h, LOC:C8h) Mailbox Register 2 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

4.5.4 (MBOX3; PCI:4Ch, LOC:CCh) Mailbox Register 3

Table 4-51. (MBOX3; PCI:4Ch, LOC:CCh) Mailbox Register 3 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

4.5.5 (MBOX4; PCI:50h, LOC:D0h) Mailbox Register 4

Table 4-52. (MBOX4; PCI:50h, LOC:D0h) Mailbox Register 4 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

4.5.6 (MBOX5; PCI:54h, LOC:D4h) Mailbox Register 5

Table 4-53. (MBOX5; PCI:54h, LOC:D4h) Mailbox Register 5 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

4.5.7 (MBOX6; PCI:58h, LOC:D8h) Mailbox Register 6

Table 4-54. (MBOX6; PCI:58h, LOC:D8h) Mailbox Register 6 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

4.5.8 (MBOX7; PCI:5Ch, LOC:DCh) Mailbox Register 7

Table 4-55. (MBOX7; PCI:5Ch, LOC:DCh) Mailbox Register 7 Description

Bit	Description	Read	Write	Value after Reset
31:0	32-Bit Mailbox Register.	Yes	Yes	0

4.5.9 (P2LDBELL; PCI:60h, LOC:E0h) PCI-to-Local Doorbell Register

Table 4-56. (P2LDBELL; PCI:60h, LOC:E0h) PCI-to-Local Doorbell Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Doorbell Register. PCI Master can write to this register and generate a Local interrupt to the Local processor. The Local processor can then read this register to determine which Doorbell bit was asserted. PCI Master sets doorbell by writing 1 to a particular bit. Local processor can clear Doorbell bit by writing 1 to that bit position.	Yes	Yes/Clr	0

4.5.10 (L2PDBELL; PCI:64h, LOC:E4h) Local-to-PCI Doorbell Register

Table 4-57. (L2PDBELL; PCI:64h, LOC:E4h) Local-to-PCI Doorbell Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Doorbell Register. Local processor can write to this register and generate PCI interrupt. PCI Master can then read this register to determine which Doorbell bit was asserted. Local processor sets doorbell by writing 1 to a particular bit. PCI Master can clear Doorbell bit by writing 1 to that bit position.	Yes	Yes/Clr	0

4.5.11 (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status Register

Table 4-58. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status Register Description

Bit	Description	Read	Write	Value after Reset
0	Enable Local Bus LSERR#. Value of 1 enables the PCI 9080 to assert LSERR# interrupt output when PCI Bus Target Abort or Master Abort Status bit is set in PCI Status Configuration register.	Yes	Yes	0
1	Enable Local Bus LSERR# when PCI parity error occurs during a PCI 9080 Master Transfer or a PCI 9080 Slave access or an Outbound Free List FIFO Overflow Init.	Yes	Yes	0
2	Generate PCI Bus SERR#. When set to 0, writing 1 generates PCI Bus SERR#.	Yes	Yes	0
3	Mailbox Interrupt Enable. Value of 1 enables a Local interrupt to be generated when PCI Bus writes to Mailbox registers 0 through 3. To clear a Local interrupt, the Local Master must read the Mailbox. Used in conjunction with Local interrupt enable.	Yes	Yes	0
7:4	Reserved.	Yes	No	0
8	PCI Interrupt Enable. Value of 1 enables PCI interrupts.	Yes	Yes	1
9	PCI Doorbell Interrupt Enable. Value of 1 enables doorbell interrupts. Used in conjunction with PCI interrupt enable. Clearing doorbell interrupt bits that caused interrupt also clears interrupt.	Yes	Yes	0
10	PCI Abort Interrupt Enable. Value of 1 enables Master abort or Master detect of Target abort to generate PCI interrupt. Used in conjunction with PCI interrupt enable. Clearing abort status bits also clears PCI interrupt.	Yes	Yes	0
11	PCI Local Interrupt Enable. Value of 1 enables Local interrupt input to generate a PCI interrupt. Use in conjunction with PCI interrupt enable. Clearing the Local Bus cause of interrupt also clears interrupt.	Yes	Yes	0
12	Retry Abort Enable. Value of 1 enables the PCI 9080 to treat 256 Master consecutive retries to a Target as a Target Abort. Value of 0 enables the PCI 9080 to attempt Master Retries indefinitely. Note: For diagnostic purposes only.	Yes	Yes	0
13	Value of 1 indicates PCI doorbell interrupt is active.	Yes	No	0
14	Value of 1 indicates PCI abort interrupt is active.	Yes	No	0
15	Value of 1 indicates Local interrupt is active (LINTi#).	Yes	No	0
16	Local Interrupt Output Enable. Value of 1 enables Local interrupt output.	Yes	Yes	1
17	Local Doorbell Interrupt Enable. Value of 1 enables doorbell interrupts. Used in conjunction with Local interrupt enable. Clearing local doorbell interrupt bits that caused interrupt also clears interrupt.	Yes	Yes	0
18	Local DMA Channel 0 Interrupt Enable. Value of 1 enables DMA Channel 0 interrupts. Used in conjunction with Local interrupt enable. Clearing DMA status bits also clears interrupt.	Yes	Yes	0
19	Local DMA Channel 1 Interrupt Enable. Value of 1 enables DMA Channel 1 interrupts. Used in conjunction with Local interrupt enable. Clearing DMA status bits also clears interrupt.	Yes	Yes	0
20	Value of 1 indicates local doorbell interrupt is active.	Yes	No	0
21	Value of 1 indicates DMA Ch 0 interrupt is active.	Yes	No	0
22	Value of 1 indicates DMA Ch 1 interrupt is active.	Yes	No	0
23	Value of 1 indicates BIST interrupt is active. Writing 1 to bit 6 of PCI Configuration BIST Register generates BIST (Built-In Self-Test) interrupt. Clearing bit 6 clears interrupt. For description of self-test, refer to PCI BISTR.	Yes	No	0

Table 4-58. (INTCSR; PCI:68h, LOC:E8h) Interrupt Control/Status Register Description (continued)

Bit	Description	Read	Write	Value after Reset
24	Value of 0 indicates Direct Master was Bus Master during a Master or Target abort. (Not valid until abort occurs.)	Yes	No	1
25	Value of 0 indicates DMA CH 0 was Bus Master during a Master or Target abort. (Not valid until abort occurs.)	Yes	No	1
26	Value of 0 indicates DMA CH 1 was Bus Master during a Master or Target abort. (Not valid until abort occurs.)	Yes	No	1
27	Value of 0 indicates Target Abort was generated by the PCI 9080 after 256 consecutive Master retries to Target. (Not valid until abort occurs.)	Yes	No	1
28	Value of 1 indicates PCI wrote data to MailBox #0. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0
29	Value of 1 indicates PCI wrote data to MailBox #1. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0
30	Value of 1 indicates PCI wrote data to MailBox #2. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0
31	Value of 1 indicates PCI wrote data to MailBox #3. Enabled only if MBOXINTENB is enabled (bit 3 high).	Yes	No	0

4.5.12 (CNTRL; PCI:6Ch, LOC:ECh) Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register

Table 4-59. (CNTRL; PCI:6Ch, LOC:ECh) Serial EEPROM Control, PCI Command Codes, User I/O Control, Init Control Register Description

Bit	Description	Read	Write	Value after Reset
3:0	PCI Read Command Code for DMA. Sent out during DMA Read cycles.	Yes	Yes	1110
7:4	PCI Write Command Code for DMA. Sent out during DMA Write cycles.	Yes	Yes	0111
11:8	PCI Memory Read Command Code for Direct Master. Sent out during Direct Master Read cycles.	Yes	Yes	0110
15:12	PCI Memory Write Command Code for Direct Master. Sent out during Direct Master Write cycles.	Yes	Yes	0111
16	General Purpose Output. Value of 1 causes USER0 output to go high. Value of 0 causes USER0 output to go low.	Yes	Yes	1
17	General Purpose Input. Value of 1 indicates USER1 input pin is high. Value of 0 indicates USER1 pin is low.	Yes	No	—
23:18	Reserved.	Yes	No	0
24	Serial EEPROM Clock for Local or PCI Bus Reads or Writes to Serial EEPROM. Toggling this bit generates serial EEPROM clock. (Refer to manufacturer's data sheet for particular serial EEPROM being used.)	Yes	Yes	0
25	Serial EEPROM Chip Select. For Local or PCI Bus Reads or Writes to serial EEPROM, setting this bit to 1 provides serial EEPROM chip select.	Yes	Yes	0
26	Write Bit to serial EEPROM. For Writes, this output bit is input to serial EEPROM. Clocked into serial EEPROM by serial EEPROM clock.	Yes	Yes	0
27	Read Serial EEPROM Data. For Reads, this input bit is output of serial EEPROM. Clocked out of serial EEPROM by serial EEPROM clock.	Yes	No	—
28	Serial EEPROM Present. Value of 1 indicates serial EEPROM is present.	Yes	No	0
29	Reload Configuration Registers. When set to 0, writing 1 causes the PCI 9080 to reload Local Configuration registers from serial EEPROM.	Yes	Yes	0
30	PCI Adapter Software Reset. Value of 1 holds Local Bus logic in the PCI 9080 reset and LRESET _# asserted. Contents of PCI Configuration registers and Shared Run Time registers are not reset. Software Reset can only be cleared from the PCI Bus. (Local Bus remains reset until this bit is cleared.)	Yes	Yes	0
31	Local Init Status. Value of 1 indicates Local Init done. Responses to PCI accesses are Retrys until this bit is set. While input pin NB _# is asserted low, this bit is forced to 1.	Yes	Yes	0

4.5.13 (PCIHIDR; PCI:70h, LOC:F0h) PCI Permanent Configuration ID Register

Table 4-60. (PCIHIDR; PCI:70h, LOC:F0h) PCI Permanent Configuration ID Register Description

Bit	Description	Read	Write	Value after Reset
15:0	Permanent Vendor ID. Identifies device manufacturer. Note: <i>Hardcoded to PCI SIG issued vendor ID of PLX (10B5h).</i>	Yes	No	10B5h
31:16	Permanent Device ID. Identifies particular device. Note: <i>Hardcoded to PLX part number for PCI interface chip PCI 9080.</i>	Yes	No	9080h

4.5.14 (PCIHREV; PCI:74h, LOC:F4h) PCI Permanent Revision ID Register

Table 4-61. (PCIHREV; PCI:74h, LOC:F4h) PCI Permanent Revision ID Register Description

Bit	Description	Read	Write	Value after Reset
7:0	Permanent Revision ID. Note: <i>Hardcoded to silicon revision of the PCI 9080.</i>	Yes	No	Current Rev #

4.6 DMA Registers

4.6.1 (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode Register

Table 4-62. (DMAMODE0; PCI:80h, LOC:100h) DMA Channel 0 Mode Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11
5:2	Internal Wait States (data to data).	Yes	Yes	0
6	Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0
7	BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI 9080 bursts four Lword maximum at a time.	Yes	Yes	0
8	Local Burst Enable. Value of 1 enables bursting. Value of 0 disables local bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0
9	Chaining. Value of 1 indicates Chaining mode is enabled. For Chaining mode, DMA source address, destination address and byte count are loaded from memory in PCI or Local Address Spaces. Value of 0 indicates Non-chaining mode is enabled.	Yes	Yes	0
10	Done Interrupt Enable. Value of 1 enables interrupt when done. Value of 0 disables interrupt when done. If DMA Clear Count mode is enabled, interrupt does not occur until byte count is cleared.	Yes	Yes	0
11	Local Addressing Mode. Value of 1 indicates Local Address LA[31:2] to be held constant. Value of 0 indicates Local Address is incremented.	Yes	Yes	0
12	Demand Mode. Value of 1 causes DMA controller to operate in Demand mode. In Demand mode, DMA controller transfers data when its DREQ[1:0]# input is asserted. Asserts DACK[1:0]# to indicate current Local Bus transfer is in response to DREQ[1:0]# input. DMA controller transfers Lwords (32 bits) of data. May result in multiple transfers for 8- or 16-bit bus.	Yes	Yes	0
13	Write and Invalidate Mode for DMA Transfers. When set to 1, the PCI 9080 performs Write and Invalidate cycles to PCI Bus. The PCI 9080 supports Write and Invalidate sizes of 8 or 16 Lwords. Size specified in PCI Cache Line Size Register. If size other than 8 or 16 is specified, the PCI 9080 performs Write transfers rather than Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries.	Yes	Yes	0
14	DMA EOT (End of Transfer) Enable. Value of 1 enables EOT[1:0]# input pin. Value of 0 disables EOT[1:0]# input pin. (Refer to Section 3.7.6.1, "End of Transfer (EOT0# or EOT1#) Input.")	Yes	Yes	0
15	DMA Stop Data Transfer Mode. Value of 0 sends BLAST to terminate DMA transfer. Value of 1 indicates EOT asserted or DREQ[1:0]# de-asserted during Demand mode DMA terminates a DMA transfer. (Refer to Section 3.7.6.1, "End of Transfer (EOT0# or EOT1#) Input.")	Yes	Yes	0
16	DMA Clear Count Mode. When set to 1, if it is in Local memory, byte count in each chaining descriptor is cleared when corresponding DMA transfer completes. Note: If the chaining descriptor is in PCI memory, the count is not cleared.	Yes	Yes	0
17	DMA Channel 0 Interrupt Select. Value of 1 routes DMA Channel 0 interrupt to PCI interrupt. Value of 0 routes DMA Channel 0 interrupt to Local Bus interrupt.	Yes	Yes	0
31:18	Reserved.	Yes	No	0

4.6.2 (DMAPADR0; PCI:84h, LOC:104h) DMA Channel 0 PCI Address Register

Table 4-63. (DMAPADR0; PCI:84h, LOC:104h) DMA Channel 0 PCI Address Register Description

Bit	Description	Read	Write	Value after Reset
31:0	PCI Address Register. Indicates from where in PCI memory space the DMA transfers (reads or writes) start.	Yes	Yes	0

4.6.3 (DMALADR0; PCI:88h, LOC:108h) DMA Channel 0 Local Address Register

Table 4-64. (DMALADR0; PCI:88h, LOC:108h) DMA Channel 0 Local Address Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Local Address Register. Indicates from where in Local memory space the DMA transfers (reads or writes) start.	Yes	Yes	0

4.6.4 (DMASIZ0; PCI:8Ch, LOC:10Ch) DMA Channel 0 Transfer Size (Bytes) Register

Table 4-65. (DMASIZ0; PCI:8Ch, LOC:10Ch) DMA Channel 0 Transfer Size (Bytes) Register Description

Bit	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to transfer during DMA operation.	Yes	Yes	0
31:23	Reserved.	Yes	No	0

4.6.5 (DMADPR0; PCI:90h, LOC:110h) DMA Channel 0 Descriptor Pointer Register

Table 4-66. (DMADPR0; PCI:90h, LOC:110h) DMA Channel 0 Descriptor Pointer Register Description

Bit	Description	Read	Write	Value after Reset
0	Descriptor Location. Value of 1 indicates PCI Address space. Value of 0 indicates Local Address Space.	Yes	Yes	0
1	End of Chain. Value of 1 indicates end of chain. Value of 0 indicates not end of chain descriptor. (Same as Non-chaining Mode.)	Yes	Yes	0
2	Interrupt after Terminal Count. Value of 1 causes interrupt to be generated after terminal count for this descriptor is reached. Value of 0 disables interrupts from being generated.	Yes	Yes	0
3	Direction of Transfer. Value of 1 indicates transfers from the Local Bus to PCI Bus. Value of 0 indicates transfers from the PCI Bus to Local Bus.	Yes	Yes	0
31:4	Next Descriptor Address. Quad word aligned (bits [3:0] = 0000).	Yes	Yes	0

4.6.6 (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode Register

Table 4-67. (DMAMODE1; PCI:94h, LOC:114h) DMA Channel 1 Mode Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Local Bus Width. Value of 00 indicates bus width of 8 bits. Value of 01 indicates bus width of 16 bits. Value of 10 or 11 indicates bus width of 32 bits.	Yes	Yes	S = 01 J = 11 C = 11
5:2	Internal Wait States (data to data).	Yes	Yes	0
6	Ready Input Enable. Value of 1 enables Ready input. Value of 0 disables Ready input.	Yes	Yes	0
7	BTERM# Input Enable. Value of 1 enables BTERM# input. Value of 0 disables BTERM# input. If set to 0, the PCI 9080 bursts four Lword maximum at a time.	Yes	Yes	0
8	Local Burst Enable. Value of 1 enables bursting. Value of 0 disables local bursting. If burst is disabled, Local Bus performs continuous single cycles for Burst PCI Read/Write cycles.	Yes	Yes	0
9	Chaining. Value of 1 indicates Chaining mode enabled. For Chaining mode, DMA source address, destination address and byte count are loaded from memory in PCI or Local address spaces. Value of 0 indicates Non-chaining mode enabled.	Yes	Yes	0
10	Done Interrupt Enable. Value of 1 enables interrupt when done. Value of 0 disables interrupt when done. If DMA Clear Count mode is enabled, interrupt does not occur until byte count is cleared.	Yes	Yes	0
11	Local Addressing Mode. Value of 1 indicates Local Address LA[31:2] to be held constant. Value of 0 indicates Local Address is incremented.	Yes	Yes	0
12	Demand Mode. Value of 1 causes DMA controller to operate in Demand mode. In Demand mode, DMA controller transfers data when its DREQ[1:0]# input is asserted. Asserts DACK[1:0]# to indicate current Local Bus transfer is in response to DREQ[1:0]# input. DMA controller transfers Lwords (32 bits) of data. May result in multiple transfers for 8- or 16-bit bus.	Yes	Yes	0
13	Write and Invalidate Mode for DMA Transfers. When set to 1, the PCI 9080 performs Write and Invalidate cycles to PCI Bus. The PCI 9080 supports Write and Invalidate sizes of 8 or 16 Lwords. Size is specified in PCI Cache Line Size Register. If size other than 8 or 16 is specified, the PCI 9080 performs Write transfers rather than Write and Invalidate transfers. Transfers must start and end at Cache Line boundaries.	Yes	Yes	0
14	DMA EOT (End of Transfer) Enable. Value of 1 enables EOT[1:0]# input pin. Value of 0 disables EOT[1:0]# input pin. (Refer to Section 3.7.6.1, "End of Transfer (EOT0# or EOT1#) Input.")	Yes	Yes	0
15	DMA Stop Data Transfer Mode. Value of 0 BLAST terminates DMA transfer. Value of 1 indicates EOT. In demand DMA mode, if set to 1, assertion of EOT causes DMA controller to terminate following current Data phase (blast may or may not be asserted). If not set, and EOT asserted, DMA controller completes current Data phase and potentially a following Data phase in which blast is asserted. (Refer to Section 3.7.6.1, "End of Transfer (EOT0# or EOT1#) Input.")	Yes	Yes	0
16	DMA Clear Count Mode. When set to 1, byte count in each chaining descriptor, if it is in Local memory, is cleared when corresponding DMA transfer completes. Note: If a chaining descriptor is in PCI memory, the count is not cleared.	Yes	Yes	0
17	DMA Channel 1 Interrupt Select. Value of 1 routes DMA Channel 1 interrupt to PCI interrupt. Value of 0 routes DMA Channel 1 interrupt to Local Bus interrupt.	Yes	Yes	0
31:18	Reserved.	Yes	No	0

4.6.7 (DMAPADR1; PCI:98h, LOC:118h) DMA Channel 1 PCI Address Register

Table 4-68. (DMAPADR1; PCI:98h, LOC:118h) DMA Channel 1 PCI Address Register Description

Bit	Description	Read	Write	Value after Reset
31:0	PCI Data Address Register. Indicates from where in PCI memory space the DMA transfers (reads or writes) start.	Yes	Yes	0

4.6.8 (DMALADR1; PCI:9Ch, LOC:11Ch) DMA Channel 1 Local Address Register

Table 4-69. (DMALADR1; PCI:9Ch, LOC:11Ch) DMA Channel 1 Local Address Register Description

Bit	Description	Read	Write	Value after Reset
31:0	Local Data Address Register. Indicates from where in Local memory space the DMA transfers (reads or writes) start.	Yes	Yes	0

4.6.9 (DMASIZ1; PCI:A0h, LOC:120h) DMA Channel 1 Transfer Size (Bytes) Register

Table 4-70. (DMASIZ1; PCI:A0h, LOC:120h) DMA Channel 1 Transfer Size (Bytes) Register Description

Bit	Description	Read	Write	Value after Reset
22:0	DMA Transfer Size (Bytes). Indicates number of bytes to transfer during DMA operation.	Yes	Yes	0
31:23	Reserved.	Yes	No	0

4.6.10 (DMADPR1; PCI:A4h, LOC:124h) DMA Channel 1 Descriptor Pointer Register

Table 4-71. (DMADPR1; PCI:A4h, LOC:124h) DMA Channel 1 Descriptor Pointer Register Description

Bit	Description	Read	Write	Value after Reset
0	Descriptor Location. Value of 1 indicates PCI Address space. Value of 0 indicates Local Address Space.	Yes	Yes	0
1	End of Chain. Value of 1 indicates end of chain. Value of 0 indicates not end of chain descriptor. (Same as Non-chaining mode.)	Yes	Yes	0
2	Interrupt after Terminal Count. Value of 1 causes interrupt to be generated after terminal count for this descriptor is reached. Value of 0 disables interrupts from being generated.	Yes	Yes	0
3	Direction of Transfer. Value of 1 indicates transfers from the Local Bus to PCI Bus. Value of 0 indicates transfers from the PCI Bus to Local Bus.	Yes	Yes	0
31:4	Next Descriptor Address. Quad word aligned (bits [3:0] = 0000).	Yes	Yes	0

4.6.11 (DMACSR0; PCI:A8h, LOC:128h) DMA Channel 0 Command/Status Register

Table 4-72. (DMACSR0; PCI:A8h, LOC:128h) DMA Channel 0 Command/Status Register Description

Bit	Description	Read	Write	Value after Reset
0	Channel 0 Enable. Value of 1 enables channel to transfer data. Value of 0 disables channel from starting DMA transfer and if in process of transferring data suspend transfer (pause).	Yes	Yes	0
1	Channel 0 Start. Value of 1 causes channel to start transferring data if channel is enabled.	No	Yes/Set	0
2	Channel 0 Abort. Value of 1 causes channel to abort current transfer. Channel Enable bit must be cleared. Channel Complete bit is set when abort is complete.	No	Yes/Set	0
3	Clear Interrupt. Writing 1 to this bit clears Channel 0 interrupts.	No	Yes/Clr	0
4	Channel 0 Done. Value of 1 indicates channel's transfer is complete. Value of 0 indicates channel's transfer is not complete.	Yes	No	1
7:5	Reserved.	Yes	No	0

4.6.12 (DMACSR1; PCI:A9h, LOC:129h) DMA Channel 1 Command/Status Register

Table 4-73. (DMACSR1; PCI:A9h, LOC:129h) DMA Channel 1 Command/Status Register Description

Bit	Description	Read	Write	Value after Reset
0	Channel 1 Enable. Value of 1 enables channel to transfer data. Value of 0 disables channel from starting DMA transfer and if in process of transferring data suspend transfer (Pause).	Yes	Yes	0
1	Channel 1 Start. Value of 1 causes channel to start transferring data if channel is enabled.	No	Yes/Set	0
2	Channel 1 Abort. Value of 1 causes channel to abort current transfer. Channel Enable bit must be cleared. Channel Complete bit set when abort is complete.	No	Yes/Set	0
3	Clear Interrupt. Writing 1 to this bit clears Channel 1 interrupts.	No	Yes/Clr	0
4	Channel 1 Done. Value of 1 indicates this channel's transfer is complete. Value of 0 indicates channel's transfer is not complete.	Yes	No	1
7:5	Reserved.	Yes	No	0

4.6.13 (DMAARB; PCI:ACH, LOC:12Ch) DMA Arbitration Register

Same as Mode/Arbitration register (MARBR).

4.6.14 (DMATHR; PCI:B0h, LOC:130h) DMA Threshold Register

Table 4-74. (DMATHR; PCI:B0h, LOC:130h) DMA Threshold Register Description

Bit	Description	Read	Write	Value after Reset
3:0	DMA Channel 0 PCI-to-Local Almost Full (C0PLAF). Number of full entries (divided by two, minus one) in the FIFO before requesting Local Bus for writes. (C0PLAF+1) + (C0PLAE+1) should be \leq FIFO Depth of 32.	Yes	Yes	0
7:4	DMA Channel 0 Local-to-PCI Almost Empty (C0LPAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting Local Bus for reads. (C0LPAF+1) + (C0LPAE+1) should be \leq FIFO depth of 32.	Yes	Yes	0
11:8	DMA Channel 0 Local-to-PCI Almost Full (C0LPAF). Number of full entries (divided by two, minus one) in the FIFO before requesting PCI Bus for writes.	Yes	Yes	0
15:12	DMA Channel 0 PCI-to-Local Almost Empty (C0PLAE). Number of empty entries (divided by two, minus one) in the FIFO before requesting PCI Bus for reads.	Yes	Yes	0
19:16	DMA Channel 1 PCI-to-Local Almost Full (C1PLAF). Number of full entries (minus one) in the FIFO before requesting Local Bus for writes. (C1PLAF+1) + (C1PLAE+1) should be \leq FIFO depth of 16.	Yes	Yes	0
23:20	DMA Channel 1 Local-to-PCI Almost Empty (C1LPAE). Number of empty entries (minus one) in the FIFO before requesting Local Bus for reads. (C1PLAF) + (C1PLAE) should be \leq FIFO depth of 16.	Yes	Yes	0
27:24	DMA Channel 1 Local-to-PCI Almost Full (C1LPAF). Number of full entries (minus one) in the FIFO before requesting PCI Bus for writes.	Yes	Yes	0
31:28	DMA Channel 1 PCI-to-Local Almost Empty (C1PLAE). Number of empty entries (minus one) in the FIFO before requesting PCI Bus for reads.	Yes	Yes	0

Note: If the number of entries needed is x , then the value is one less than half the number of entries (DMA Channel 0 only).

4.7 Messaging Queue Registers

4.7.1 (OPLFIS; PCI:30h, LOC:B0) Outbound Post List FIFO Interrupt Status Register

Table 4-75. (OPLFIS; PCI:30h, LOC:B0) Outbound Post List FIFO Interrupt Status Register Description

Bit	Description	Read	Write	Value after Reset
2:0	Reserved.	Yes	No	0
3	Outbound Post List FIFO Interrupt. Set when the Outbound Post List FIFO is not empty. Not affected by the Interrupt Mask bit.	Yes	No	0
31:4	Reserved.	Yes	No	0

4.7.2 (OPLFIM; PCI:34h, LOC:B4) Outbound Post List FIFO Interrupt Mask Register

Table 4-76. (OPLFIM; PCI:34h, LOC:B4) Outbound Post List FIFO Interrupt Mask Register Description

Bit	Description	Read	Write	Value after Reset
2:0	Reserved.	Yes	No	0
3	Outbound Post List FIFO Interrupt Mask. Interrupt is masked when set.	Yes	Yes	1
31:4	Reserved.	Yes	No	0

4.7.3 (IQP; PCI:40h) Inbound Queue Port Register

Table 4-77. (IQP; PCI:40h) Inbound Queue Port Register Description

Bit	Description	Read	Write	Value after Reset
31:0	<p>Value written by the PCI Master is stored into the Inbound Post List FIFO, which is located in Local memory at an address pointed to by Queue Base Address + FIFO Size + Inbound Post Head Pointer. From the time of a PCI write until a Local Memory write and update of the Inbound Post Queue Head Pointer, further accesses to this register result in a Retry. A Local interrupt is generated when the Inbound Post List FIFO is not empty.</p> <p>When the port is read by a PCI Master, the value is read from the Inbound Free List FIFO, which is located in Local memory at an address pointed to by Queue Base Address + Inbound Free Tail Pointer. If the FIFO is empty, a value of FFFFFFFh is returned.</p>	PCI	PCI	0

4.7.4 (OQP; PCI:44h) Outbound Queue Port Register

Table 4-78. (OQP; PCI:44h) Outbound Queue Port Register Description

Bit	Description	Read	Write	Value after Reset
31:0	<p>Value written by the PCI Master is stored into the Outbound Free List FIFO, which is located in Local memory at an address pointed to by Queue Base Address + (3*FIFO Size) + Outbound Free Head Pointer. From the time of the PCI write until the Local Memory write and update of the Outbound Free Head Pointer, further accesses to this register result in a Retry. If the FIFO fills up, a local LSERR interrupt is generated.</p> <p>When the port is read by a PCI Master, the value is read from the Outbound Post List FIFO, which is located in Local memory at an address pointed to by Queue Base Address + (2*FIFO Size) + Outbound Post Tail Pointer. If the FIFO is empty, a value of FFFFFFFh is returned. A PCI interrupt is generated if the Outbound Post List FIFO is not empty.</p>	PCI	PCI	0

4.7.5 (MQCR; PCI:C0h, LOC:140h) Messaging Queue Configuration Register

Table 4-79. (MQCR; PCI:C0h, LOC:140h) Messaging Queue Configuration Register Description

Bit	Description	Read	Write	Value after Reset																								
0	Queue Enable. Value of 1 allows accesses to the Inbound and Outbound Queue Ports. If cleared to 0, writes are accepted but ignored, and reads return FFFFFFFF. Complete all pointer initializations and frame allocations before enabling this bit.	Yes	Yes	0																								
5:1	<p>Circular FIFO Size. Defines size of one of the circular FIFOs. Each of the four FIFOs are the same size. Each FIFO entry is one 32-bit word.</p> <p><u>FIFO Size Encoding</u></p> <table border="1"> <thead> <tr> <th>5:1</th> <th>Max entries per FIFO</th> <th>FIFO Size</th> <th>Total FIFO Memory</th> </tr> </thead> <tbody> <tr> <td>00001</td> <td>4K entries</td> <td>16 KB</td> <td>64 KB</td> </tr> <tr> <td>00010</td> <td>8K entries</td> <td>32 KB</td> <td>128 KB</td> </tr> <tr> <td>00100</td> <td>16K entries</td> <td>64 KB</td> <td>256 KB</td> </tr> <tr> <td>01000</td> <td>32K entries</td> <td>128 KB</td> <td>512 KB</td> </tr> <tr> <td>10000</td> <td>64K entries</td> <td>256 KB</td> <td>1 MB</td> </tr> </tbody> </table>	5:1	Max entries per FIFO	FIFO Size	Total FIFO Memory	00001	4K entries	16 KB	64 KB	00010	8K entries	32 KB	128 KB	00100	16K entries	64 KB	256 KB	01000	32K entries	128 KB	512 KB	10000	64K entries	256 KB	1 MB	Yes	Yes	00001
5:1	Max entries per FIFO	FIFO Size	Total FIFO Memory																									
00001	4K entries	16 KB	64 KB																									
00010	8K entries	32 KB	128 KB																									
00100	16K entries	64 KB	256 KB																									
01000	32K entries	128 KB	512 KB																									
10000	64K entries	256 KB	1 MB																									
31:6	Reserved.	Yes	No	0																								

4.7.6 (QBAR; PCI:C4h, LOC:144h) Queue Base Address Register

Table 4-80. (QBAR; PCI:C4h, LOC:144h) Queue Base Address Register Description

Bit	Description	Read	Write	Value after Reset
19:0	Reserved.	Yes	No	0
31:20	Queue Base Address. Local memory base address of Inbound and Outbound Queues (four contiguous and equal size FIFOs). Queue base address must be aligned on 1 MB boundary.	Yes	Yes	0

4.7.7 (IFHPR; PCI:C8h, LOC:148h) Inbound Free Head Pointer Register

Table 4-81. (IFHPR; PCI:C8h, LOC:148h) Inbound Free Head Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Inbound Free Head Pointer. Local Memory Offset for the Inbound Free List FIFO. Initialized as (0*FIFO Size) and maintained by local CPU software.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.8 (IFTPR; PCI:CCh, LOC:14Ch) Inbound Free Tail Pointer Register

Table 4-82. (IFTPR; PCI:CCh, LOC:14Ch) Inbound Free Tail Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Inbound Free Tail Pointer. Local Memory Offset for the Inbound Free List FIFO. Initialized as (0*FIFO Size) by local CPU software. Maintained by MU hardware and incremented modulo the FIFO size.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.9 (IPHPR; PCI:D0h, LOC:150h) Inbound Post Head Pointer Register

Table 4-83. (IPHPR; PCI:D0h, LOC:150h) Inbound Post Head Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Inbound Post Head Pointer. Local Memory Offset for the Inbound Post List FIFO. Initialized as (1*FIFO Size) by local CPU software. Maintained by MU hardware and incremented modulo the FIFO size.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.10 (IPTPR; PCI:D4h, LOC:154h) Inbound Post Tail Pointer Register

Table 4-84. (IPTPR; PCI:D4h, LOC:154h) Inbound Post Tail Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Inbound Post Tail Pointer. Local Memory Offset for the Inbound Post List FIFO. Initialized as (1*FIFO Size) and maintained by local CPU software.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.11 (OFHPR; PCI:D8h, LOC:158h) Outbound Free Head Pointer Register

Table 4-85. (OFHPR; PCI:D8h, LOC:158h) Outbound Free Head Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Outbound Free Head Pointer. Local Memory Offset for the Outbound Free List FIFO. Initialized as (3*FIFO Size) by local CPU software. Maintained by MU hardware and incremented modulo the FIFO size.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.12 (OFTPR; PCI:DCh, LOC:15Ch) Outbound Free Tail Pointer Register

Table 4-86. (OFTPR; PCI:DCh, LOC:15Ch) Outbound Free Tail Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Outbound Free Tail Pointer. Local Memory Offset for the Outbound Free List FIFO. Initialized as (3*FIFO Size) and maintained by local CPU software.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.13 (OPHPR; PCI:E0h, LOC:160h) Outbound Post Head Pointer Register

Table 4-87. (OPHPR; PCI:E0h, LOC:160h) Outbound Post Head Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Outbound Post Head Pointer. Local Memory Offset for the Outbound Post List FIFO. Initialized as (2*FIFO Size) and maintained by local CPU software.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.14 (OPTPR; PCI:E4h, LOC:164h) Outbound Post Tail Pointer Register

Table 4-88. (OPTPR; PCI:E4h, LOC:164h) Outbound Post Tail Pointer Register Description

Bit	Description	Read	Write	Value after Reset
1:0	Reserved.	Yes	No	0
19:2	Outbound Post Tail Pointer. Local Memory Offset for the Outbound Post List FIFO. Initialized as (2*FIFO Size). Maintained by MU hardware and incremented modulo the FIFO size.	Yes	Yes	0
31:20	Queue Base Address.	Yes	No	0

4.7.15 (QSR; PCI:E8h, LOC:168h) Queue Status/Control Register

Table 4-89. (QSR; PCI:E8h, LOC:168h) Queue Status/Control Register

Bit	Description	Read	Write	Value after Reset
0	I ₂ O Decode Enable. When set, replaces Mailbox registers 0 and 1 with the Inbound and Outbound Queue Port registers and redefines Space 1 as PCI Base Address 0 to be accessed by PCIBAR0. Former Space 1 registers F0, F4, and F8 should be programmed to configure their shared I ₂ O memory space, defined as PCI Base Address 0.	Yes	Yes	0
1	Queue Local Space Select. When set to 0, use Local Address Space 0 Bus Region descriptor for Queue accesses. When set to 1, use Local Address Space 1 Bus Region descriptor for Queue accesses.	Yes	Yes	0
2	Outbound Post List FIFO Prefetch Enable. When set, prefetching occurs from the Outbound Post List FIFO if it is not empty.	Yes	Yes	0
3	Inbound Free List FIFO Prefetch Enable. When set, prefetching occurs from the Inbound Free List FIFO if it is not empty.	Yes	Yes	0
4	Inbound Post List FIFO Interrupt Mask. When set, Interrupt is masked.	Yes	Yes	1
5	Inbound Post List FIFO Interrupt. Set when the Inbound Post List FIFO is not empty. Not affected by the Interrupt Mask bit.	Yes	No	0
6	Outbound Free List FIFO Overflow Interrupt Mask. When set, Interrupt is masked.	Yes	Yes	1
7	Outbound Free List FIFO Overflow Interrupt. Set when the Outbound Free List FIFO becomes full. A Local LSERR (NMI) interrupt is generated if enabled in the Interrupt Control/Status register. Writing 1 clears interrupt.	Yes	Yes/Clr	0
31:8	Unused.	Yes	No	0

5. PIN DESCRIPTION

5.1 Pin Summary

The tables in this section describe the PCI 9080 pins. Table 5-2 through Table 5-5 provide pin information common to all three Local Bus modes of operation—C, J, and S:

- Power and Ground Pin Description
- Serial EEPROM Interface Pin Description
- PCI System Bus Interface Pin Description
- Local Bus Mode and Processor Independent Interface Pin Description

The pins in Table 5-6 through Table 5-8 correspond to the Local Bus modes of the PCI 9080:

- C Bus Mode Interface Pin Description (32-bit address/32-bit data, nonmultiplexed)
- J Bus Mode Interface Pin Description (32-bit address/32-bit data, multiplexed)
- S Bus Mode Interface Pin Description (32-bit address/16-bit data, multiplexed)

The following pins have internal pull-ups:

ADMODE, BIGEND#, BTERM#, DREQ[1:0]#, EEDO, EESEL, LINTi#, LLOCK#, LRESETi#, NB#, READYi#, S[2:0], SHORT#, and WAITi#.

The following pins have internal pull-downs: BREQ, LHOLDA, TEST, and USERI.

For a visual view of the chip pin out, refer to Figure 7-3 in Section 7.3, “PCI 9080 Pin Out (S, J, and C Modes).”

Table 5-1 lists the abbreviations used in this section to represent the various pin types.

Table 5-1. Pin Type Abbreviations

Abbreviation	Pin Type
I/O	Input and output pin
I	Input pin only
O	Output pin only
TS	Tri-state pin
OC	Open collector pin
TP	Totem pole pin
STS	Sustained tri-state pin, driven high for one CLK before float
DTS	Driven tri-state pin, driven high for one-half CLK before float

All Local Bus internal pull-ups go through a 2 k Ω resistor. All Local Bus internal pull-downs go through a 100 k Ω resistor.

All local tri-state I/O pins should have external pull-ups (use 3 k Ω - 10 k Ω).

Unspecified pins are not connected.

Note: For PCI Pins, DO NOT pull any pins up or down unless the PCI 9080 is being used in an embedded design. Refer to the PCI Local Bus Specification, v2.1, page 123.

5.2 Pin Out Common to All Bus Modes

Table 5-2. Power and Ground Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
TEST	Test	1	I	49	Test Pin. Pull high for test, low for normal operation. When TEST is pulled high, all outputs except USERO (pin 27) are placed in tri-state. USERO provides a NAND-TREE output when TEST is pulled high.
VDDL (Core)	Power (+5V)	6	I	53, 68, 105, 144, 157, 167	Five volt power supply pins for core. Liberal .01 μ F to .1 μ F decoupling capacitors should be placed near the PCI 9080.
VDDH (PCI)	Power (+5V or +3.3V)	3	I	38, 60, 83	Power supply pins for PCI Bus pins. Liberal .01 μ F to .1 μ F decoupling capacitors should be placed near the PCI 9080.
VDDH (Local)	Power (+5V)	3	I	1, 124, 184	Power supply pins for Local Bus pins. Liberal .01 μ F to .1 μ F decoupling capacitors should be placed near the PCI 9080.
VSS	Ground	20	I	22, 37, 45, 52, 59, 67, 75, 82, 90, 98, 104, 114, 123, 134, 143, 156, 166, 183, 193, 208	Ground pins.

Table 5-3. Serial EEPROM Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
EECS	Serial EEPROM Chip Select	1	O TP 8 mA	176	Serial EEPROM chip select.
EEDI	Serial EEPROM Data IN	1	O TP 8 mA	172	Write data to serial EEPROM.
EEDO	Serial EEPROM Data OUT	1	I	171	Read data from serial EEPROM.
EESK	Serial Data Clock	1	O TP 8 mA	173	Serial EEPROM clock.
SHORT#	Load Short	1	I	174	When active low, only five 32-bit registers are loaded from the serial EEPROM. When active high, all Local Configuration registers are also loaded from serial EEPROM.
EESEL	Serial EEPROM Select	1	I	175	When high, use 93CS46 (1K bit) serial EEPROM. When low, use 93CS56 (2K bit) serial EEPROM.

Note: Serial EEPROM interface operates at the core voltage (+5V). The PCI 9080 requires the use of a serial EEPROM that can operate up to 1 MHz.

Table 5-4. PCI System Bus Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
AD[31:0]	Address and Data	32	I/O TS PCI	32-36, 39-44, 46-47, 76-81, 84-89, 91-97	All multiplexed on the same PCI pins. Bus transaction consists of an Address phase followed by one or more Data phases. The PCI 9080 supports both Read and Write bursts.
C/BE[3:0]#	Bus Command and Byte Enables	4	I/O TS PCI	70-73	All multiplexed on the same PCI pins. During Address phase of a transaction, C/BE[3:0]# defines the bus command. During Data phase C/BE[3:0]# are used as Byte Enables. Refer to PCI Specification v2.1 for further detail.
CLK	Clock	1	I	54	Provides timing for all transactions on PCI and is an input to every PCI device. PCI operates up to 33 MHz.
DEVSEL#	Device Select	1	I/O STS PCI	64	When actively driven, indicates driving device has decoded its address as Target of current access. As an input, indicates whether any device on bus is selected.
FRAME#	Cycle Frame	1	I/O STS PCI	57	Driven by current Master to indicate beginning and duration of an access. FRAME# is asserted to indicate a bus transaction is beginning. While FRAME# is asserted, Data transfers continue. When FRAME# is de-asserted, transaction is in final Data phase.
GNT#	Grant	1	I	51	Indicates to agent that access to bus is granted. Every Master has its own REQ# and GNT#.
IDSEL	Initialization Device Select	1	I	63	Used as chip select during configuration Read and Write transactions.
INTA#	Interrupt A	1	O OC PCI	55	Used to request interrupt.
IRDY#	Initiator Ready	1	I/O STS PCI	61	Indicates ability of initiating agent (Bus Master) to complete current Data phase of transaction.
LOCK#	Lock	1	I/O STS PCI	69	Indicates an atomic operation that may require multiple transactions to complete.
PAR	Parity	1	I/O TS PCI	74	Even parity across AD[31:0] and C/BE[3:0]#. All PCI agents require parity generation. PAR is stable and valid one clock after Address phase. For Data phases, PAR is stable and valid one clock after either IRDY# is asserted on a Write transaction or TRDY# is asserted on a Read transaction. Once PAR is valid, it remains valid until one clock after completion of current Data phase.
PERR#	Parity Error	1	I/O STS PCI	65	Reporting of data parity errors during all PCI transactions, except during a Special Cycle.
REQ#	Request	1	O PCI	50	Indicates to arbiter that this agent needs to use the bus. Every Master has its own GNT# and REQ#.
RST#	Reset	1	I	56	Used to bring PCI-specific registers, sequencers and signals to a consistent state.
SERR#	Systems Error	1	O OC PCI	66	Reports address parity errors, data parity errors on Special Cycle command, or any other system error where result will be catastrophic.
STOP#	Stop	1	I/O STS PCI	62	Indicates current Target is requesting Master to stop current transaction.
TRDY#	Target Ready	1	I/O STS PCI	58	Indicates ability of Target agent (selected device) to complete current Data phase of transaction.

Table 5-5. Local Bus Mode and Processor Independent Interface Pin Description

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADMODE	Address Decode Mode	1	I	20	Determines how S[2:0] are used to access the PCI 9080 Internal registers.
BIGEND#	Big Endian Select	1	I	48	Can be asserted during Local Bus Address phase of Direct Master transfer or Configuration Register access to specify use of Big Endian byte ordering. Big Endian byte order for Direct Master transfers or Configuration Register accesses is also programmable through Configuration registers.
BPCLKo	Buffered PCI Clock Output	1	O TP 8 mA	168	Provides a buffered PCI clock output.
BREQ	Bus Request	1	I	169	Asserted to indicate a Local Bus Master requires the bus. If enabled through the PCI 9080 Configuration registers, the PCI 9080 releases bus during a DMA transfer if this signal is asserted.
BREQo	Bus Request Out	1	O TP 8 mA	21	Asserted to indicate the PCI 9080 requires bus to perform a direct PCI-to-Local Bus access while a Direct Master access is pending on Local Bus. It can be used with external logic to generate Backoff to a Local Bus Master. Its operational parameters are set up through the PCI 9080 Configuration registers.
BTERMo#	Burst Terminate Out	1	O DTS 8 mA	28	Asserted, along with READYo#, to request break up of a burst and start of a new Address cycle (Abort only).
DACK[1:0]#	DMA Acknowledge Outputs	2	O TP 8 mA	25, 30	When a channel is programmed through the Configuration registers to operate in Demand mode, its DACK output indicates a DMA transfer is being executed. DACK0# corresponds to the PCI 9080 DMA Ch 0 and DACK1# to DMA Ch 1.
DMPAF#	Direct Master Programmable Almost Full	1	O TP 8 mA	8	Direct Master Write FIFO almost full status output. Programmable through a Configuration register.
DP[3:0]	Data Parity	4	I/O TS 8 mA	12-15	Parity is even for each of up to four byte lanes on Local Bus. Parity is checked for writes to the PCI 9080 or reads by the PCI 9080. Parity is generated for reads from the PCI 9080 or writes by the PCI 9080.
DREQ[1:0]#	DMA Request Inputs	2	I	24, 29	When a channel is programmed through the Configuration registers to operate in Demand mode, its DREQ input serves as a DMA request. DREQ0# corresponds to the PCI 9080 DMA Ch 0 and DREQ1# to DMA Ch 1.
LDShOLD	Direct Slave HOLD Request	1	O TP 8 mA	165	Asserted concurrent with LHOLD to indicate the PCI 9080 is requesting use of Local Bus to perform a Direct Slave transfer.
LINTi#	Local Interrupt In	1	I	151	When asserted low, causes a PCI interrupt.
LINTo#	Local Interrupt Out	1	O TP 8 mA	152	Synchronous level output that remains asserted as long as an interrupt condition exists. If an edge level interrupt is required, disabling and then enabling Local interrupts through the Interrupt Control/Status register (INTCSR) creates an edge if the interrupt condition still exists or a new interrupt condition occurs.
LLOCKo#	Bus Lock	1	O TP 8 mA	7	Indicates an atomic operation for a Direct Slave PCI-to-Local Bus access may require multiple transactions to complete.
LRESETi#	Local Reset Input	1	I	150	Resets Local Bus portion of the PCI 9080, Local Configuration registers and DMA Configuration registers. Also causes local reset output to be asserted.

Table 5-5. Local Bus Mode and Processor Independent Interface Pin Description (continued)

Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function															
LSERR#	System Error Interrupt Output	1	O TP 8 mA	23	Synchronous level output asserted when PCI Bus Target Abort or Master Abort Status bit is set in PCI Status Configuration register. If an edge level interrupt is required, disabling and then enabling LSERR# interrupts through interrupt/control status creates an edge if interrupt condition still exists or new interrupt condition occurs.															
MODE[1:0]	Bus Mode	2	I	9, 10	Selects bus operation mode of the PCI 9080: <table border="1"> <thead> <tr> <th>Bit 1</th> <th>Bit 0</th> <th>Bus Mode</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>C</td> </tr> <tr> <td>0</td> <td>1</td> <td>J</td> </tr> <tr> <td>1</td> <td>0</td> <td>S</td> </tr> <tr> <td>1</td> <td>1</td> <td>Reserved</td> </tr> </tbody> </table>	Bit 1	Bit 0	Bus Mode	0	0	C	0	1	J	1	0	S	1	1	Reserved
Bit 1	Bit 0	Bus Mode																		
0	0	C																		
0	1	J																		
1	0	S																		
1	1	Reserved																		
NB#	No Local Bus Initialization	1	I	26	Externally forces Local Init Done bit in Init Control Register to 1. Init Done bit is also programmable through Local Bus Configuration accesses. The PCI 9080 issues Retrys to all PCI accesses until Local Init Done bit is set. If this bit is not going to be set by a Local processor, tie NB# low.															
PCHK#	Data Parity Check	1	O TP 8 mA	16	Parity is checked for writes to the PCI 9080 or reads by the PCI 9080. Parity is checked for each byte lane with its byte enable asserted. Asserted in Clock cycle following data being checked if a parity error is detected.															
S[2:0]	Address Select	3	I	17-19	If ADMODE is high, internal PCI 9080 registers are selected when LA[31:29] match S[2:0]. If ADMODE is low, internal PCI 9080 registers are selected when S0 is asserted low.															
USERI	User Input	1	I	31	General-purpose input that can be read from the PCI 9080 Configuration registers.															
USERO	User Output	1	O TP 12 mA	27	General-purpose output controlled from the PCI 9080 Configuration registers.															
WAITI#	Wait Input	1	I	6	Can be asserted to cause the PCI 9080 to insert wait states for Local Direct Master accesses to PCI Bus. Can be thought of as a ready input for Direct Master accesses.															
WAITO#	Wait Out	1	O TS 8 mA	149	Indicates the PCI 9080 programmable wait state generator status. WAITO# is asserted when wait states are being caused by internal wait state generator. Can be thought of as an output providing Ready Out status.															

5.3 C Bus Mode Pin Out

Table 5-6. C Bus Mode Interface Pin Description

C Mode Bus Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ADS#	Address Strobe	1	I/O TS 12 mA	154	Indicates a valid address and start of a new Bus access. Asserted for first clock of a Bus access.
BLAST#	Burst Last	1	I/O TS 8 mA	155	Signal driven by current Local Bus Master to indicate last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	146	For processors that burst up to four Lwords. If Bterm is disabled through the PCI 9080 Configuration registers, the PCI 9080 also bursts up to four Lwords. If enabled, the PCI 9080 continues to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9080 programmable wait state generator.
DEN#	Data Enable	1	O TS 12 mA	145	Used in conjunction with DT/R# to provide control for data transceivers attached to Local Bus.
DT/R#	Data Transmit/Receive	1	O TS 12 mA	138	Used in conjunction with DEN# to provide control for data transceivers attached to Local Bus. When asserted, signal indicates the PCI 9080 receives data.
LW/R#	Write/Read	1	I/O TS 12 mA	137	Asserted low for reads and high for writes.
LLOCK#	Bus Lock	1	I	153	Indicates an atomic operation that may require multiple transactions to complete. Used by the PCI 9080 for Direct Local access to PCI Bus.
LA[31:2]	Address Bus	30	I/O TS 8 mA	136, 135, 133-125, 122-115, 113-106, 103-101	Carries upper 30 bits of physical address bus. During bursts, LA[31:2] increment to indicate successive Data cycles.
LD[31:0]	Data Bus	32	I/O TS 8 mA	177-182, 185-192, 194-207, 2-5	Carries 32-, 16-, or 8-bit data quantities depending on bus width configuration.

Table 5-6. C Bus Mode Interface Pin Description (continued)

C Mode Bus Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LBE[3:0]#	Byte Enables	4	I/O TS 12 mA	139-142	<p>Encoded, based on configured bus width, as follows:</p> <p>32-bit bus: For a 32-bit bus, the four byte enables indicate which of the four bytes are active during a Data cycle: BE3# Byte Enable 3—LD[31:24] BE2# Byte Enable 2—LD[23:16] BE1# Byte Enable 1—LD[15:8] BE0# Byte Enable 0—LD[7:0]</p> <p>16-bit bus: For a 16-bit bus, BE3#, BE1# and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively: BE3# Byte High Enable (BHE#)—LD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#)—LD[7:0]</p> <p>8-bit bus: For an 8-bit bus, BE1# and BE0# are encoded to provide LA1 and LA0, respectively: BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)</p>
LCLK	Local Processor Clock	1	I	160	Local clock input.
LHOLD	Hold Request	1	O TP 8 mA	158	Asserted to request use of Local Bus. The Local Bus arbiter asserts LHOLDA when control is granted.
LHOLDA	Hold Acknowledge	1	I	159	Asserted by Local Bus arbiter when control is granted in response to LHOLD. The bus should not be granted to the PCI 9080 unless requested by LHOLD.
LRESETo#	Local Bus Reset Out	1	O TP 8 mA	11	Asserted when the PCI 9080 chip is reset. Used to drive RESET# input of Local processor.
READYi#	Ready In	1	I	147	When the PCI 9080 is a Bus Master, indicates that Read data on bus is valid or that a Write Data transfer is complete. Used in conjunction with the PCI 9080 programmable wait state generator.
READYo#	Ready Out	1	O DTS 8 mA	148	When a Local Bus access is made to the PCI 9080, indicates Read data on bus is valid or a Write Data transfer is complete. READYo# can be connected to READYi#.
EOT0#	End of Transfer for DMA Ch 0	1	I	163	Terminates current DMA Ch 0 transfer.
EOT1#	End of Transfer for DMA Ch 1	1	I	164	Terminates current DMA Ch 1 transfer.

5.4 J Bus Mode Pin Out

Table 5-7. J Bus Mode Interface Pin Description

J Bus Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ALE	Address Latch Enable	1	O TS 8 mA	161	Asserted during Address phase and de-asserted before Data phase.
ADS#	Address Strobe	1	I/O TS 12 mA	154	Indicates valid address and start of a new Bus access. Asserted for first clock of a Bus access.
BLAST#	Burst Last	1	I/O TS 8 mA	155	Signal driven by current Local Bus Master to indicate last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	146	For processors that burst up to four Lwords. If Bterm is disabled through the PCI 9080 Configuration registers, the PCI 9080 also bursts up to four Lwords. If enabled, the PCI 9080 continues to burst until a BTERM# input is asserted. BTERM# is a ready input that breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9080 programmable wait state generator.
DEN#	Data Enable	1	I/O TS 12 mA	145	As an input, DEN# must only be asserted during Data phases. For processor systems in which ADS# is not asserted during Data phase, DEN# can be pulled high. As an output, DT/R# is used in conjunction with DEN# to provide control for data transceivers attached to Local Bus.
DT/R#	Data Transmit/Receive	1	O TS 12 mA	138	Used in conjunction with DEN# to provide control for data transceivers attached to Local Bus. When asserted, signal indicates the PCI 9080 receives data.
LW/R#	Write/Read	1	I/O TS 12 mA	137	Asserted low for reads and high for writes.
LABS[3:2]	Address Bus Burst	2	I/O TS 8 mA	162,163	Carries word address of 32-bit memory address. Incremented during Burst access.
LAD[31:0]	Address/Data Bus	32	I/O TS 8 mA	136, 135, 133-125, 122-115, 113-106, 103-99	During Address phase, bus carries upper 30 bits of physical address bus. During Data phase, bus carries 32 bits of data.

Table 5-7. J Bus Mode Interface Pin Description (continued)

J Mode Bus Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LBE[3:0]#	Byte Enables	4	I/O TS 12 mA	139-142	<p>Byte enables are encoded based on configured bus width as follows:</p> <p>32-Bit Bus:</p> <p>For a 32-bit bus, the four byte enables indicate which of the four bytes are active during a Data cycle:</p> <p>BE3# Byte Enable 3—LAD[31:24] BE2# Byte Enable 2—LAD[23:16] BE1# Byte Enable 1—LAD[15:8] BE0# Byte Enable 0—LAD[7:0]</p> <p>16-Bit Bus:</p> <p>For a 16-bit bus, BE3#, BE1# and BE0# are encoded to provide BHE#, LA1, and BLE#, respectively:</p> <p>BE3# Byte High Enable (BHE#)—LAD[15:8] BE2# not used BE1# Address bit 1 (LA1) BE0# Byte Low Enable (BLE#)—LAD[7:0]</p> <p>8-Bit Bus:</p> <p>For an 8-bit bus, BE1# and BE0# are encoded to provide LA1 and LA0, respectively:</p> <p>BE3# not used BE2# not used BE1# Address bit 1 (LA1) BE0# Address bit 0 (LA0)</p>
LCLK	System Clock	1	I	160	Local clock input.
LHOLD	Hold Request	1	O TP 8 mA	158	Asserted to request use of Local Bus. The Local Bus arbiter asserts LHOLDA when control is granted.
LHOLDA	Hold Acknowledge	1	I	159	Asserted by Local Bus arbiter when control is granted in response to LHOLD. The bus should not be granted to the PCI 9080 unless requested by LHOLD.
LLOCK#	Bus Lock	1	I	153	Indicates an atomic operation that may require multiple transactions to complete. Used by the PCI 9080 for Direct Local access to PCI Bus.
LRESETo#	Local Bus Reset Out	1	O TP 8 mA	11	Asserted when the PCI 9080 chip is reset.
READYi#	Ready In	1	I	147	When the PCI 9080 is a Bus Master, READYi# is used to indicate Read data on bus is valid or a Write Data transfer is complete. READYi# is used in conjunction with the PCI 9080 programmable wait state generator.
READYo#	Ready Out	1	O DTS 8 mA	148	When a Local Bus access is made to the PCI 9080, indicates that Read data on bus is valid or that a Write Data transfer is complete. READYo# can be connected to READYi#.
EOT0#	End of Transfer for DMA Ch 0	1	I	4	Terminates current DMA Ch 0 transfer.
EOT1#	End of Transfer for DMA Ch 1	1	I	5	Terminates current DMA Ch 1 transfer.

5.5 S Bus Mode Pin Out

Table 5-8. S Bus Mode Interface Pin Description

S Bus Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
ALE	Address Latch Enable	1	O TS 8 mA	161	Asserted during Address phase and de-asserted before Data phase.
AS#	Address Strobe	1	I/O TS 12 mA	154	Indicates valid address and start of a new Bus access. Asserted for first clock of a Bus access.
BLAST#	Burst Last	1	I/O TS 8 mA	155	Signal driven by current Local Bus Master to indicate last transfer in a Bus access.
BTERM#	Burst Terminate	1	I	146	For processors that burst up to eight words and do not use BTERM# input. If Bterm is disabled through the PCI 9080 Configuration registers, the PCI 9080 also bursts up to eight words. If enabled, the PCI 9080 continues to burst until a BTERM# input is asserted. BTERM# breaks up a Burst cycle and causes another Address cycle to occur. Used in conjunction with the PCI 9080 programmable wait state generator.
DEN#	Data Enable	1	O TS 12 mA	145	Used in conjunction with DT/R# to provide control for data transceivers attached to Local Bus.
DT/R#	Data Transmit/Receive	1	O TS 12 mA	138	Used in conjunction with DEN# to provide control for data transceivers attached to Local Bus. When asserted, signal indicates the PCI 9080 is receiving data.
LA[31:16]	Address Bus	16	I/O TS 8 mA	136, 135, 133-125, 122-118	Carries upper 16 bits of address.
LABS[3:1]	Address Bus Burst	3	I/O TS 8 mA	162-164	Carries word address of 32-bit memory address. Incremented during Burst access.
LAD[15:1], D0	Address/Data Bus	16	I/O TS 8 mA	117-115, 113-106, 103-99	During Address phase, carries lower physical address bits. During Data phase, carries 16 bits of data.
LBE[1:0]#	Byte Enables	2	I/O TS 12 mA	141, 142	Indicate which of the two bytes are active during a Data cycle.
LCLK	Local Clock	1	I	160	Local clock input. Note: For i960 [®] S processor systems, CLK2 input. i960 [®] S processor's RESET# input must be connected to the PCI 9080 LRESET# output. This enables the PCI 9080 to determine phase of 2x clock processor.
LHOLD	Hold Request	1	O TP 8 mA	158	Asserted to request use of Local Bus. The Local Bus arbiter asserts LHOLDA when control is granted.
LHOLDA	Hold Acknowledge	1	I	159	Asserted by Local Bus arbiter when control is granted in response to LHOLD. The bus should not be granted to the PCI 9080 unless requested by LHOLD.

Table 5-8. S Bus Mode Interface Pin Description (continued)

S Bus Mode Symbol	Signal Name	Total Pins	Pin Type	Pin Number	Function
LLOCK#	Bus Lock	1	I	153	Indicates an atomic operation that may require multiple transactions to complete. Used by the PCI 9080 for Direct Local access to PCI Bus.
LRESETo#	Local Bus Reset Out	1	O TP 8 mA	11	Asserted when the PCI 9080 chip is reset. Note: For i960 [®] S processors, this output must be used to drive Reset Input of i960 [®] S processor. Enables the PCI 9080 to determine phase of 2x clock processor.
LW/R#	Write/Read	1	I/O TS 12 mA	137	Asserted low for reads and high for writes.
READYi#	Ready In	1	I	147	When the PCI 9080 is a Bus Master, READYi# is used to indicate Read data on bus is valid or a Write Data transfer is complete. READYi# is used in conjunction with the PCI 9080 programmable wait state generator.
READYo#	Ready Out	1	O DTS 8 mA	148	When a Local Bus access is made to the PCI 9080, indicates that Read data on bus is valid or that a Write Data transfer is complete. READYo# can be connected to READYi#.
EOT0#	End of Transfer for DMA Ch 0	1	I	4	Terminates current DMA Ch 0 transfer.
EOT1#	End of Transfer for DMA Ch 1	1	I	5	Terminates current DMA Ch 1 transfer.

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6. ELECTRICAL SPECIFICATIONS

Table 6-1. Absolute Maximum Ratings

Specification	Maximum Rating
Storage Temperature	-65 °C to +150 °C
Ambient Temperature with Power Applied	-55 °C to +125 °C
Supply Voltage to Ground	-0.5V to +7.0V
Input Voltage (VIN) (5V only)	VSS -0.5V , VDD +0.5V
Output Voltage (VOUT) (5V only)	VSS -0.5V , VDD +0.5V
Input Voltage (VIN) (3V only)	VSS -0.3V , VDD +0.3V
Output Voltage (VOUT) (3V only)	VSS -0.3V , VDD +0.3V

Table 6-2. Operating Ranges

Ambient Temperature	Supply Voltage (VDD)	Input Voltage (VIN)	
		Min	Max
-40 °C to +85 °C	5V ±5%	VSS	VDD
	3V ±5%	VSS	VDD

Table 6-3. Capacitance (sample tested only)

Parameter	Test Conditions	Pin Type	Typical Value	Units
CIN	VIN = 2.0V , f = 1 MHz	Input	5	pF
COUT	VOUT = 2.0V , f = 1 MHz	Output	10	pF

Table 6-4. Electrical Characteristics Estimated over Operating Range

Parameter	Description	Test Conditions		Min	Max	Units
VOH	Output High Voltage	1.5V	IOH = -4.0 mA	2.4	Vcc	V ⁽¹⁾
VOL	Output Low Voltage		IOL per Tables	VSS	0.4	V ⁽¹⁾
VIH	Input High Level	Vcc	—	TTL = 2.0	VDD+10%	V ⁽¹⁾
VIL	Input Low Level	Vss	—	TTL = -0.5v	TTL = 0.8v	V ⁽¹⁾
VOH3	PCI 3.3V Output High Voltage	1.8V	IOH = -4.0 mA	0.9 Vcc	Vcc	V
VOL3	PCI 3.3V Output Low Voltage	1.8V	IOL per Tables	Vss	0.1 Vcc	V
VIH3	PCI 3.3V Input High Level	Vcc	—	0.5 Vcc	Vcc +0.5	V
VIL3	PCI 3.3V Input Low Level	Vss	—	-0.5 Vcc	0.3 Vcc	V
ILI	Input Leakage Current	VSS ≤ VIN ≤ VDD, VDD = Max		-10	+10	μA
IOZ	Tri-State Output Leakage Current	VDD = Max, VSS ≤ VIN ≤ VDD		-10	+10	μA
ICC	Power Supply Current	VDD=5.25V, PCLK=LCLK=33 MHz		60	130	mA

⁽¹⁾ **Note:** Assume Local = 5V PCI.

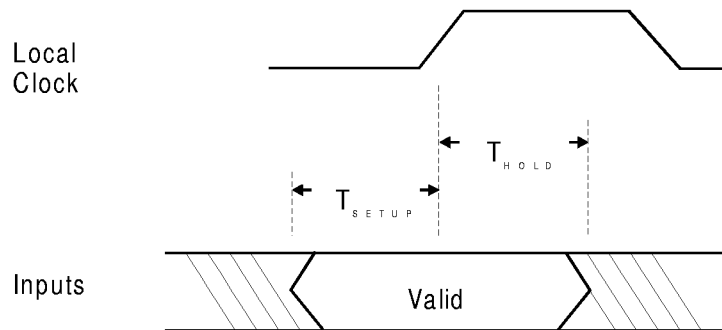


Figure 6-1. PCI 9080 Local Input Setup and Hold Waveform

Table 6-5. AC Electrical Characteristics (Local Inputs) Estimated over Operating Range

Signals (Synchronous Inputs) $C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \pm 5\%$	T_{SETUP} (ns) (WORST CASE)	T_{HOLD} (ns) (WORST CASE)
ADS#	6	1
BIGEND	4	0
BLAST#	6	0
BREQi	7	0
BTERM#	7	1
DP[3:0]	4	0
DREQ[1:0]#	3	1
EOT0#	7	1
EOT1#	1	1
LA[31:0]	5	0
LAD	5	0
LBE[3:0]#	7	0
LD[31:0]	5	0
LHOLDA	7	2
LINTi	7	0
LLOCK	4	0
LW/R#	9	0
READYi#	8	1
S[2:0]	1	2
USERi	4	0
WAITi#	13	0
Input Clocks	Min	Max
Local Clock Input Frequency	0	40 MHz
PCI Clock Input Frequency	0	33 MHz

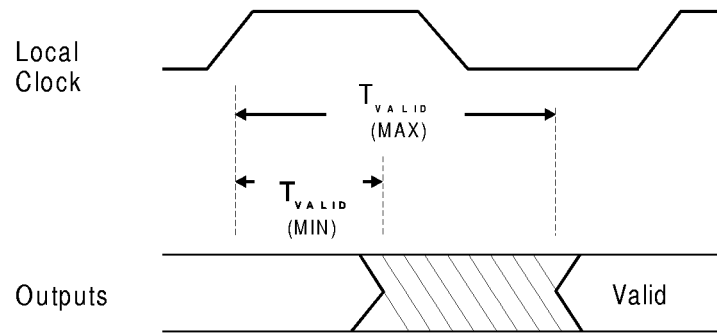


Figure 6-2. PCI 9080 Local Output Delay

Table 6-6. AC Electrical Characteristics (Local Outputs) Estimated over Operating Range

Signals (Synchronous Outputs) $C_L = 50 \text{ pF}$, $V_{CC} = 5.0 \pm 5\%$	Output $T_{VALID} (Max)$
ADS#	14.5
BLAST#	16
BREQo	13
BTERMo#	15
DACK[1:0]#	14
DEN#	13
DMPAF#	17
DP[3:0]	20
DT/R#	14
LA (Address, C Mode)	15.8
LABS[3:1]	12
LAD (Address, J Mode)	12.1
LAD (Data, J Mode)	15
LD (32- and 16-Bit Data, C Mode)	15
LD (8-Bit Data, C Mode)	20
LBE[3:0]#	16
LDSHOLD	12
LHOLD	13
LINTo#	13
LLOCKo#	12
LSERR#	12
LW/R#	14
PCHK#	12
READYo#	14
USERO	11
WAITo#	18

Note: All $T_{VALID} (Mins)$ values are greater than 5 ns.

Table 6-7. ALE Operation

Signal	T _{VALID} (ns) from Local Clock Min./Max.	Pulse Width (ns) Min./Max.
ALE	4.0 / 8.8	5.0 / 10.9
LAD[31:0]	5.5 / 12.1	N/A

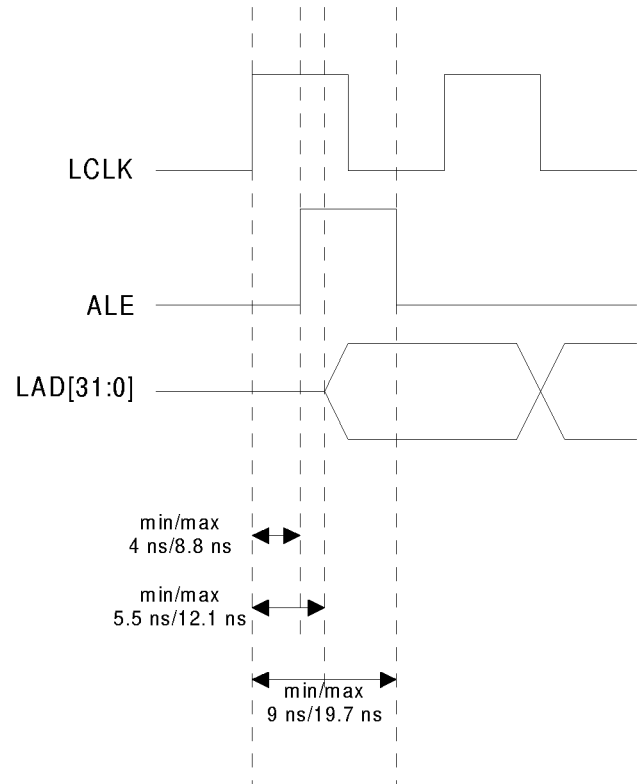


Figure 6-3. ALE Operation

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7. PACKAGE, SIGNAL, AND PIN OUT SPECS

7.1 Package Mechanical Dimensions

For 208-pin PQFP, $\theta_{JC} = 5 \text{ }^{\circ}\text{C/watt}$

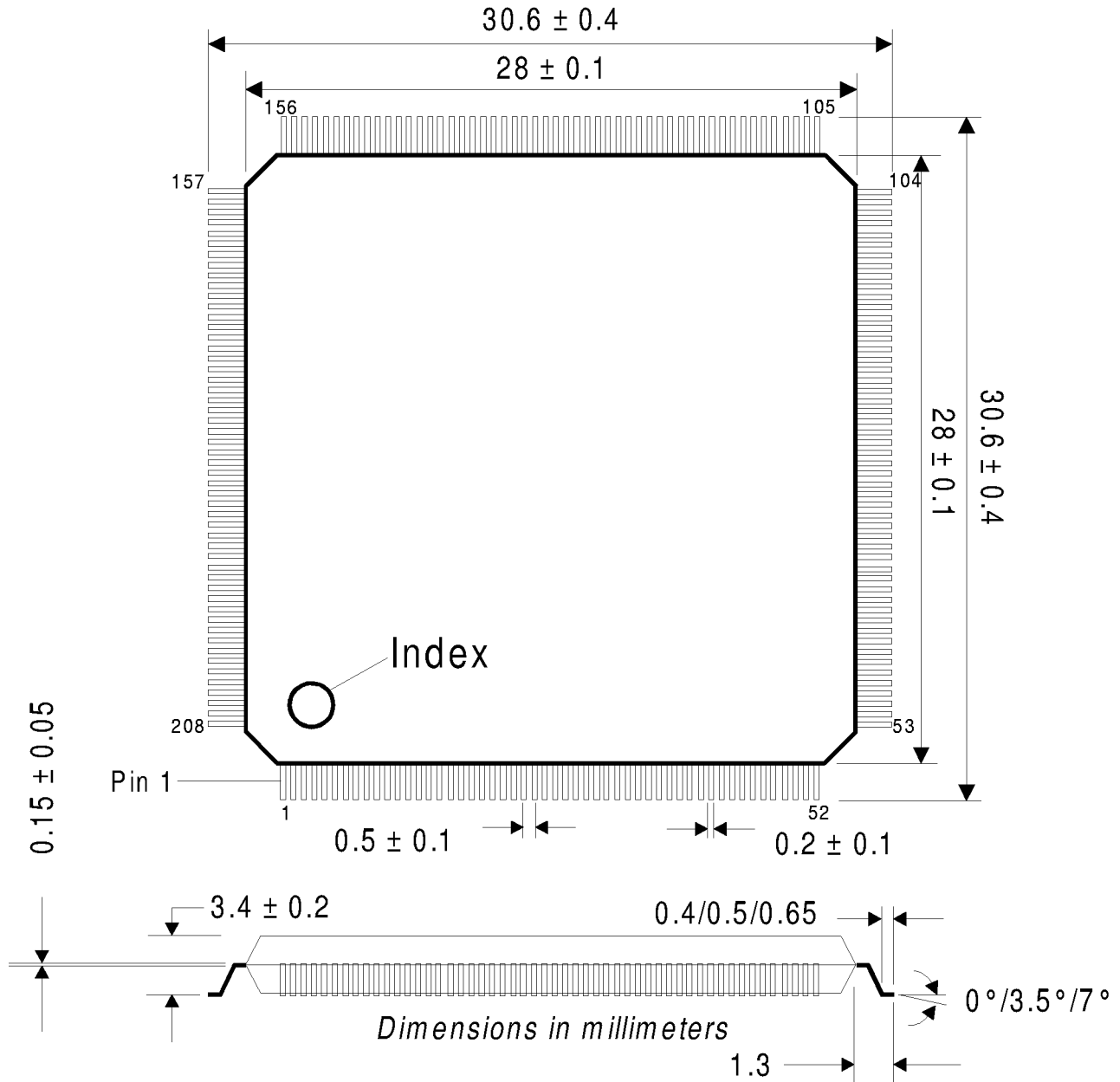


Figure 7-1. Package Mechanical Dimensions

7.2 Typical PCI Bus Master Adapter

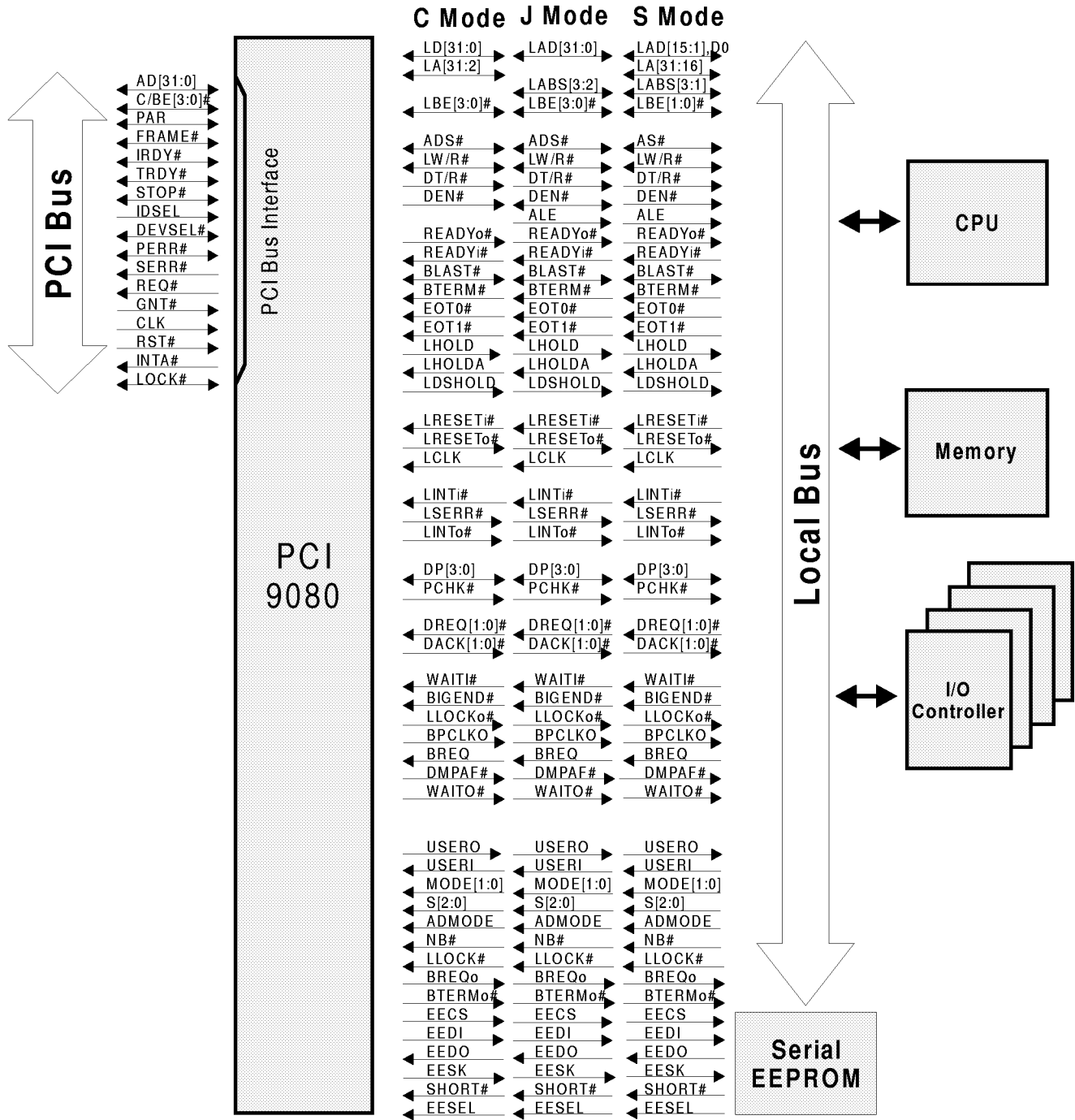


Figure 7-2. Typical PCI Bus Master Adapter

7.3 PCI 9080 Pin Out (S, J, and C Modes)

Refer to Section 5, "Pin Description," for a complete description of each pin used in S, J, and C modes.

S
J
C

Pin	S Mode	J Mode	C Mode
1	VDDH(Local)	VDDH(Local)	VDDH(Local)
2	LD3	LD2	LD1
3	NC	NC	NC
4	EOT0#	EOT1#	LD0
5	EOT1#	LD0	LD0
6	WAIT#	WAIT#	WAIT#
7	LOCK#	LOCK#	LOCK#
8	DMIPAF#	DMIPAF#	DMIPAF#
9	MODE1	MODE1	MODE1
10	MODE0	MODE0	MODE0
11	LRESET0#	LRESET0#	LRESET0#
12	DP3	DP3	DP3
13	DP2	DP2	DP2
14	DP1	DP1	DP1
15	DP0	DP0	DP0
16	PCHK#	PCHK#	PCHK#
17	S2	S2	S2
18	S1	S1	S1
19	S0	S0	S0
20	ADMODE	ADMODE	ADMODE
21	BREQ0	BREQ0	BREQ0
22	VSS	VSS	VSS
23	LSERR#	LSERR#	LSERR#
24	DREQ1#	DREQ1#	DREQ1#
25	DACK1#	DACK1#	DACK1#
26	NB#	NB#	NB#
27	USER0	USER0	USER0
28	BTERM0#	BTERM0#	BTERM0#
29	DREQ0#	DREQ0#	DREQ0#
30	DACK0#	DACK0#	DACK0#
31	USER1	USER1	USER1
32	AD31	AD31	AD31
33	AD30	AD30	AD30
34	AD29	AD29	AD29
35	AD28	AD28	AD28
36	AD27	AD27	AD27
37	VSS	VSS	VSS
38	VDDH(PCI)	VDDH(PCI)	VDDH(PCI)
39	AD26	AD26	AD26
40	AD25	AD25	AD25
41	AD24	AD24	AD24
42	AD23	AD23	AD23
43	AD22	AD22	AD22
44	AD21	AD21	AD21
45	VSS	VSS	VSS
46	AD20	AD20	AD20
47	AD19	AD19	AD19
48	BIGEND#	BIGEND#	BIGEND#
49	TEST	TEST	TEST
50	REQ#	REQ#	REQ#
51	GNT#	GNT#	GNT#
52	VSS	VSS	VSS
53	CLK	CLK	CLK
54	INTA#	INTA#	INTA#
55	INTB#	INTB#	INTB#
56	RST#	RST#	RST#
57	FRAME#	FRAME#	FRAME#
58	TRDY#	TRDY#	TRDY#
59	VSS	VSS	VSS
60	VDDH(PCI)	VDDH(PCI)	VDDH(PCI)
61	IRDY#	IRDY#	IRDY#
62	STOP#	STOP#	STOP#
63	IDSEL	IDSEL	IDSEL
64	DEVSEL#	DEVSEL#	DEVSEL#
65	PERR#	PERR#	PERR#
66	SERR#	SERR#	SERR#
67	VSS	VSS	VSS
68	VDDL(core)	VDDL(core)	VDDL(core)
69	LOCK#	LOCK#	LOCK#
70	C/BE3#	C/BE3#	C/BE3#
71	C/BE2#	C/BE2#	C/BE2#
72	C/BE1#	C/BE1#	C/BE1#
73	C/BE0#	C/BE0#	C/BE0#
74	PAR	PAR	PAR
75	VSS	VSS	VSS
76	AD18	AD18	AD18
77	AD17	AD17	AD17
78	AD16	AD16	AD16
79	AD15	AD15	AD15
80	AD14	AD14	AD14
81	AD13	AD13	AD13
82	VSS	VSS	VSS
83	VDDH(PCI)	VDDH(PCI)	VDDH(PCI)
84	AD12	AD12	AD12
85	AD11	AD11	AD11
86	AD10	AD10	AD10
87	AD9	AD9	AD9
88	AD8	AD8	AD8
89	AD7	AD7	AD7
90	VSS	VSS	VSS
91	AD6	AD6	AD6
92	AD5	AD5	AD5
93	AD4	AD4	AD4
94	AD3	AD3	AD3
95	AD2	AD2	AD2
96	AD1	AD1	AD1
97	AD0	AD0	AD0
98	VSS	VSS	VSS
99	NC	LAD0	D0
100	NC	LAD1	LAD1
101	LAD2	LAD2	LAD2
102	LAD3	LAD3	LAD3
103	LAD4	LAD4	LAD4
104	VSS	VSS	VSS
105	VDDL(core)	VDDL(core)	VDDL(core)
106	LAD5	LAD5	LAD5
107	LAD6	LAD6	LAD6
108	LAD7	LAD7	LAD7
109	LAD8	LAD8	LAD8
110	LAD9	LAD9	LAD9
111	LAD10	LAD10	LAD10
112	LAD11	LAD11	LAD11
113	LAD12	LAD12	LAD12
114	VSS	VSS	VSS
115	LAD13	LAD13	LAD13
116	LAD14	LAD14	LAD14
117	LAD15	LAD15	LAD15
118	LAD16	LAD16	LAD16
119	LAD17	LAD17	LAD17
120	LAD18	LAD18	LAD18
121	LAD19	LAD19	LAD19
122	VSS	VSS	VSS
123	VDDH(Local)	VDDH(Local)	VDDH(Local)
124	LAD20	LAD20	LAD20
125	LAD21	LAD21	LAD21
126	LAD22	LAD22	LAD22
127	LAD23	LAD23	LAD23
128	LAD24	LAD24	LAD24
129	LAD25	LAD25	LAD25
130	LAD26	LAD26	LAD26
131	LAD27	LAD27	LAD27
132	LAD28	LAD28	LAD28
133	LAD29	LAD29	LAD29
134	VSS	VSS	VSS
135	LAD30	LAD30	LAD30
136	LAD31	LAD31	LAD31
137	LWR#	LWR#	LWR#
138	DTR#	DTR#	DTR#
139	LBES3#	LBES3#	LBES3#
140	LBES2#	LBES2#	LBES2#
141	LBES1#	LBES1#	LBES1#
142	LBES0#	LBES0#	LBES0#
143	VSS	VSS	VSS
144	VDDL(core)	VDDL(core)	VDDL(core)
145	DEN#	DEN#	DEN#
146	BTERM#	BTERM#	BTERM#
147	READY#	READY#	READY#
148	READY#	READY#	READY#
149	WAIT#	WAIT#	WAIT#
150	LRESET#	LRESET#	LRESET#
151	UNTE#	UNTE#	UNTE#
152	UNTE#	UNTE#	UNTE#
153	UNTE#	UNTE#	UNTE#
154	ADS#	ADS#	ADS#
155	BLAST#	BLAST#	BLAST#
156	VSS	VSS	VSS

PCI 9080

Figure 7-3. PCI 9080 Pin Out (S, J, and C Modes)

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8. TIMING DIAGRAMS

PCI 9080 operates in three modes, selected through mode pins, corresponding to three bus types—C, J, and S. Timing Diagrams are provided for each mode. For some functions, a timing diagram may only be provided for one mode of operation. Even though a different mode is used, that timing diagram can be used to determine functionality.

8.1 LIST OF TIMING DIAGRAMS

Initialization

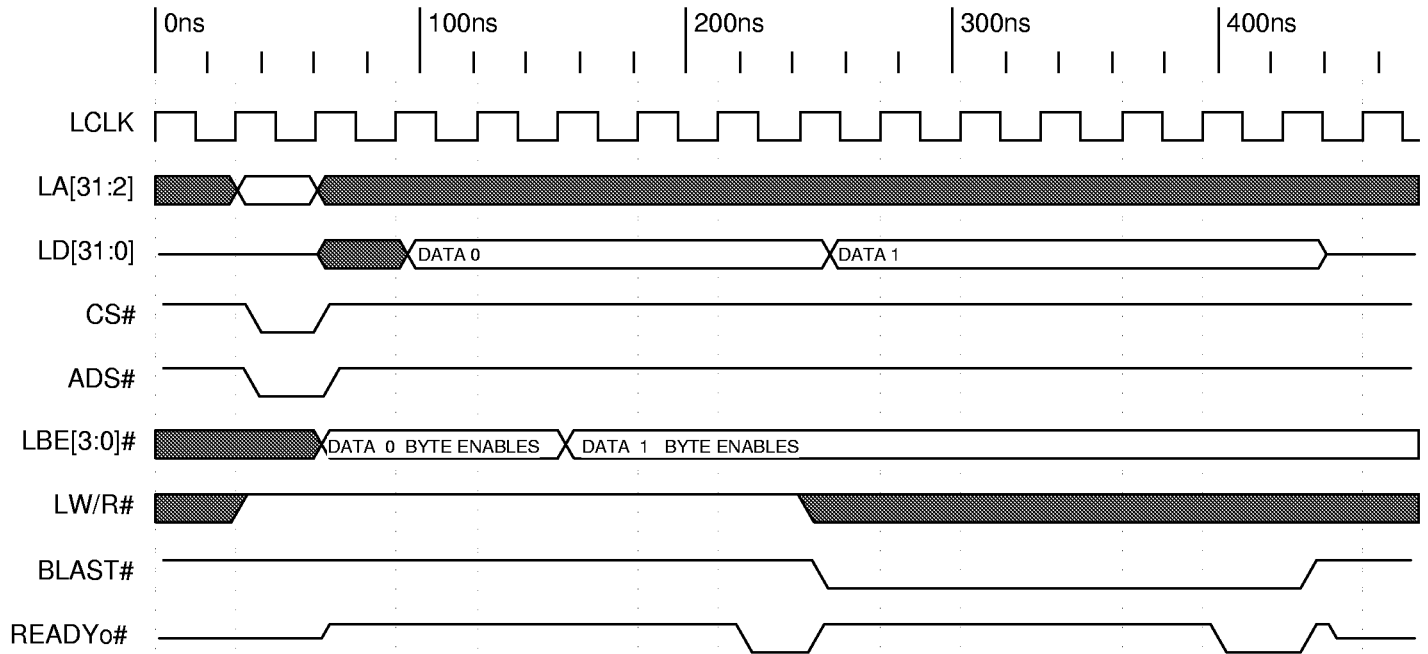
- Timing Diagram 8-1. (C, J Modes) PCI RST# Asserting Local Output LRESETo#
- Timing Diagram 8-2. (S Mode) Two Phase Clock Synchronization Using LRESETo#
- Timing Diagram 8-3. PCI 9080 Local Bus Arbitration
- Timing Diagram 8-4. PCI 9080 1K Serial EEPROM PCI Initialization
- Timing Diagram 8-5. Local Interrupt (LINTi#) Input Asserting PCI Output INTA#

C Mode Direct Slave

- Timing Diagram 8-6. (C Mode) PCI Configuration Write to PCI 9080 PCI Configuration Register
- Timing Diagram 8-7. (C Mode) PCI Configuration Read to PCI 9080 PCI Configuration Register
- Timing Diagram 8-8. (C Mode) PCI Memory Write to PCI 9080 Local Configuration Register
- Timing Diagram 8-9. (C Mode) PCI Memory Read to PCI 9080 Local Configuration Register
- Timing Diagram 8-10. (C Mode) Direct Slave Single Cycle Read
- Timing Diagram 8-11. (C Mode) Direct Slave Single Cycle Write
- Timing Diagram 8-12. (C Mode) PCI 9080 DMA or Direct Slave Burst Read from Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-13. (C Mode) DMA or Direct Slave PCI 9080 Burst Write to Local Bus, Bterm Enabled
- Timing Diagram 8-14. (C Mode) Direct Slave PCI-to-Local Burst Read, Bterm Disabled
- Timing Diagram 8-15. (C Mode) PCI 9080 DMA or Direct Slave Burst Write, Bterm Disabled
- Timing Diagram 8-16. (C Mode) Direct Slave Read with Prefetch Counter Set to 5
- Timing Diagram 8-17. (C Mode) Direct Slave or DMA Burst Write to 32-Bit Local Bus Suspended by BREQ Input
- Timing Diagram 8-18. (C Mode) Direct Slave Burst Read of Five Lwords with One Wait State
- Timing Diagram 8-19. (C Mode) Direct Slave Burst Write of Five Lwords with One Wait State
- Timing Diagram 8-20. (C Mode) Direct Slave Read 2.1 Spec
- Timing Diagram 8-21. (C Mode) Direct Slave Read No Flush Mode (Read Ahead Mode)
- Timing Diagram 8-22. (C Mode) Direct Slave Read of Two Lwords from 8-Bit Bus
- Timing Diagram 8-23. (C Mode) PCI 9080 DMA or Direct Slave Two Lword Burst Write to 8-Bit Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-24. (C Mode) Direct Slave Read of Two Lwords from 16-Bit Bus
- Timing Diagram 8-25. (C Mode) PCI 9080 DMA or Direct Slave Two Lword Burst Write to 16-Bit Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-26. (C Mode) Direct Slave Read of Two Lwords from 8-Bit I/O Local Bus, Burst Disabled
- Timing Diagram 8-27. (C Mode) Direct Slave Write of Two Lwords to 8-Bit I/O Local Bus, Burst Disabled
- Timing Diagram 8-28. (C Mode) Direct Slave in BIGEND Local Bus with BIGEND# Input or Internal Register Setting
- Timing Diagram 8-29. (C Mode) Locked Direct Slave Read Followed by Write and Release (LLOCKo#)

C Mode Direct Master

Timing Diagram 8-30. (C Mode) Local Bus Read from PCI 9080 CFG Registers



First READYo# will be delayed at least five clocks for access to shared registers

Timing Diagram 8-31. (C Mode) Local Bus Write to PCI 9080 CFG Registers

Timing Diagram 8-32. (C Mode) Local Bus Direct Master Single Memory Read

Timing Diagram 8-33. (C Mode) Local Bus Direct Master Single Memory Write Cycle

Timing Diagram 8-34. (C Mode) PCI 9080 Direct Master Memory Read, 12 Lword Burst

Timing Diagram 8-35. (C Mode) PCI 9080 Direct Master Memory Write of 12 Lwords

Timing Diagram 8-36. (C Mode) PCI 9080 Direct Master Memory Read with WAITI#

Timing Diagram 8-37. (C Mode) PCI 9080 Direct Master Memory Write with WAITI#

Timing Diagram 8-38. (C Mode) PCI 9080 Direct Master Configuration Read—Type 1 or Type 0

Timing Diagram 8-39. (C Mode) PCI 9080 Direct Master Configuration Write—Type 1 or Type 0

Timing Diagram 8-40. (C Mode) Local Bus Direct Master Read from PCI I/O

Timing Diagram 8-41. (C Mode) Direct Master Write to PCI I/O

Timing Diagram 8-42. (C Mode) PCI 9080 Direct Master Memory Read—Keep Bus

Timing Diagram 8-43. (C Mode) PCI 9080 Direct Master Memory Read—Drop Bus

Timing Diagram 8-44. (C Mode) PCI Bus Request (REQ#) Delay During Direct Master Write (8 PCI Clock Delay)

Timing Diagram 8-45. (C Mode) Direct Master Memory Read, Prefetch of 16

Timing Diagram 8-46. (C Mode) Direct Master Memory Write and Invalidate (MWI)—Cache Line Size of 8

Timing Diagram 8-47. (C Mode) Direct Master in BIGEND Local Bus with BIGEND# Input or Interrupt

Timing Diagram 8-48. (C Mode) Direct Master Burst, Memory Read Cycles (Changing LBE[3:0]#)

Timing Diagram 8-49. (C Mode) Direct Master Five Lword Burst Write (Changing LBE[3:0]#)

Timing Diagram 8-50. (C Mode) Direct Master Locked Read Followed by Write and Release (LLOCK# and LOCK#)

Timing Diagram 8-51. (C Mode) BREQo and Deadlock

C Mode DMA

Timing Diagram 8-52. (C Mode) DMA Aligned PCI Address to Aligned Local Address, Bterm Disabled

- Timing Diagram 8-53. (C Mode) DMA Aligned Local Address to Aligned PCI Address, Burst Enabled, Bterm Enabled
- Timing Diagram 8-54. (C Mode) DMA Aligned PCI Address to Aligned Local Address (External Generation of Wait States)
- Timing Diagram 8-55. (C Mode) Read of DMA Chaining Parameters from PCI and Local Buses
- Timing Diagram 8-56. (C Mode) PCI 9080 DMA Read of Chaining Parameters from Local Bus, No Wait States
- Timing Diagram 8-57. (C Mode) Read of DMA Chaining Parameters from PCI Bus (Local-to-PCI Transfer)
- Timing Diagram 8-58. (C Mode) Single Cycle DMA Demand Mode PCI-to-Local
- Timing Diagram 8-59. (C Mode) Multiple Cycle (Burst) DMA Demand Mode PCI-to-Local, No Wait States
- Timing Diagram 8-60. (C Mode) DMA Demand Mode Terminated with BLAST# (Local-to-PCI)
- Timing Diagram 8-61. (C Mode) DMA Local-to-PCI, Terminated with EOT[1:0]#
- Timing Diagram 8-62. (C Mode) DMA PCI-to-Local, Terminated with EOT[1:0]#
- Timing Diagram 8-63. (C Mode) DMA PCI-to-Local with Local Pause Timer and Local Latency Timer

J Mode Direct Slave

- Timing Diagram 8-64. (J Mode) PCI 9080 Direct Slave Burst Read from Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-65. (J Mode) PCI 9080 Direct Slave Burst Write to Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-66. (J Mode) PCI 9080 DMA or Direct Slave Burst Write to Local Bus, No Wait States, Bterm Disabled
- Timing Diagram 8-67. (J Mode) Direct Slave in BIGEND Local Bus with BIGEND# Input or Internal Register Setting
- Timing Diagram 8-68. (J Mode) Direct Slave Read v2.1 Spec
- Timing Diagram 8-69. (J Mode) Direct Slave Read No Flush Mode (Read Ahead Mode), Prefetch Mode Enabled
- Timing Diagram 8-70. (J Mode) Local Bus Read from PCI 9080 CFG Registers
- Timing Diagram 8-71. (J Mode) Local Bus Write to PCI 9080 CFG Registers

J Mode Direct Master

- Timing Diagram 8-72. (J Mode) Direct Master Read Access from PCI Bus (Keep PCI Bus If Read FIFO Full Mode), No PCI Disconnects
- Timing Diagram 8-73. (J Mode) Local Bus Direct Master Burst Write Access to PCI Bus, Continuous If Same Clock Rate and No PCI Disconnects
- Timing Diagram 8-74. (J Mode) Local Bus Direct Master Lock Memory Read Access from PCI Bus Followed by Write and Release

J Mode DMA

- Timing Diagram 8-75. (J Mode) PCI 9080 DMA Local-to-PCI, No Wait States, Bterm Enabled
- Timing Diagram 8-76. (J Mode) PCI 9080 DMA PCI-to-Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-77. (J Mode) DMA Read of Chaining Parameters, No Wait States
- Timing Diagram 8-78. (J Mode) PCI 9080 Write to Local Bus BREQ Asserted

S Mode

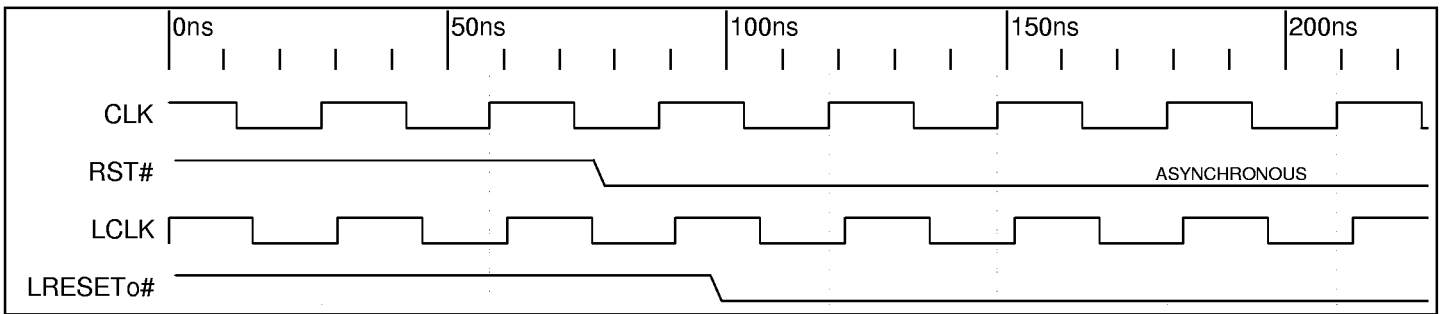
- Timing Diagram 8-79. (S Mode) PCI 9080 DMA or Direct Slave Two Lword Burst Write to 16-Bit Local Bus, No Wait States, Bterm Enabled
- Timing Diagram 8-80. (S Mode) Local Bus Read from PCI 9080 CFG Registers
- Timing Diagram 8-81. (S Mode) Local Bus Write to PCI 9080 CFG Registers

and the two I have no clue where to put...

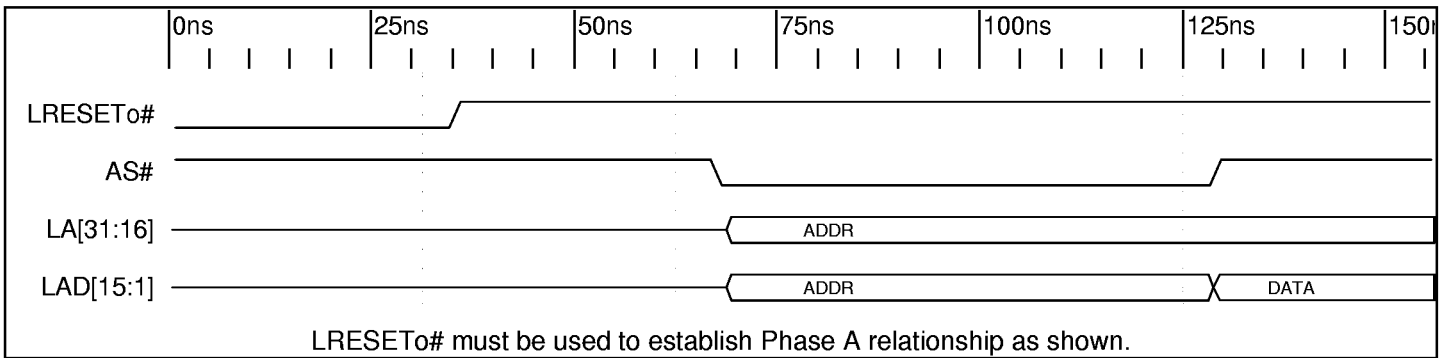
Timing Diagram 8-82. PCI 9080 Local Bus Read

Timing Diagram 8-83. PCI 9080 Local Bus Write

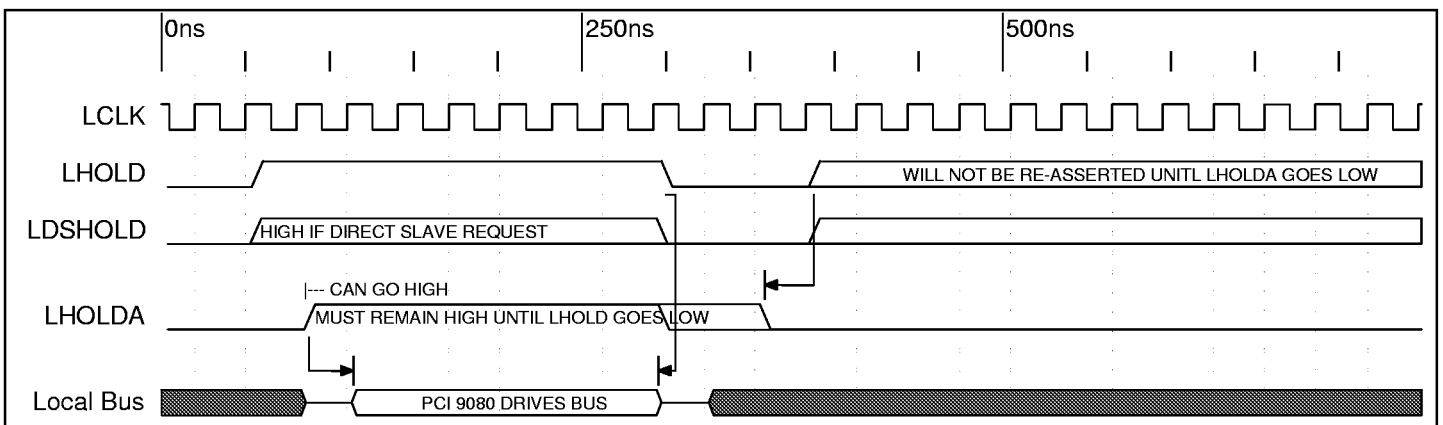
8.2 INITIALIZATION



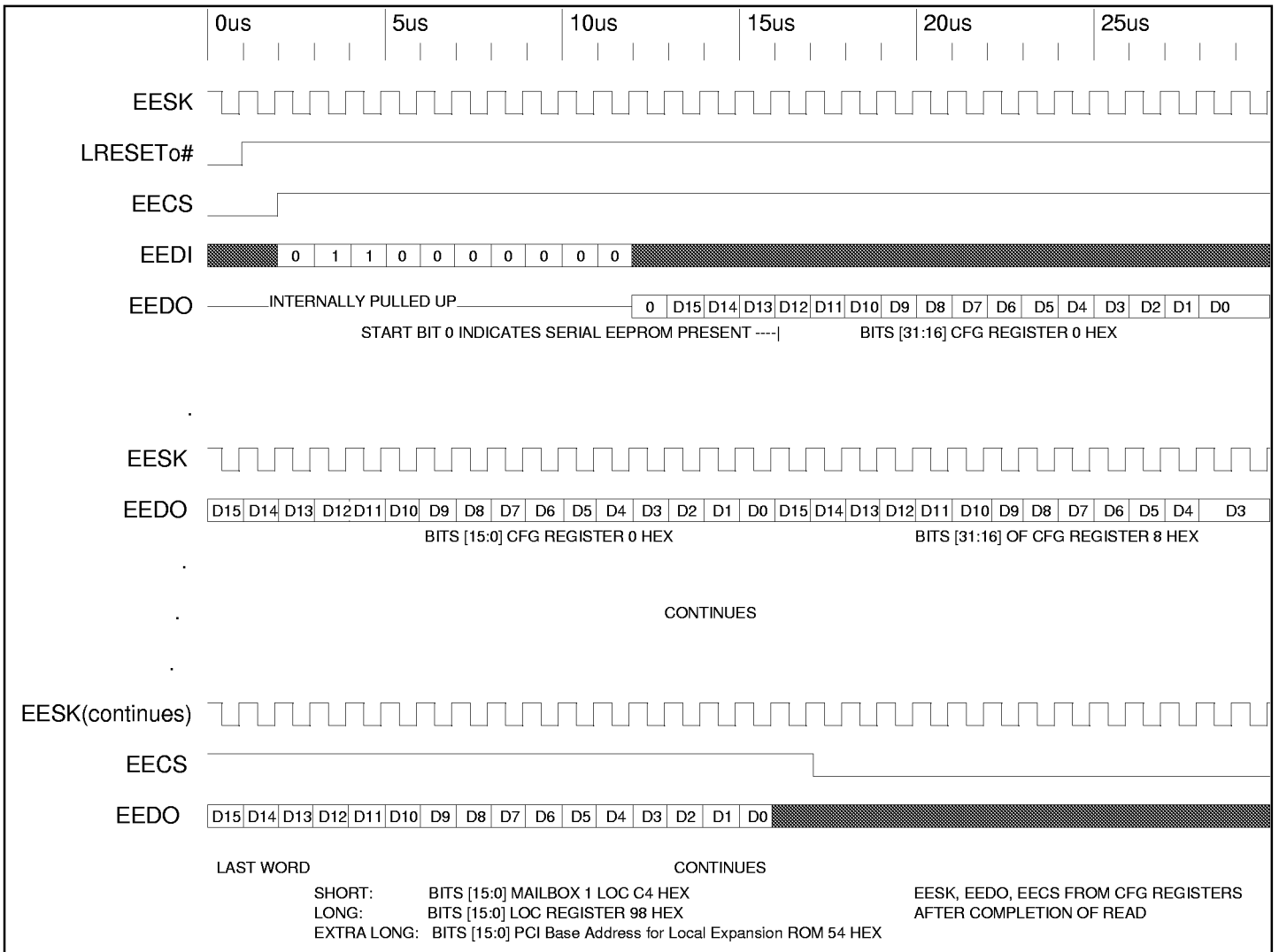
Timing Diagram 8-1. (C, J Modes) PCI RST# Asserting Local Output LRESETo#



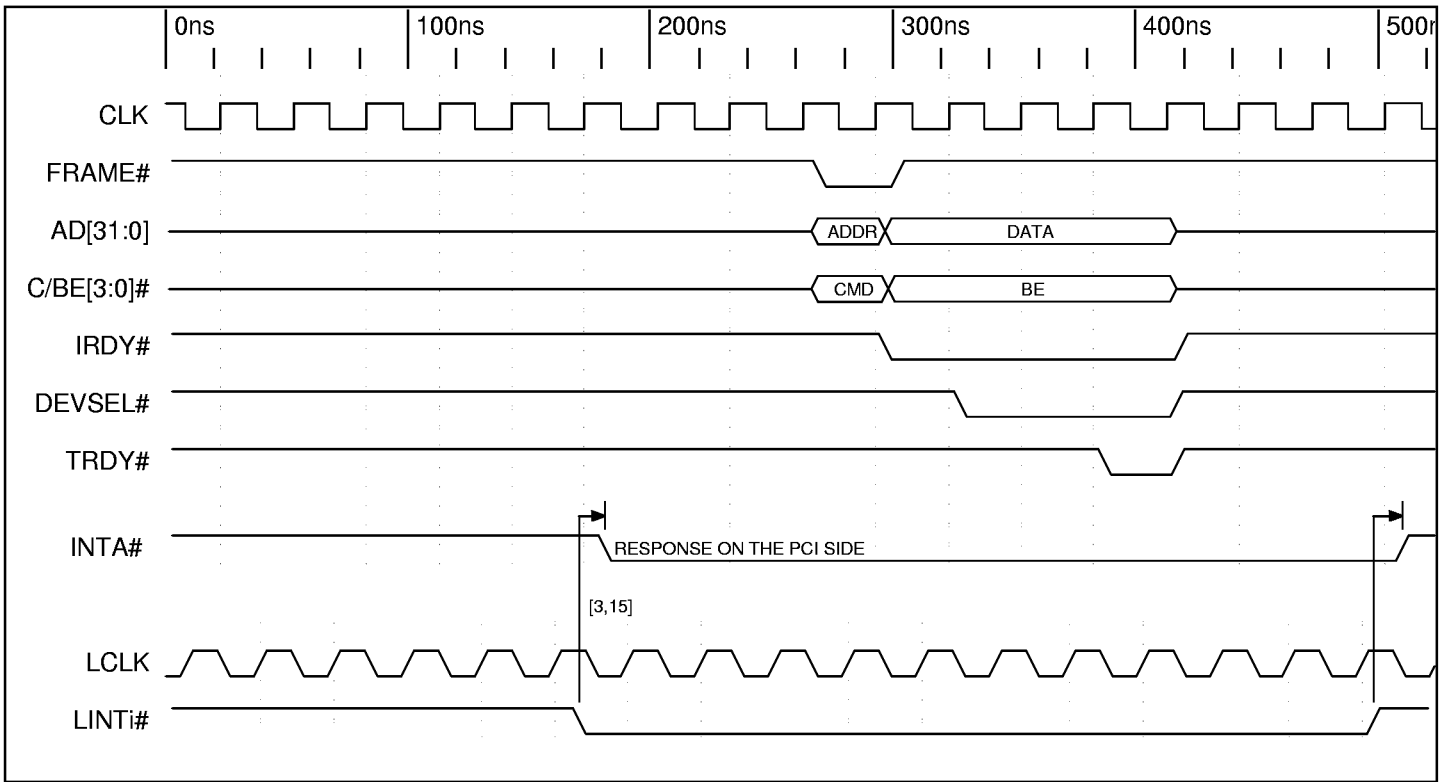
Timing Diagram 8-2. (S Mode) Two Phase Clock Synchronization Using LRESETo#



Timing Diagram 8-3. PCI 9080 Local Bus Arbitration



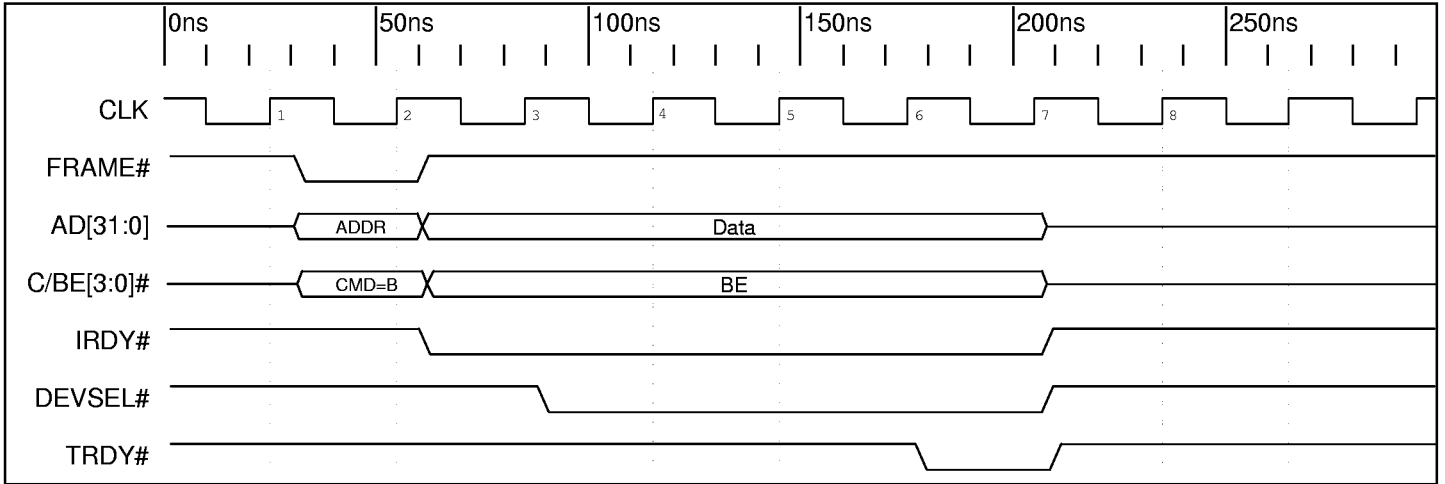
Timing Diagram 8-4. PCI 9080 1K Serial EEPROM PCI Initialization



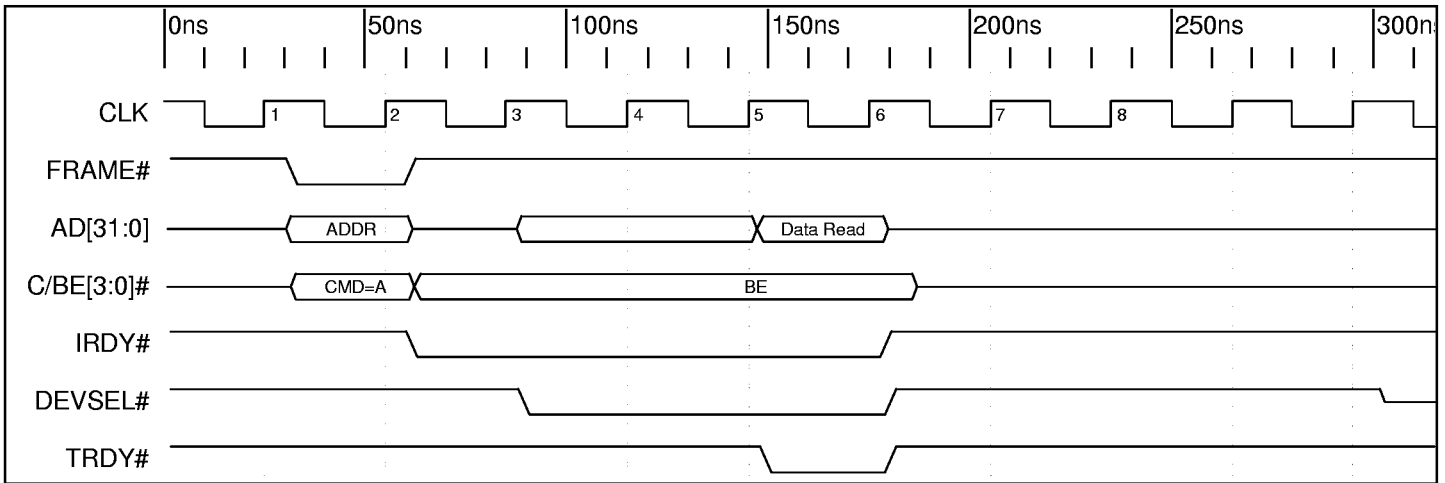
Timing Diagram 8-5. Local Interrupt (LINTi#) Input Asserting PCI Output INTA#

8.3 C MODE

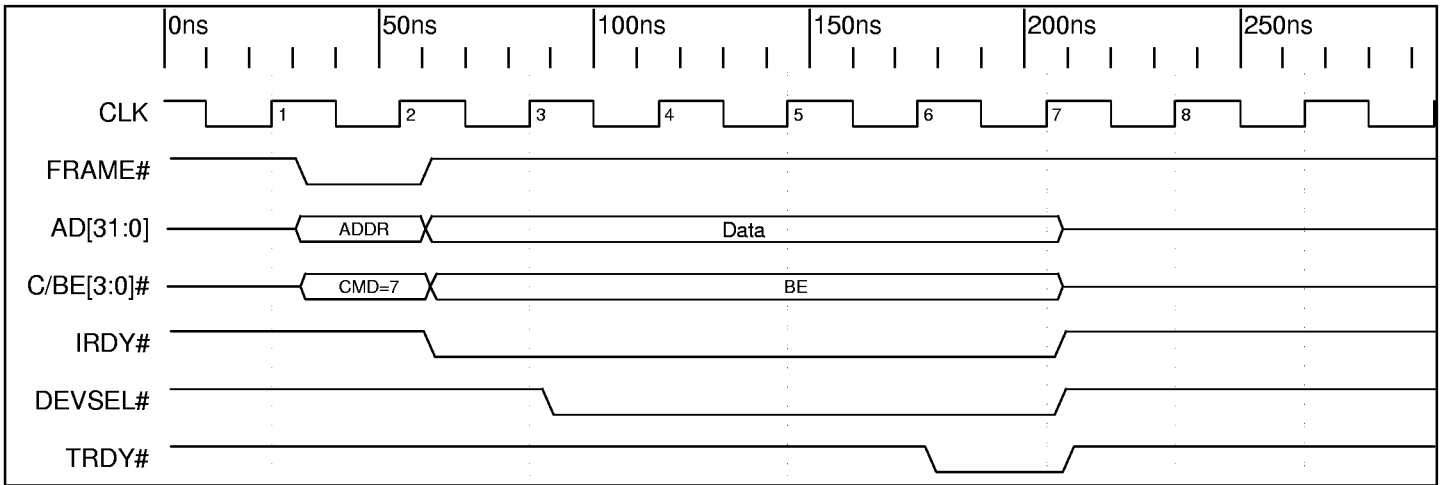
8.3.1 C Mode Direct Slave



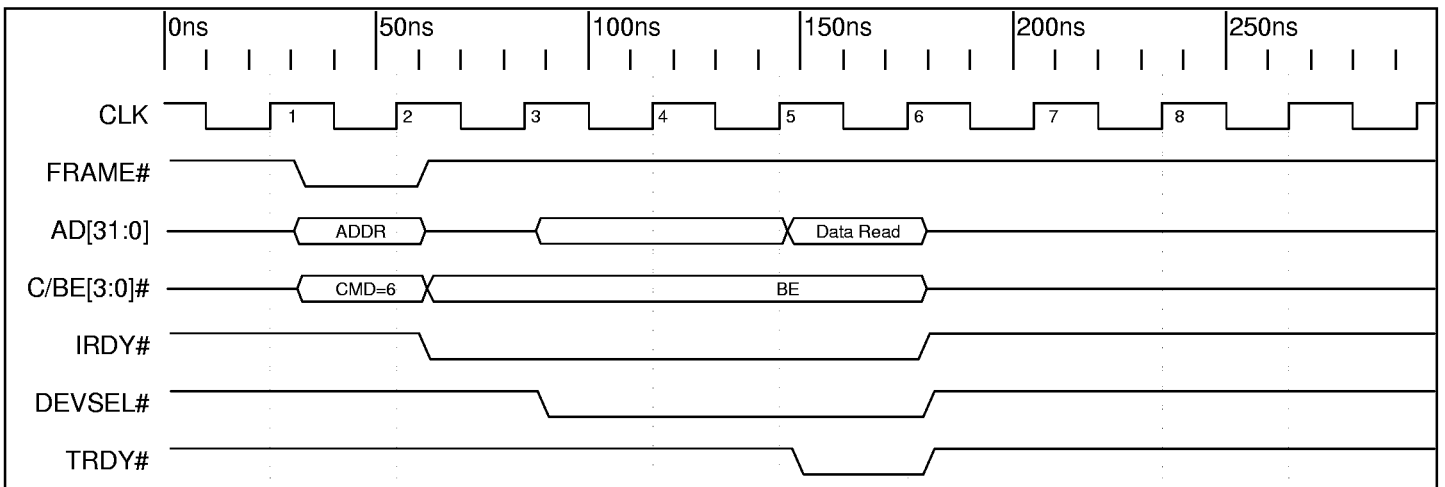
Timing Diagram 8-6. (C Mode) PCI Configuration Write to PCI 9080 PCI Configuration Register



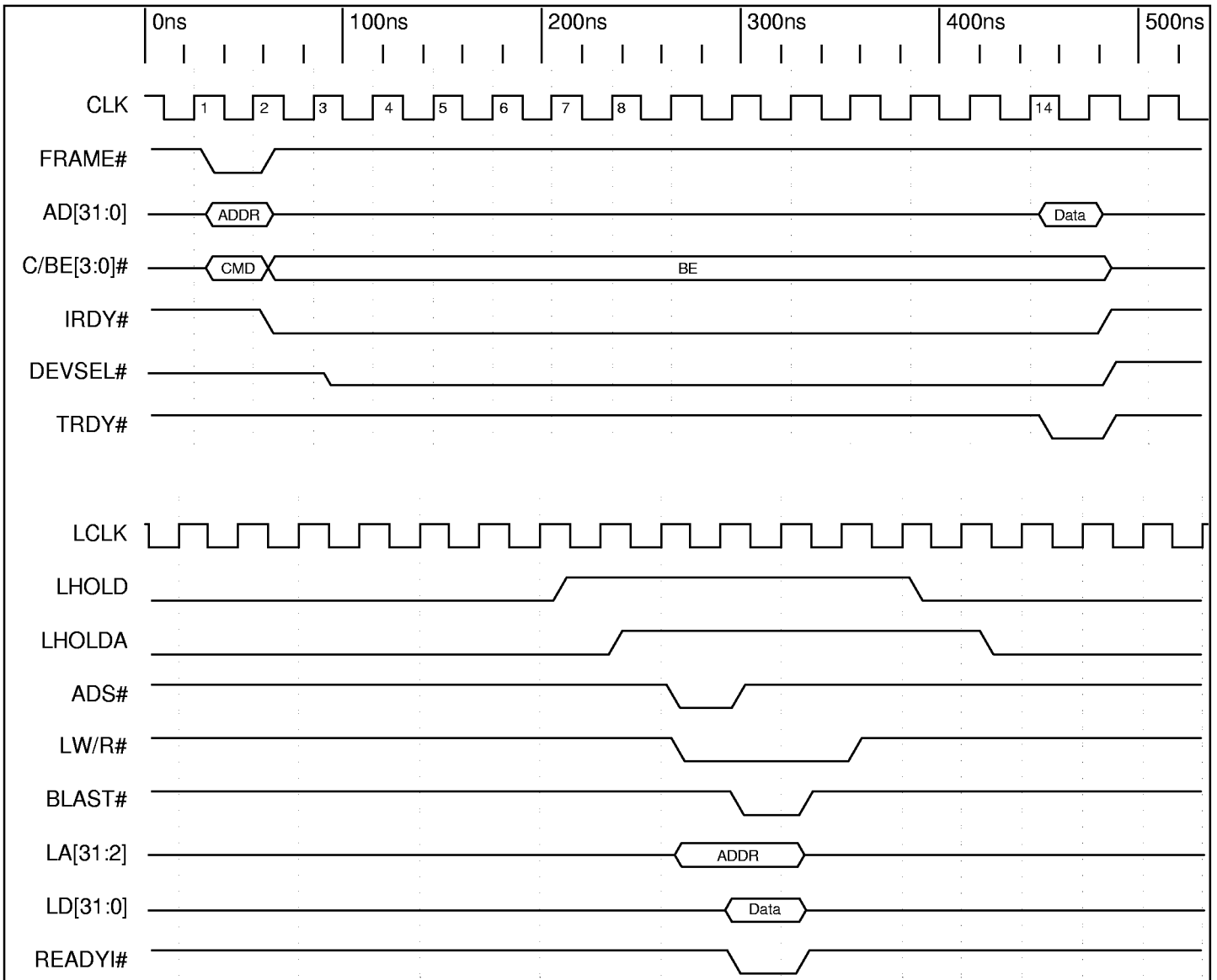
Timing Diagram 8-7. (C Mode) PCI Configuration Read to PCI 9080 PCI Configuration Register



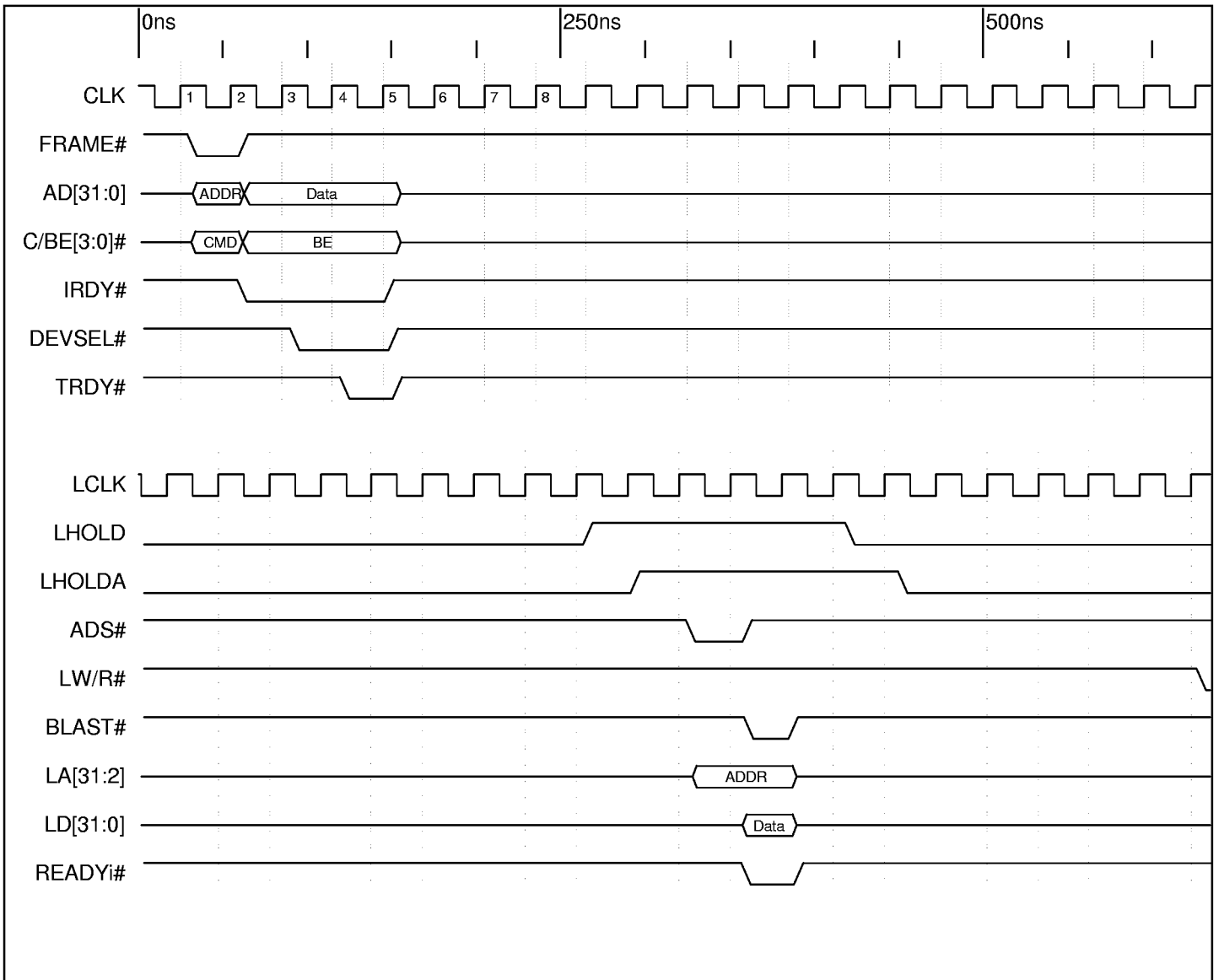
Timing Diagram 8-8. (C Mode) PCI Memory Write to PCI 9080 Local Configuration Register



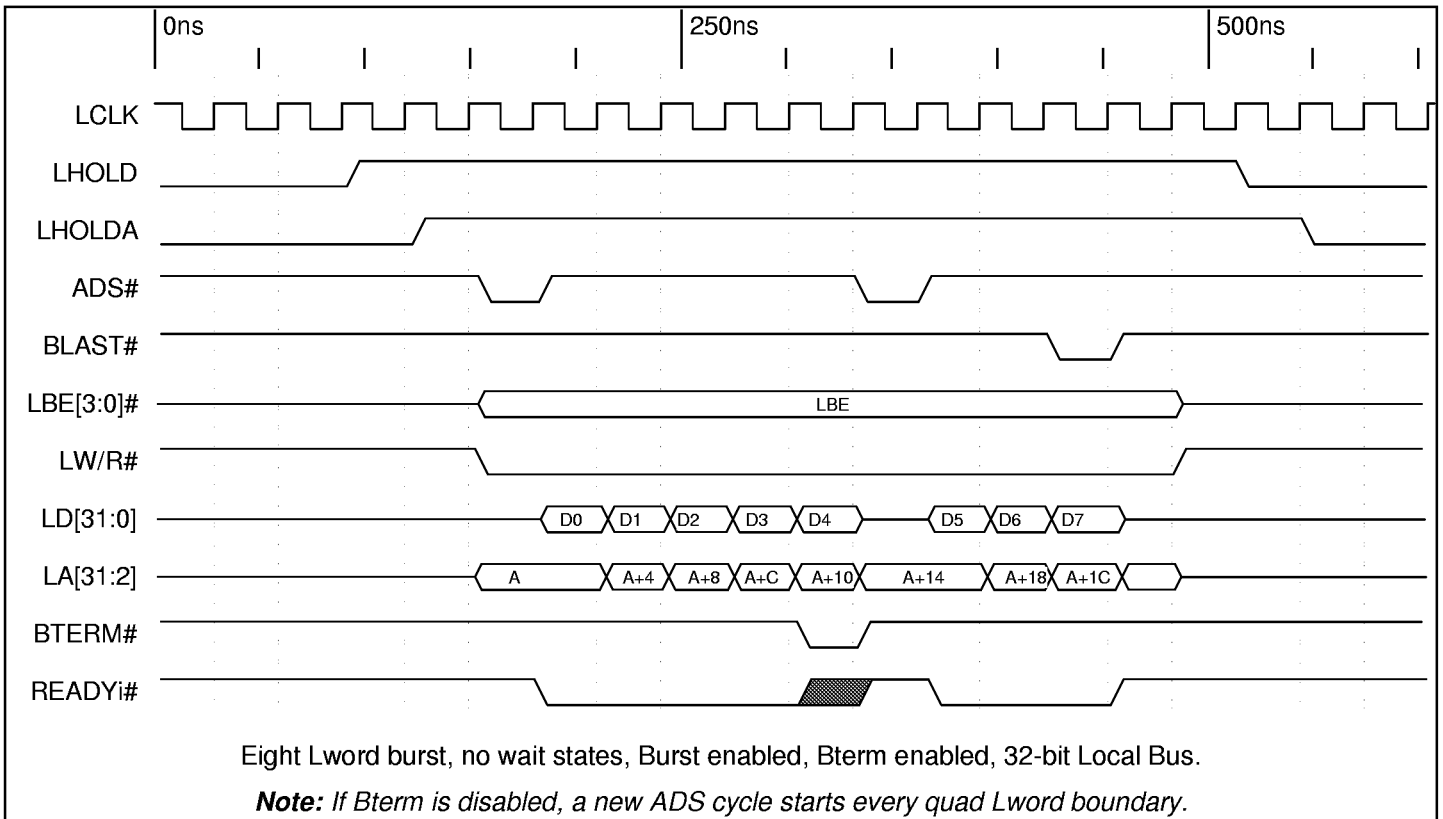
Timing Diagram 8-9. (C Mode) PCI Memory Read to PCI 9080 Local Configuration Register



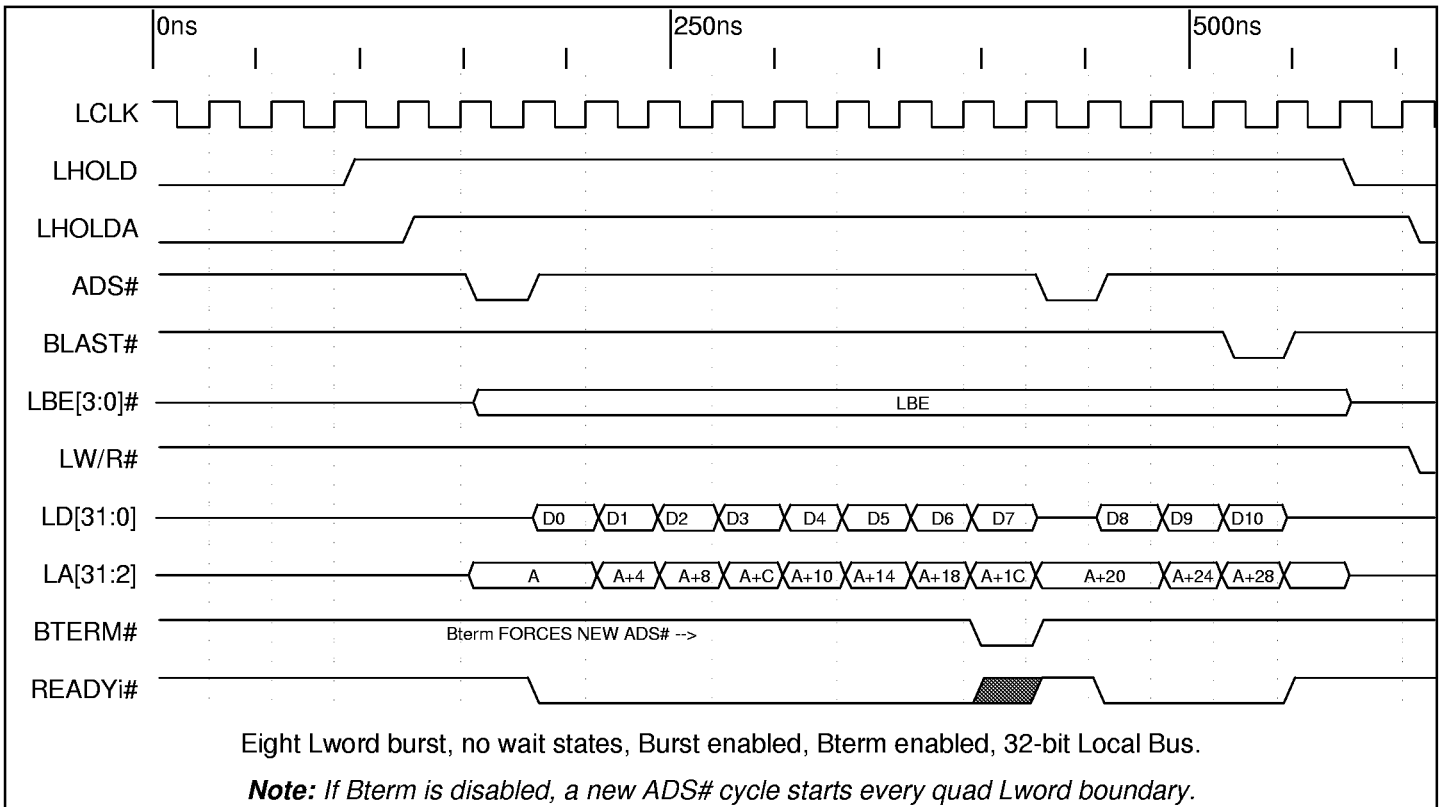
Timing Diagram 8-10. (C Mode) Direct Slave Single Cycle Read (32-Bit Local Bus)



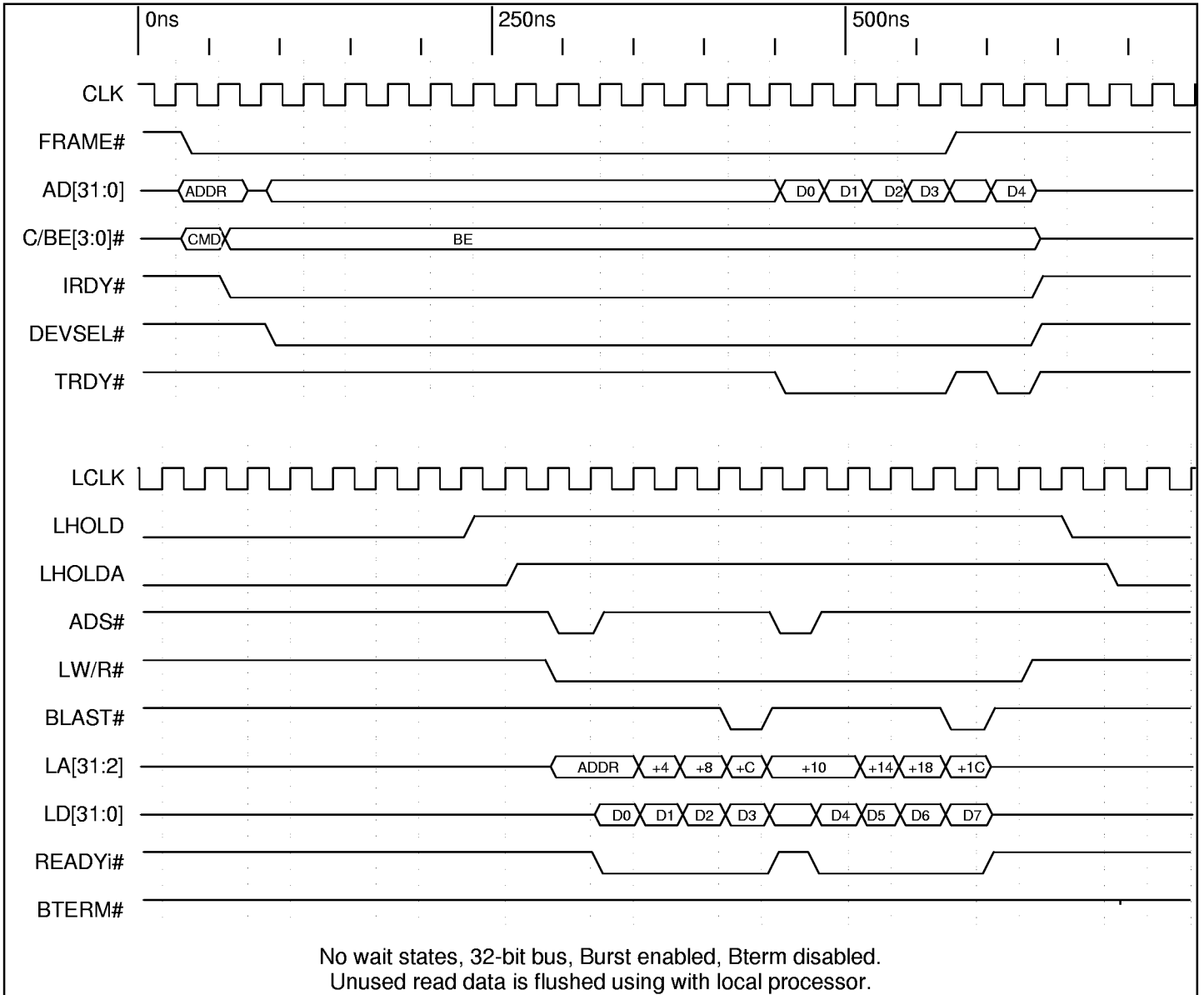
Timing Diagram 8-11. (C Mode) Direct Slave Single Cycle Write



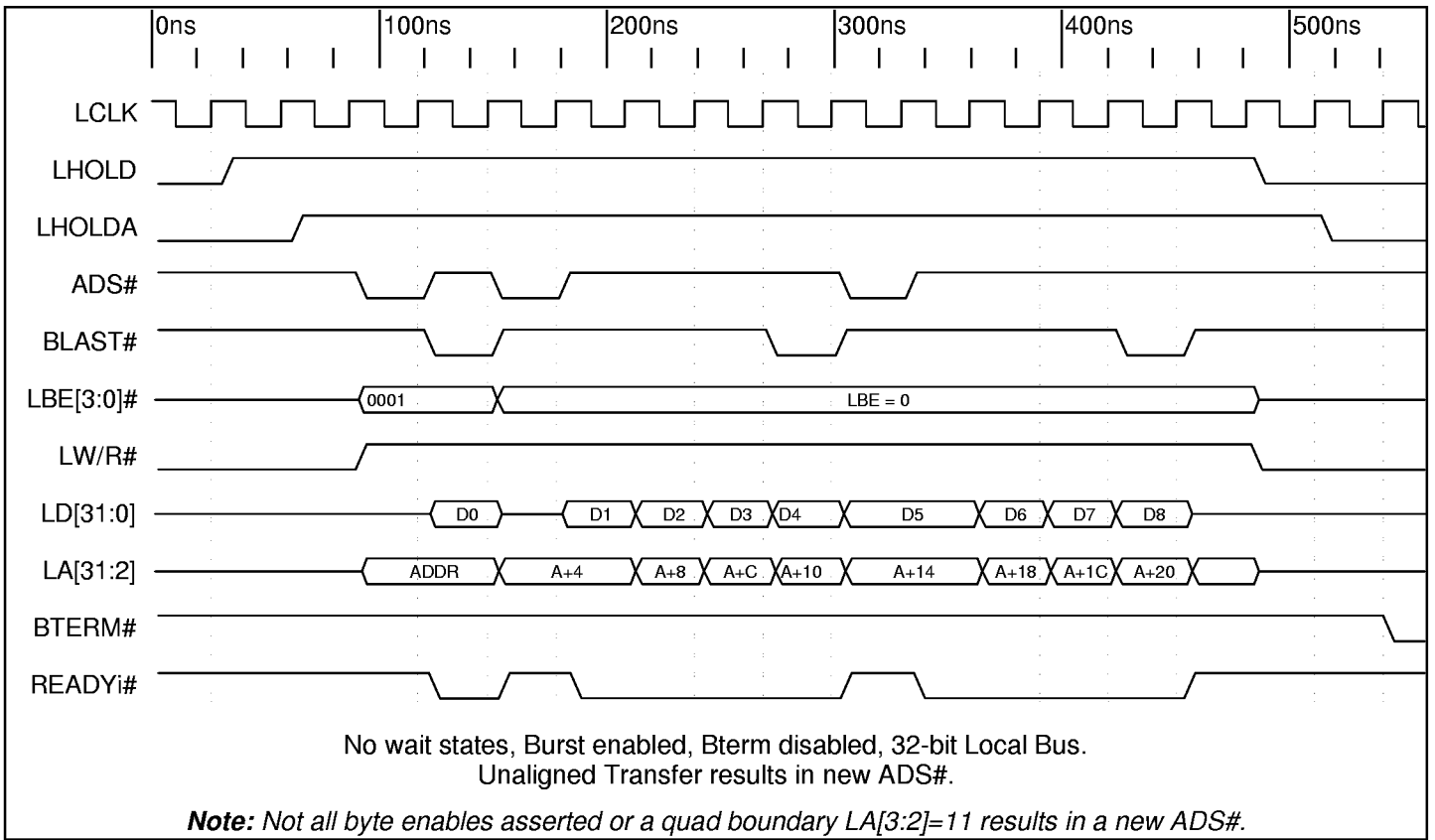
Timing Diagram 8-12. (C Mode) PCI 9080 DMA or Direct Slave Burst Read from Local Bus, No Wait States, Bterm Enabled



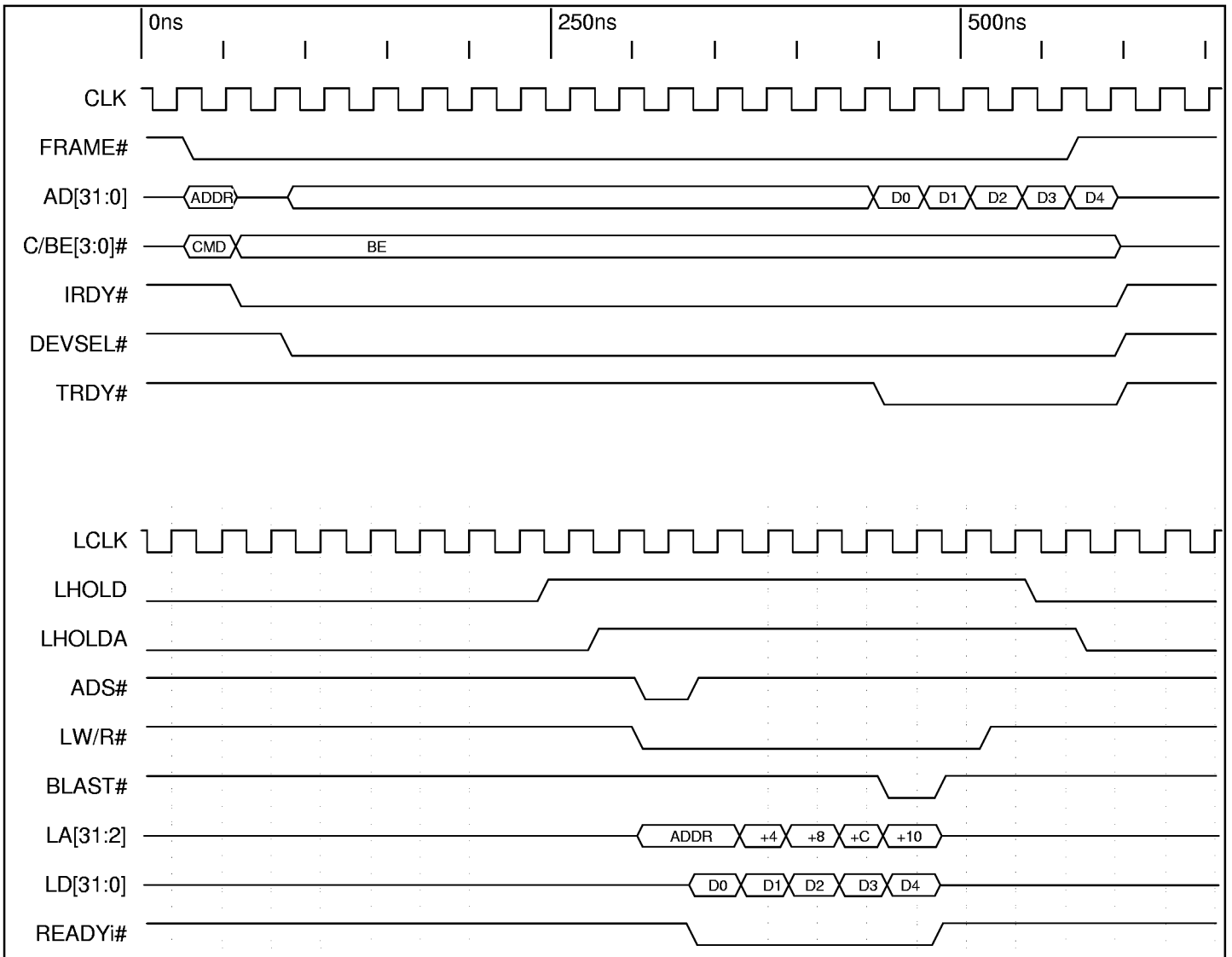
Timing Diagram 8-13. (C Mode) DMA or Direct Slave PCI 9080 Burst Write to Local Bus, Bterm Enabled



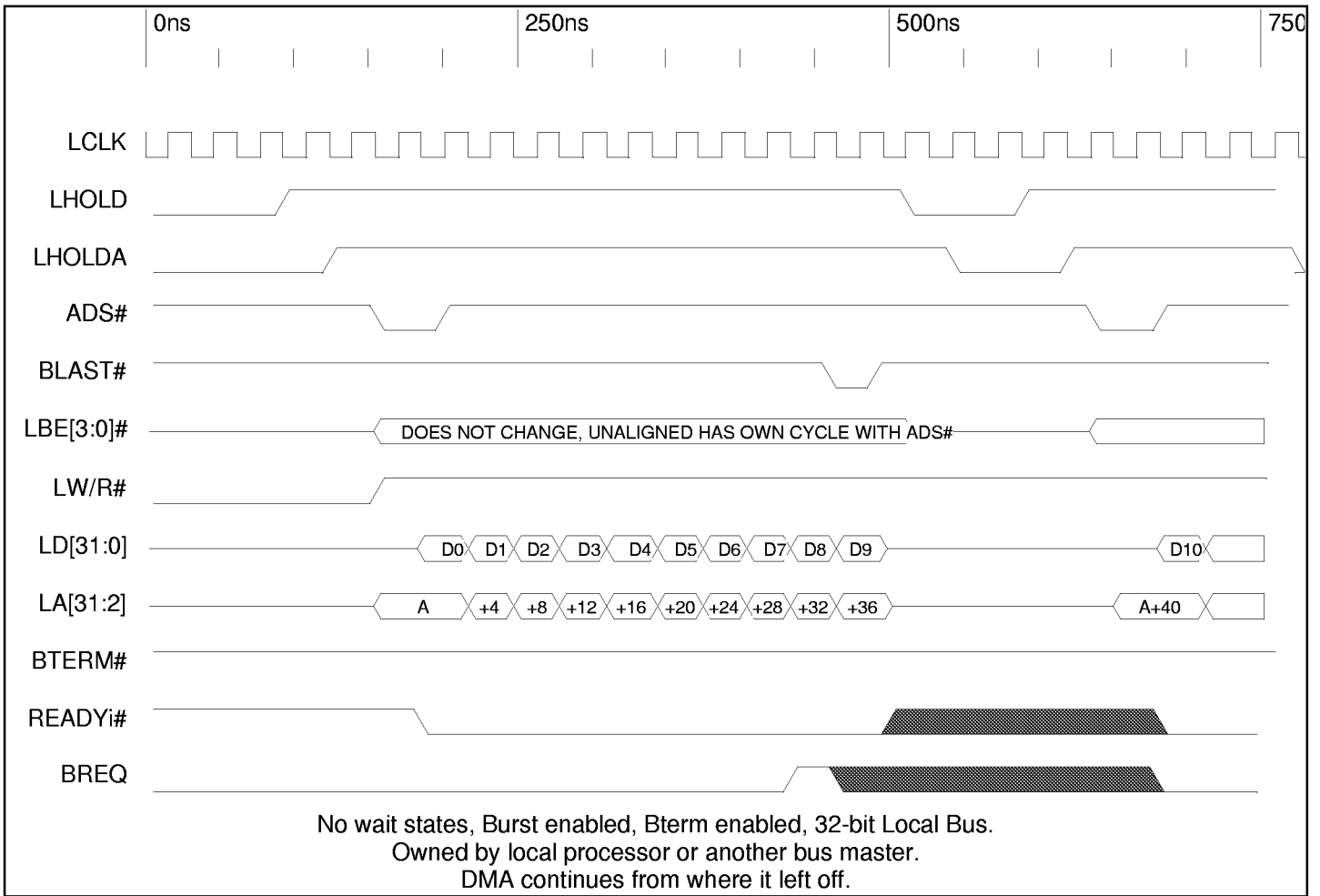
Timing Diagram 8-14. (C Mode) Direct Slave PCI-to-Local Burst Read, Bterm Disabled



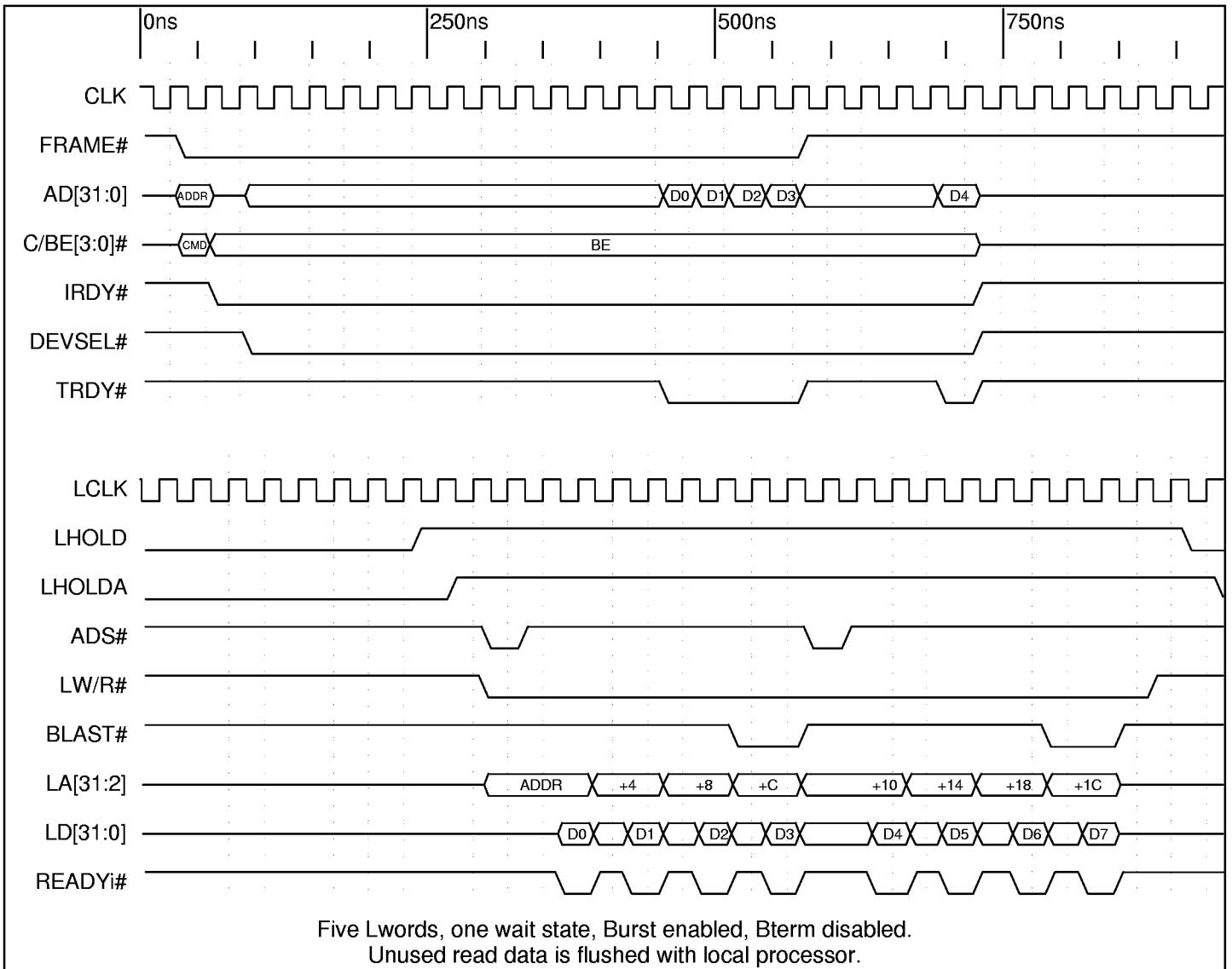
Timing Diagram 8-15. (C Mode) PCI 9080 DMA or Direct Slave Burst Write, Bterm Disabled



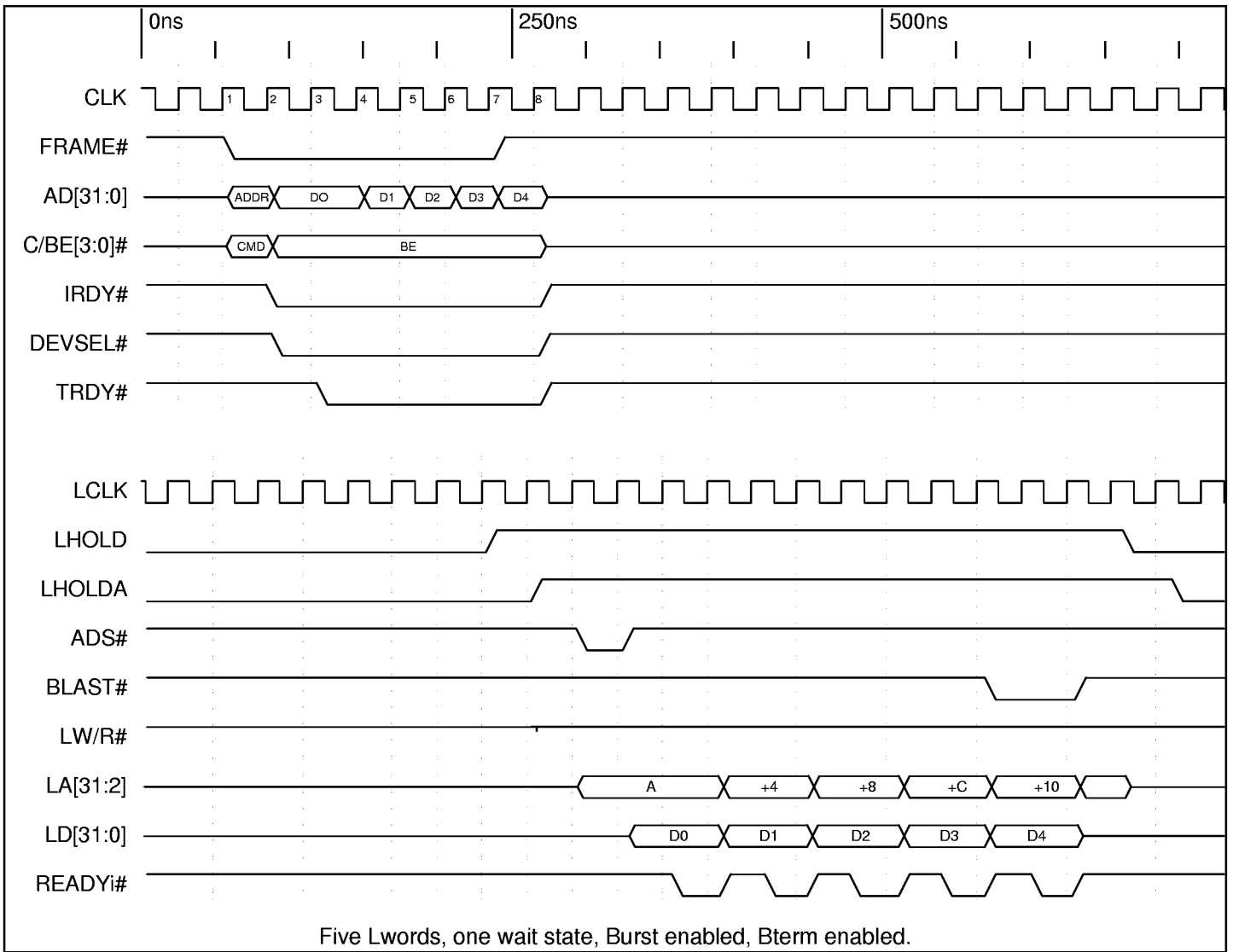
Timing Diagram 8-16. (C Mode) Direct Slave Read with Prefetch Counter Set to 5



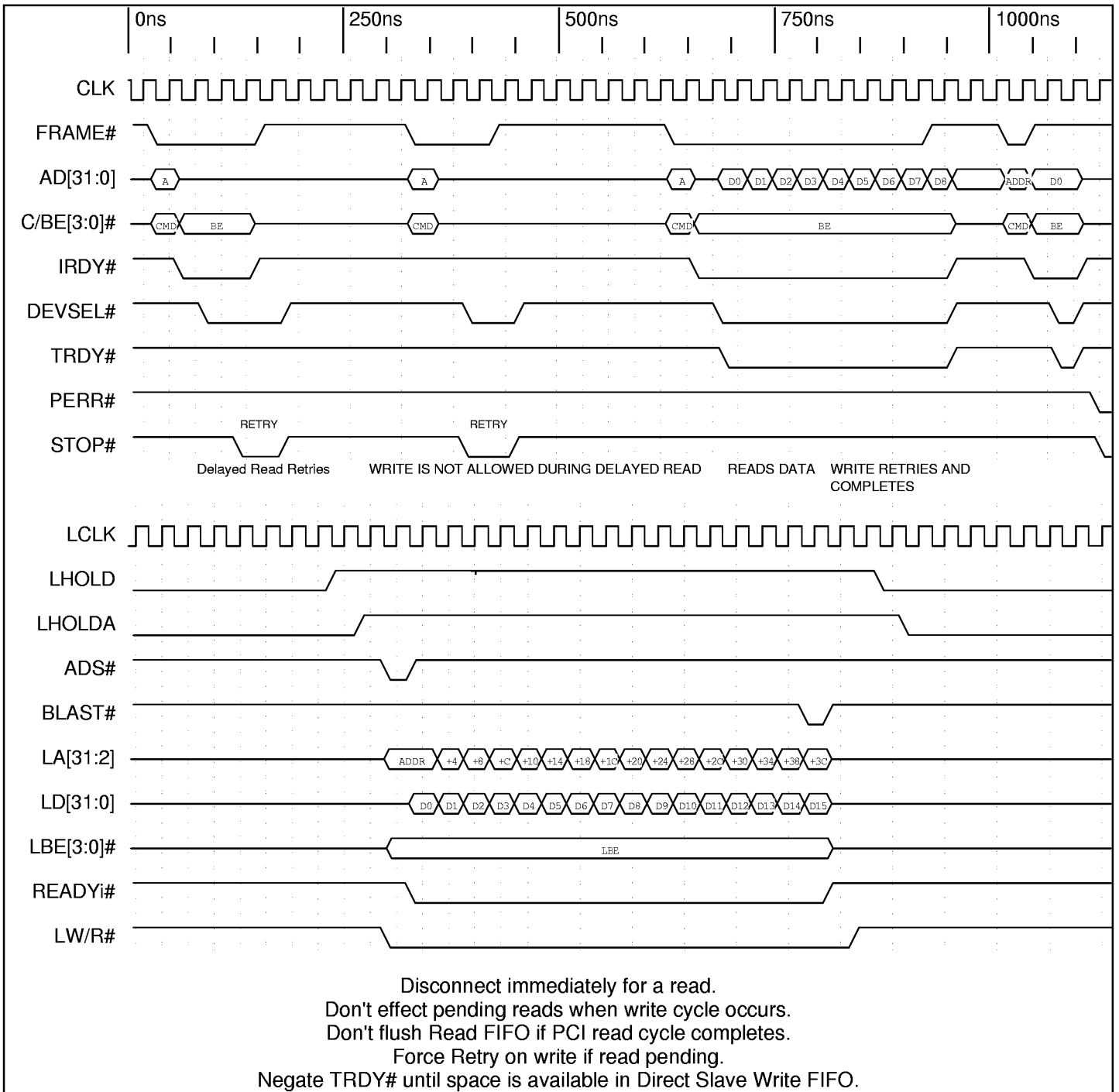
Timing Diagram 8-17. (C Mode) Direct Slave or DMA Burst Write to 32-Bit Local Bus Suspended by BREQ Input



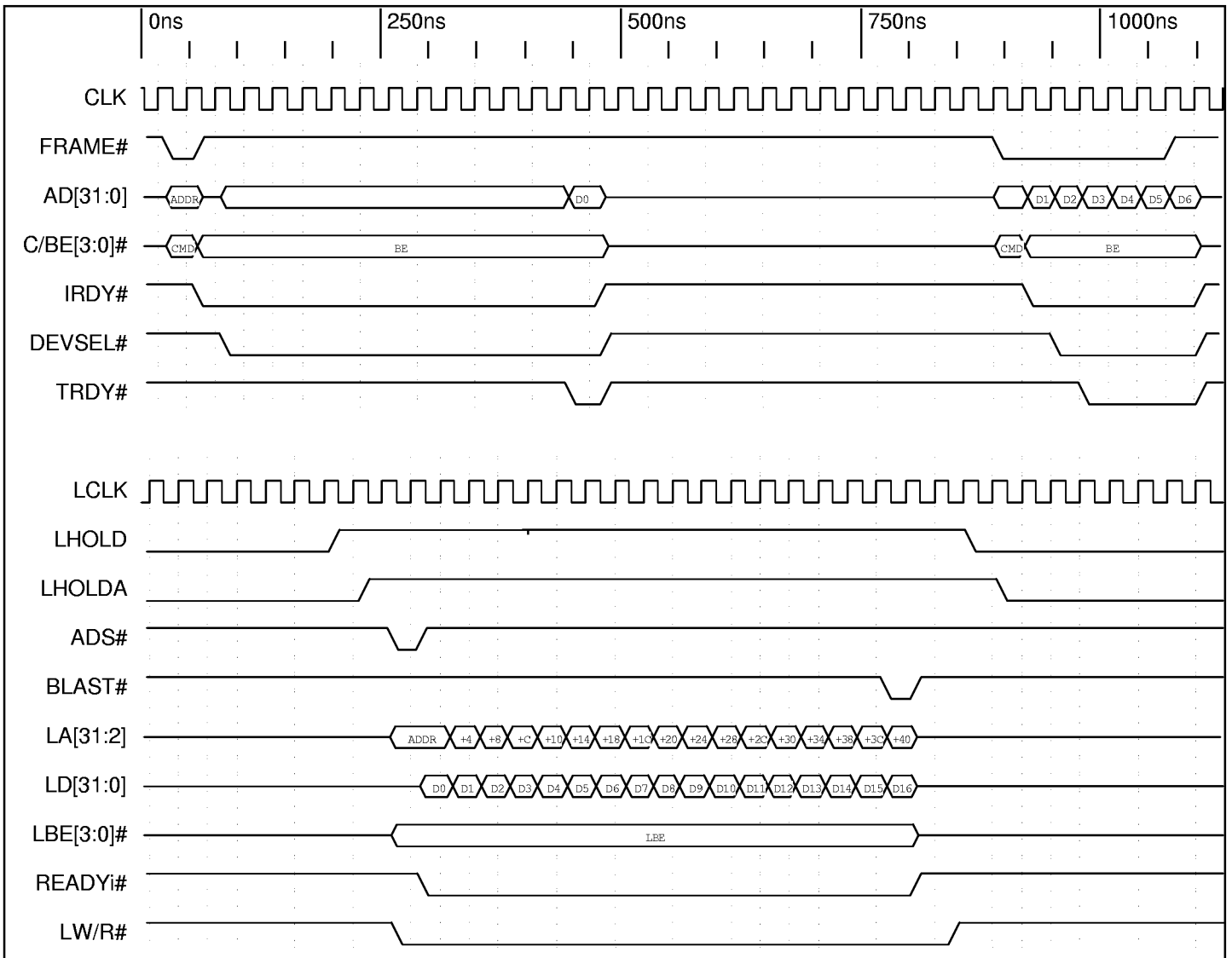
Timing Diagram 8-18. (C Mode) Direct Slave Burst Read of Five Lwords with One Wait State



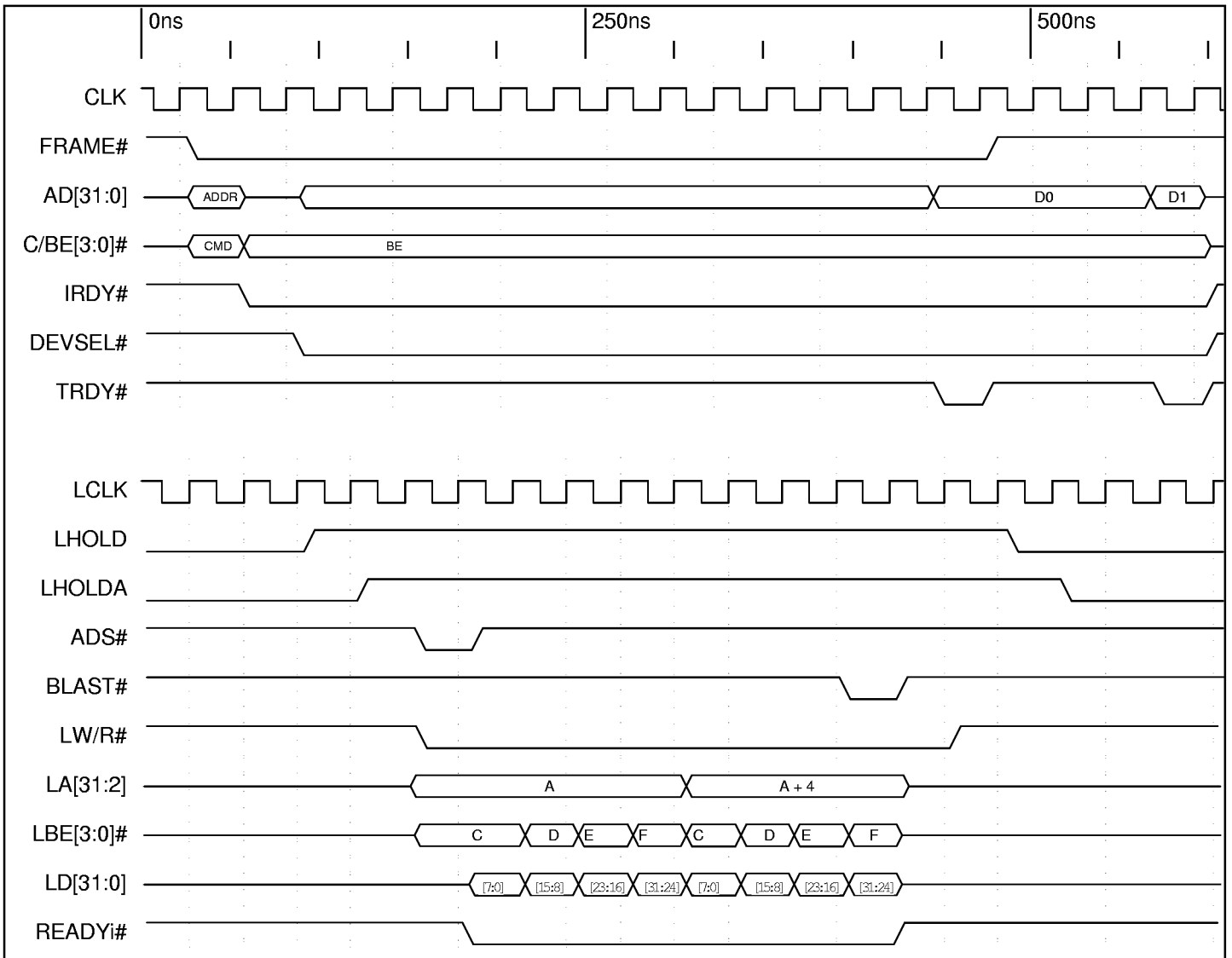
Timing Diagram 8-19. (C Mode) Direct Slave Burst Write of Five Lwords with One Wait State



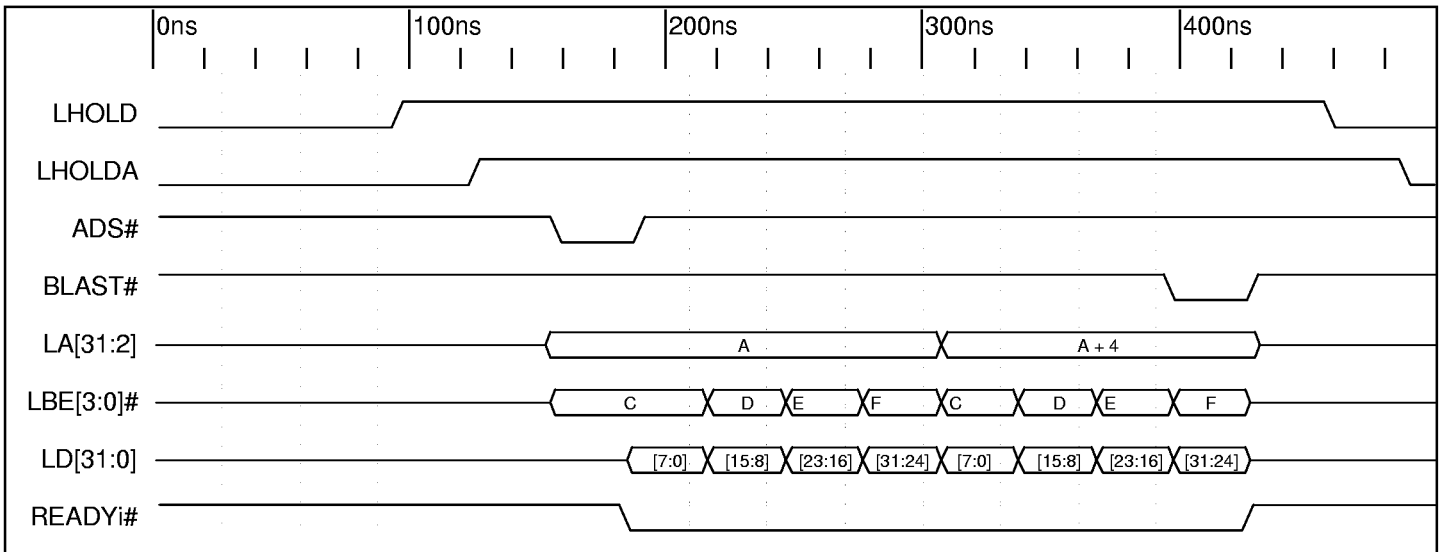
Timing Diagram 8-20. (C Mode) Direct Slave Read 2.1 Spec



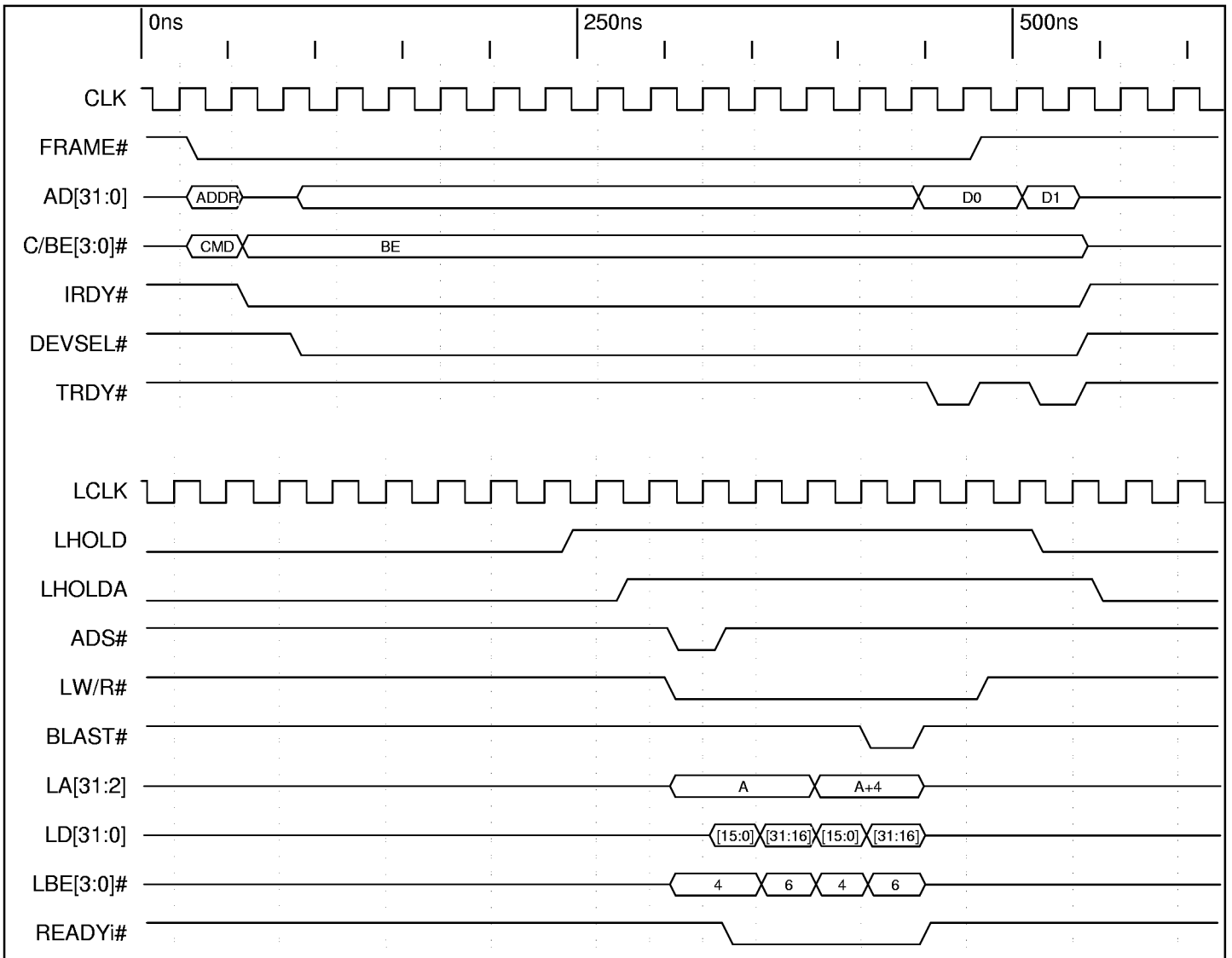
Timing Diagram 8-21. (C Mode) Direct Slave Read No Flush Mode (Read Ahead Mode)



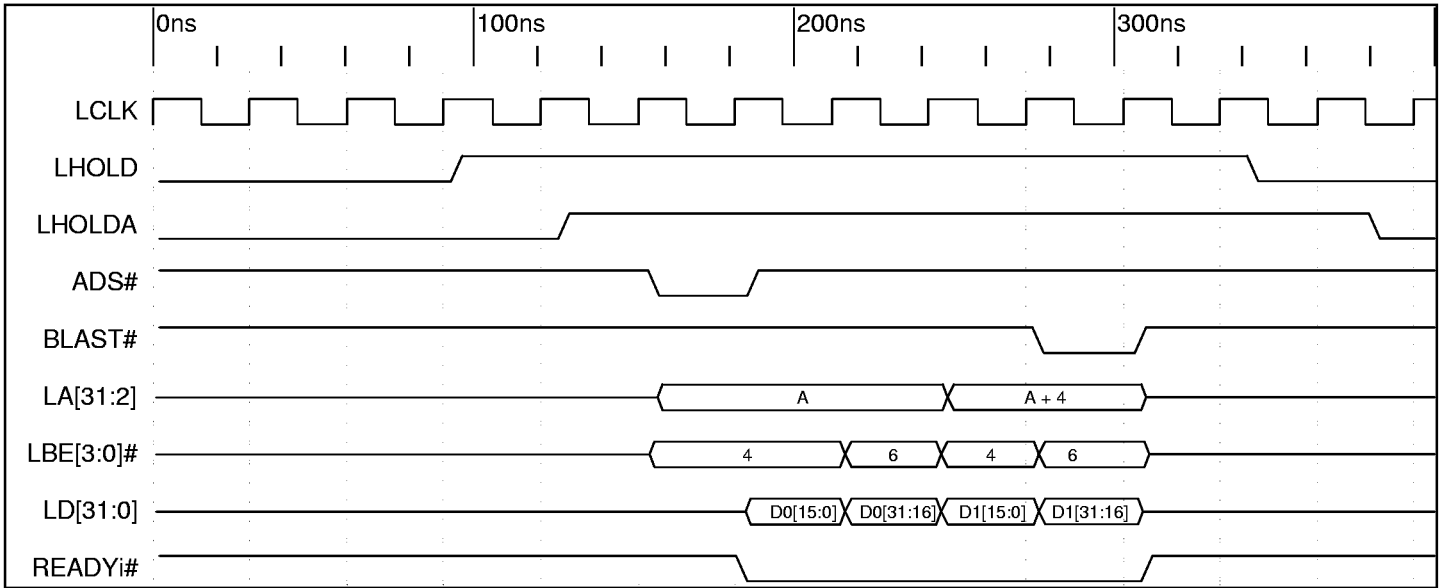
Timing Diagram 8-22. (C Mode) Direct Slave Read of Two Lwords from 8-Bit Bus



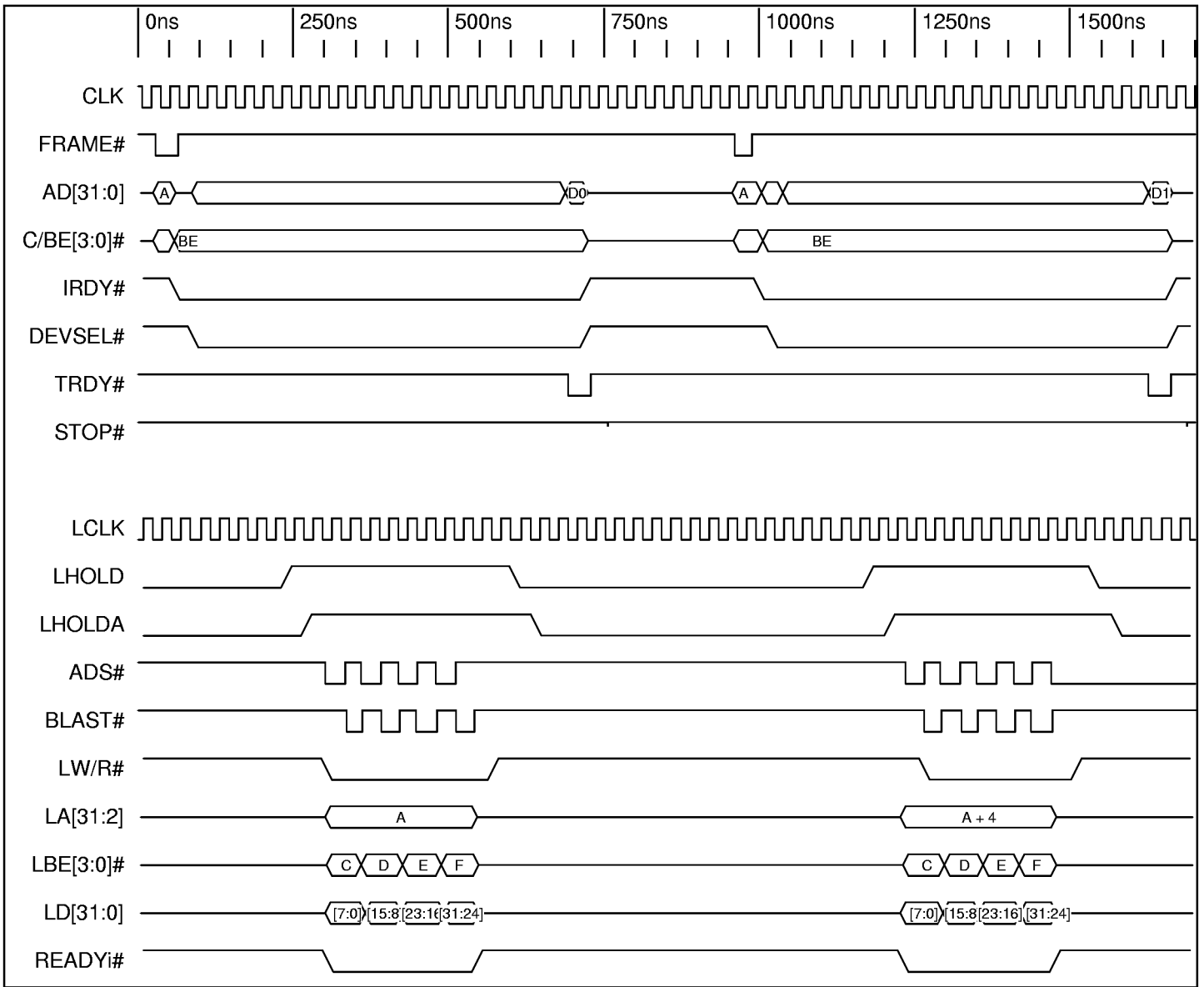
Timing Diagram 8-23. (C Mode) PCI 9080 DMA or Direct Slave Two Lword Burst Write to 8-Bit Local Bus, No Wait States, Bterm Enabled



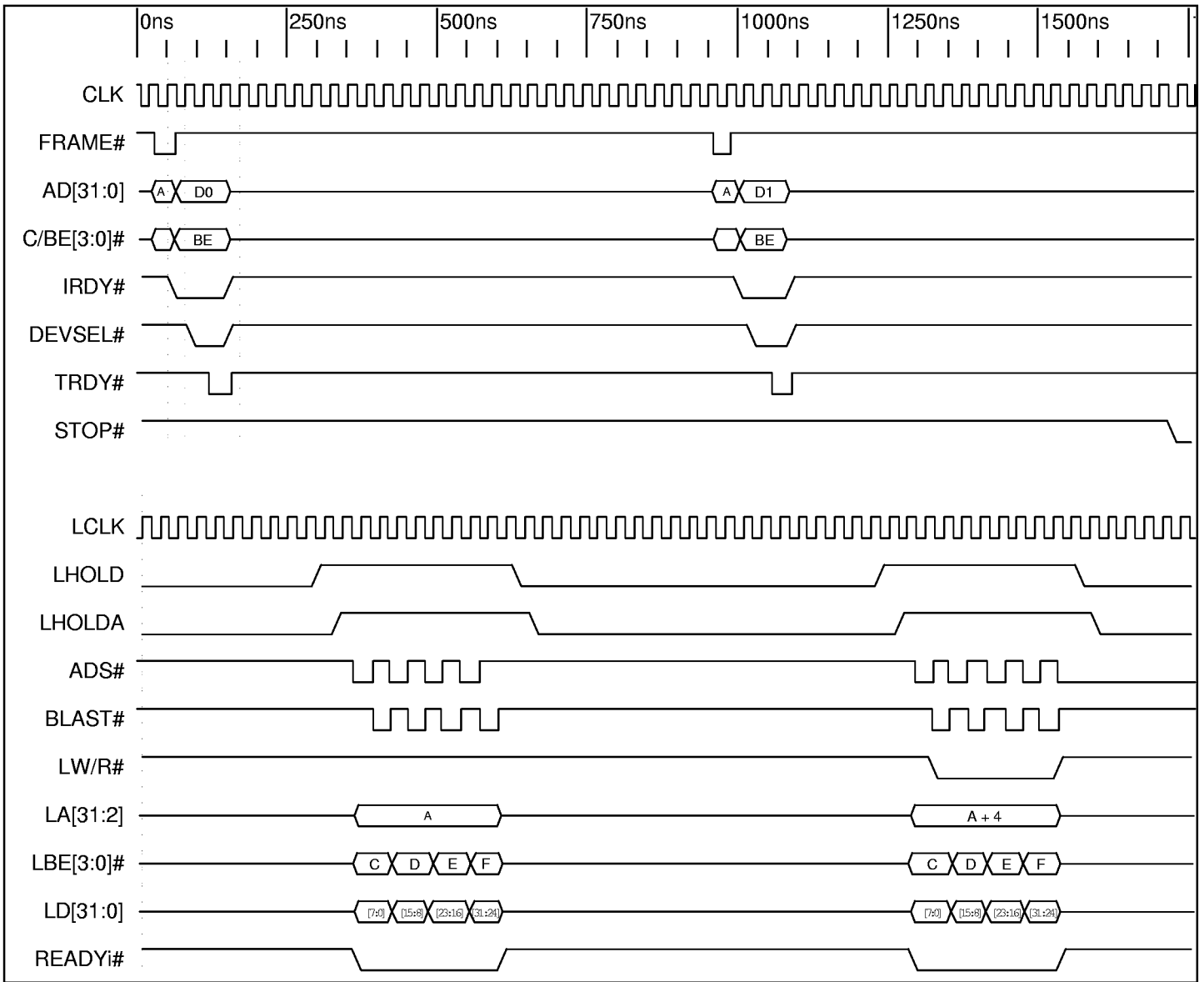
Timing Diagram 8-24. (C Mode) Direct Slave Read of Two Lwords from 16-Bit Bus



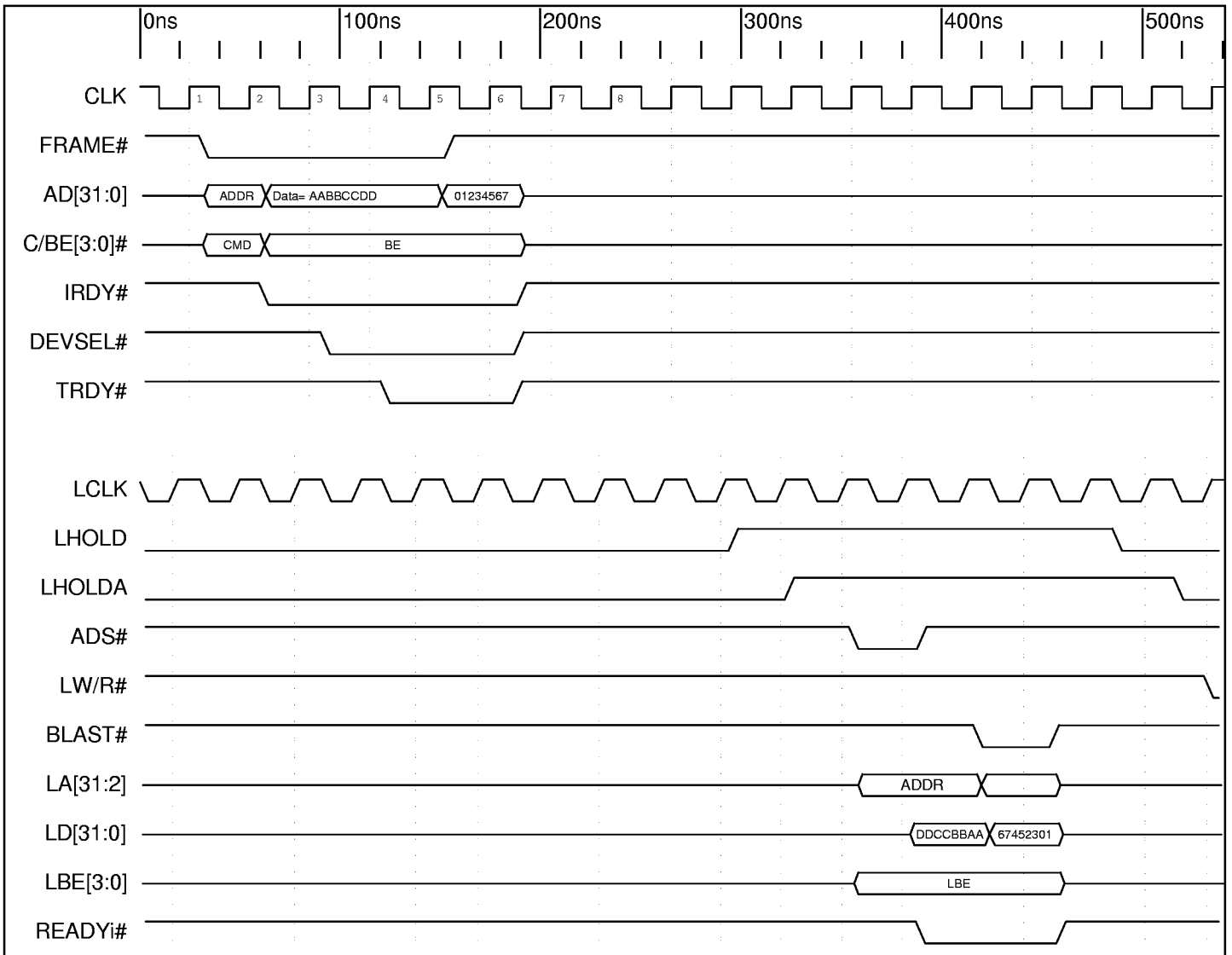
Timing Diagram 8-25. (C Mode) PCI 9080 DMA or Direct Slave Two Lword Burst Write to 16-Bit Local Bus, No Wait States, Bterm Enabled



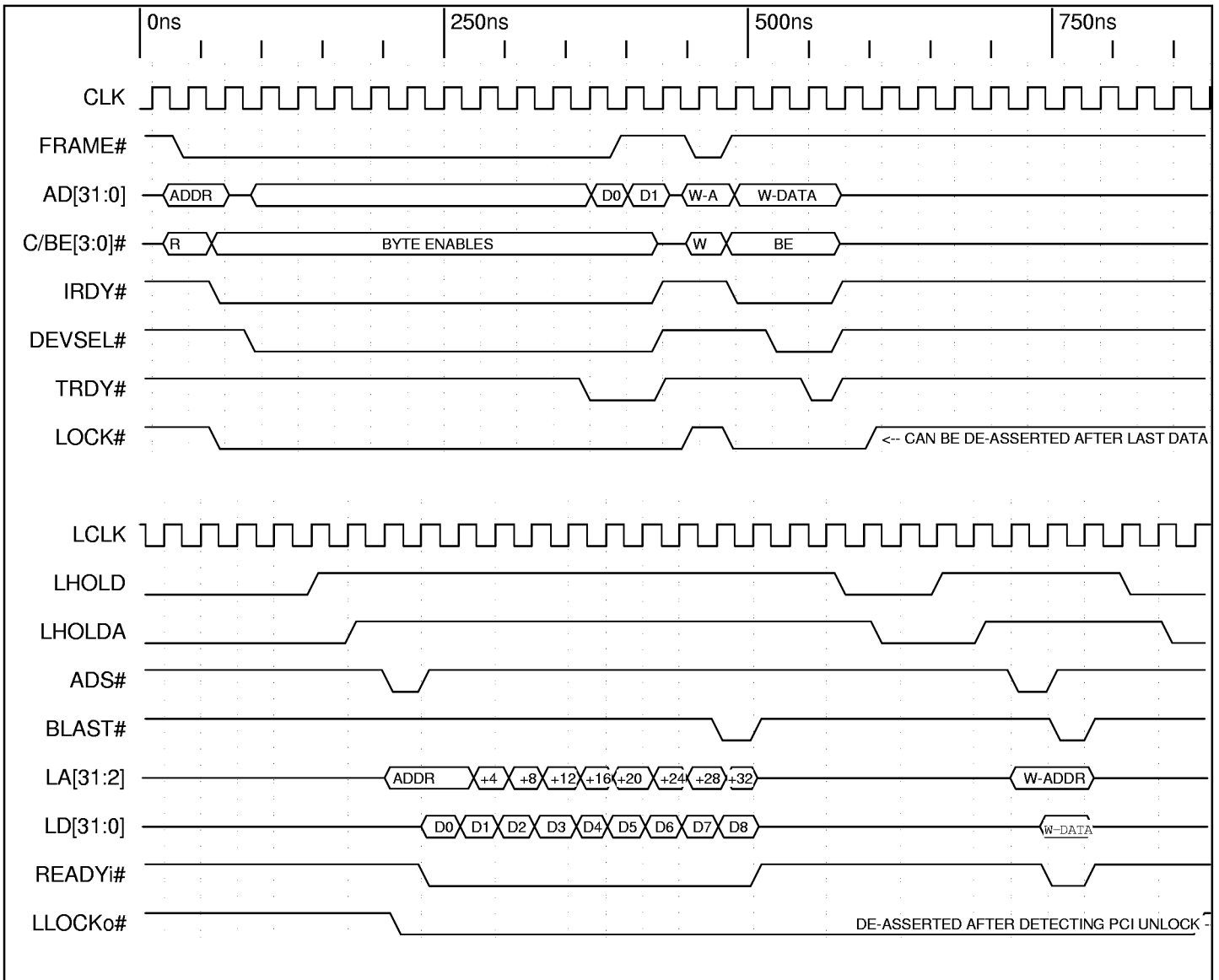
Timing Diagram 8-26. (C Mode) Direct Slave Read of Two Lwords from 8-Bit I/O Local Bus, Burst Disabled



Timing Diagram 8-27. (C Mode) Direct Slave Write of Two Lwords to 8-Bit I/O Local Bus, Burst Disabled

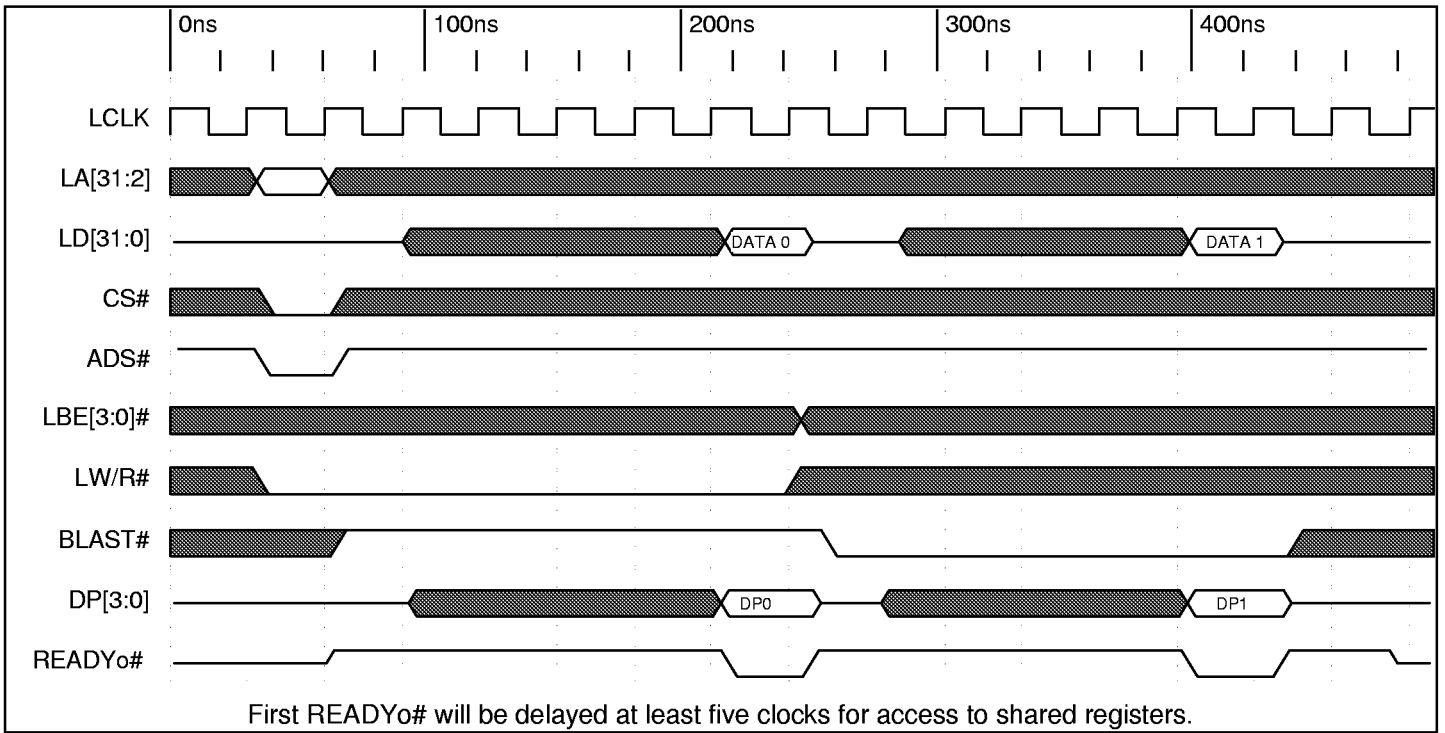


Timing Diagram 8-28. (C Mode) Direct Slave in BIGEND Local Bus with BIGEND# Input or Internal Register Setting

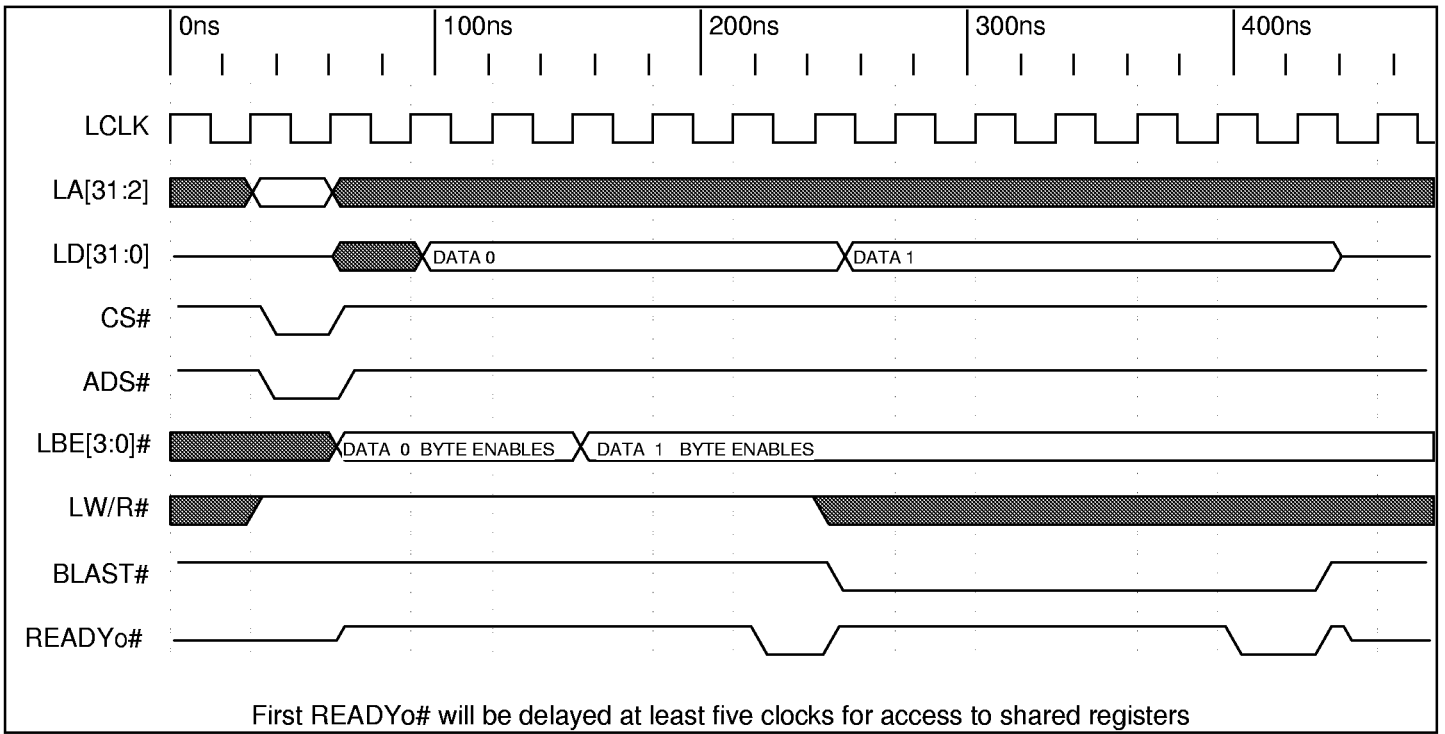


Timing Diagram 8-29. (C Mode) Locked Direct Slave Read Followed by Write and Release (LLOCKo#)

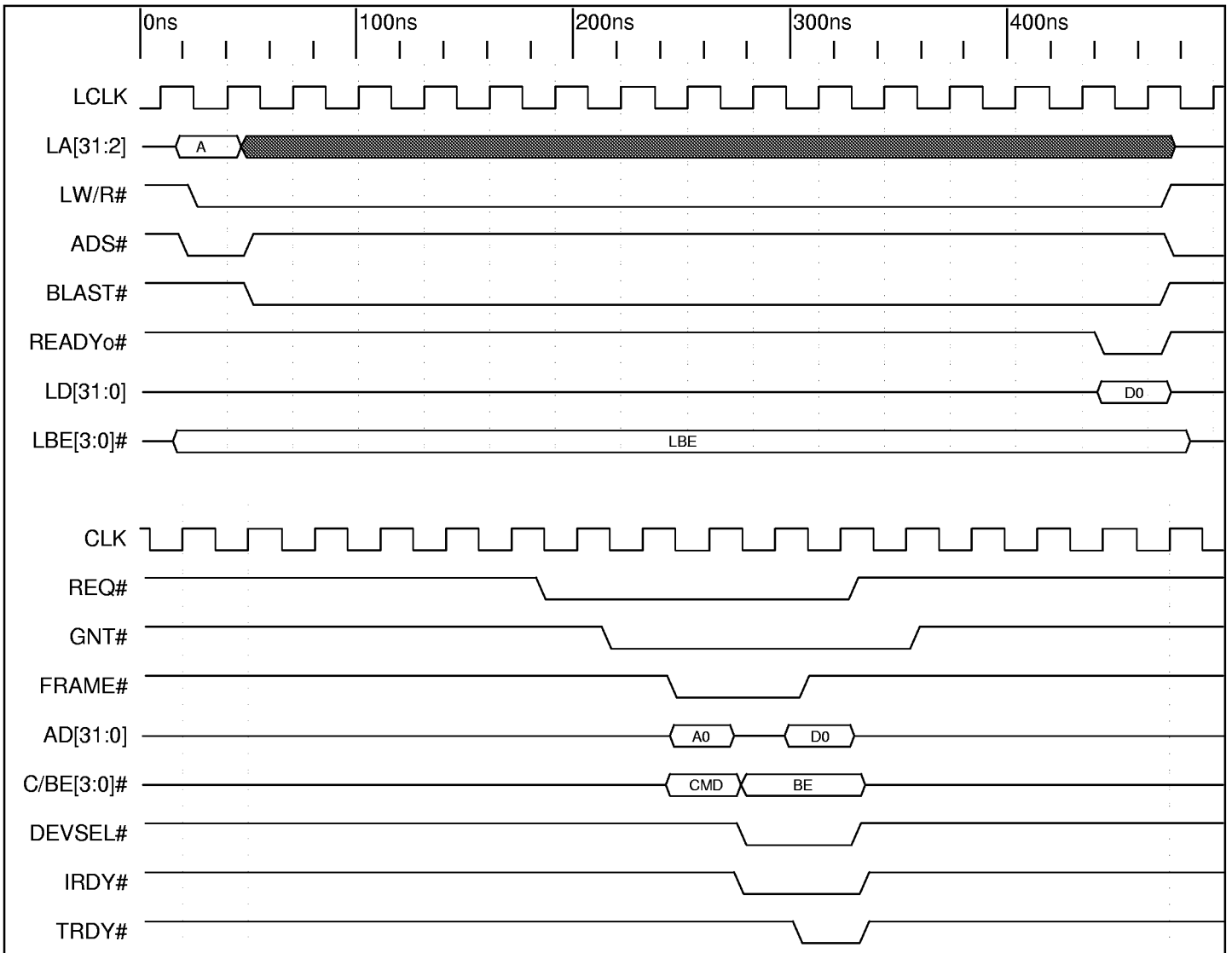
8.3.2 C Mode Direct Master



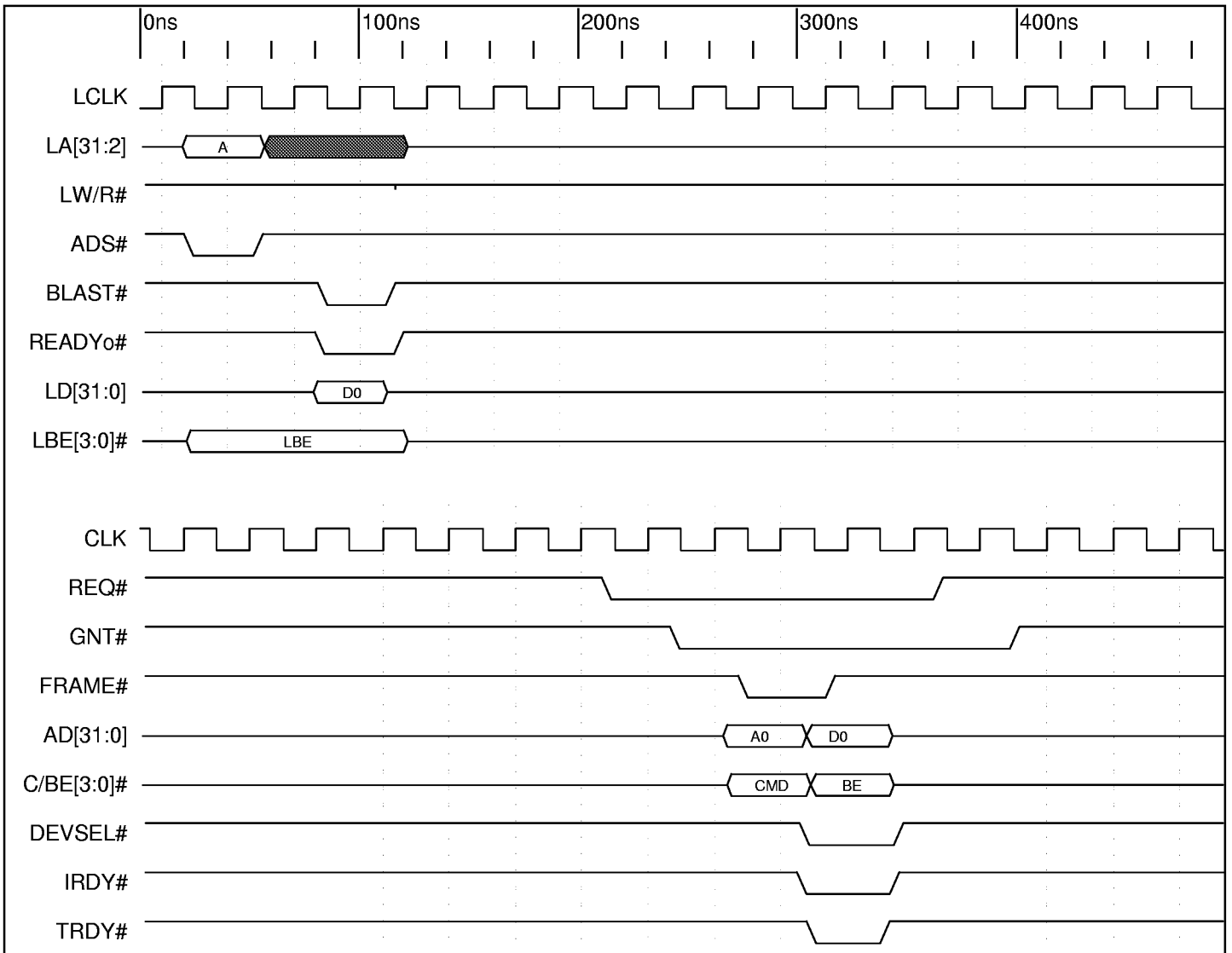
Timing Diagram 8-30. (C Mode) Local Bus Read from PCI 9080 CFG Registers



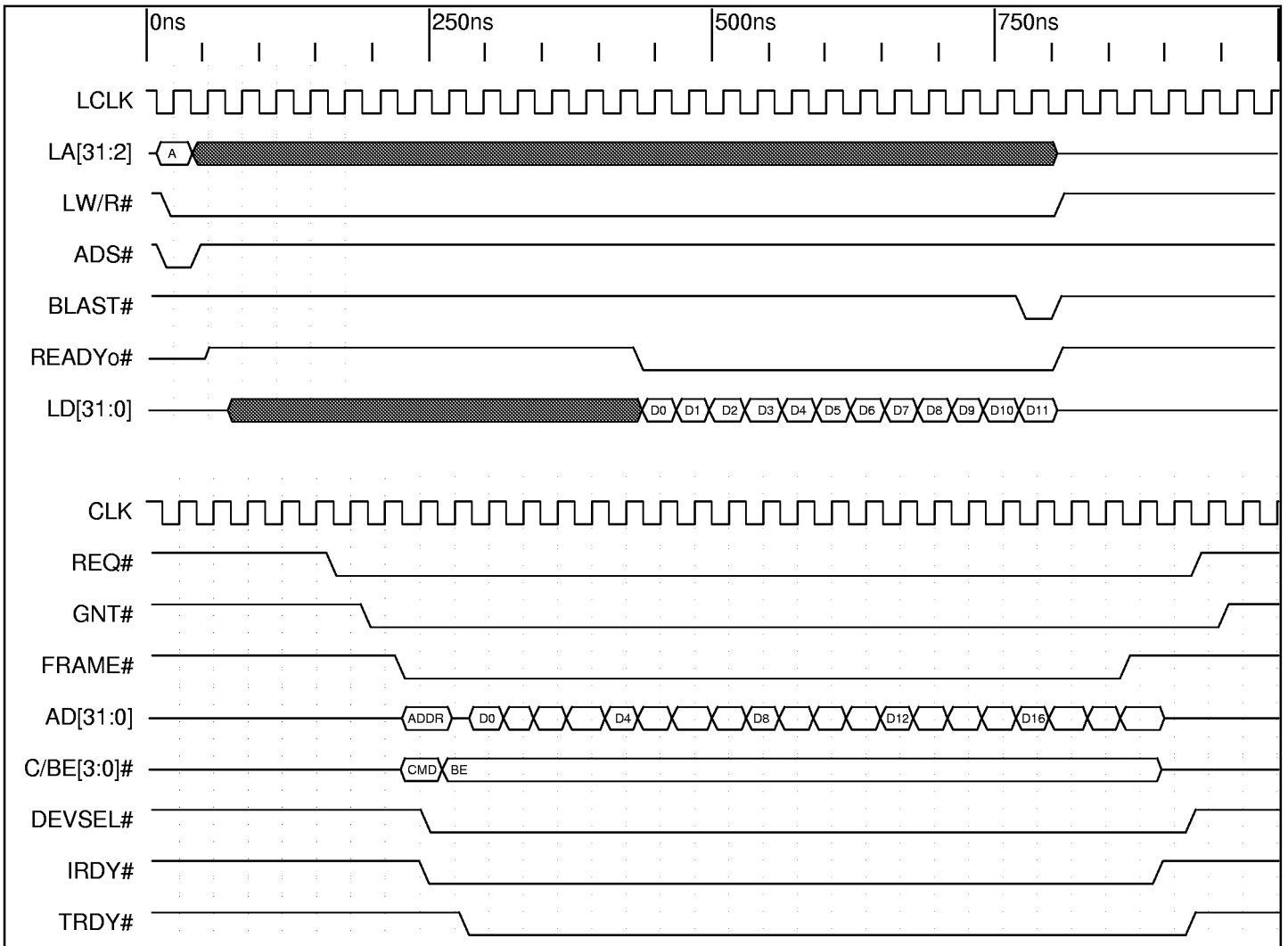
Timing Diagram 8-31. (C Mode) Local Bus Write to PCI 9080 CFG Registers



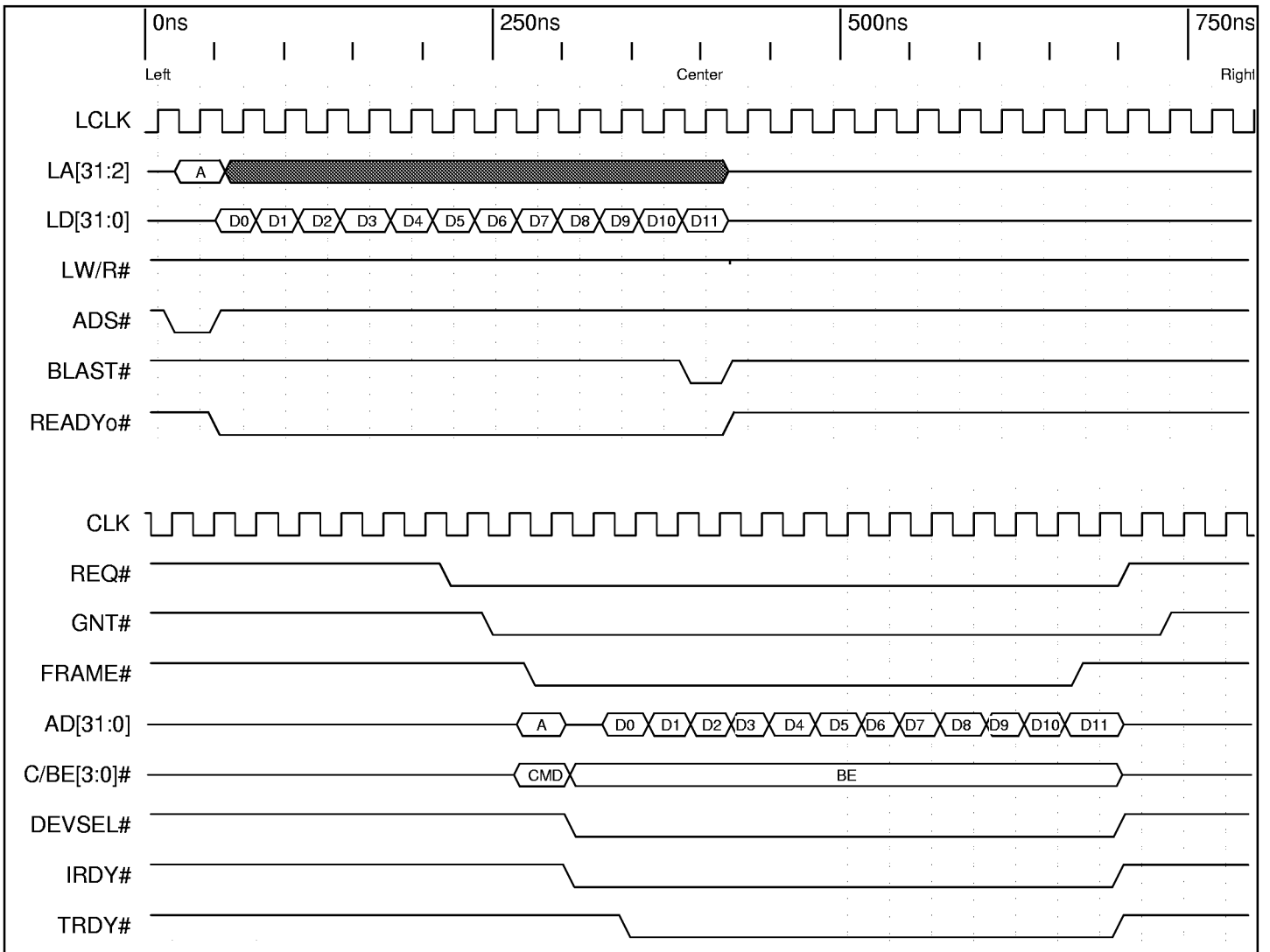
Timing Diagram 8-32. (C Mode) Local Bus Direct Master Single Memory Read



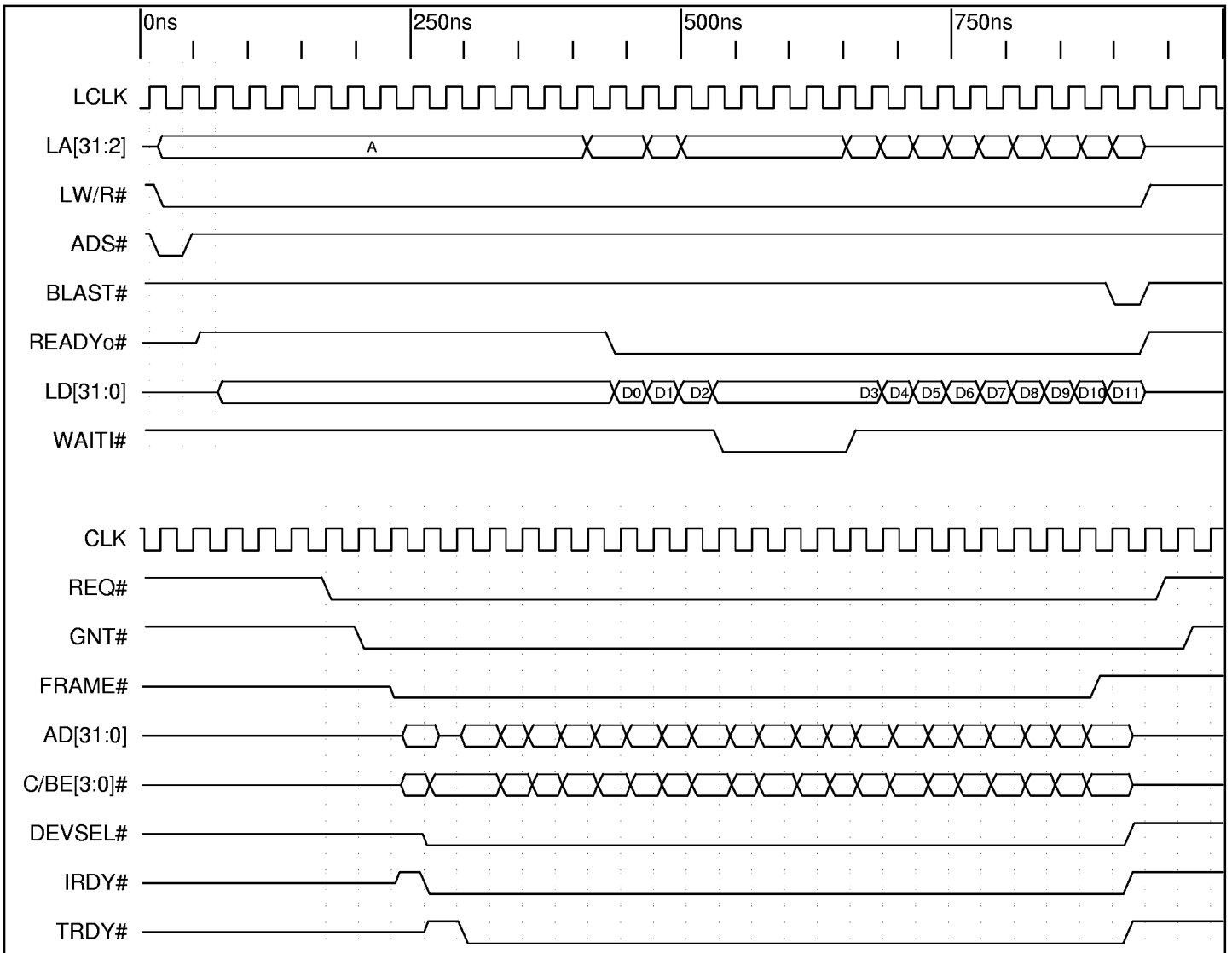
Timing Diagram 8-33. (C Mode) Local Bus Direct Master Single Memory Write Cycle



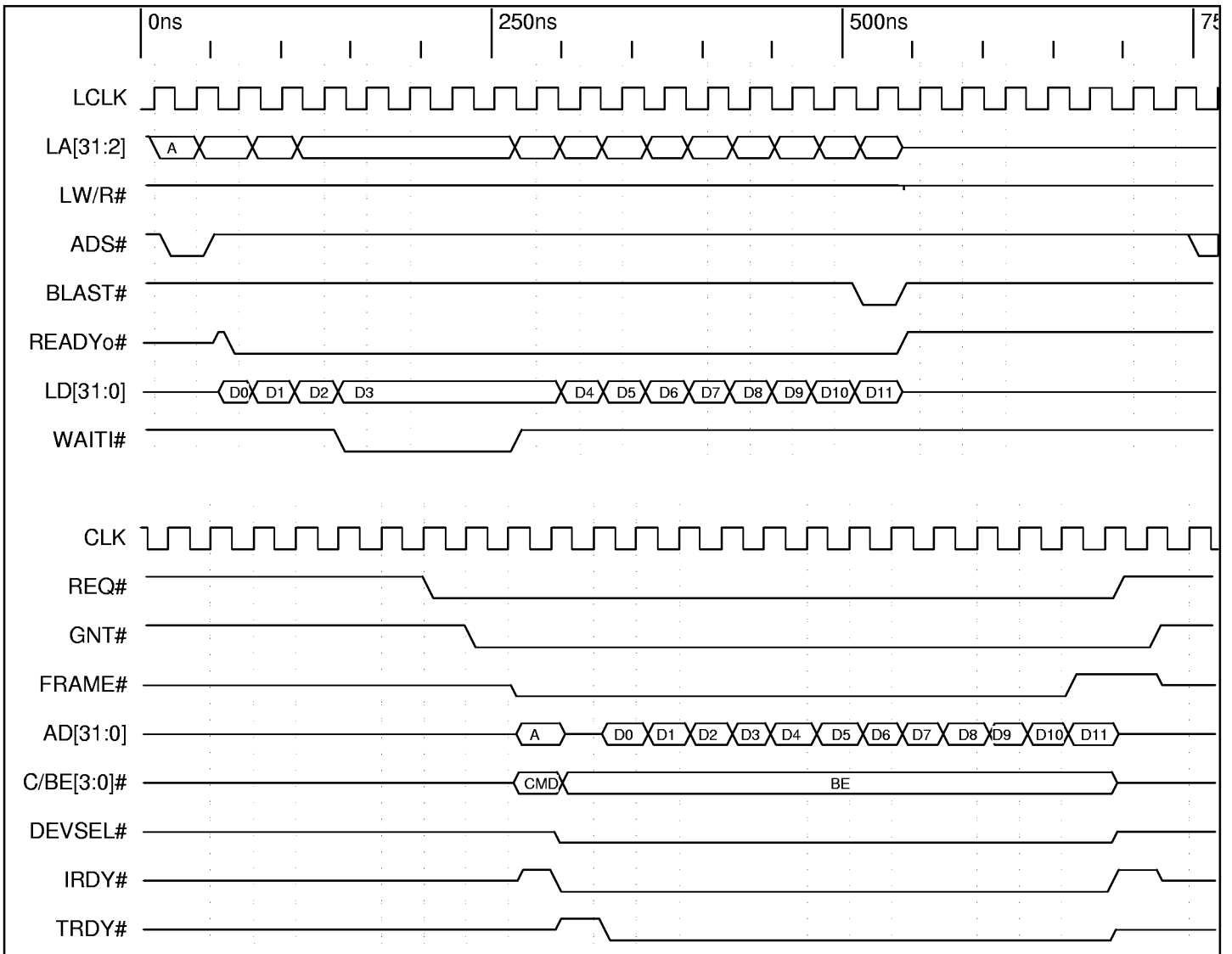
Timing Diagram 8-34. (C Mode) PCI 9080 Direct Master Memory Read, 12 Lword Burst



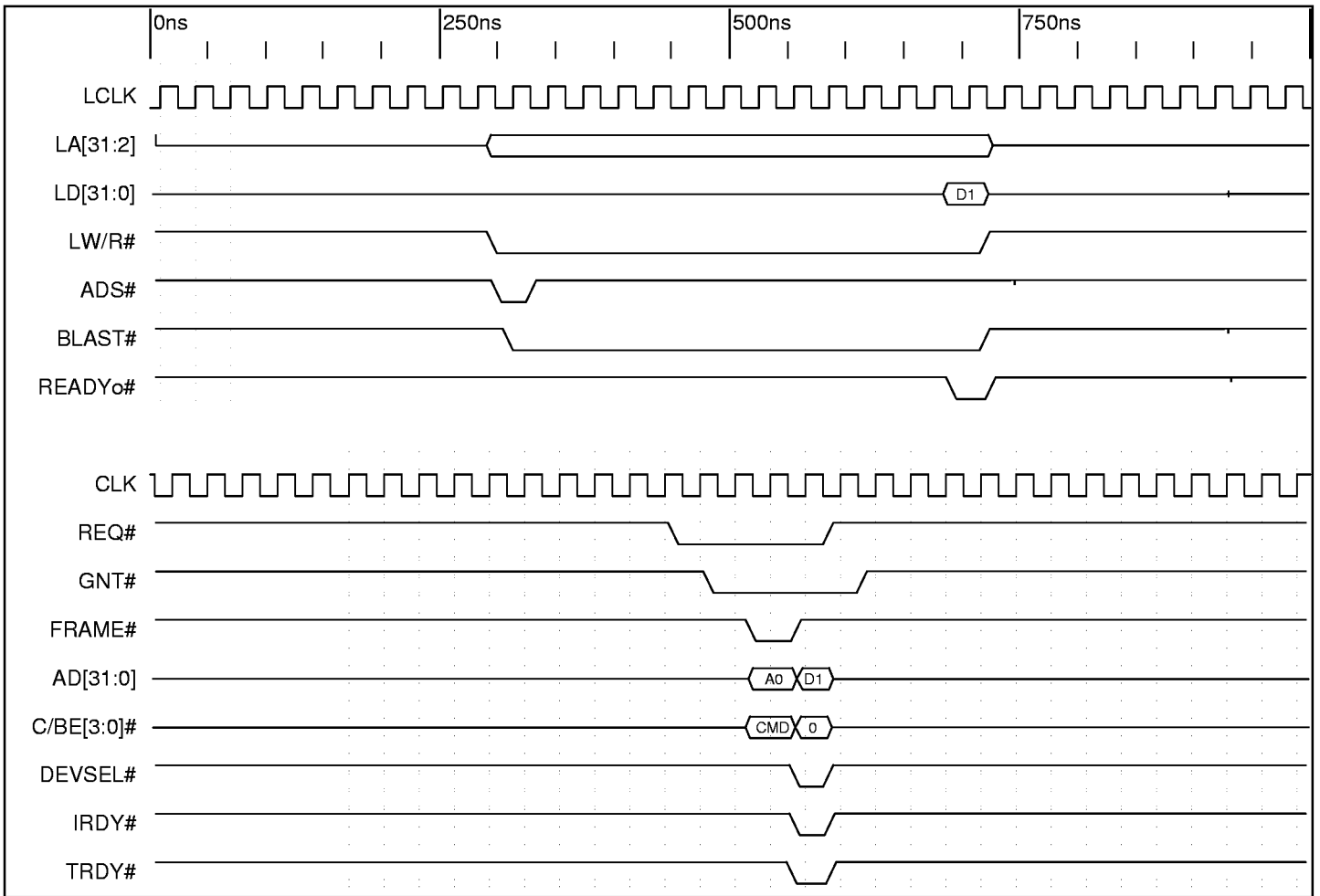
Timing Diagram 8-35. (C Mode) PCI 9080 Direct Master Memory Write of 12 Lwords



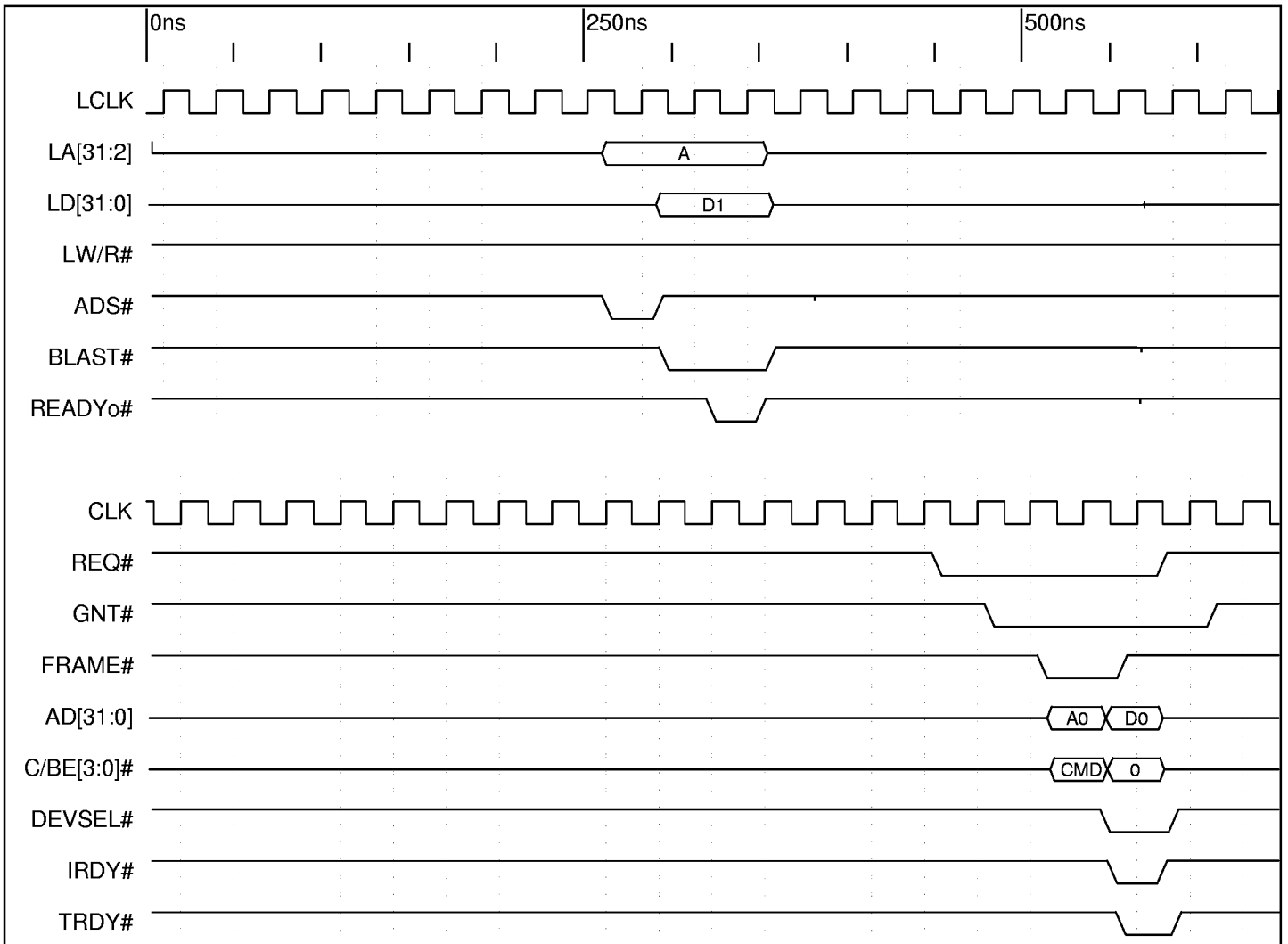
Timing Diagram 8-36. (C Mode) PCI 9080 Direct Master Memory Read with WAITI#



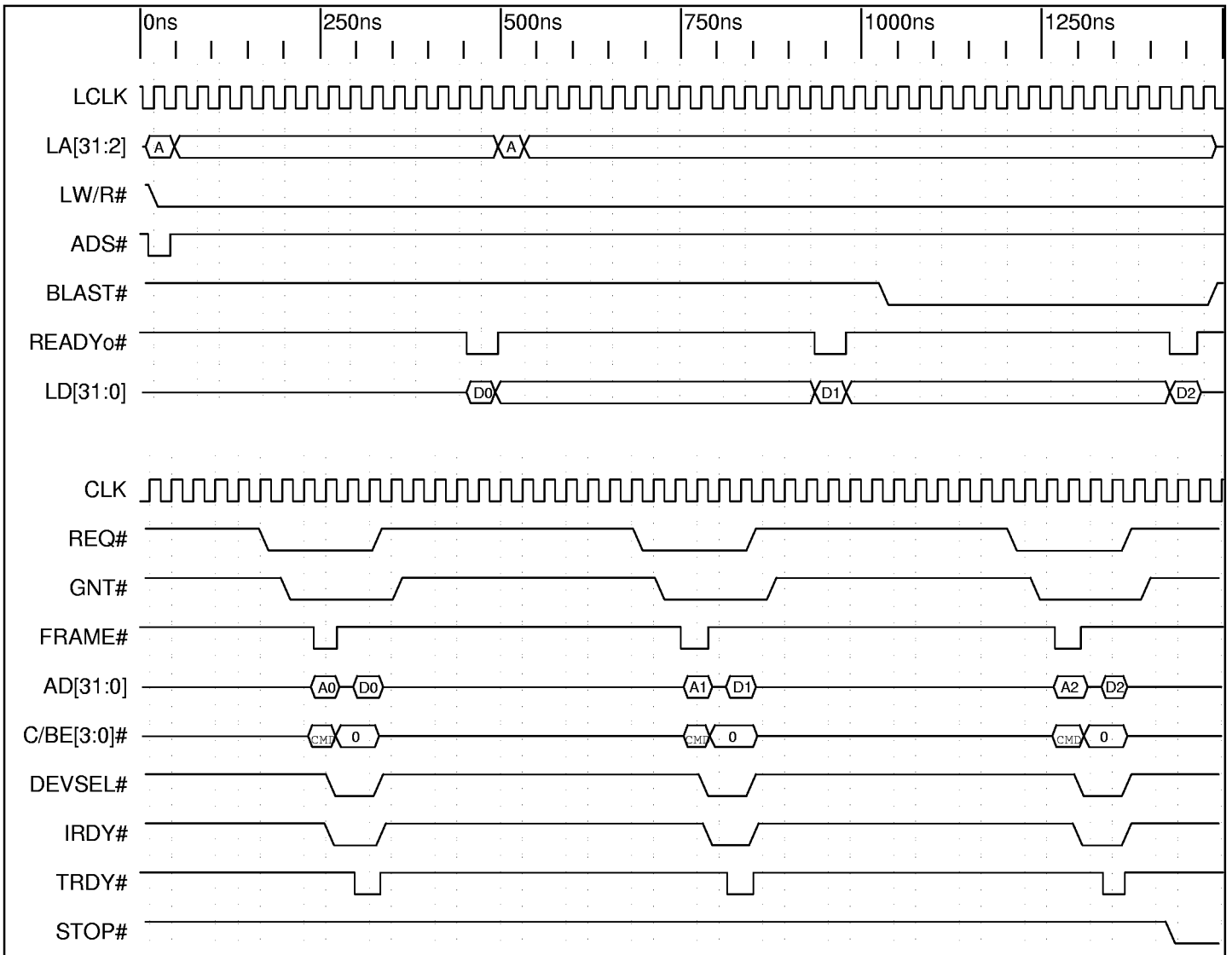
Timing Diagram 8-37. (C Mode) PCI 9080 Direct Master Memory Write with WAITI#



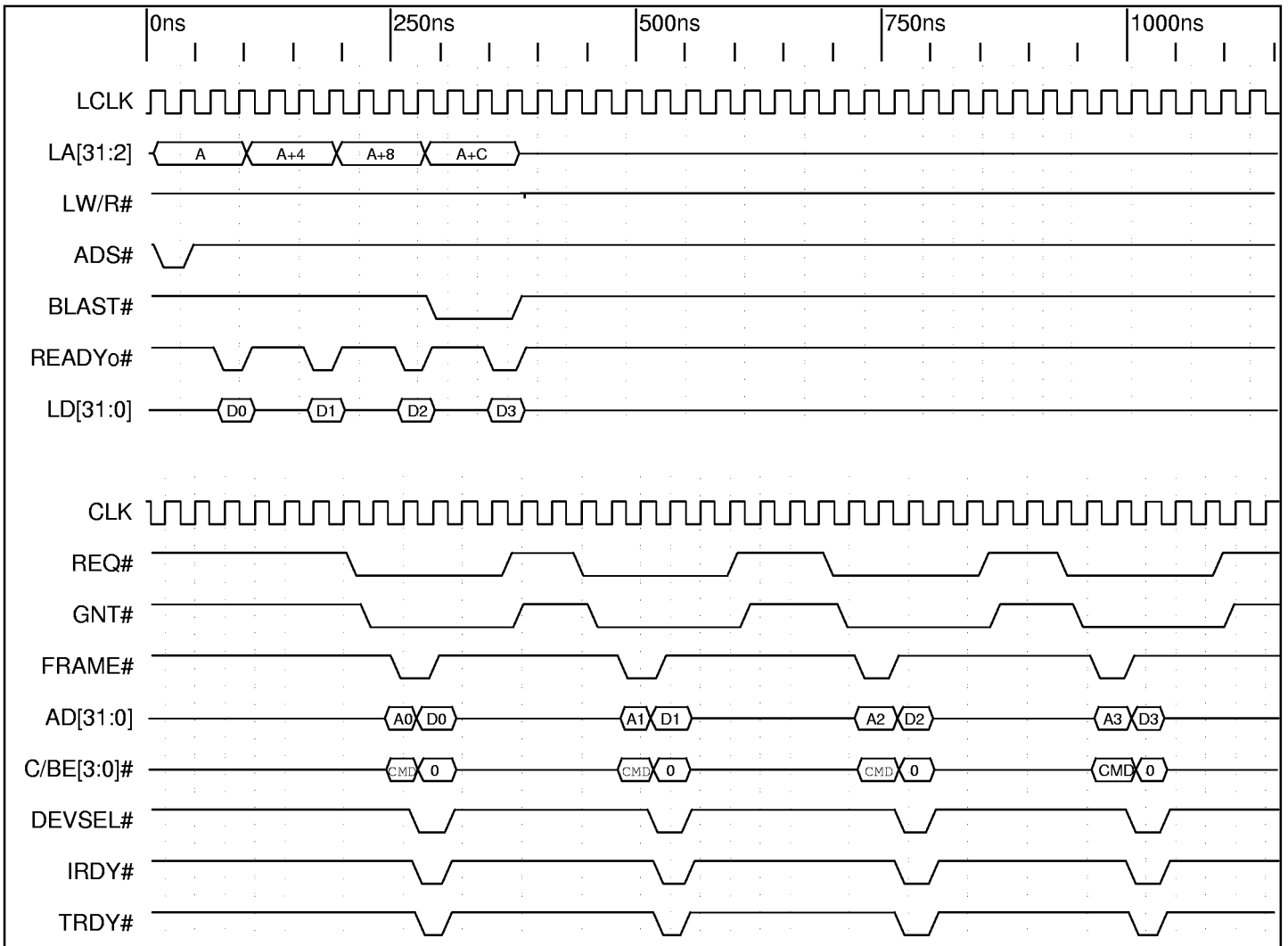
Timing Diagram 8-38. (C Mode) PCI 9080 Direct Master Configuration Read—Type 1 or Type 0



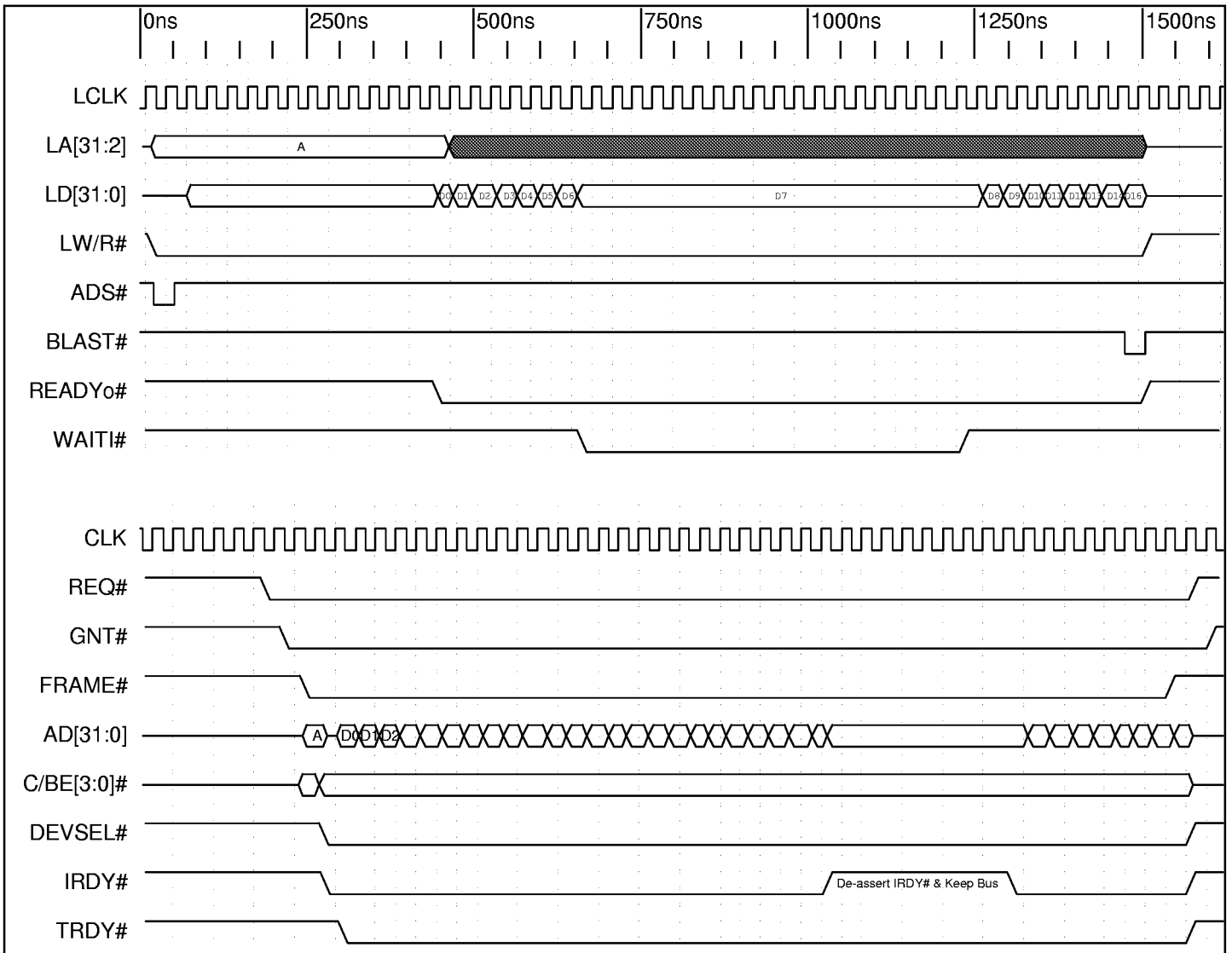
Timing Diagram 8-39. (C Mode) PCI 9080 Direct Master Configuration Write—Type 1 or Type 0



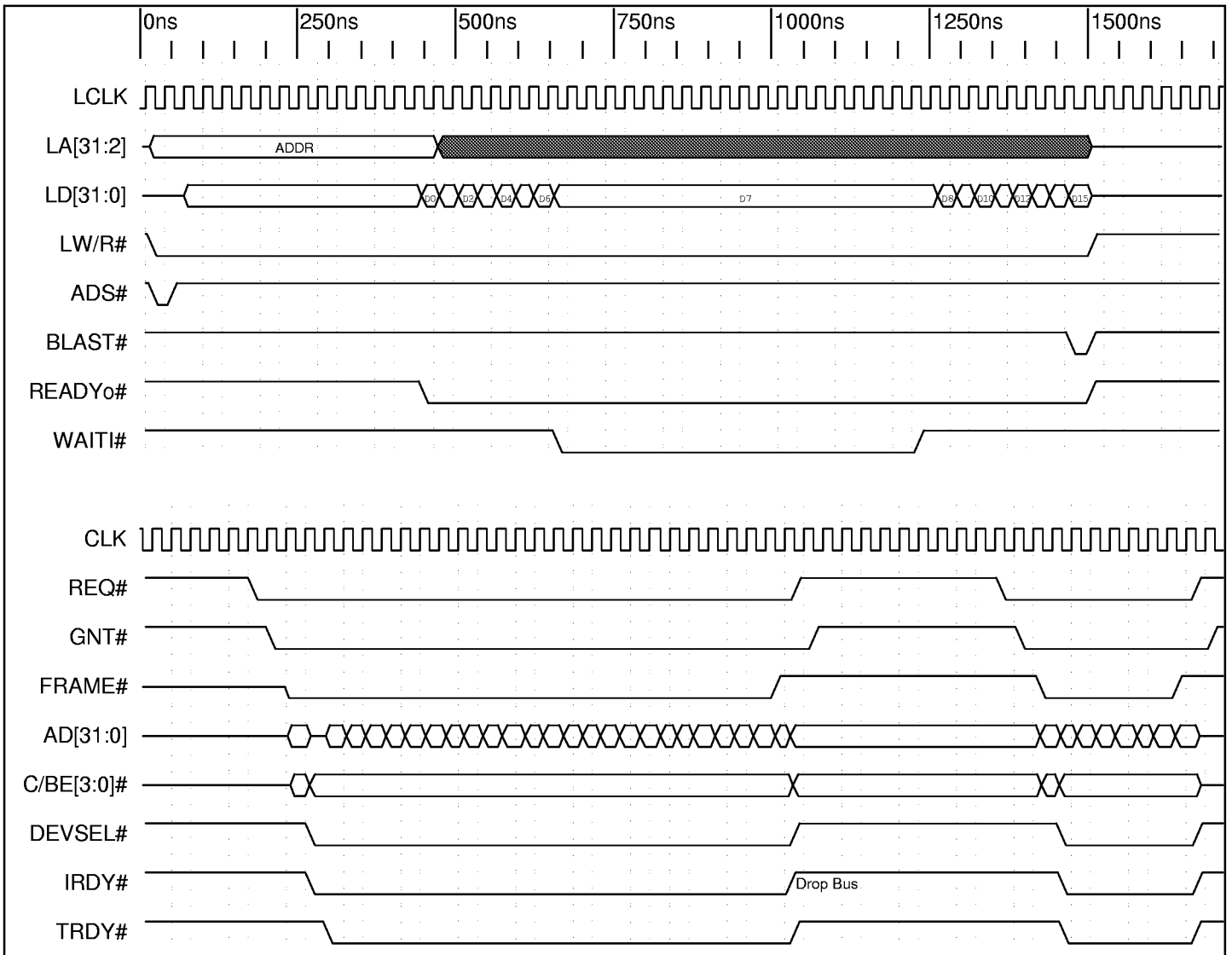
Timing Diagram 8-40. (C Mode) Local Bus Direct Master Read from PCI I/O



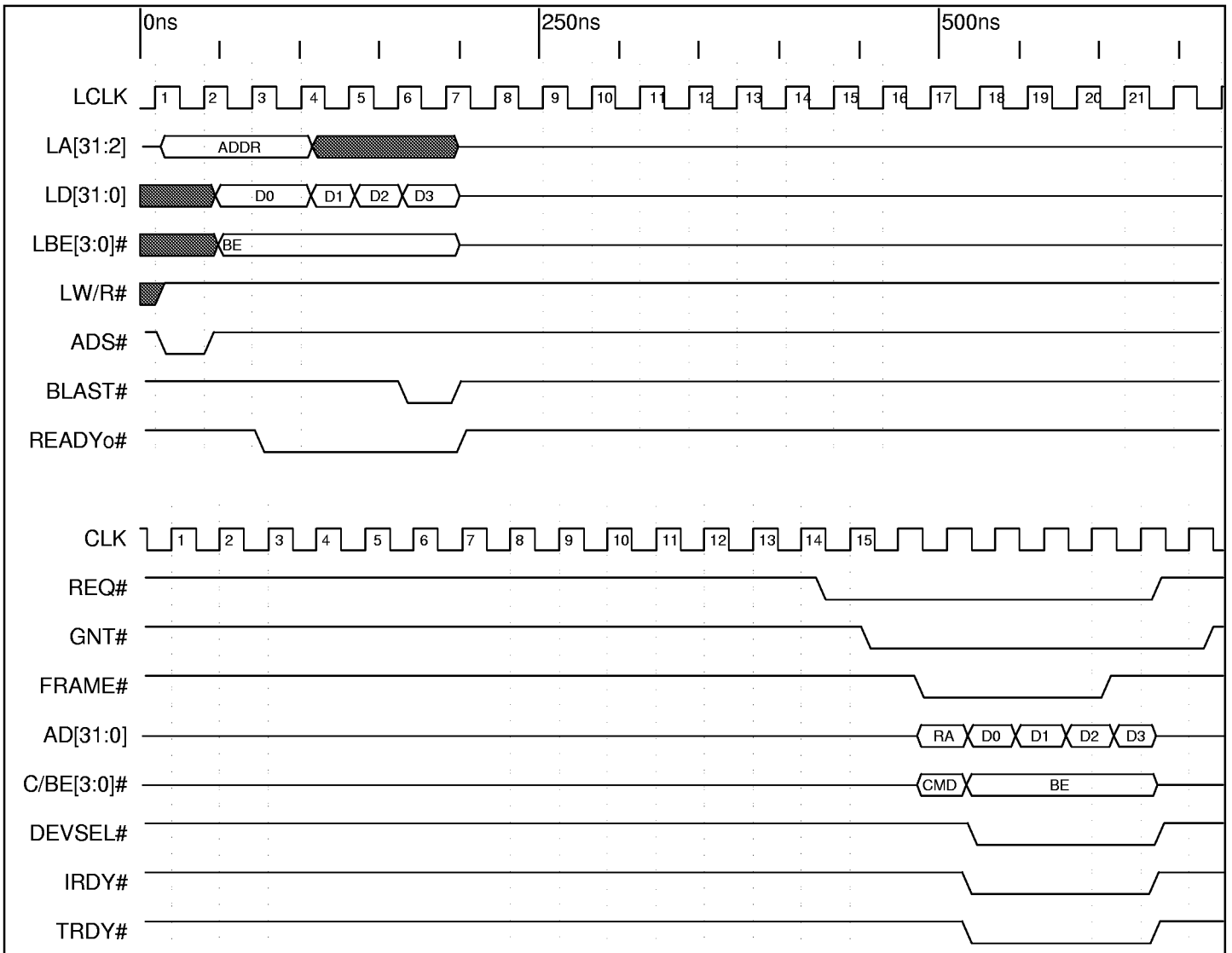
Timing Diagram 8-41. (C Mode) Direct Master Write to PCI I/O



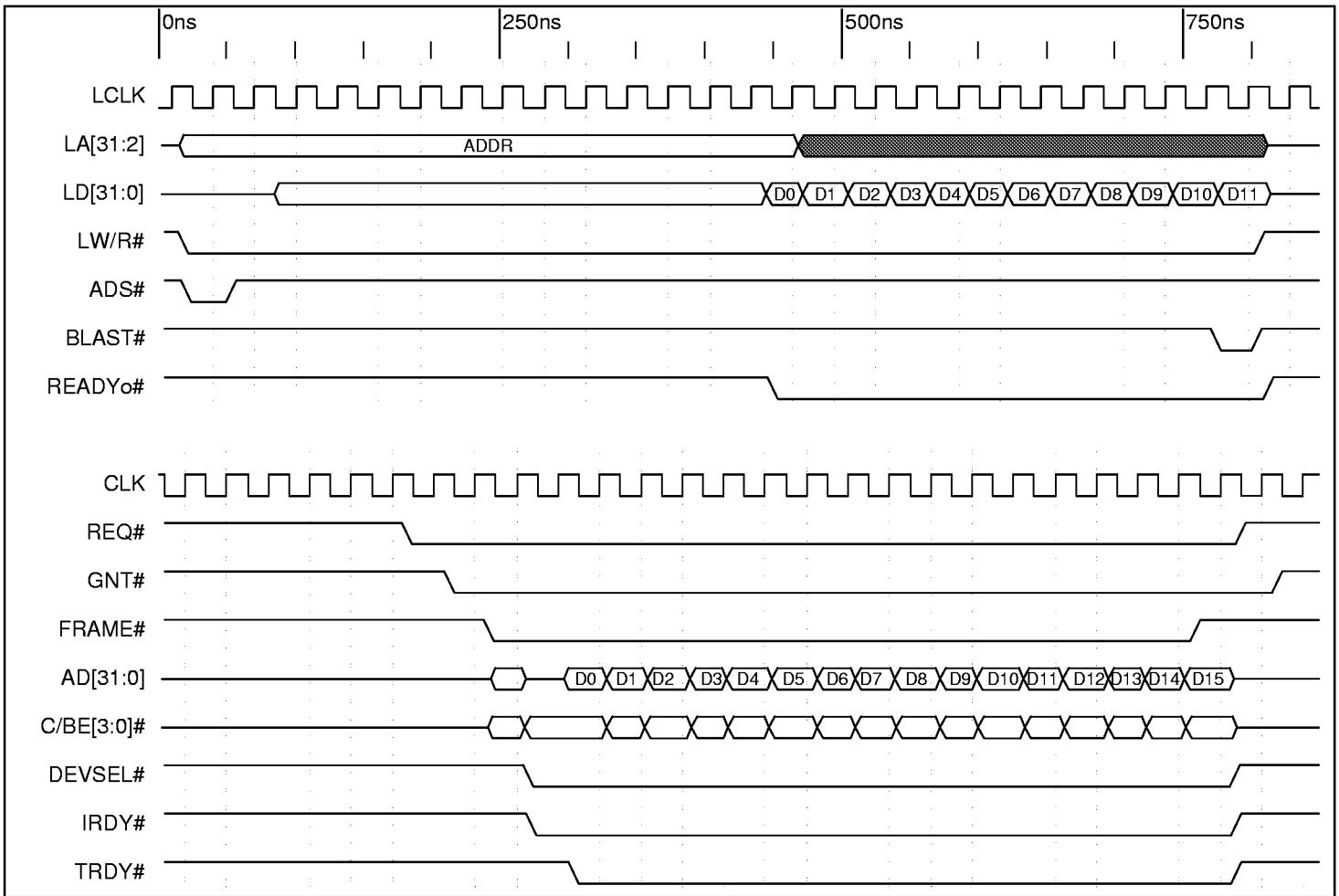
Timing Diagram 8-42. (C Mode) PCI 9080 Direct Master Memory Read—Keep Bus



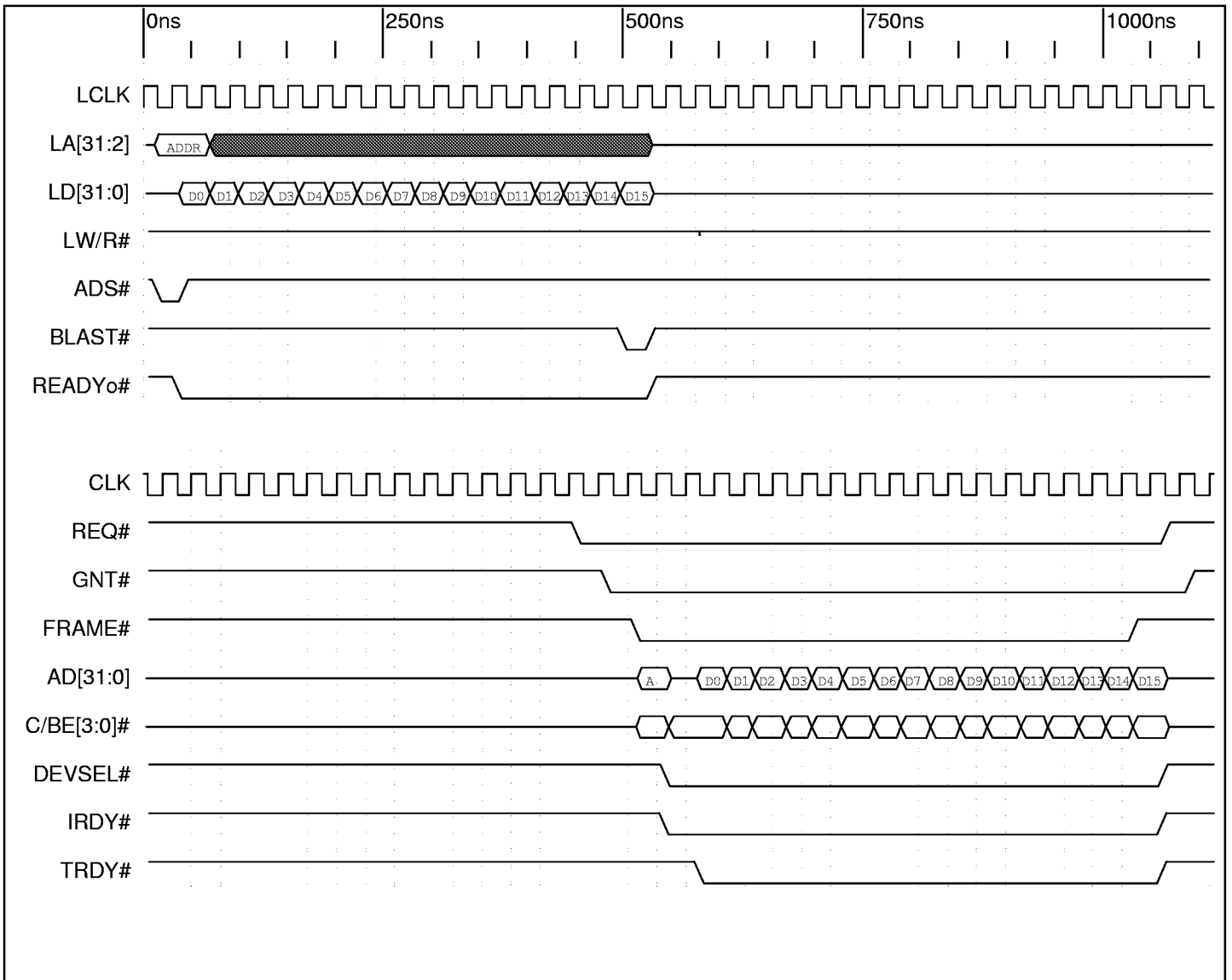
Timing Diagram 8-43. (C Mode) PCI 9080 Direct Master Memory Read—Drop Bus



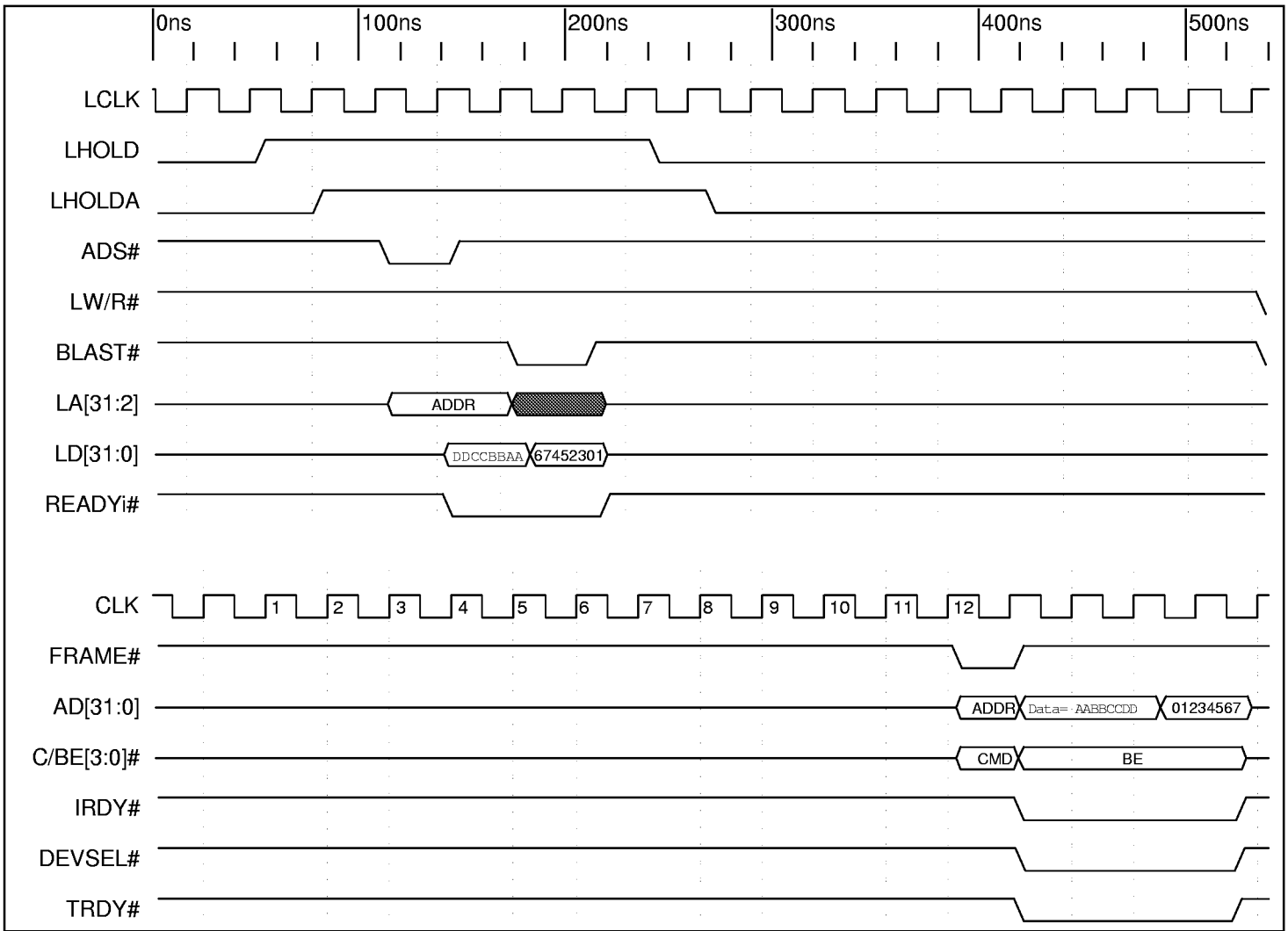
Timing Diagram 8-44. (C Mode) PCI Bus Request (REQ#) Delay During Direct Master Write (8 PCI Clock Delay)



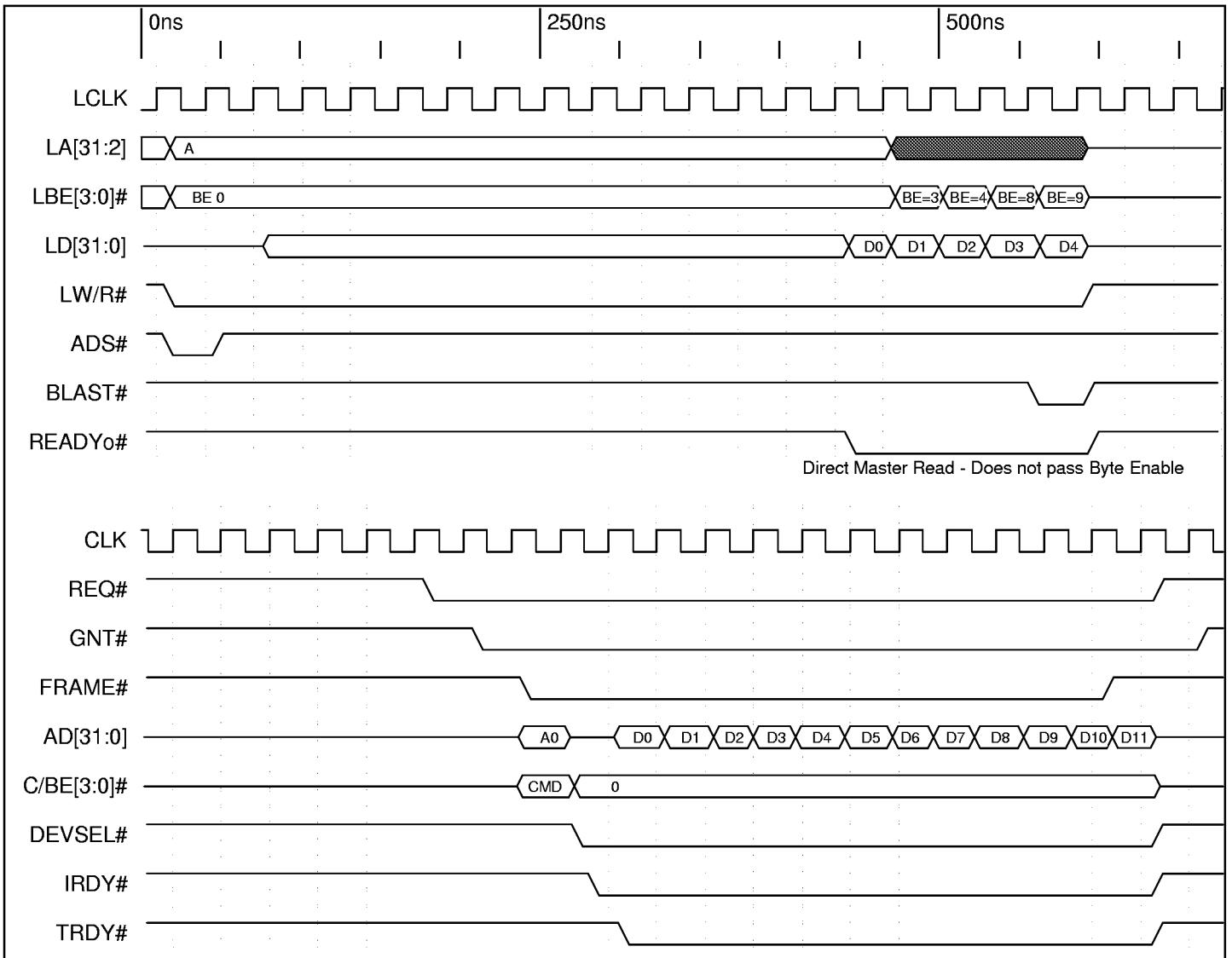
Timing Diagram 8-45. (C Mode) Direct Master Memory Read, Prefetch of 16



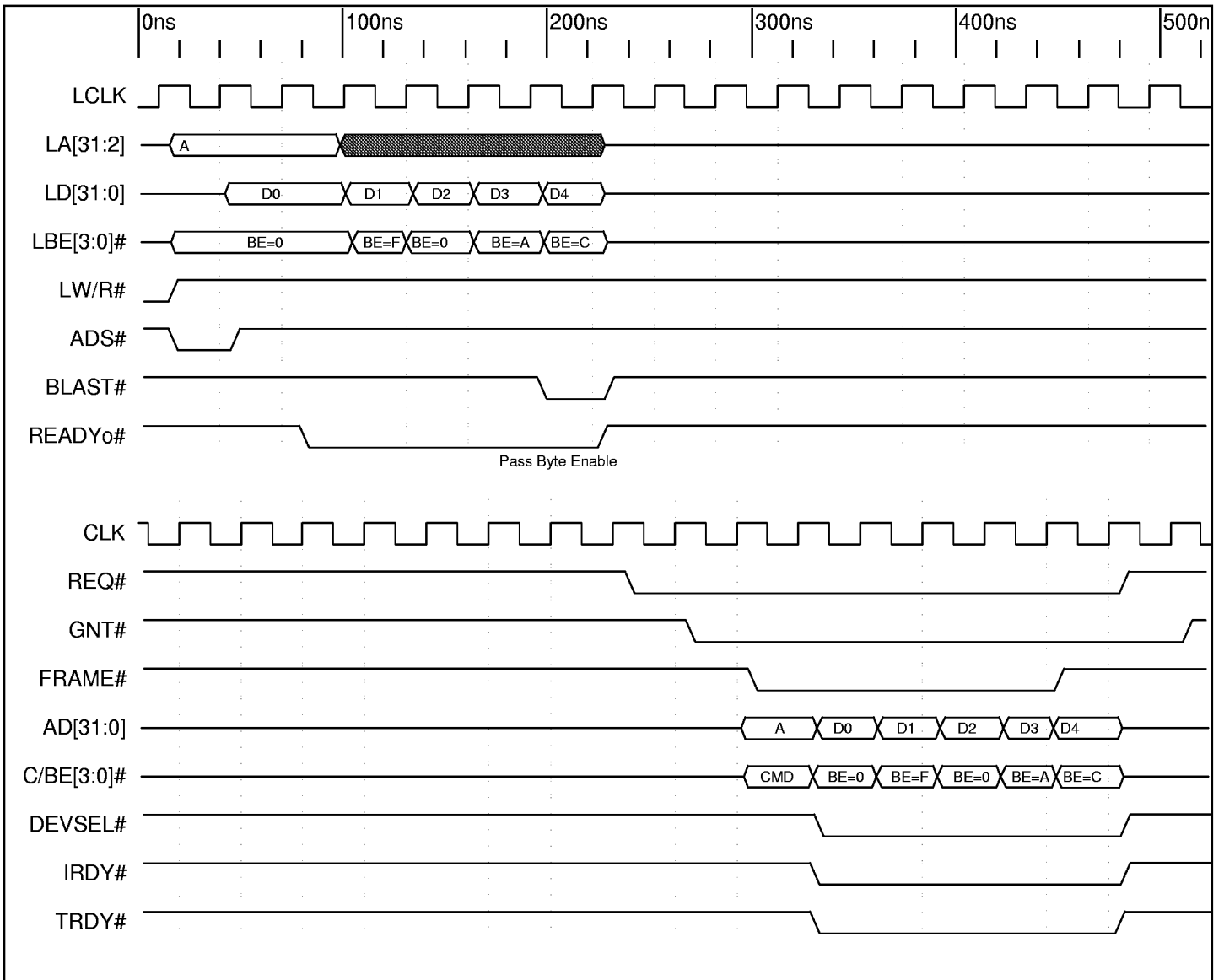
Timing Diagram 8-46. (C Mode) Direct Master Memory Write and Invalidate (MWI)—Cache Line Size of 8



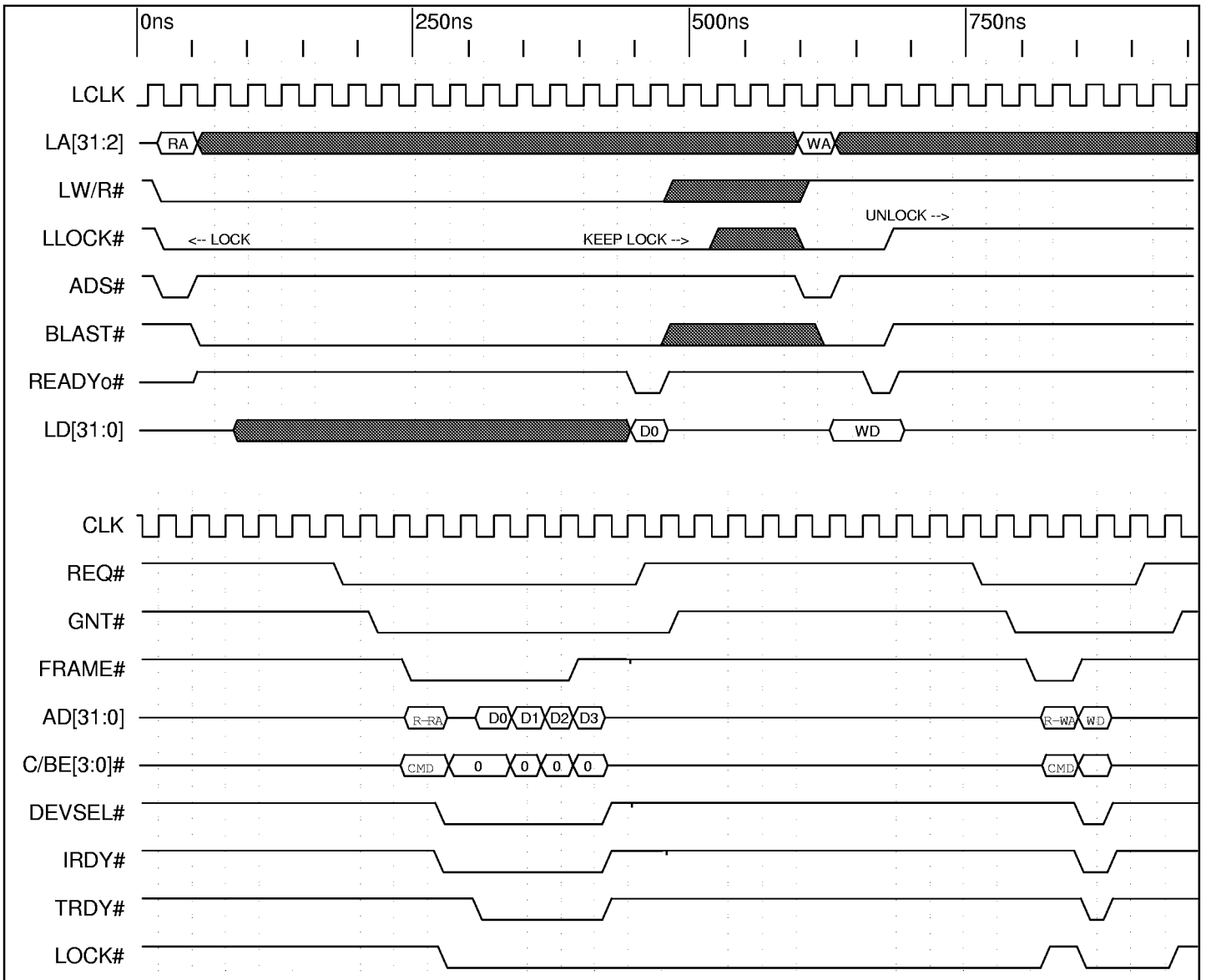
Timing Diagram 8-47. (C Mode) Direct Master in BIGEND Local Bus with BIGEND# Input or Interrupt



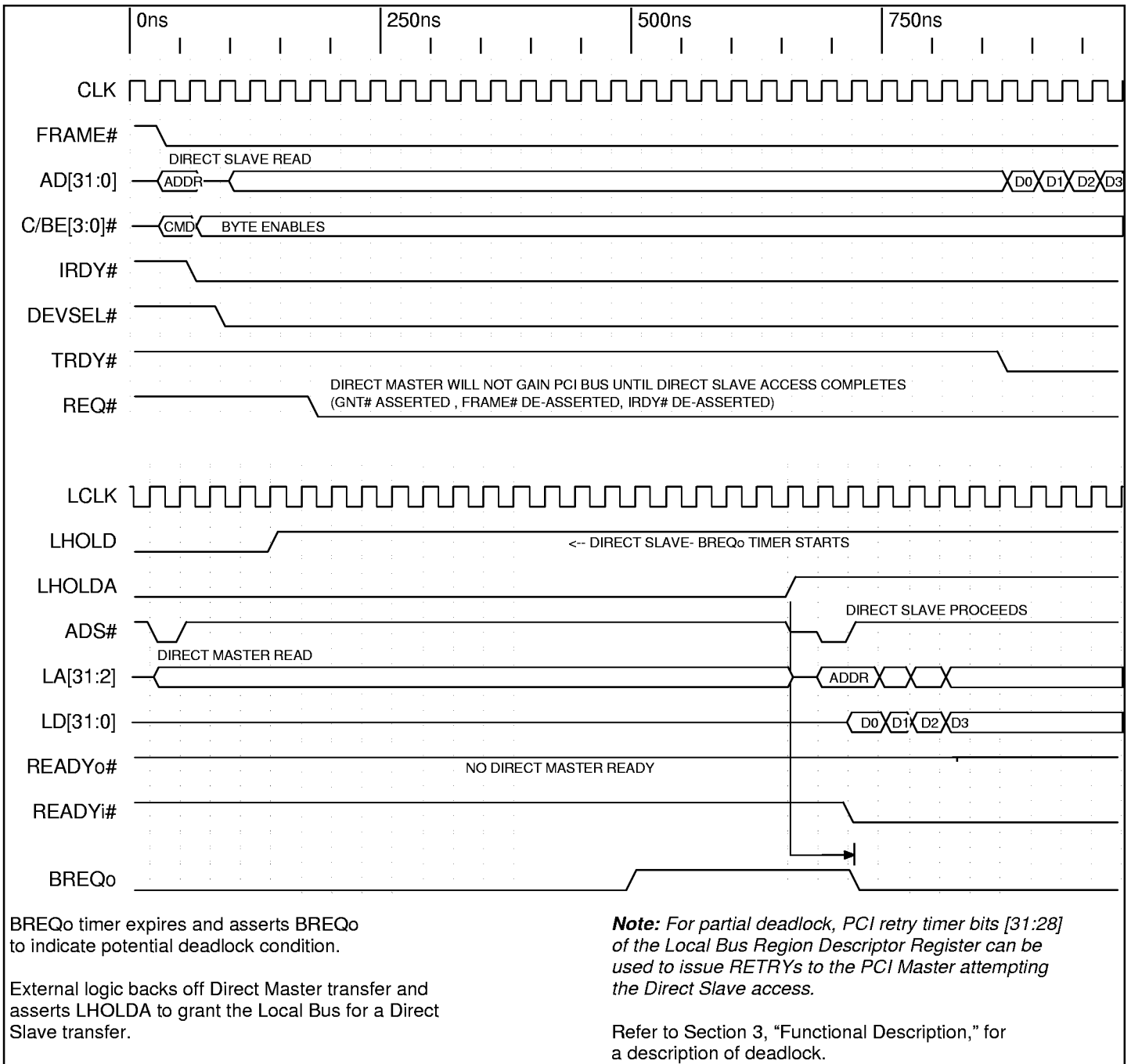
Timing Diagram 8-48. (C Mode) Direct Master Burst, Memory Read Cycles (Changing LBE[3:0]#)



Timing Diagram 8-49. (C Mode) Direct Master Five Lword Burst Write (Changing LBE[3:0]#)

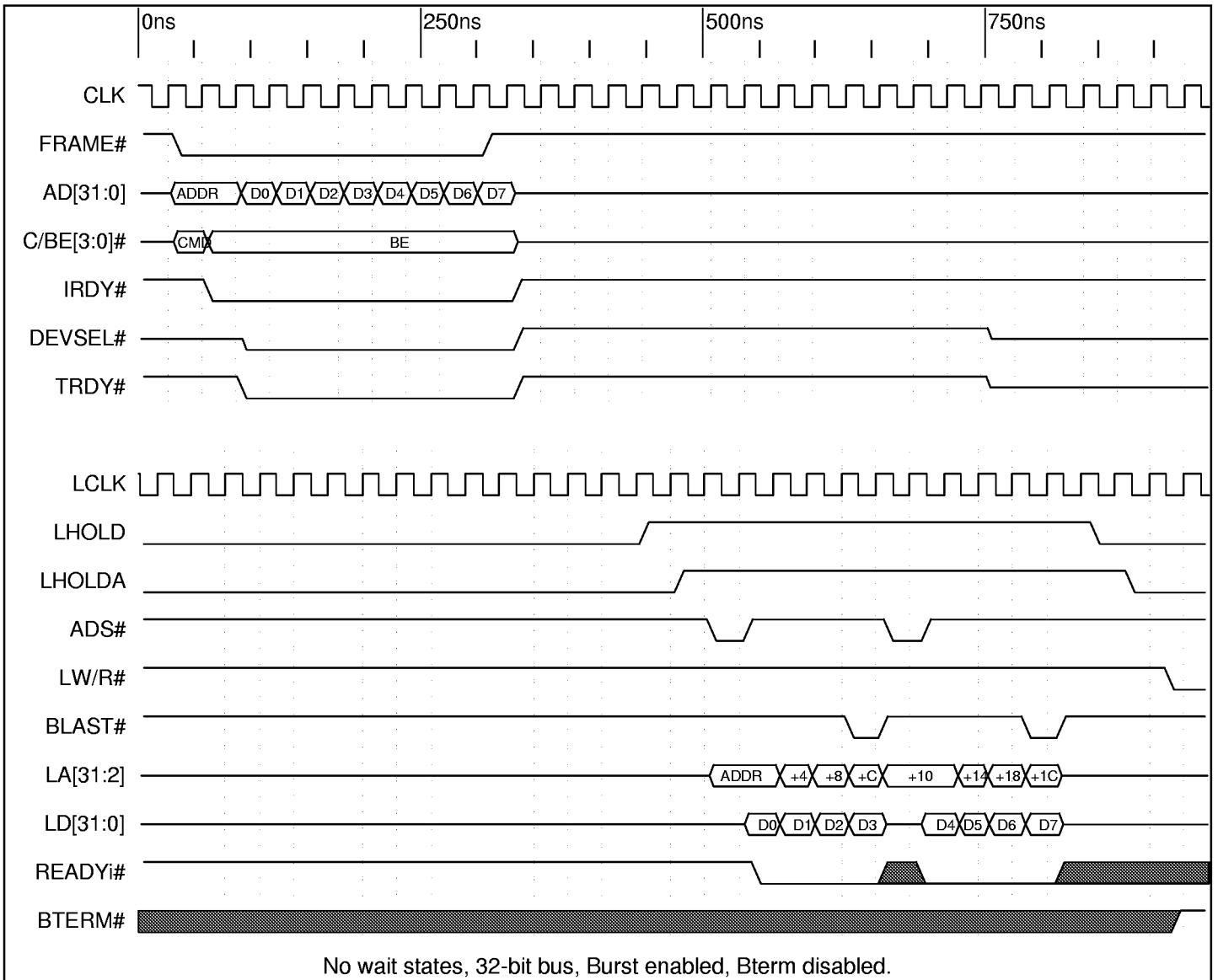


Timing Diagram 8-50. (C Mode) Direct Master Locked Read Followed by Write and Release (LLOCK# and LOCK#)

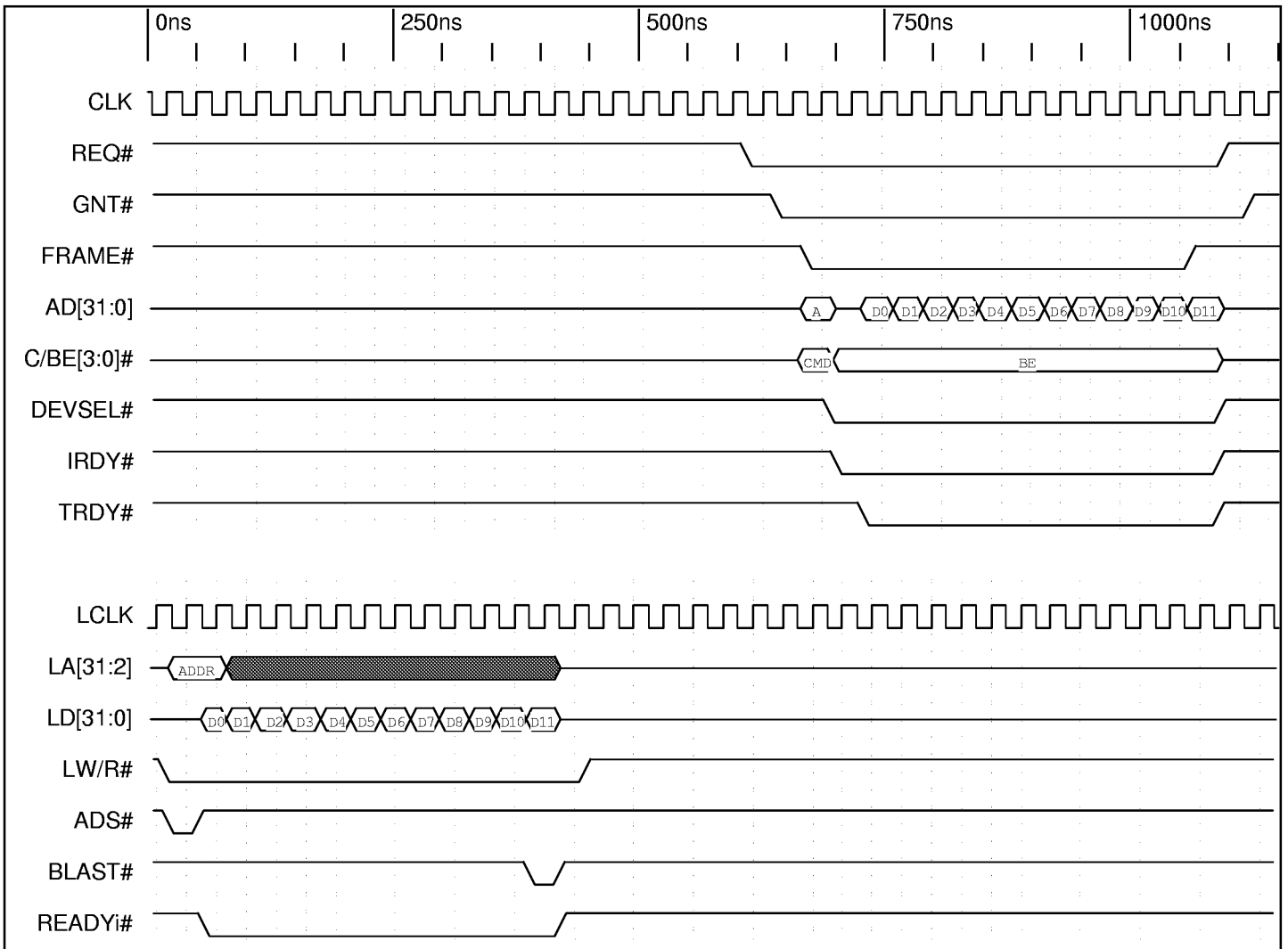


Timing Diagram 8-51. (C Mode) BREQo and Deadlock

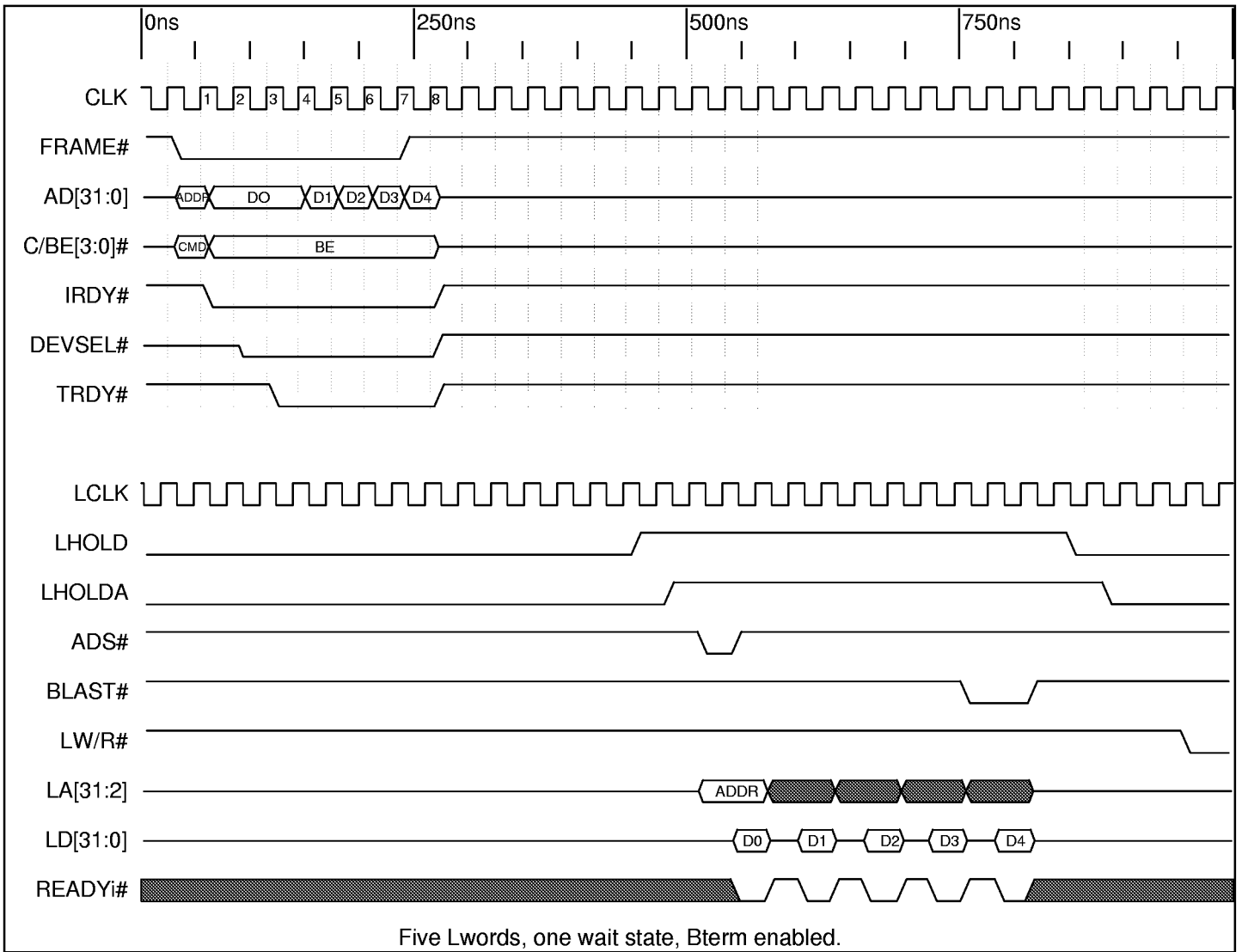
8.3.3 C Mode DMA



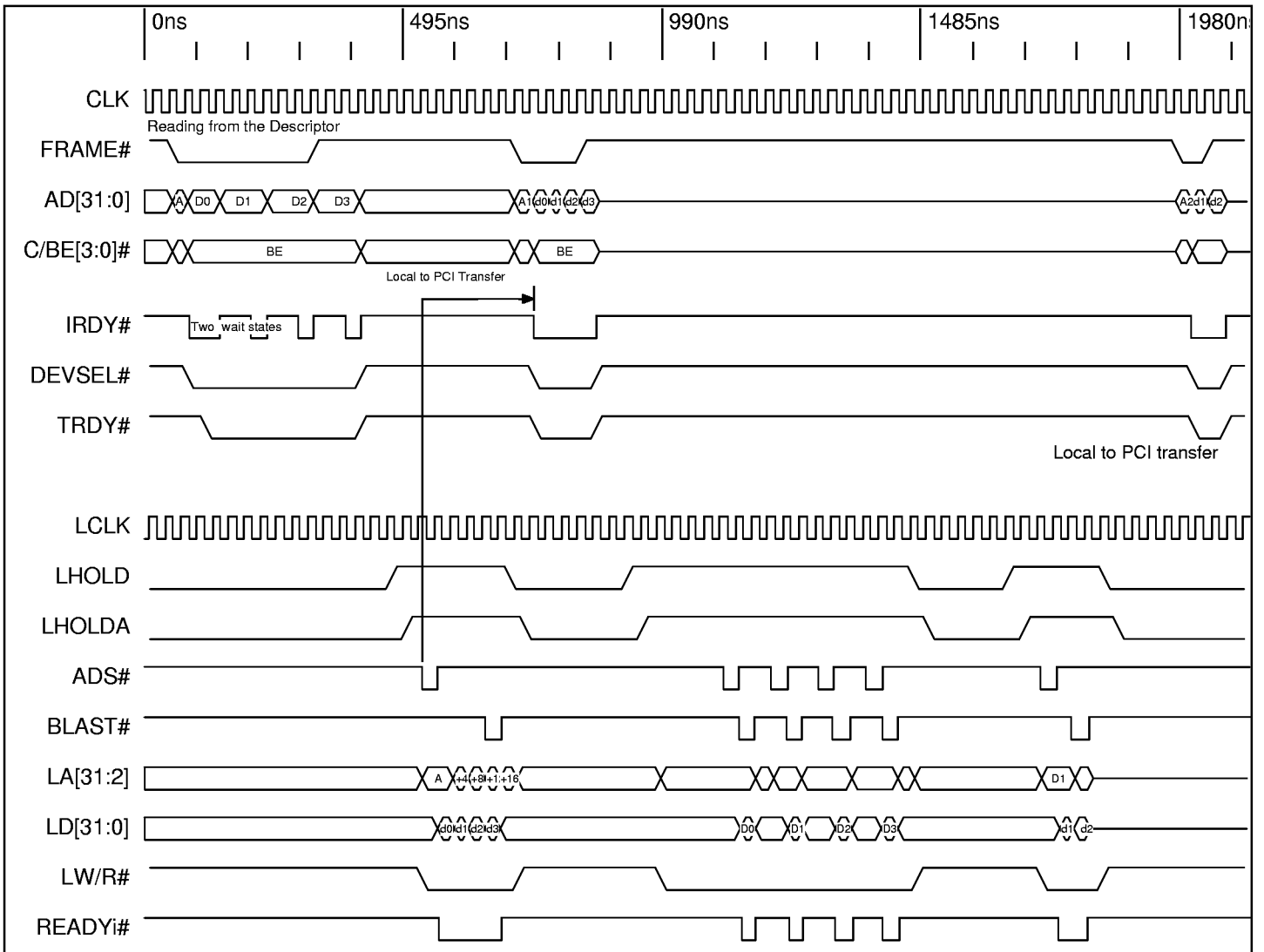
Timing Diagram 8-52. (C Mode) DMA Aligned PCI Address to Aligned Local Address, Bterm Disabled



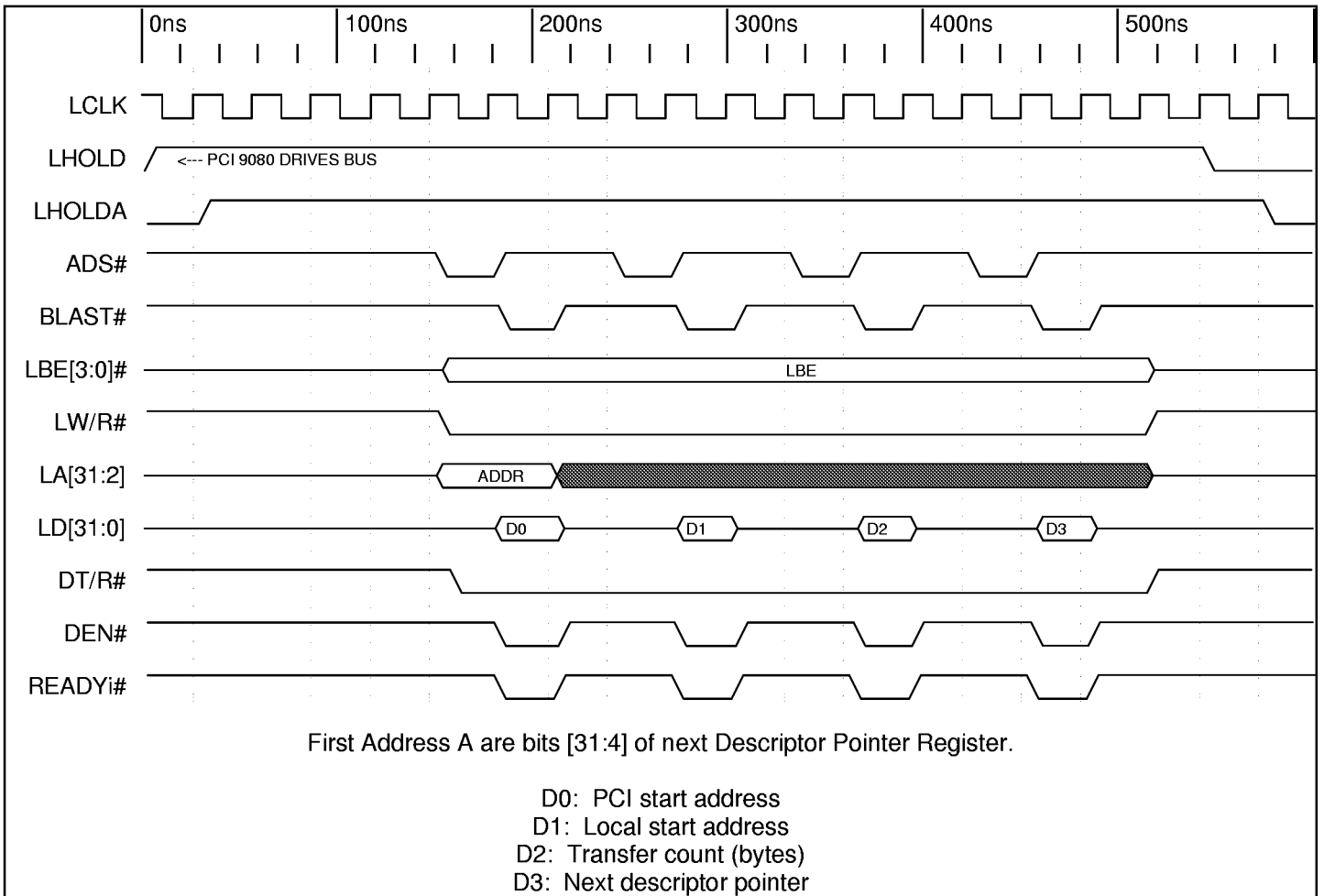
Timing Diagram 8-53. (C Mode) DMA Aligned Local Address to Aligned PCI Address, Burst Enabled, Bterm Enabled



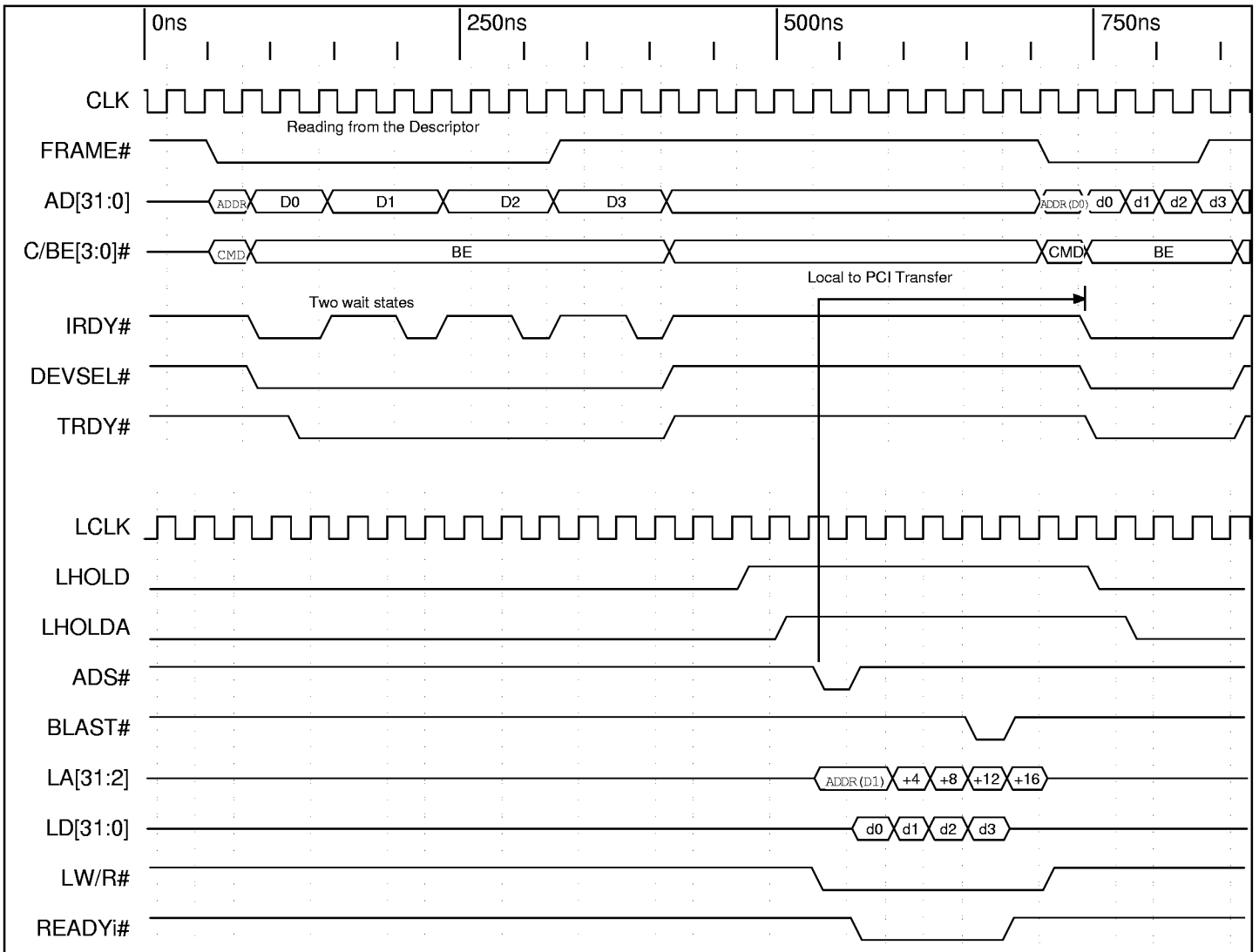
Timing Diagram 8-54. (C Mode) DMA Aligned PCI Address to Aligned Local Address (External Generation of Wait States)



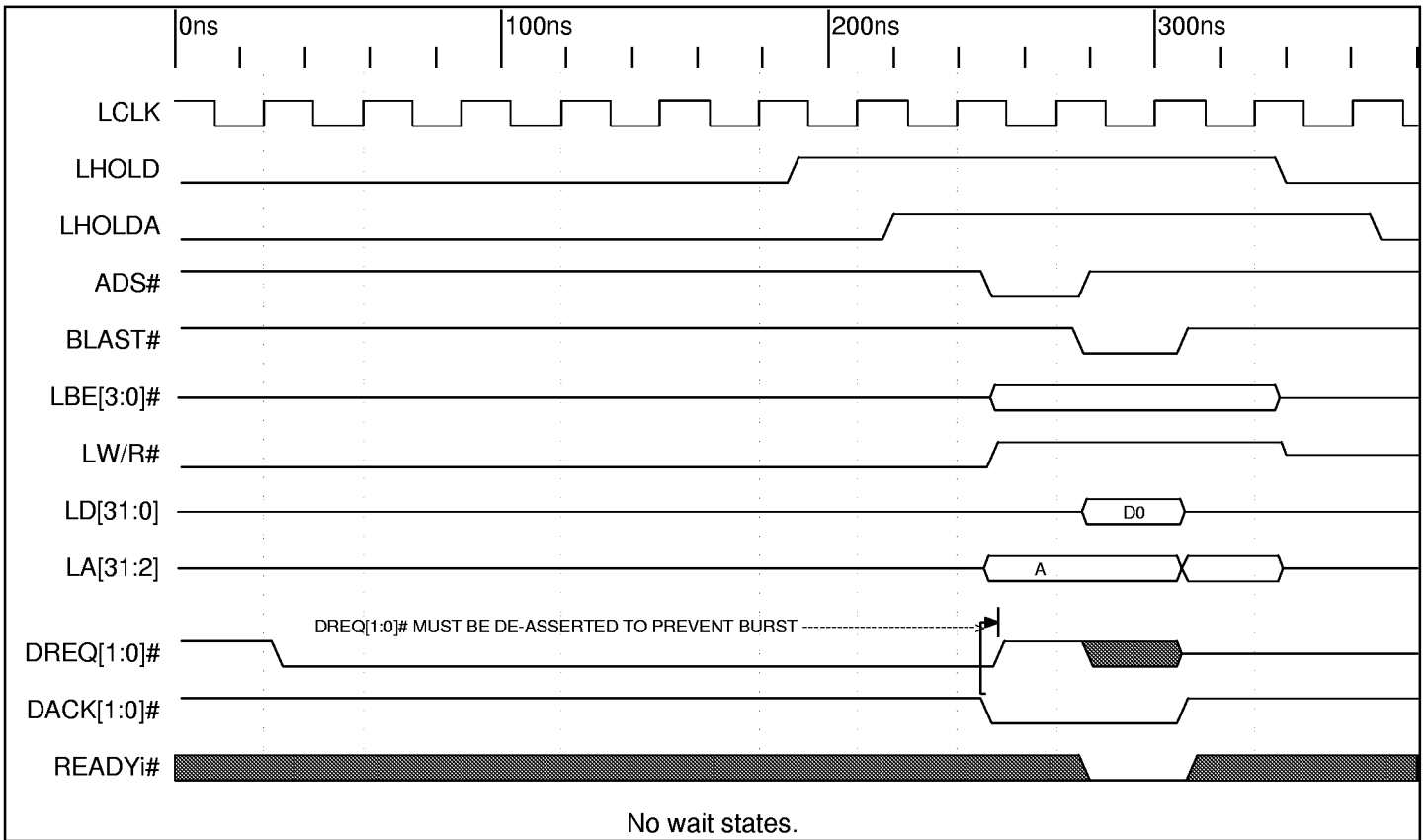
Timing Diagram 8-55. (C Mode) Read of DMA Chaining Parameters from PCI and Local Buses



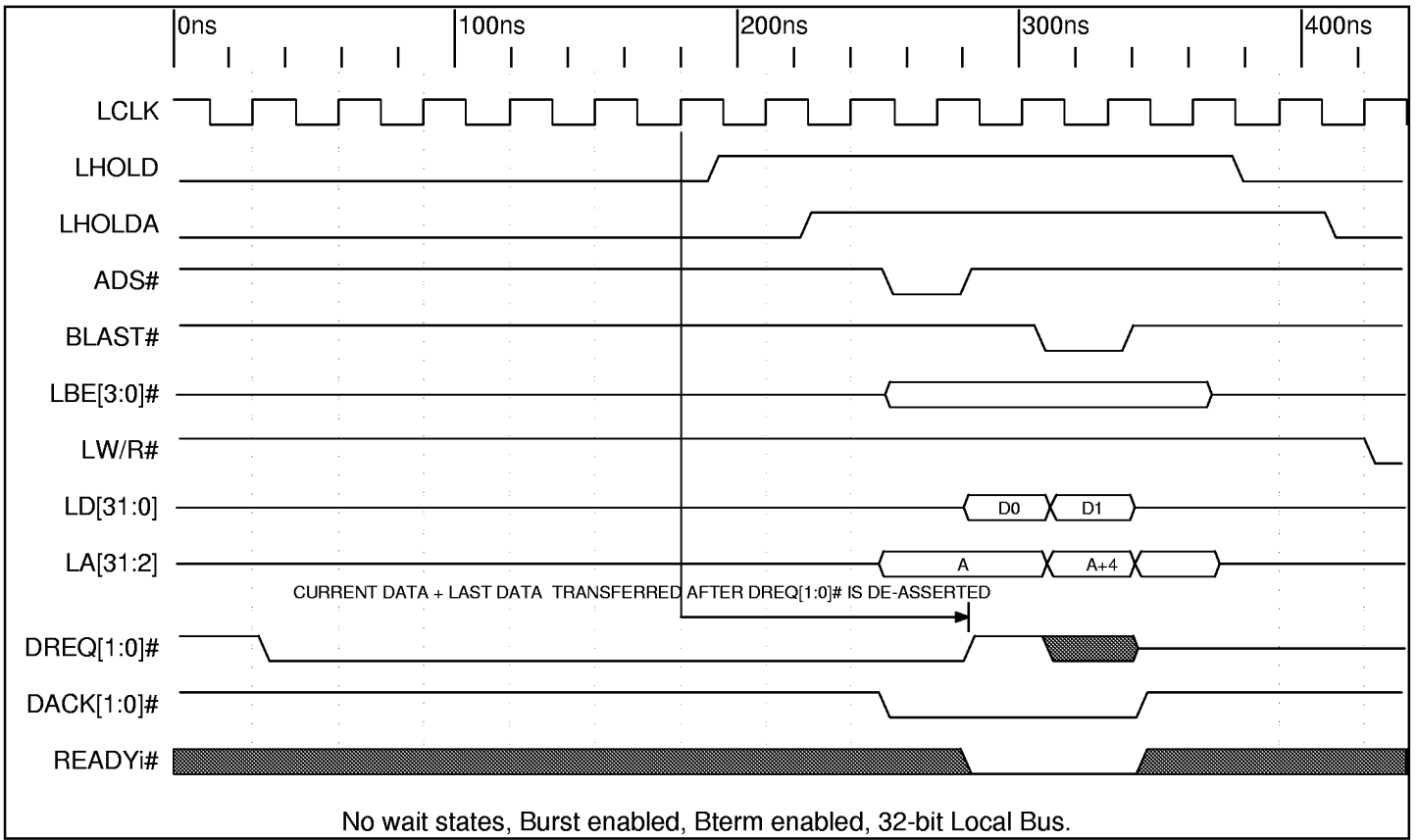
Timing Diagram 8-56. (C Mode) PCI 9080 DMA Read of Chaining Parameters from Local Bus, No Wait States



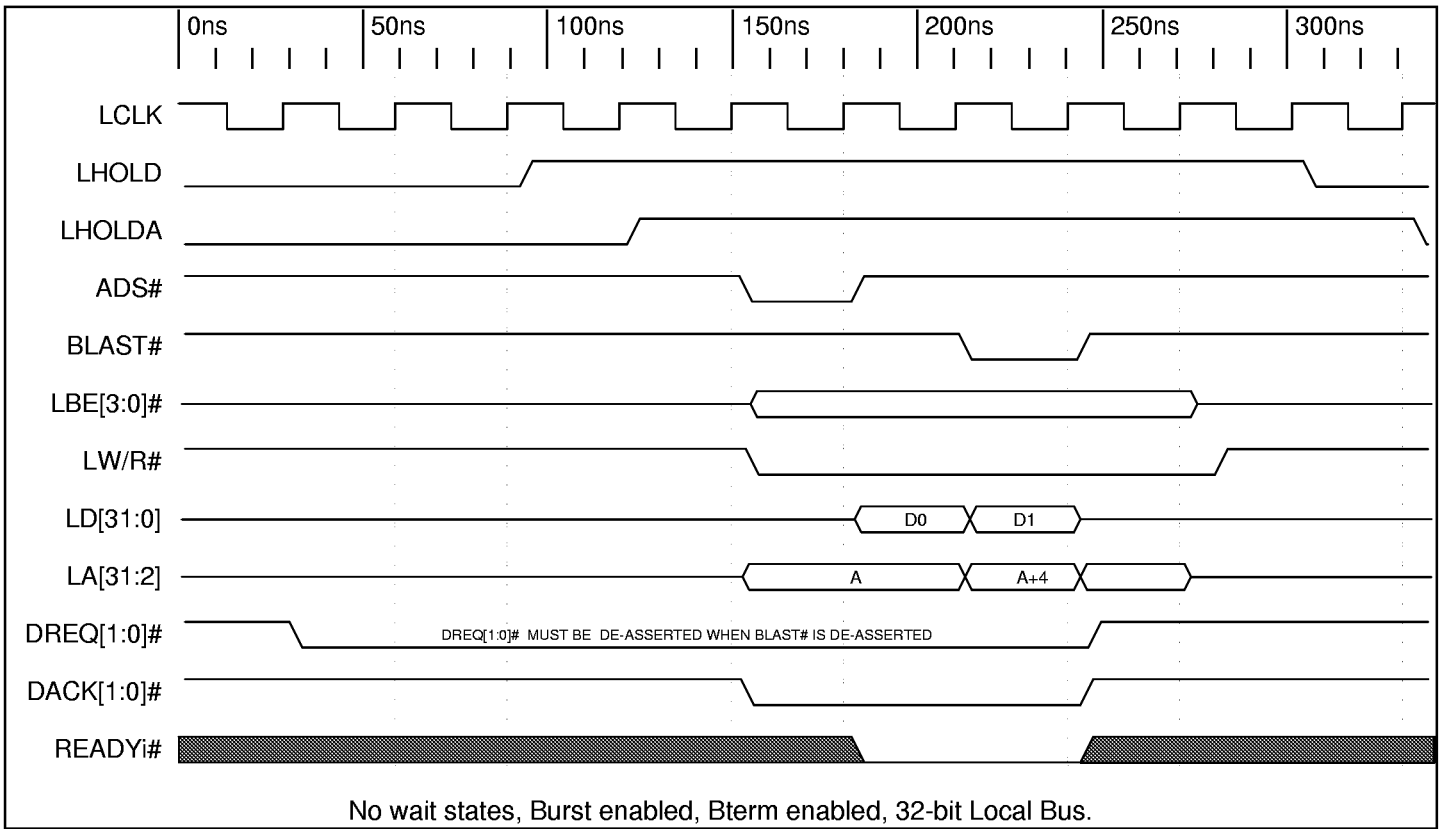
Timing Diagram 8-57. (C Mode) Read of DMA Chaining Parameters from PCI Bus (Local-to-PCI Transfer)



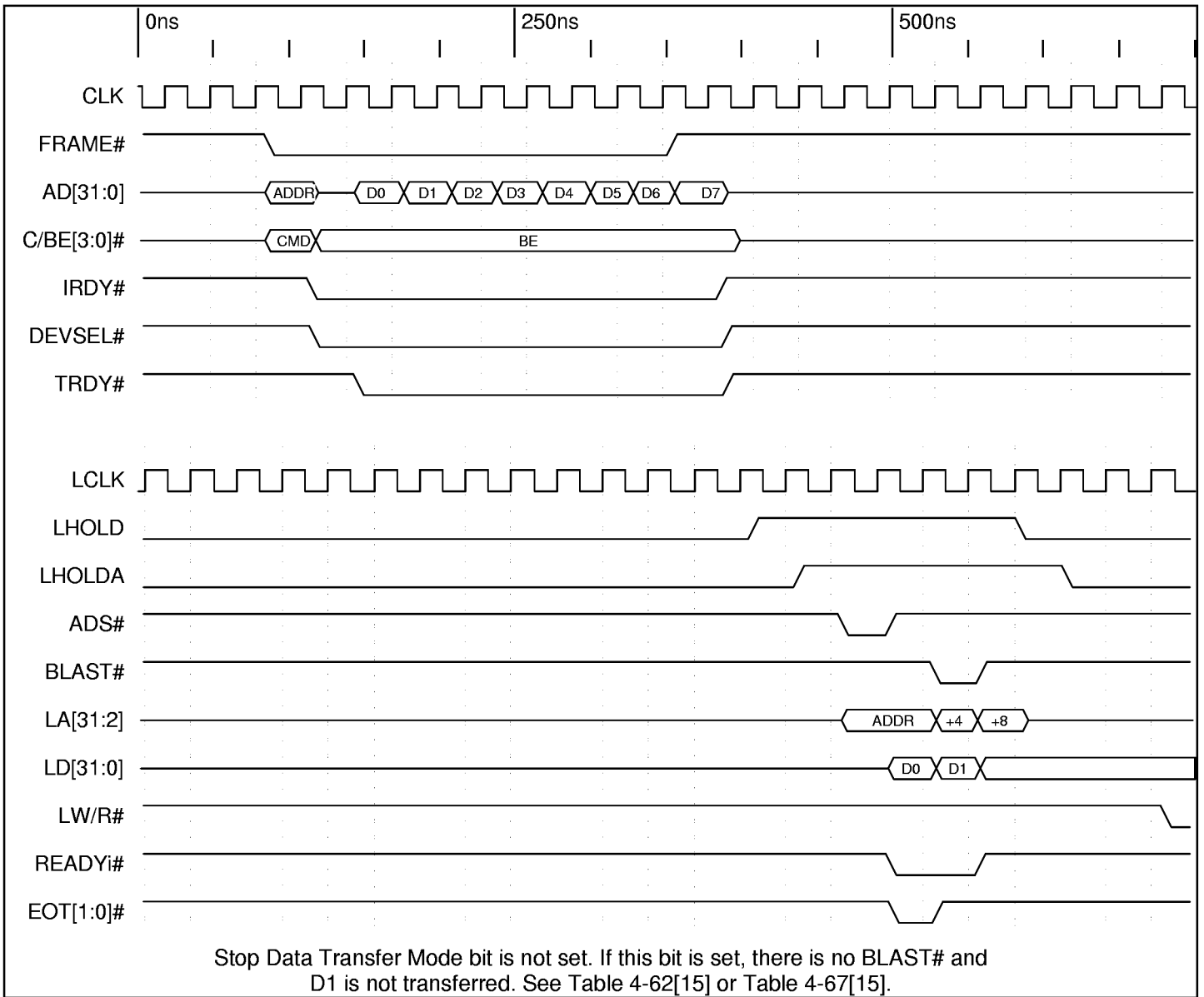
Timing Diagram 8-58. (C Mode) Single Cycle DMA Demand Mode PCI-to-Local



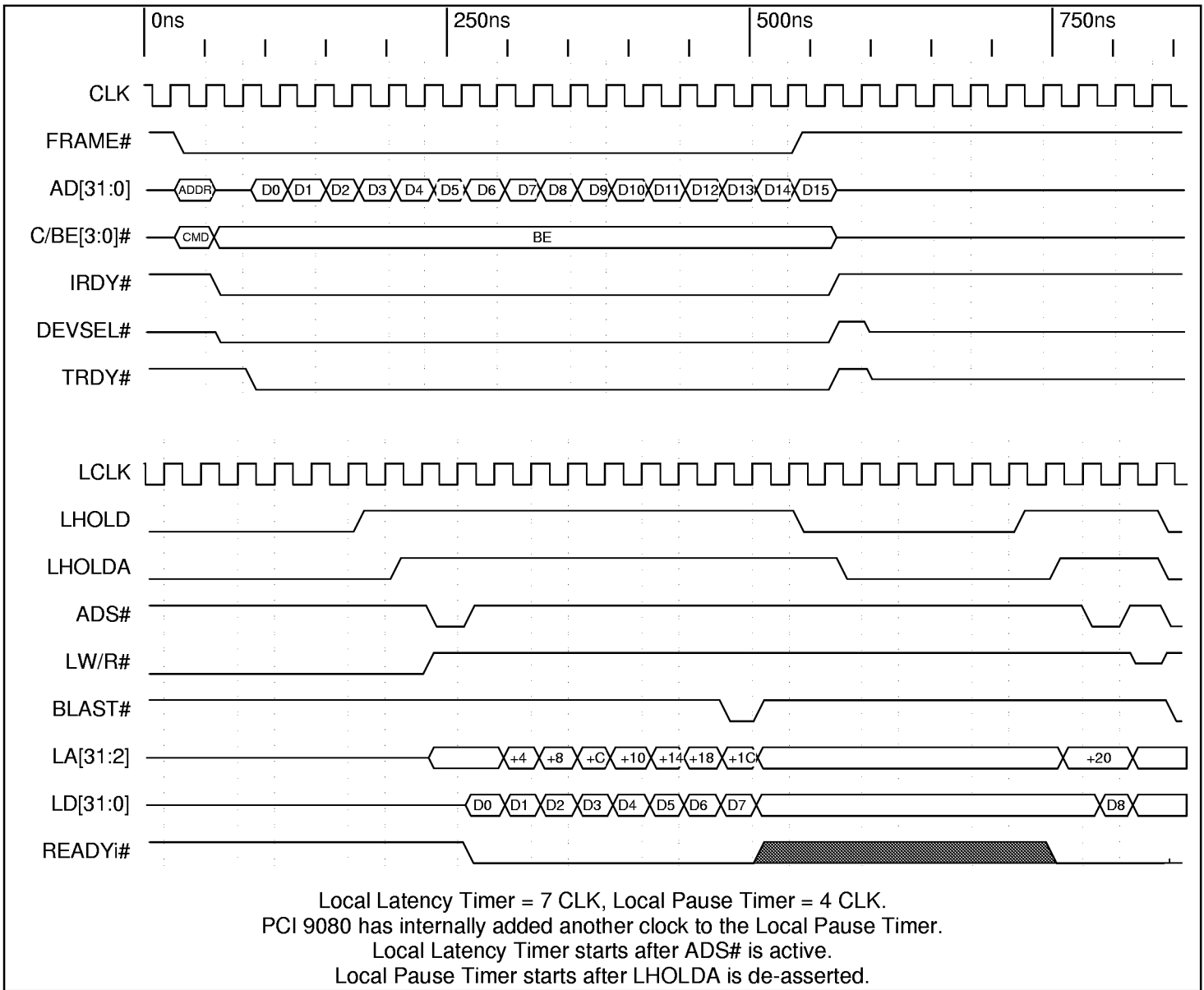
Timing Diagram 8-59. (C Mode) Multiple Cycle (Burst) DMA Demand Mode PCI-to-Local, No Wait States



Timing Diagram 8-60. (C Mode) DMA Demand Mode Terminated with BLAST# (Local-to-PCI)



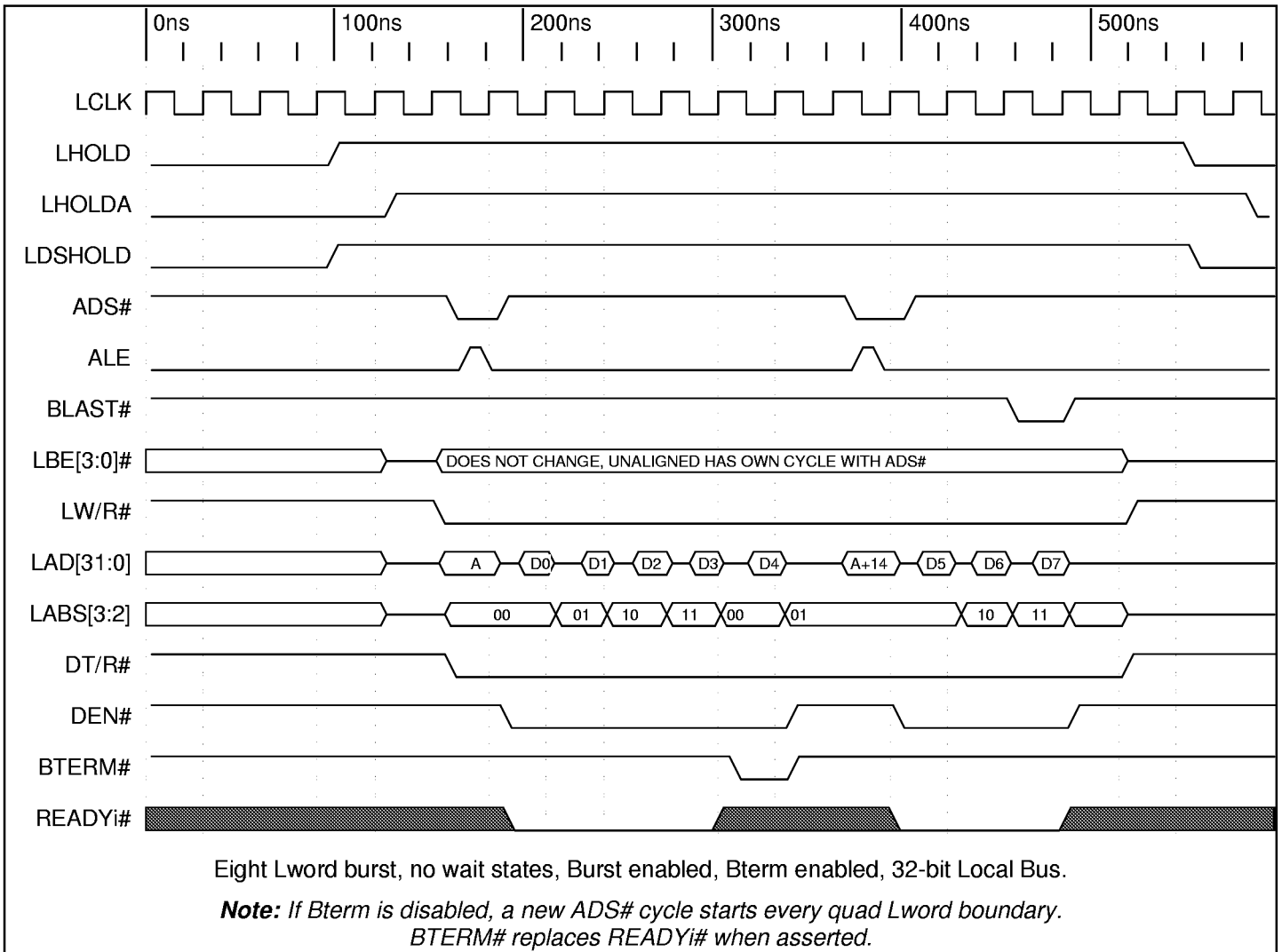
Timing Diagram 8-62. (C Mode) DMA PCI-to-Local, Terminated with EOT[1:0]#



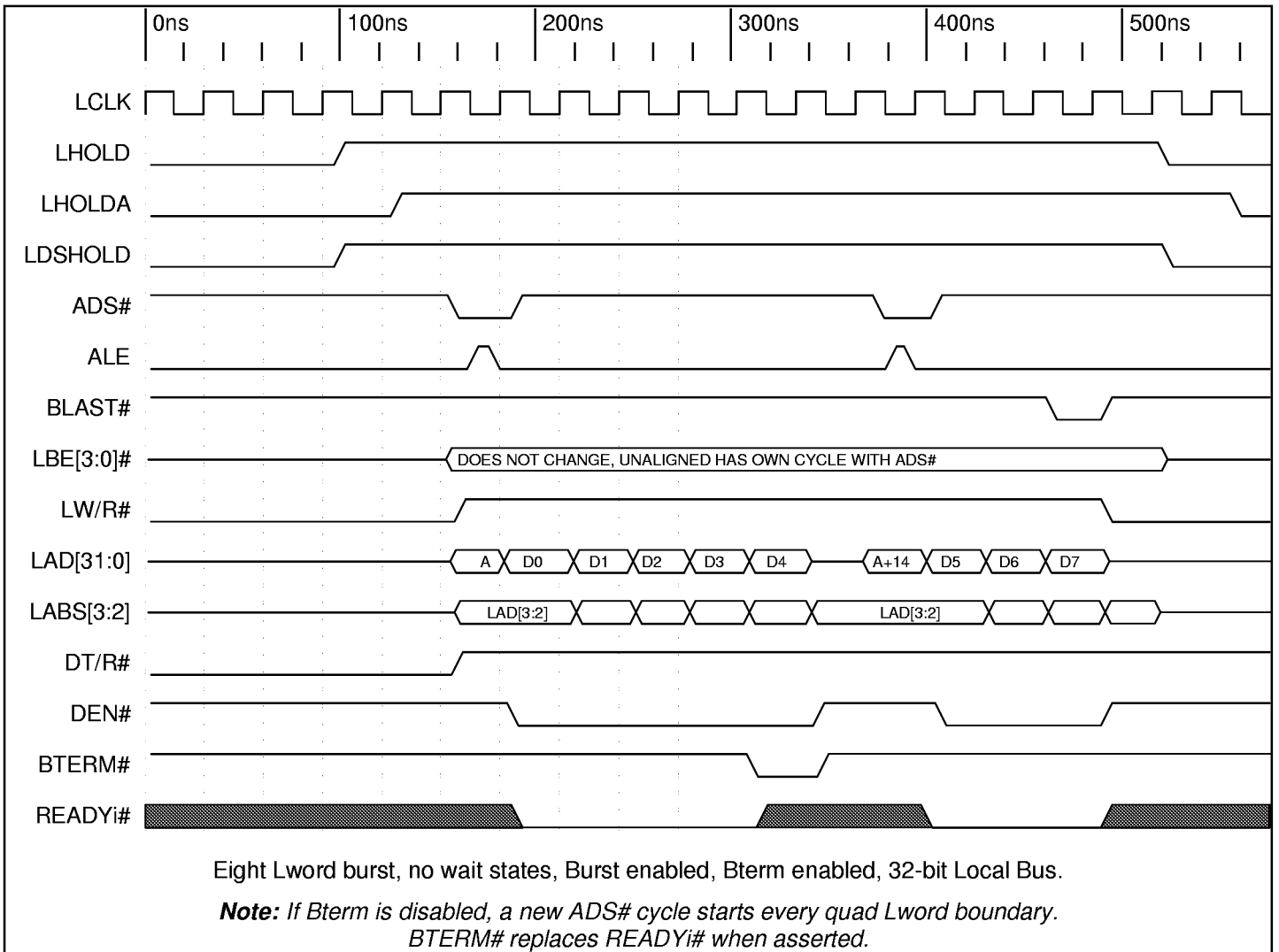
Timing Diagram 8-63. (C Mode) DMA PCI-to-Local with Local Pause Timer and Local Latency Timer

8.4 J MODE

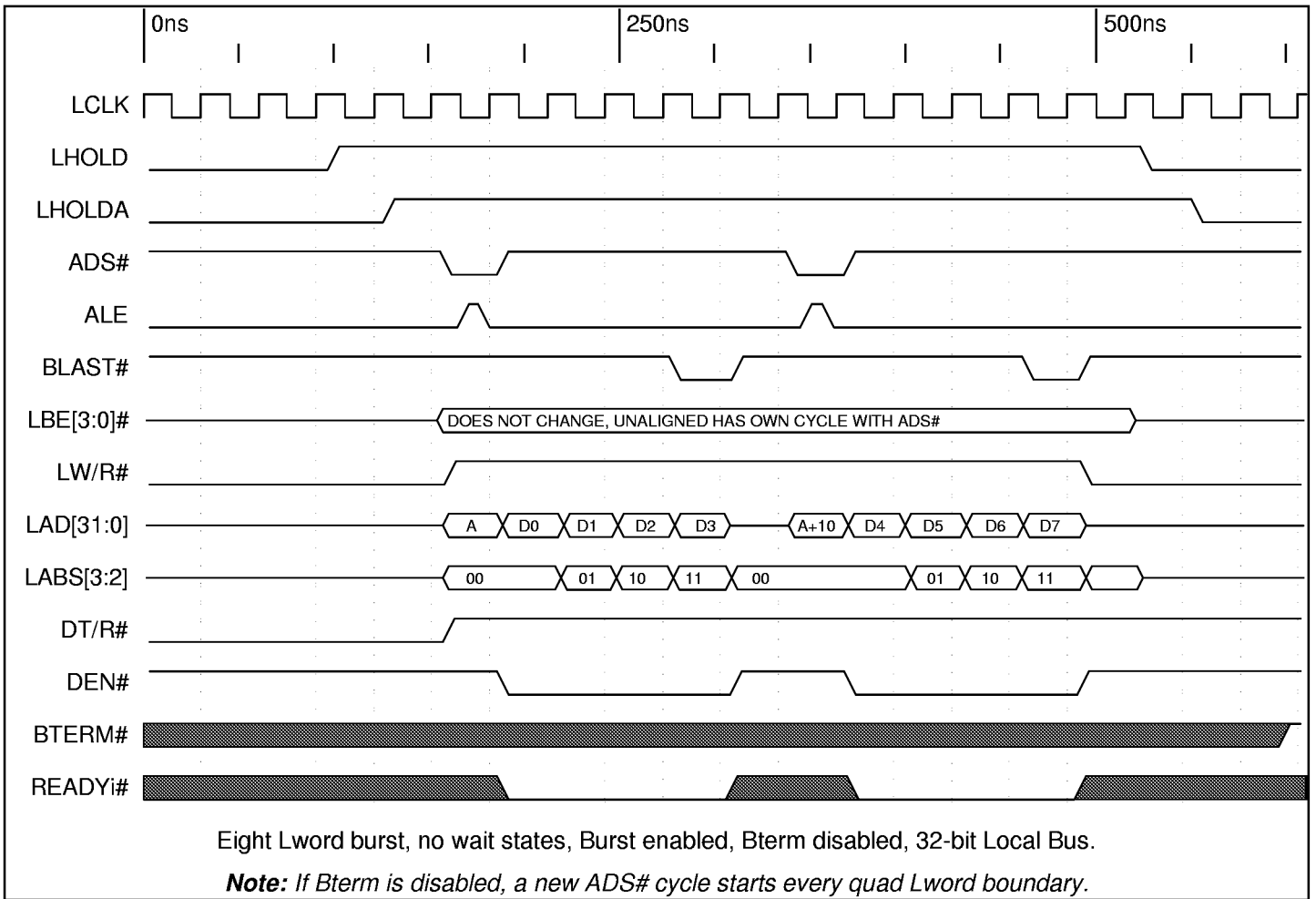
8.4.1 J Mode Direct Slave



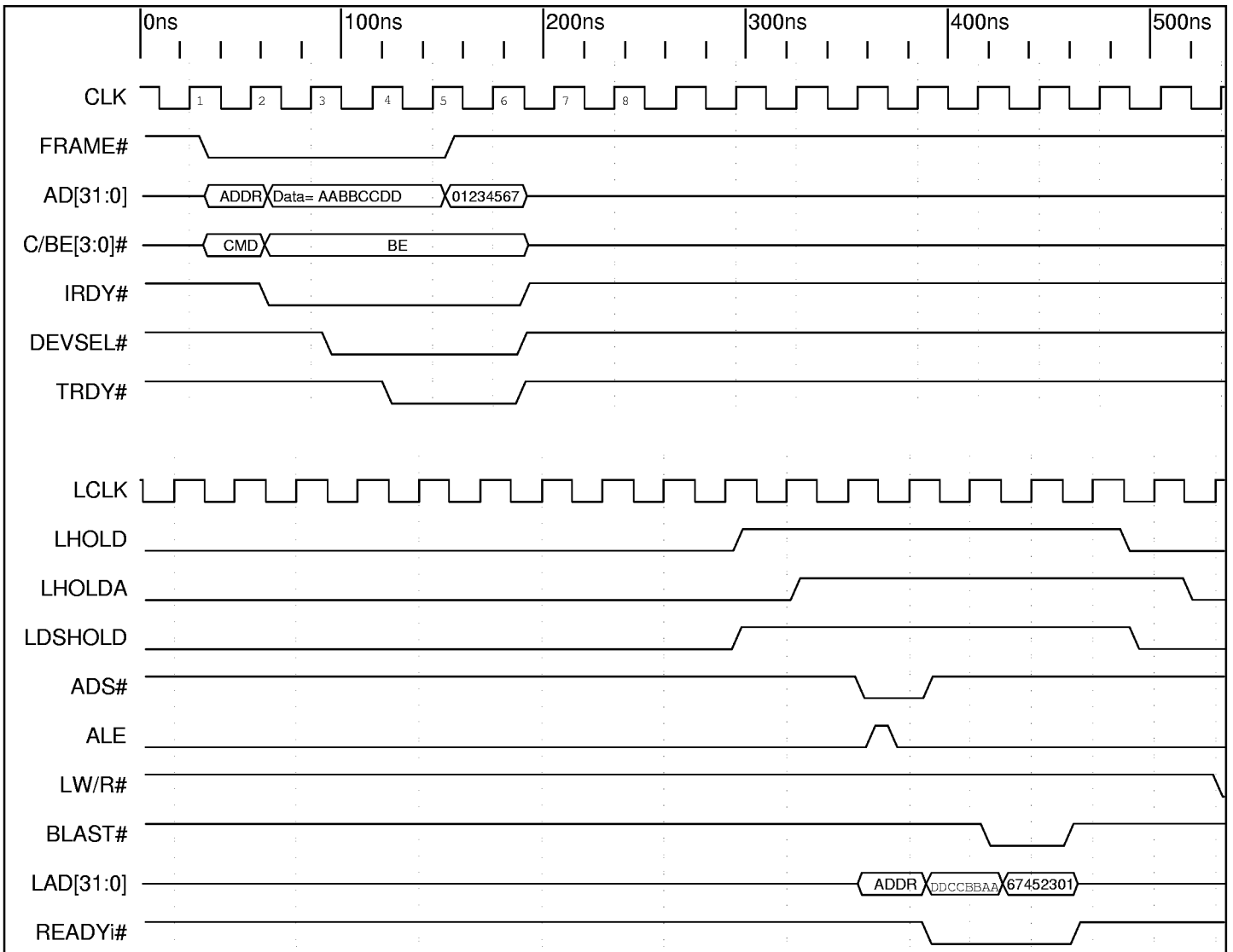
Timing Diagram 8-64. (J Mode) PCI 9080 Direct Slave Burst Read from Local Bus, No Wait States, Bterm Enabled



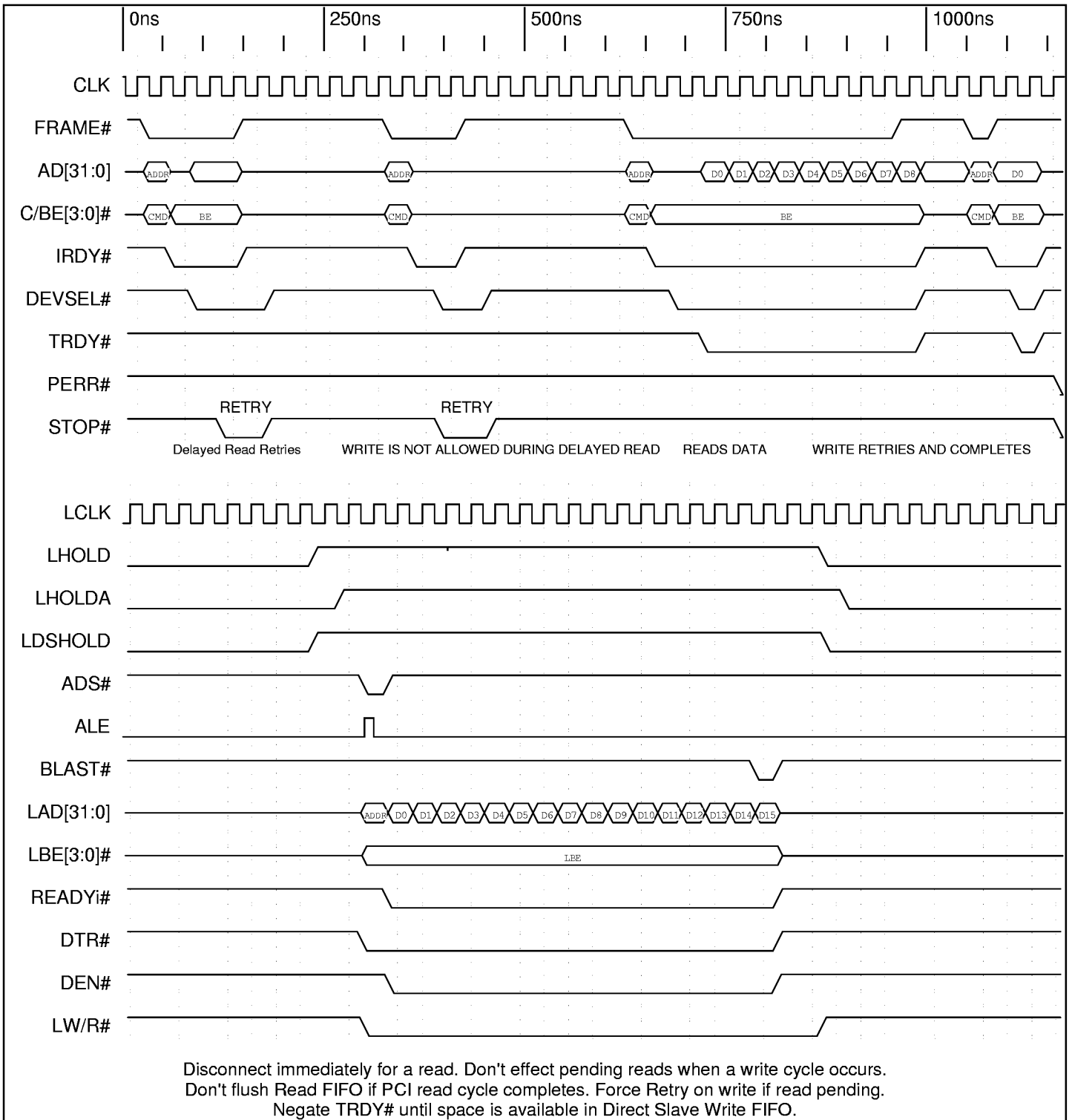
Timing Diagram 8-65. (J Mode) PCI 9080 Direct Slave Burst Write to Local Bus, No Wait States, Bterm Enabled



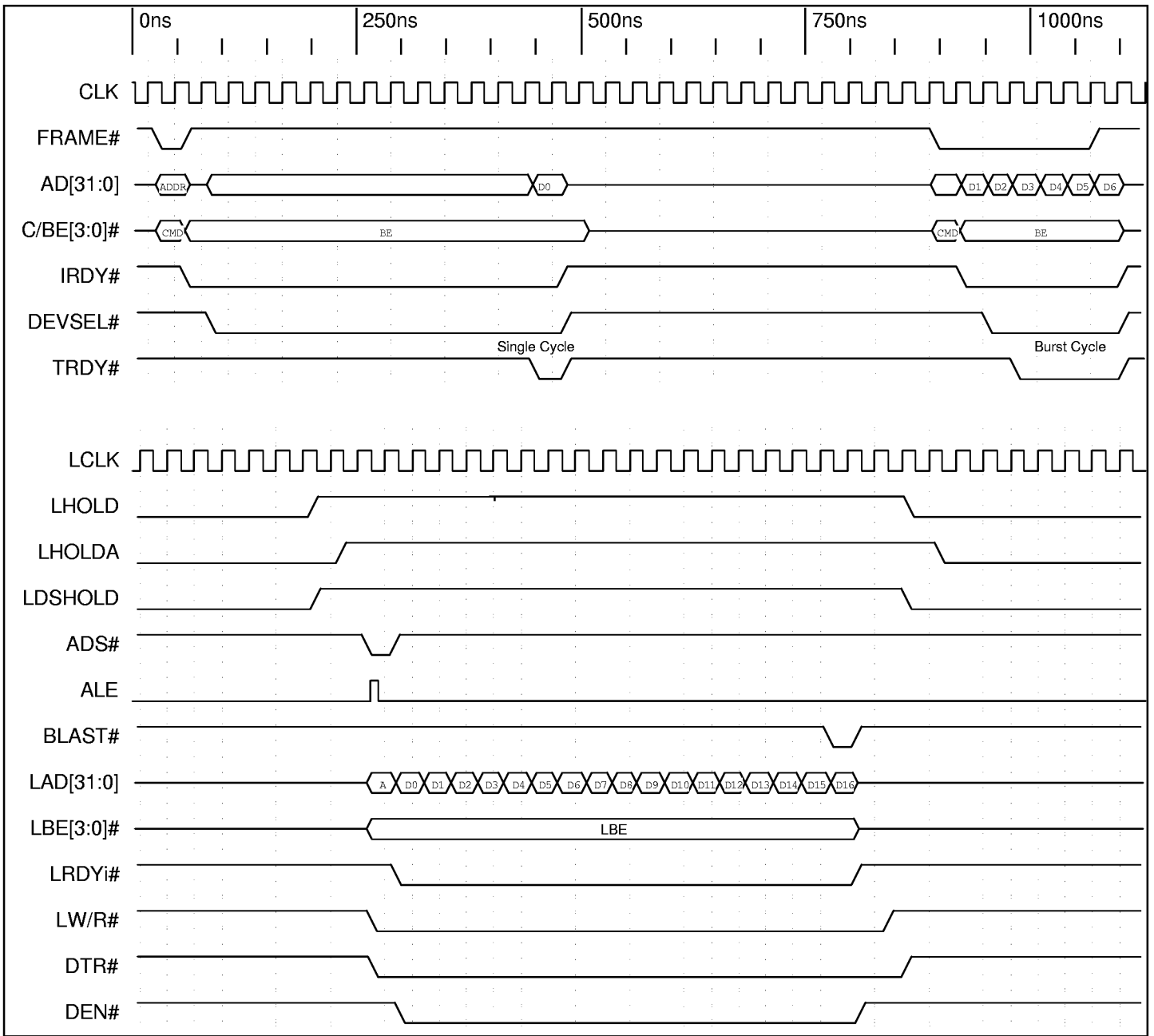
Timing Diagram 8-66. (J Mode) PCI 9080 DMA or Direct Slave Burst Write to Local Bus, No Wait States, Bterm Disabled



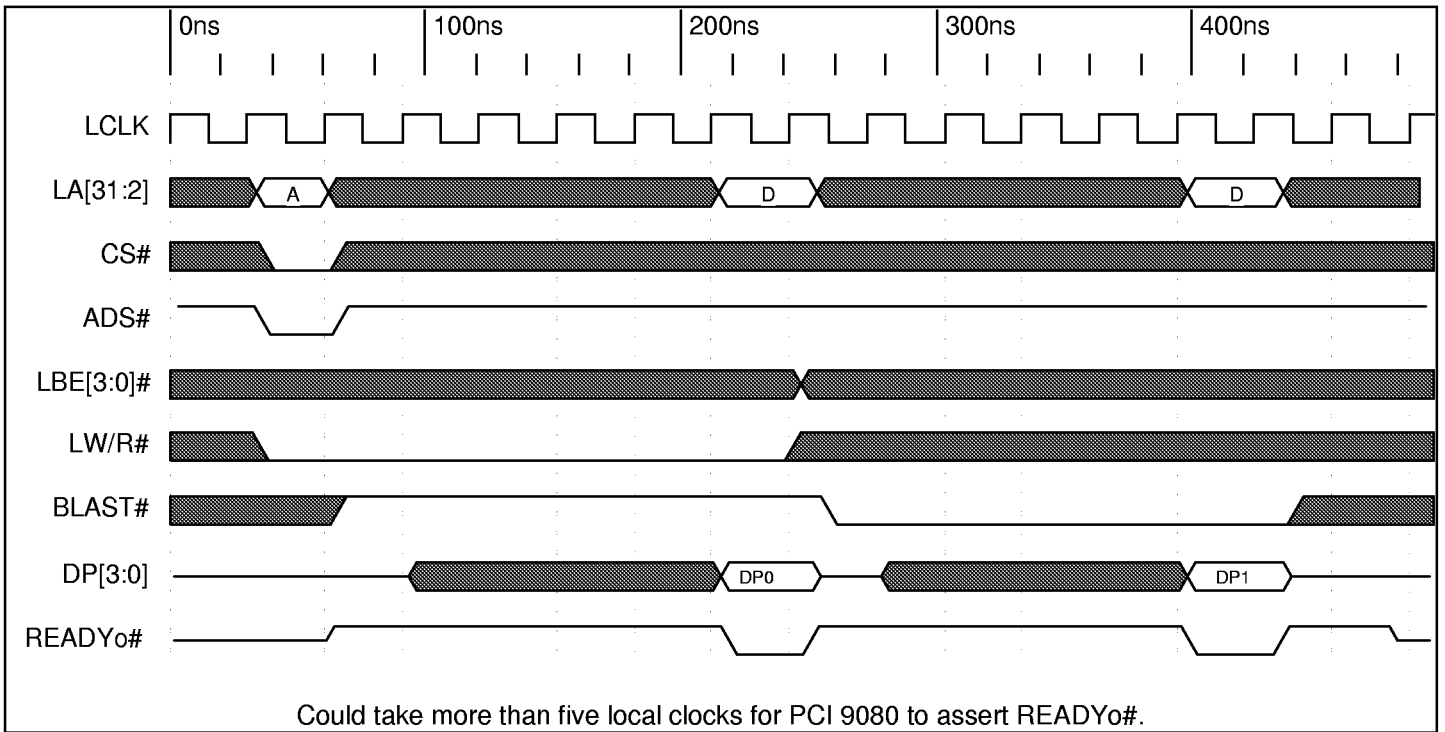
Timing Diagram 8-67. (J Mode) Direct Slave in BIGEND Local Bus with BIGEND# Input or Internal Register Setting



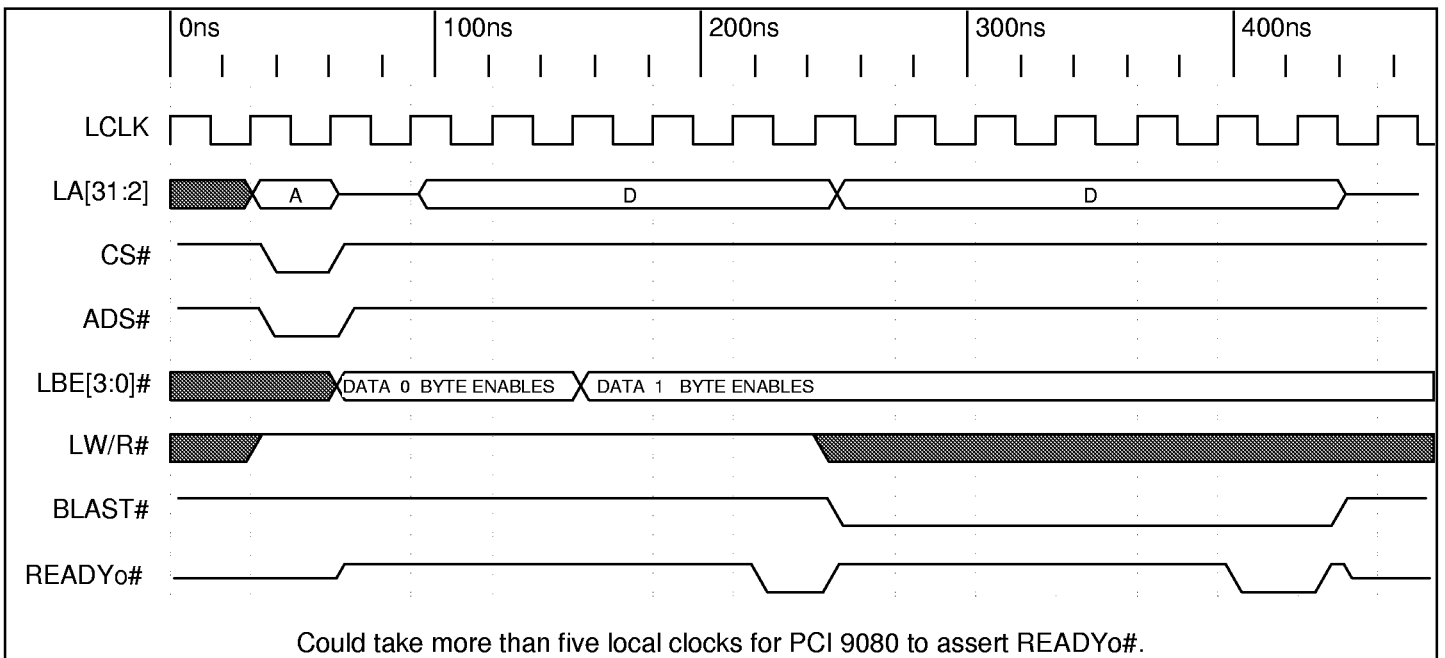
Timing Diagram 8-68. (J Mode) Direct Slave Read v2.1 Spec



Timing Diagram 8-69. (J Mode) Direct Slave Read No Flush Mode (Read Ahead Mode), Prefetch Mode Enabled

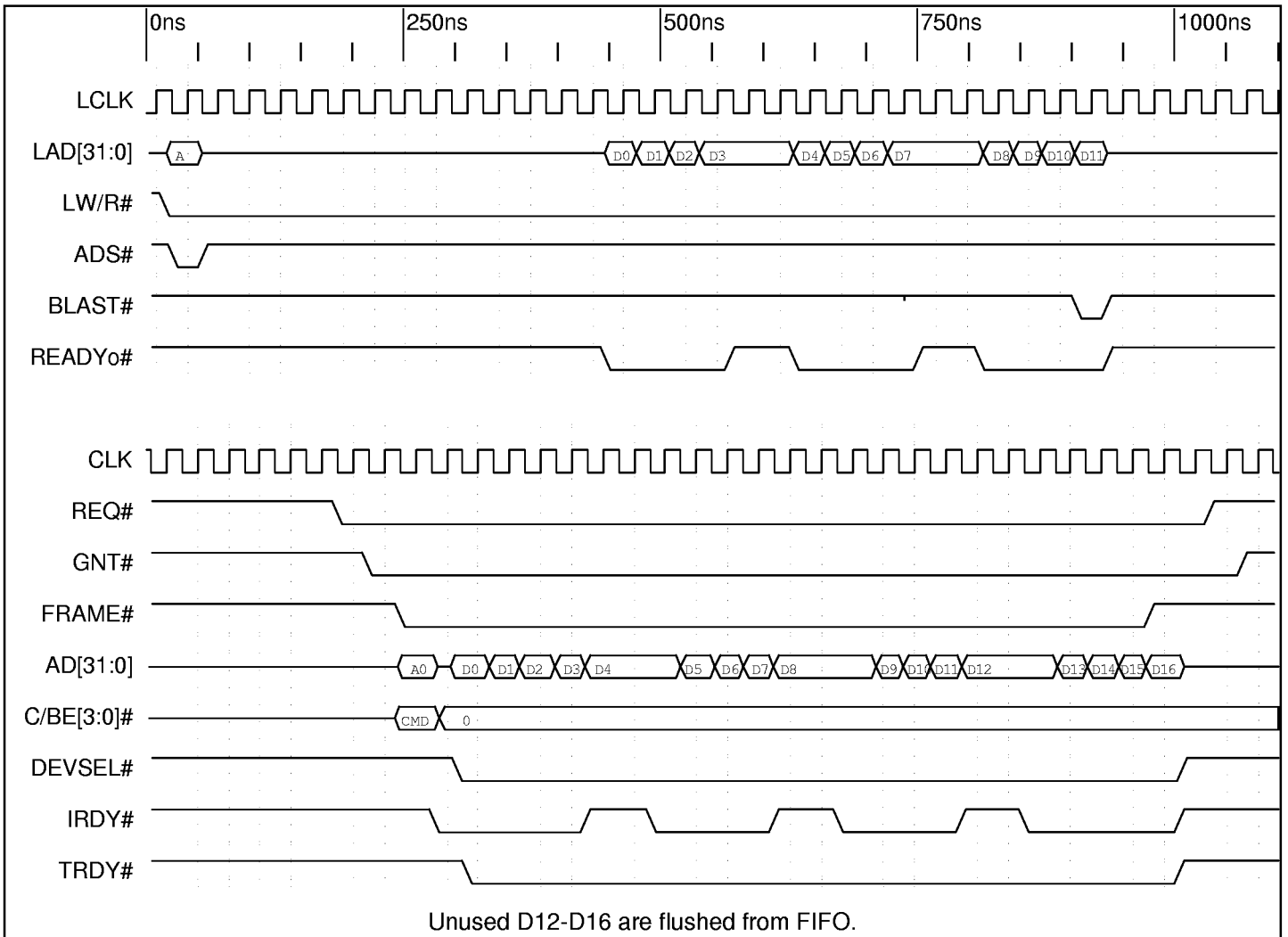


Timing Diagram 8-70. (J Mode) Local Bus Read from PCI 9080 CFG Registers

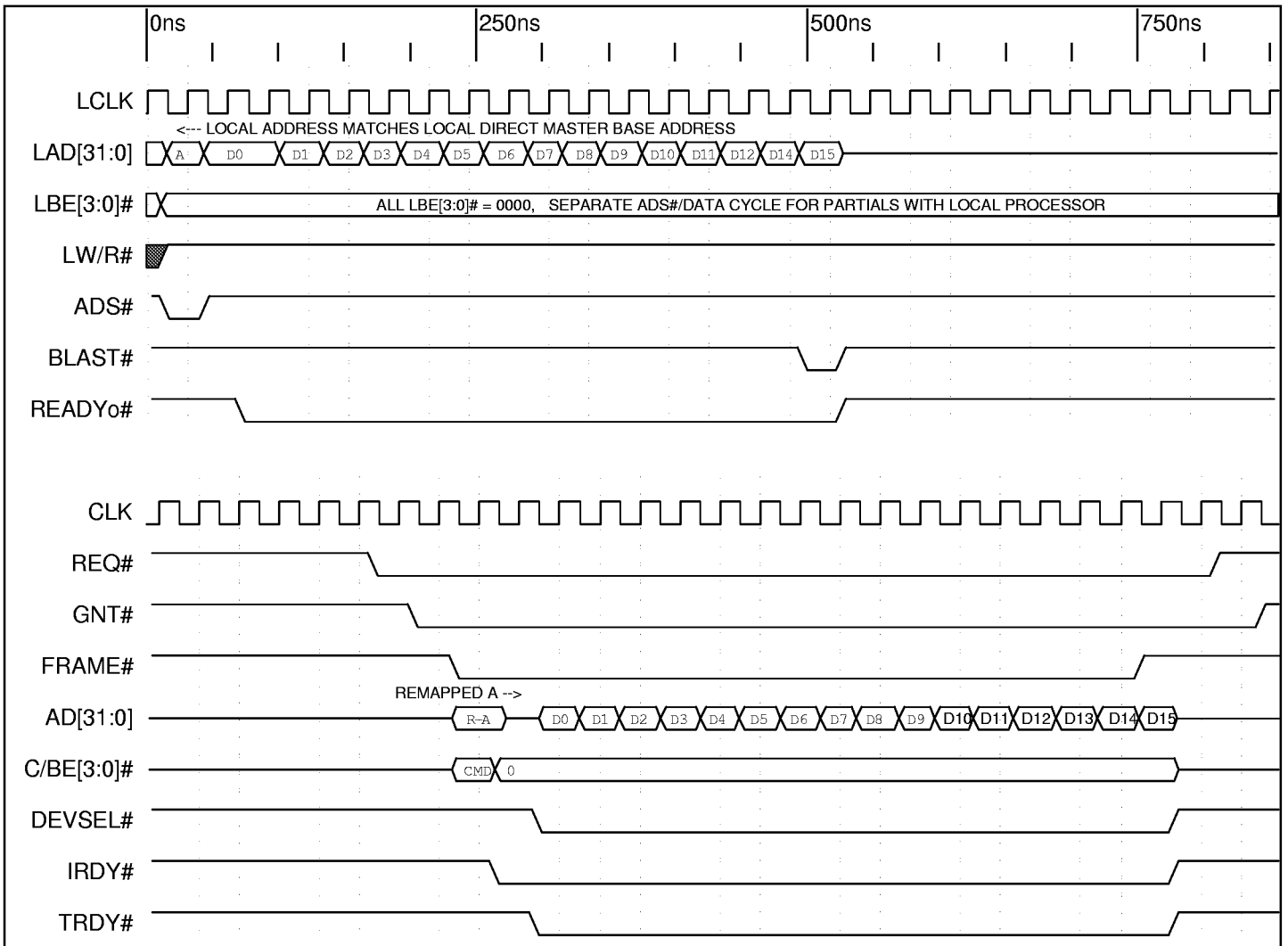


Timing Diagram 8-71. (J Mode) Local Bus Write to PCI 9080 CFG Registers

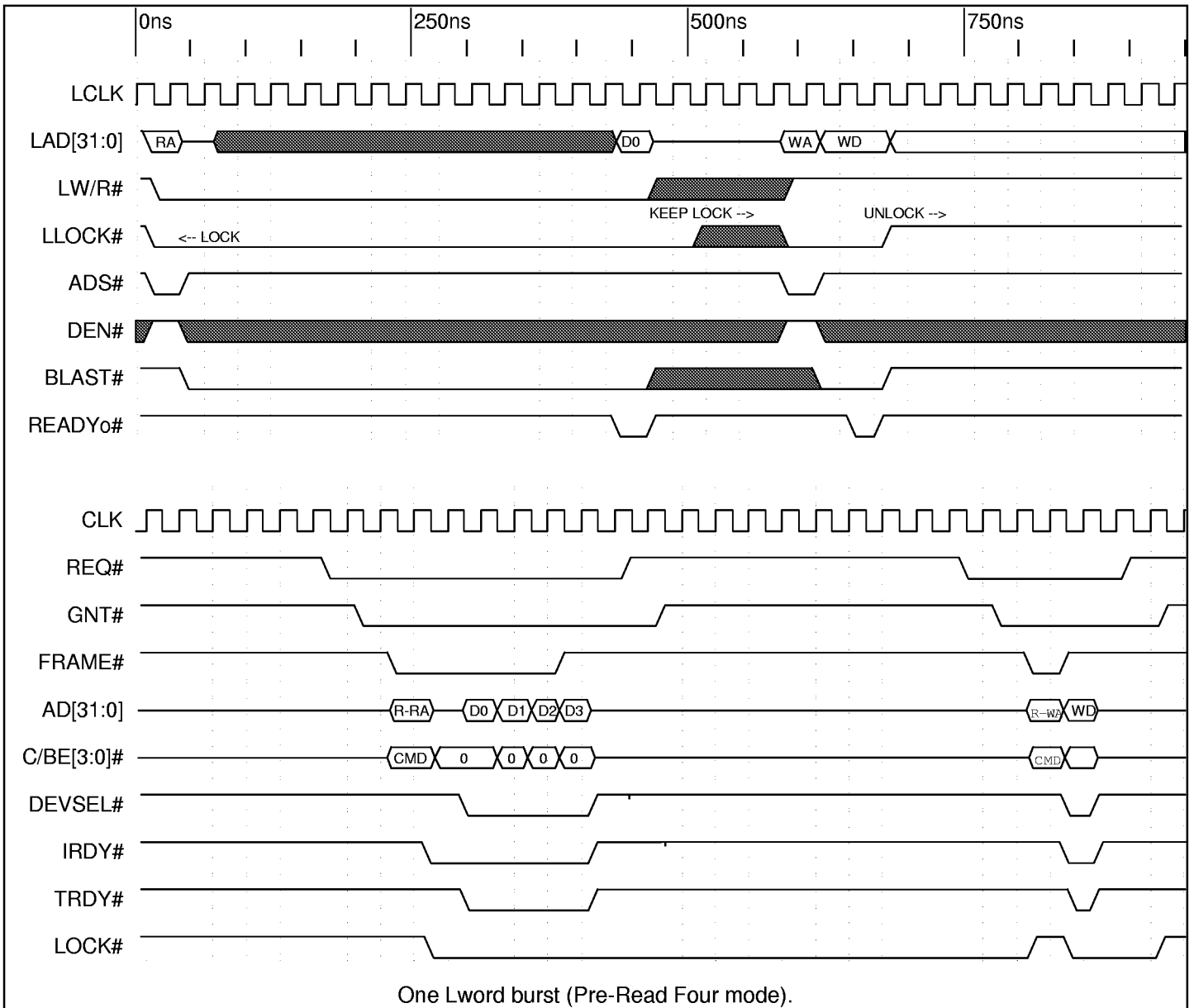
8.4.2 J Mode Direct Master



Timing Diagram 8-72. (J Mode) Direct Master Read Access from PCI Bus (Keep PCI Bus If Read FIFO Full Mode), No PCI Disconnects

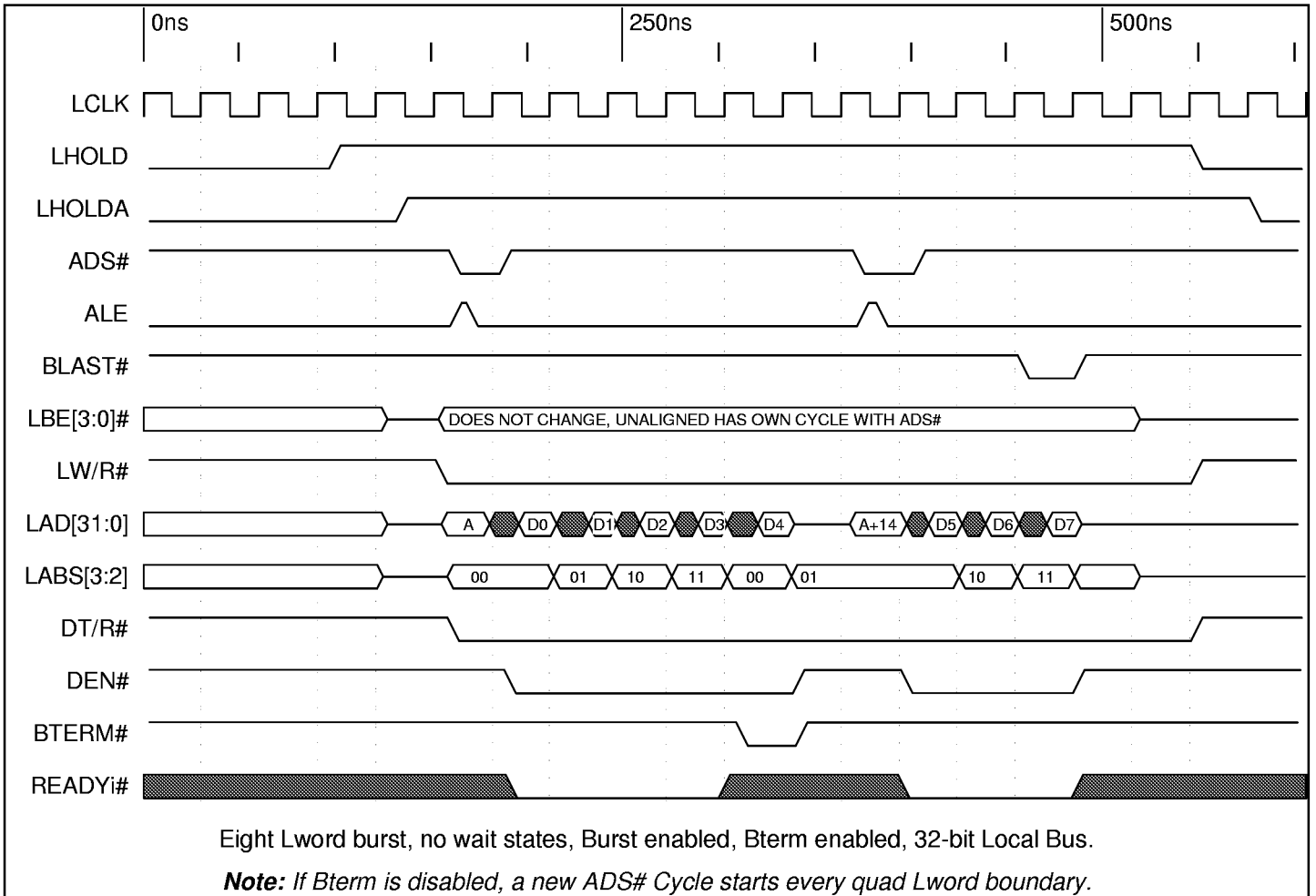


Timing Diagram 8-73. (J Mode) Local Bus Direct Master Burst Write Access to PCI Bus, Continuous If Same Clock Rate and No PCI Disconnects

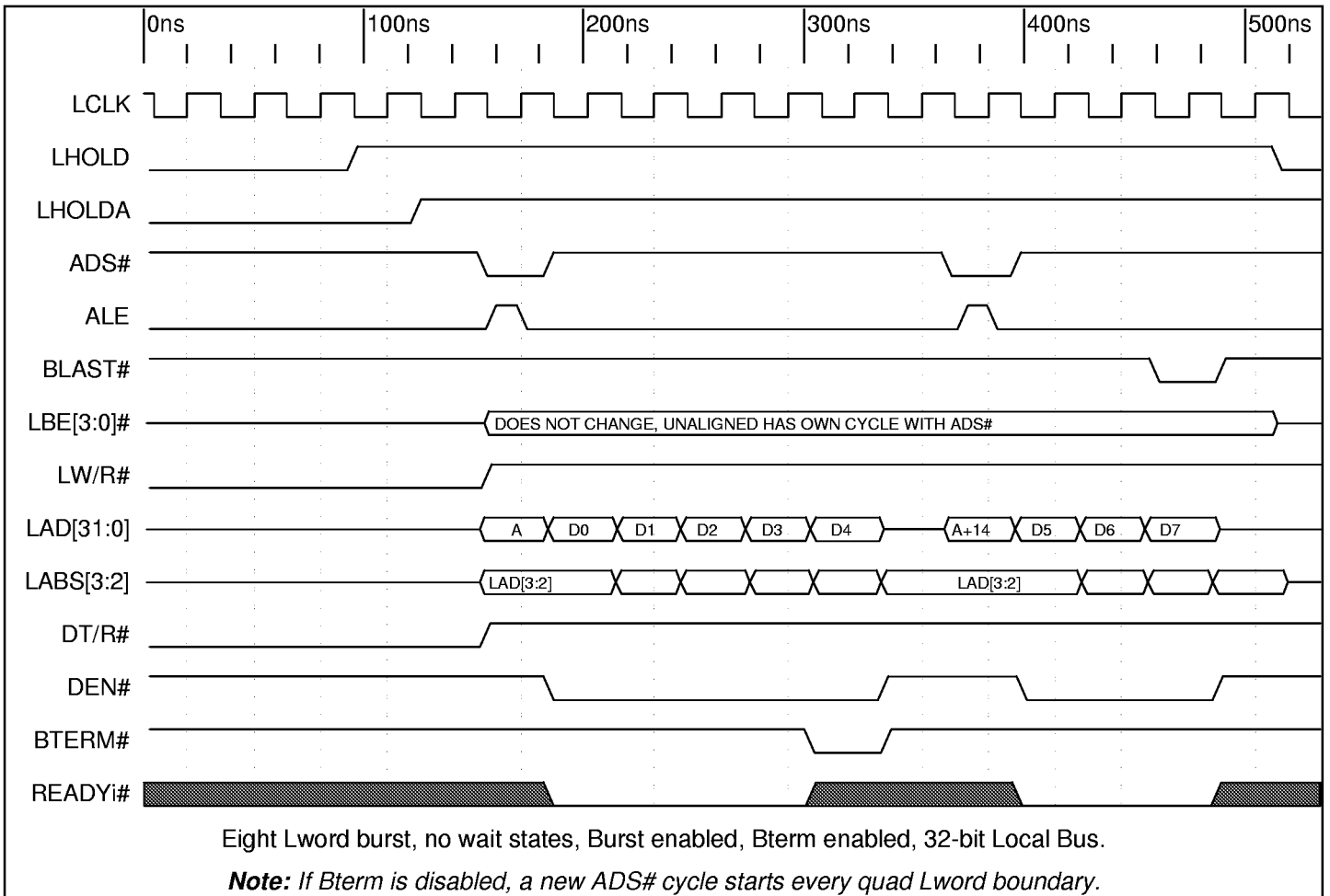


Timing Diagram 8-74. (J Mode) Local Bus Direct Master Lock Memory Read Access from PCI Bus Followed by Write and Release

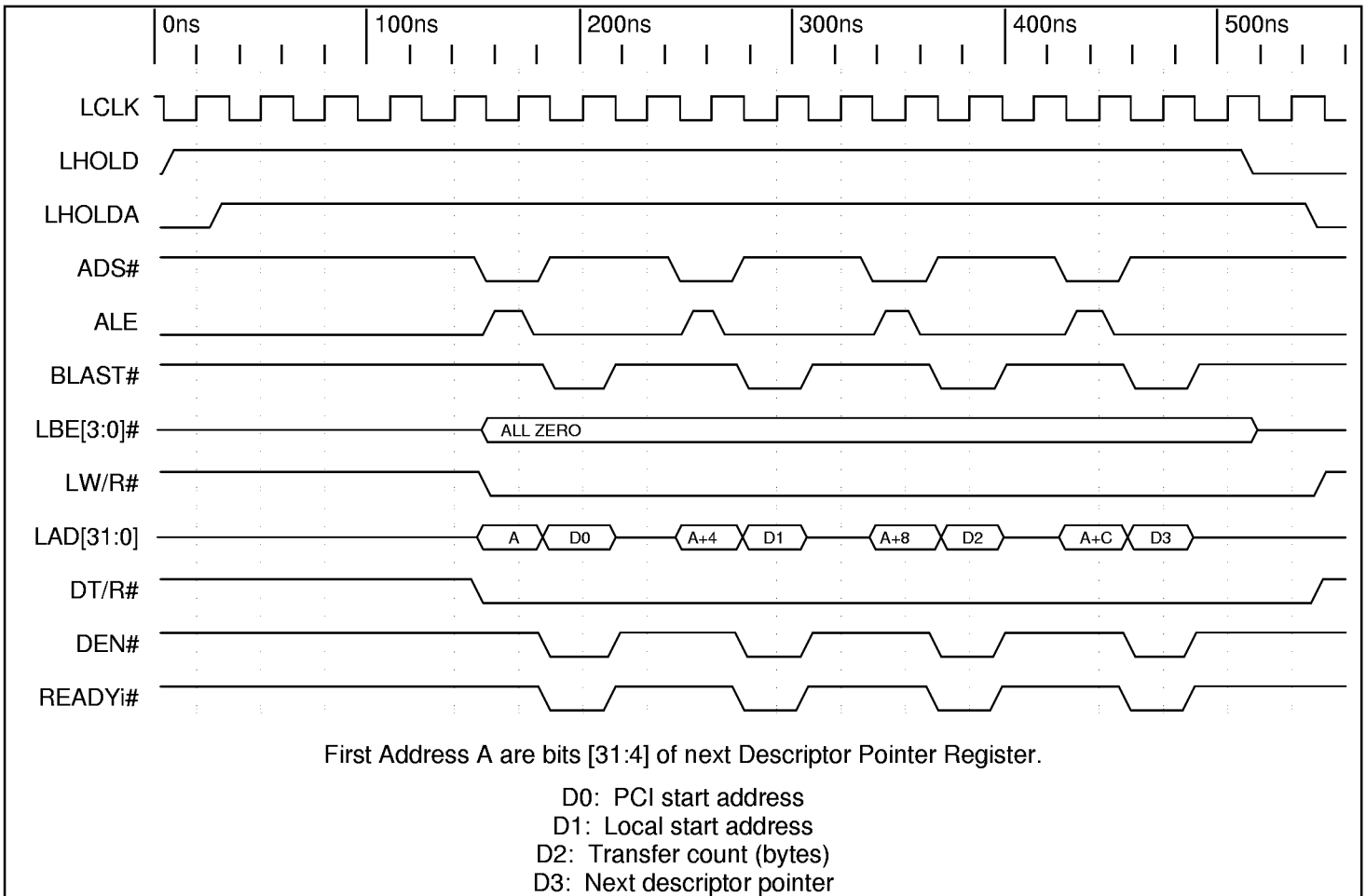
8.4.3 J Mode DMA



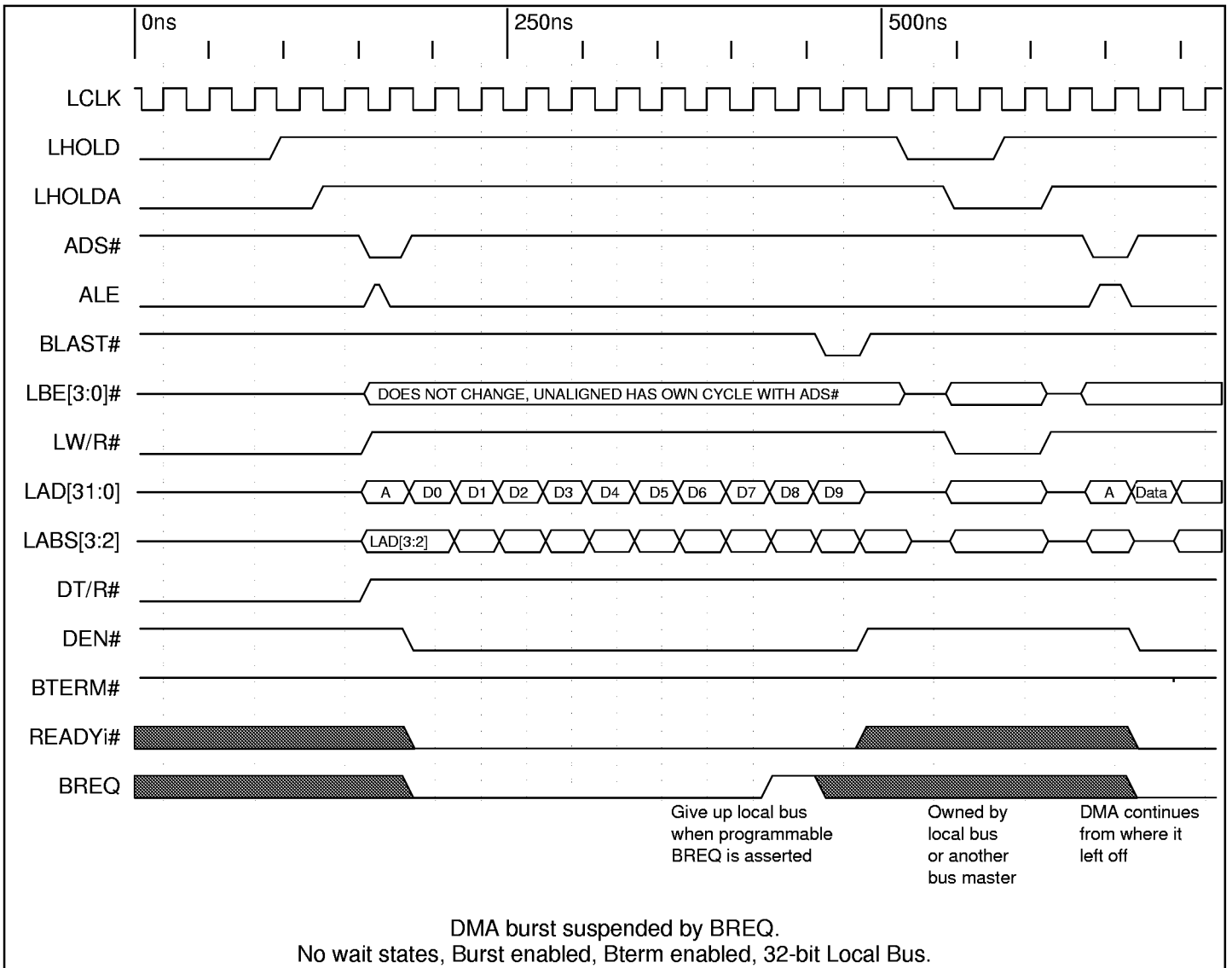
Timing Diagram 8-75. (J Mode) PCI 9080 DMA Local-to-PCI, No Wait States, Bterm Enabled



Timing Diagram 8-76. (J Mode) PCI 9080 DMA PCI-to-Local Bus, No Wait States, Bterm Enabled

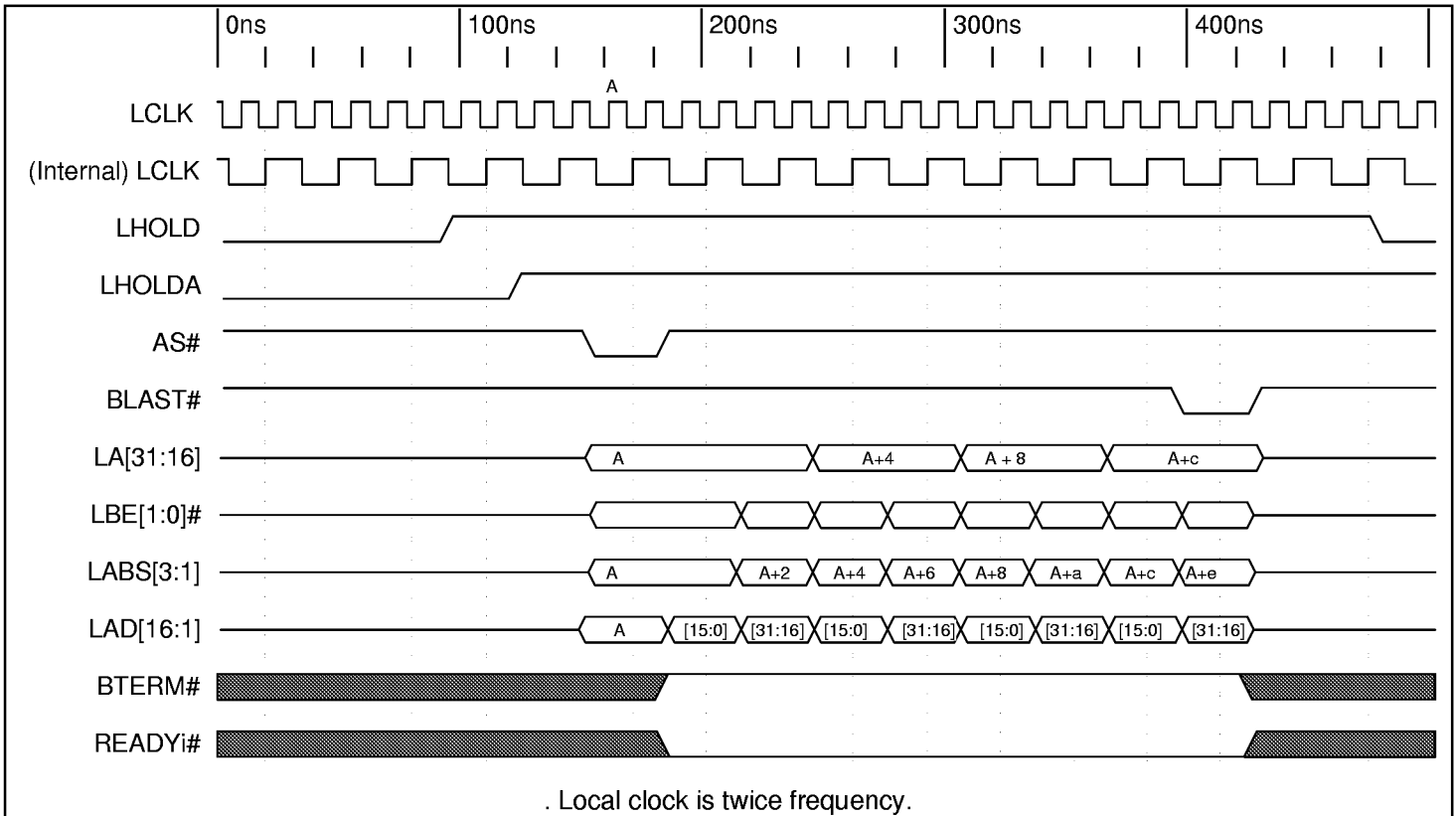


Timing Diagram 8-77. (J Mode) DMA Read of Chaining Parameters, No Wait States

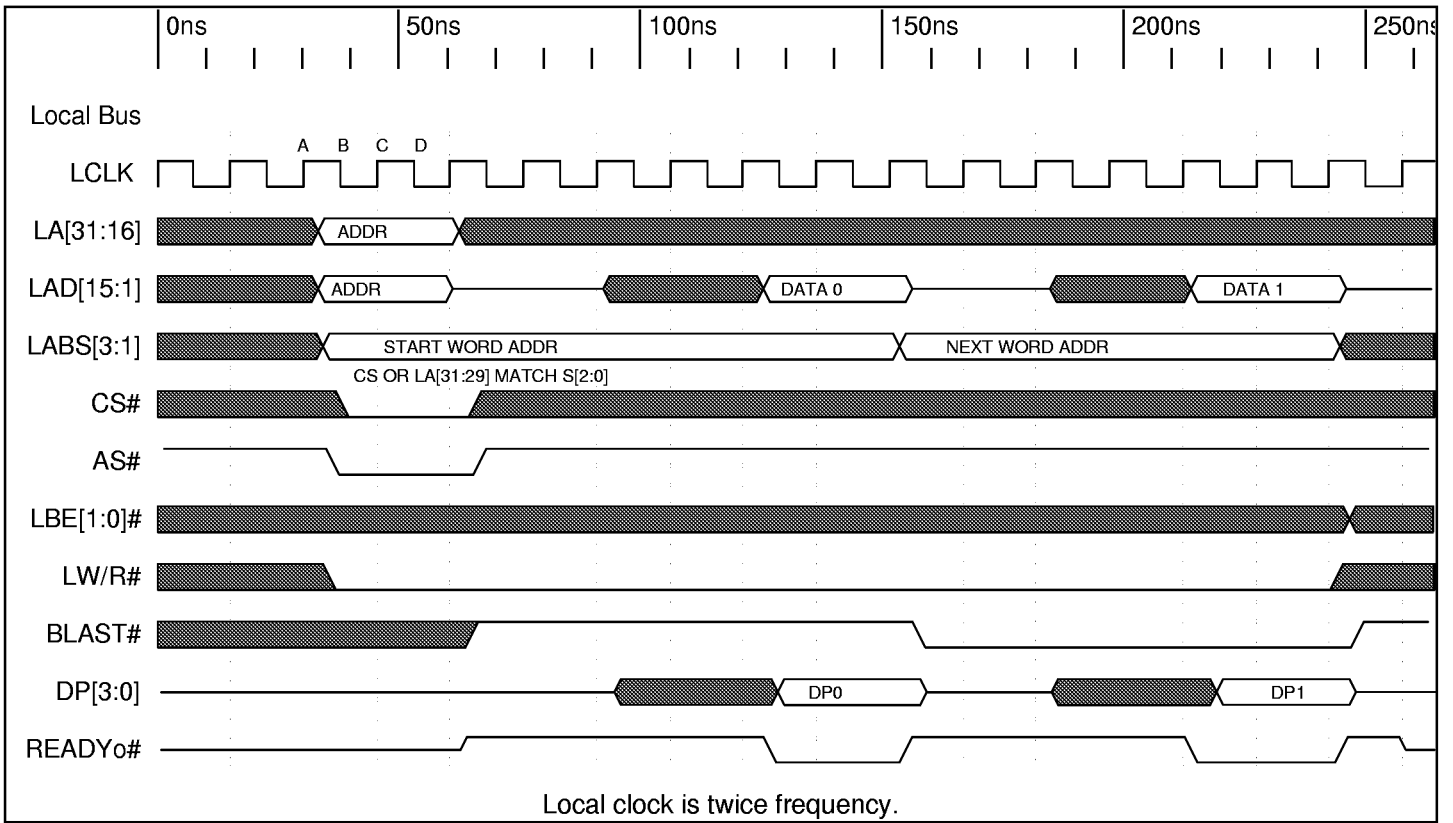


Timing Diagram 8-78. (J Mode) PCI 9080 Write to Local Bus BREQ Asserted

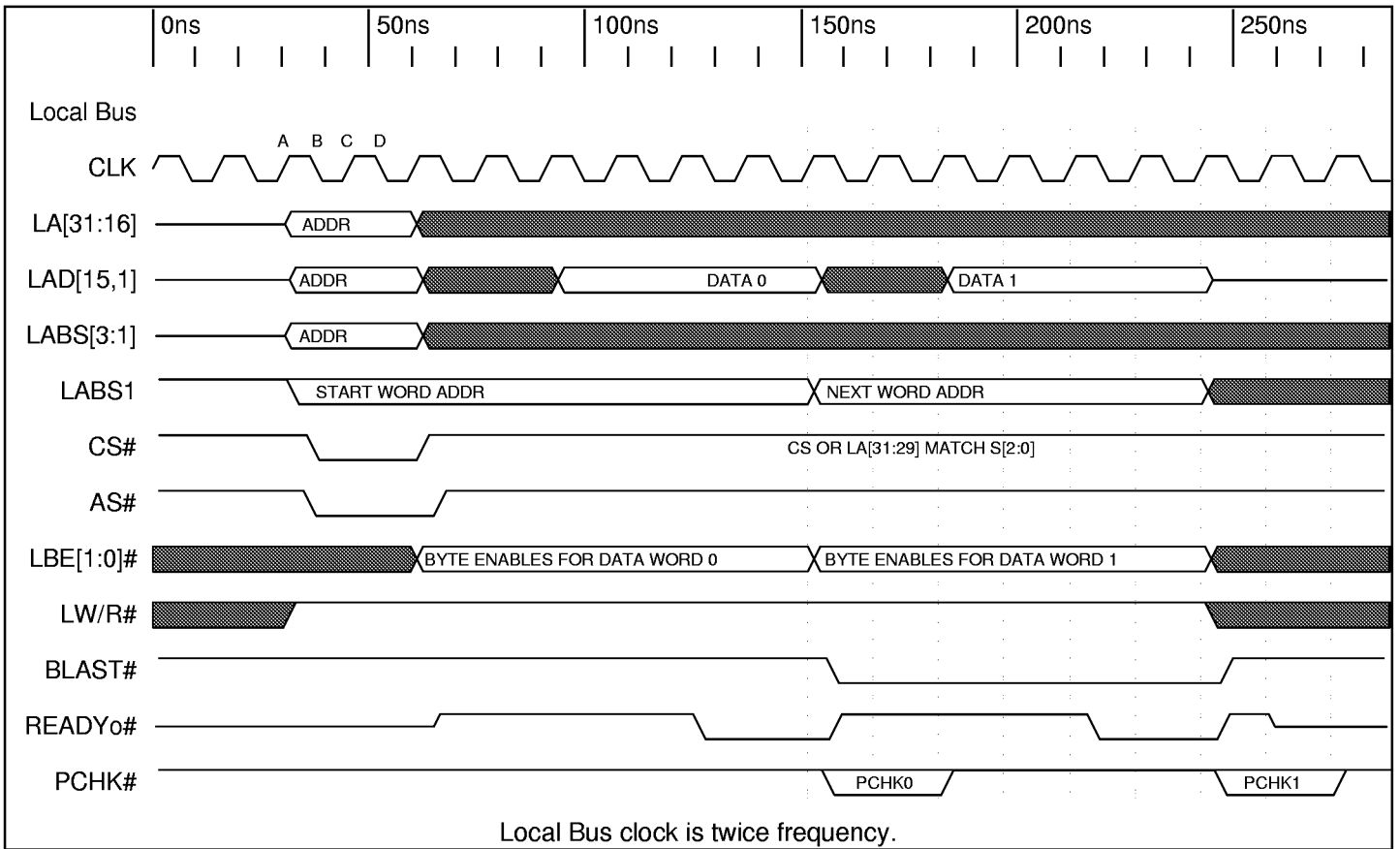
8.5 S MODE



Timing Diagram 8-79. (S Mode) PCI 9080 DMA or Direct Slave Two Lword Burst Write to 16-Bit Local Bus, No Wait States, Bterm Enabled

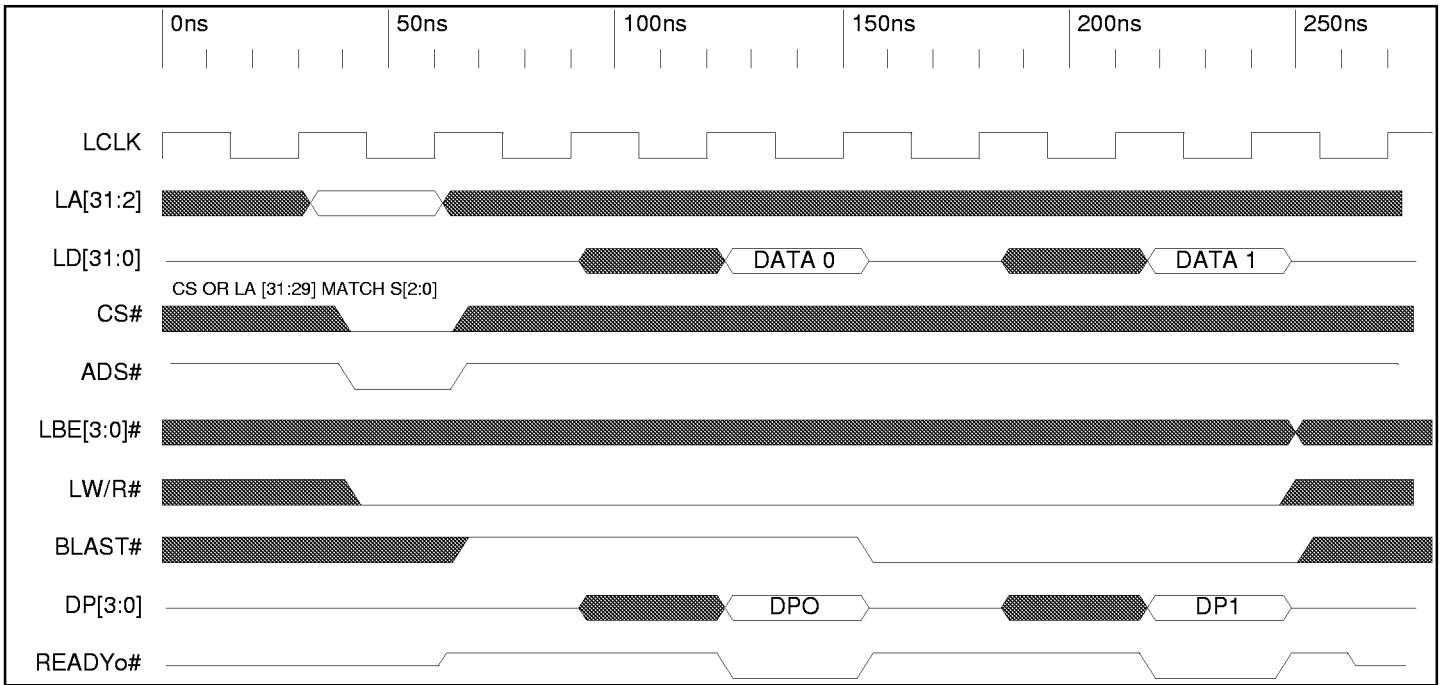


Timing Diagram 8-80. (S Mode) Local Bus Read from PCI 9080 CFG Registers

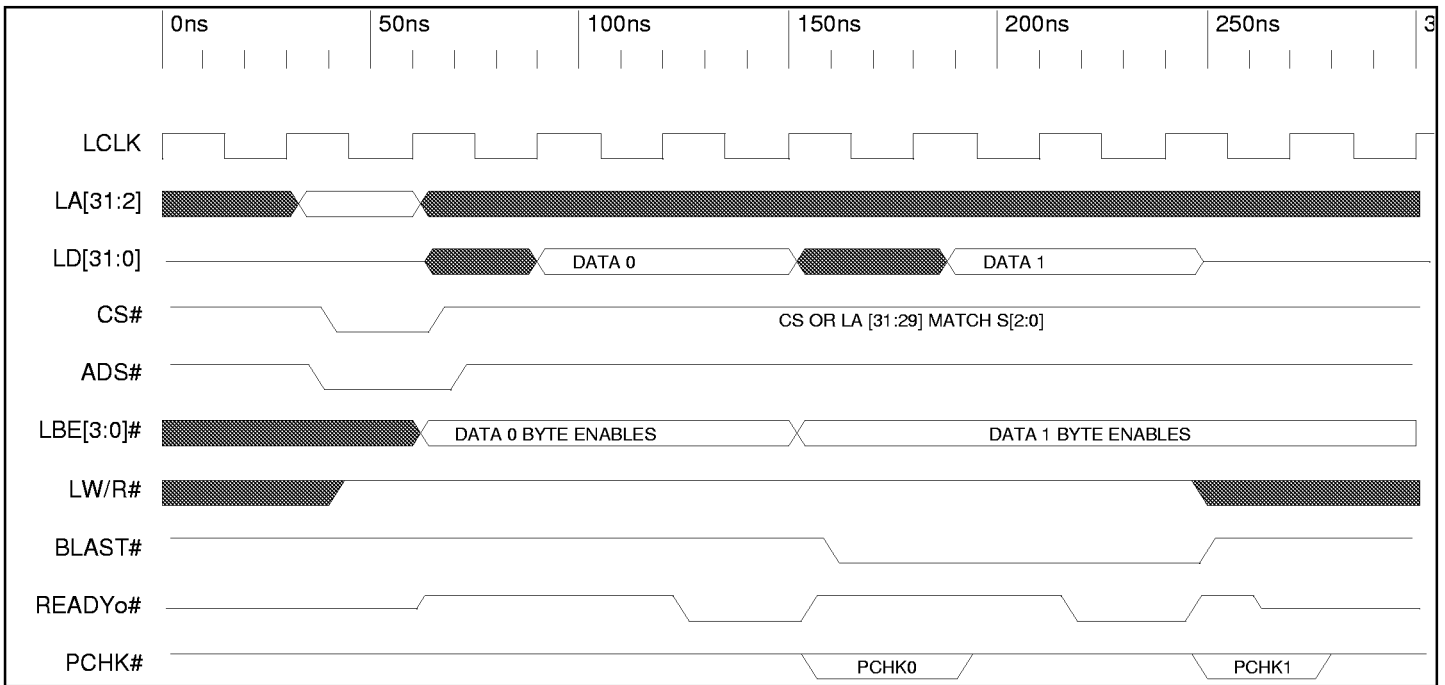


Timing Diagram 8-81. (S Mode) Local Bus Write to PCI 9080 CFG Registers

Editor's Note: I don't know where these go. There's one named like this for each mode. Phil, please resolve before we finalize this document.



Timing Diagram 8-82. PCI 9080 Local Bus Read



Timing Diagram 8-83. PCI 9080 Local Bus Write