CMOS 4-BIT MICROCONTROLLER

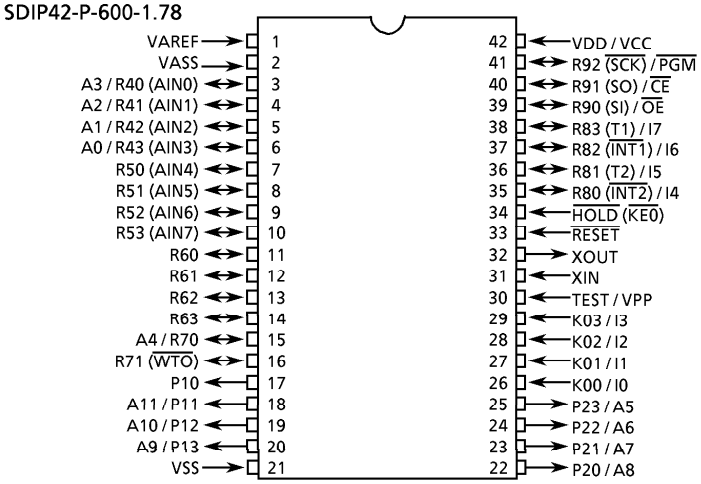
TMP47P440VN
TMP47P440VF

The 47P440V is the system evaluation LSI of 47C440B with 32K bits one-time PROM. The 47P440V programs / verifies using an adapter socket to connect with PROM programmer, as it is in TMM2764AD.
In addition, the 47P440V and the 47C440B are pin compatible. The 47P440V operates as the same as the 47C440B by programming to the internal PROM.

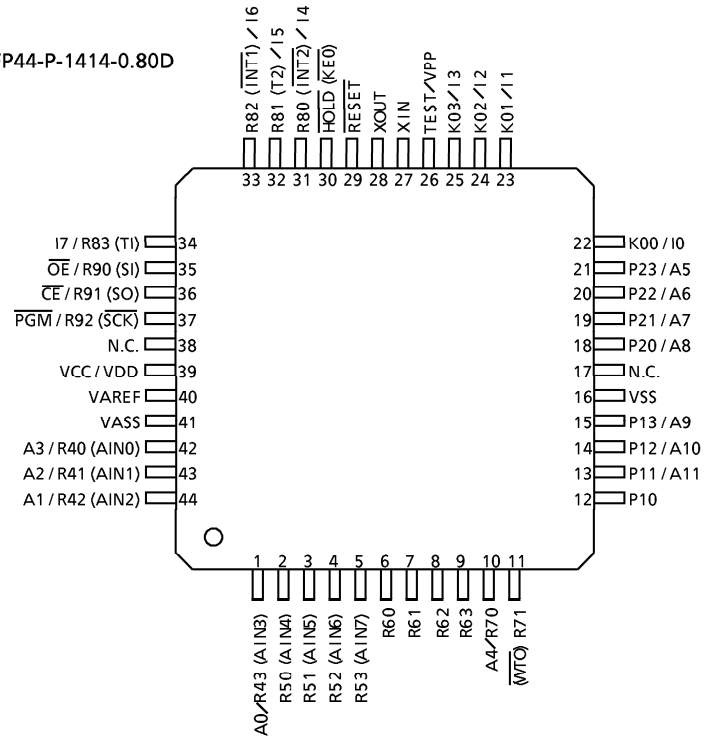
PART No.	ROM	RAM	PACKAGE	ADAPTOR SOCKET
TMP47P440VN	OTP 4096 × 8-bit	256 × 4-bit	SDIP42-P-600-1.78	BM1118
TMP47P440VF			QFP44-P-1414-0.80D	BM1125

PIN ASSIGNMENT (TOPVIEW)

SDIP42-P-600-1.78



QFP44-P-1414-0.80D



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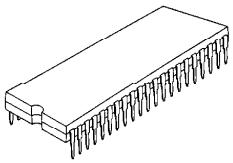
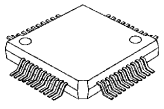


TMP47P440VN

QFP44-P-1414-0.80D



TMP47P440VF

PIN FUNCTION

The 47P440V has MCU mode and PROM mode.

(1) MCU mode

The 47C440B and the 47P440V are pin compatible (TEST pin for out-going test. Be fixed to low level.).

(2) PROM mode

PIN NAME	INPUT / OUTPUT	FUNCTIONS	PIN NAME(MCU mode)
A11 - A9	INPUT	Address inputs	P11 - P13
A8 - A5			P20 - P23
A4			R70
A3 - A0			R40 - R43
I7 - I4	I/O	Data outputs (Inputs)	R83 - R80
I3 - I0			K03 - K00
$\overline{PGM}$	Input	Program control input	R92
$\overline{CE}$		Chip Enable input	R91
$\overline{OE}$		Output Enable input	R90
VPP	Power supply	+ 12.5V / 5V (Program supply voltage)	TEST
VCC		+ 5V	VDD
VSS		0V	VSS
P10	Output	Open	
R53 - R50	I/O	Be fixed to Low Level	
R63 - R60			
R71			
$\overline{RESET}$	Input	PROM mode setting pin. Be fixed to low level.	
$\overline{HOLD}$	Input		
XIN	Input	Resonator connecting pin	
XOUT	output		
VAREF	Power supply	Be fixed to low level	
VASS			

OPERATIONAL DESCRIPTION

The following is an explanation of hardware configuration and operation in relation to the 47P440V. The 47P440V is the same as the 47C440B except that an OTP is used instead of a built-in mask ROM.

1. OPERATION mode

The 47P440V has an MCU mode and a PROM mode.

1.1 MCU mode

The MCU mode is set by fixing the TEST/VPP pin at the "L" level. Operation in the MCU mode is the same as for the 47C440B, except that the TEST/VPP pin does not have built in pull-down resistor and cannot be used open.

1.1.1 Program Memory

The program storage area is the same as for the 47C440B.

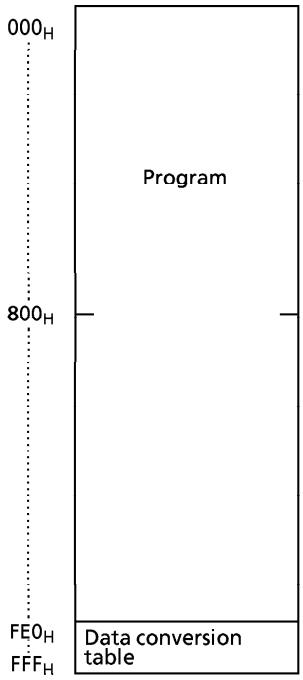


Figure 1-1. Program area

1.1.2 Data Memory

The 47P440V has 256 × 4-bit data memory (RAM).

1.1.3 Input/Output Circuitry

(1) Control pins
This is the same as for the 47C440B except that there is no built-in pull-down resistance for the TEST pin.

(2) I/O Ports
The input/output circuit of the 47P440V is the same as I/O code SA of the 47C440B.
External resistance, for example, is required when using as evaluator of other I/O codes (SB, SC), (Refer to Figure 1.2)

(a) Equivalent to IO code SB (b) Equivalent to IO code SC

Figure 1-2. I/O code and external circuitry

1.2 PROM mode

The PROM mode is set by setting the $\overline{\text{RESET}}$ and $\overline{\text{HOLD}}$ pins to the "L" level. The PROM mode can be used as a general-purpose PROM writer for program writing and verification. (A high-speed program mode is used set the ROM type the same as for the TMM 2764D and an end address of FFFH).

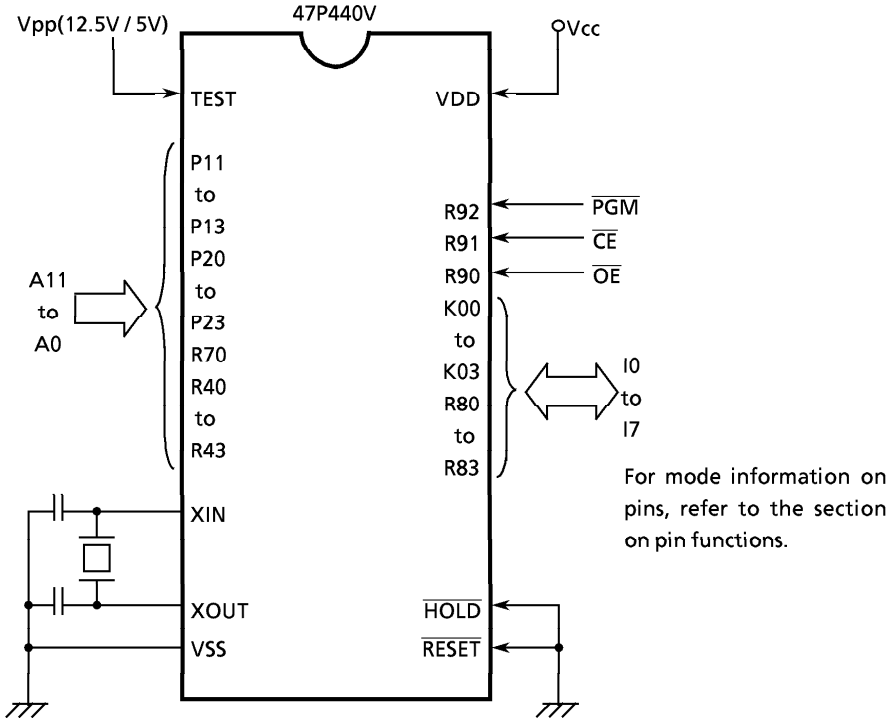


Figure 1-3. Setting for PROM mode

When writing a program, set a ROM type to "TMM2764AD" (programming voltage : 12.5V).
Since the 47P440V has 4096 × 8 bit internal PROM (000 to FFF_H), set a stop address of a PROM writer to "FFF_H", or store the same data of "FF_H" to the latter half addresses 1000 to $1FFF_H$.

1.2.1 High Speed Programming Mode

The device is set up in the high speed programming mode when the programming voltage (12.5V) is applied to the Vpp pin with Vcc = 6V and $\overline{PGM} = V_{IH4}$. The programming is achieved by applying a single TTL low level 1 msec, pulse the $\overline{PGM}$ input after addresses and data are stable. Then the programmed data is verified by using Program Verify mode. If the programmed data is not correct, another program pulse of 1 msec is applied and then programmed data is verified. This should be repeated until the program operates correctly (max. 25 times) After correclly programming the selected address, one additional program pulse with pulse width 3 times that needed for programming is applied. When programming has been completed, the data in all addresses should be verified with Vcc = Vpp = 5V.

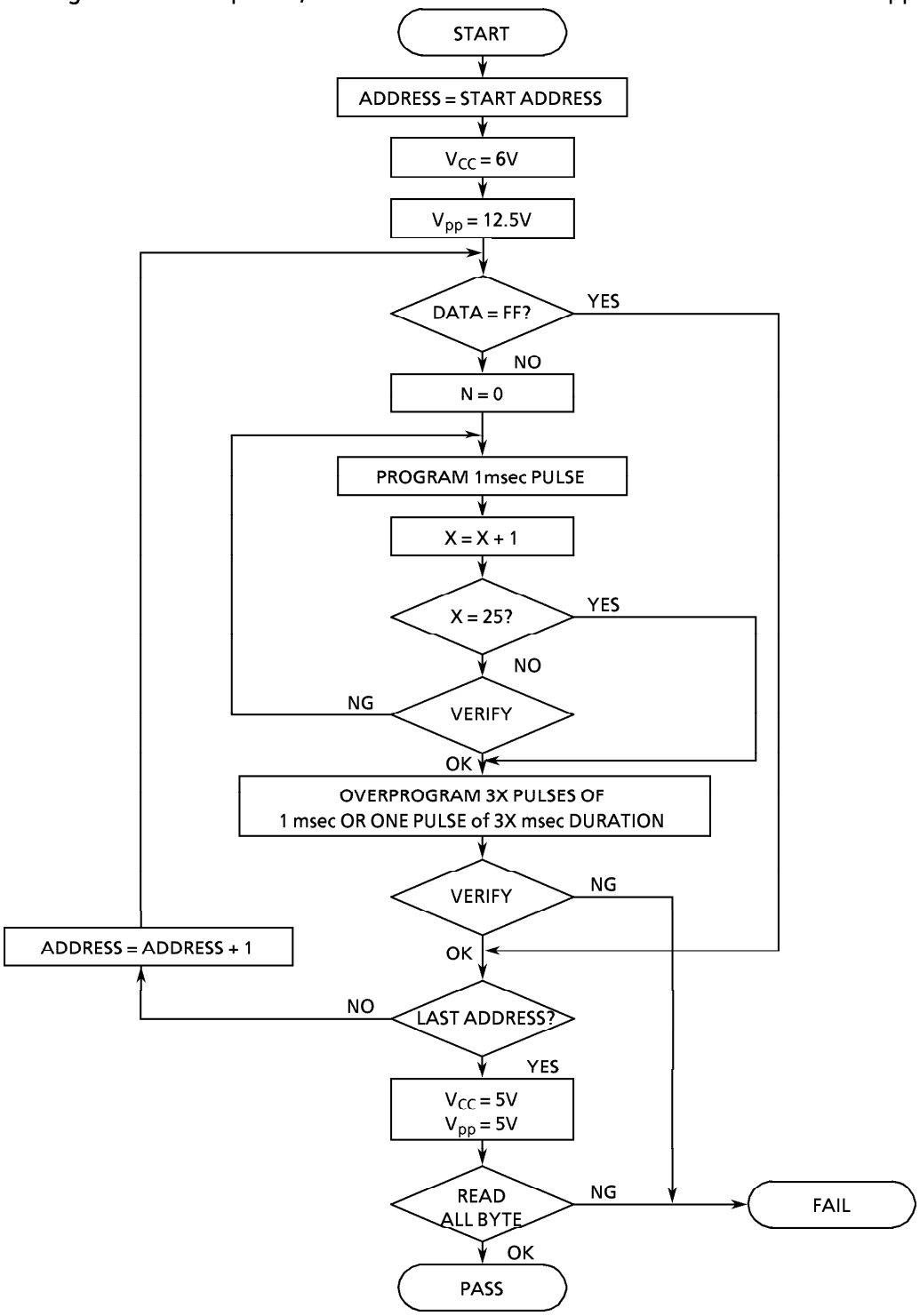


Figure1-4. FLOW CHART

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

PARAMETER	SYMBOL	PINS	RATING	UNIT
Supply Voltage	V_{DD}		– 0.3 to 6.5	V
Supply Voltage	V_{PP}	TEST/VPP pin	– 0.3 to 13.0	V
Input Voltage	V_{IN}		– 0.3 to V_{DD} + 0.3	V
Output Voltage	V_{OUT}	Ports R	– 0.3 to V_{DD} + 0.3	V
Output Current (Per 1pin)	I_{OUT1}	Ports R	3.2	mA
	I_{OUT2}	Ports P1, P2	30	
Output Current (Total)	ΣI_{OUT1}	Ports P1, P2	120	mA
Power Dissipation [T_{opr} = 70°C]	PD		600	mW
Soldering Temperture (time)	T_{sld}		260 (10 s)	℃
Strorage Temperture	T_{stg}		– 55 to 125	℃
Operating Temperature	T_{opr}		– 30 to 70	℃

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Max.	UNIT
Supply Voltage	V_{DD}		fc = 6.0 MHz	4.5	5.5	V
			fc = 4.2 MHz	2.7		
			In the HOLD mode	2.0		
Input High Voltage	V_{IH1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	$V_{DD} \times 0.7$	V_{DD}	V
	V_{IH2}	Hysteresis Input		$V_{DD} \times 0.75$		
	V_{IH3}		$V_{DD} < 4.5$ V	$V_{DD} \times 0.9$		
Input Low Voltage	V_{IL1}	Except Hysteresis Input	$V_{DD} \geqq 4.5$ V	0	$V_{DD} \times 0.3$	V
	V_{IL2}	Hysteresis Input			$V_{DD} \times 0.25$	
	V_{IL3}		$V_{DD} < 4.5$ V		$V_{DD} \times 0.1$	
Clock Frequency	fc		High-frequency	0.4	6.0	MHz

Note. Input voltage V_{IH3}, V_{IL3} : in the HOLD mode

D.C. CHARACTERISTICS

(V_{SS} = 0V, T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	PINS	CONDITIONS	Min.	Typ.	Max.	UNIT
Hysteresis Voltage	V_{HS}	Hysteresis Input		–	0.7	–	V
Input Current	I_{IN1}	Port K0, TEST, $\overline{RESET}$, $\overline{HOLD}$	V_{DD} = 5.5V, V_{IN} = 5.5V / 0V	–	–	± 2	μA
	I_{IN2}	Ports R (open drain)					
Low Input Current	I_{IL}	Ports R (push-pull)	V_{DD} = 5.5V, V_{IN} = 0.4V	–	–	-2	mA
Input Resistance	R_{IN2}	$\overline{RESET}$		100	220	450	kΩ
Output Leakage Current	I_{LO}	Ports R (open drain)	V_{DD} = 5.5V, V_{OUT} = 5.5V	–	–	2	μA
Output Low Voltage	V_{OL2}	Except XOUT, ports P	V_{DD} = 4.5V, I_{OL} = 1.6mA	–	–	0.4	V
Low output Current	I_{OL1}	Ports P1, P2	V_{DD} = 4.5V, V_{OL} = 1.0V	–	20	–	mA
Supply Current (in the Normal mode)	I_{DD}		V_{DD} = 5.5V, fc = 4MHz	–	3	6	mA
Supply Current (in the HOLD mode)	I_{DDH}		V_{DD} = 5.5V	–	0.5	10	μA

Note 1. Typ. values show those at T_{opr} = 25°C, V_{DD} = 5V.

Note 2. Input Current I_{IN1} ; The current through resistor is not included, when the input resistor (pull-up/pull-down) is contained.

Note 3. Supply Current I_{DD}, I_{DDH} ; V_{IN} = 5.3V/0.2V
The voltage applied to the R port is within the valid range.

A / D CONVERSION CHARACTERISTICS

(T_{opr} = – 30 to 70 °C)

PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Analog Reference Voltage	V_{AREF}		V_{DD} – 1.5	–	V_{DD}	V
	V_{ASS}		V_{SS}	–	1.5	
Analog Reference Voltage Range	ΔV_{AREF}	V_{AREF} – V_{ASS}	2.5	–	–	V
Analog Input Voltage	V_{AIN}		V_{ASS}	–	V_{AREF}	V
Analog Supply Current	I_{REF}		–	0.5	1.0	mA
Nonlinearity Error		V_{DD} = 5.0V, V_{SS} = 0.0V, V_{AREF} = 5.000V, V_{ASS} = 0.000V	–	–	± 1	LSB
Zero Point Error			–	–	± 1	
Full Scale Error			–	–	± 1	
Total Error			–	–	± 2	

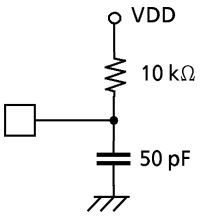
A. C. CHARACTERISTICS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 70 °C)

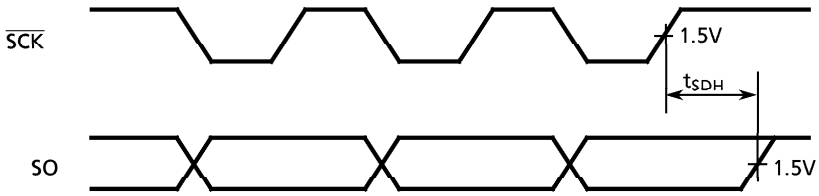
PARAMETER	SYMBOL	CONDITIONS	Min.	Typ.	Max.	UNIT
Instruction Cycle Time	t_{cy}		1.9	—	20	μs
High level Clock pulse Width	t_{WCH}	External clock mode	80	—	—	ns
Low level Clock pulse Width	t_{WCL}					
A/D Sampling Time	t_{AIN}	fc = 4 MHz	—	4	—	μs
Shift Data Hold Time	t_{SDH}		0.5 t_{cy} – 300	—	—	ns

Note. Shift Data Hold Time

External circuit for $\overline{SCK}$ pin and SO pin



Serial port (completion of transmission)



RECOMMENDED OSCILLATING CONDITIONS

(V_{SS} = 0V, V_{DD} = 4.5 to 5.5V, T_{opr} = – 30 to 70 ℃)

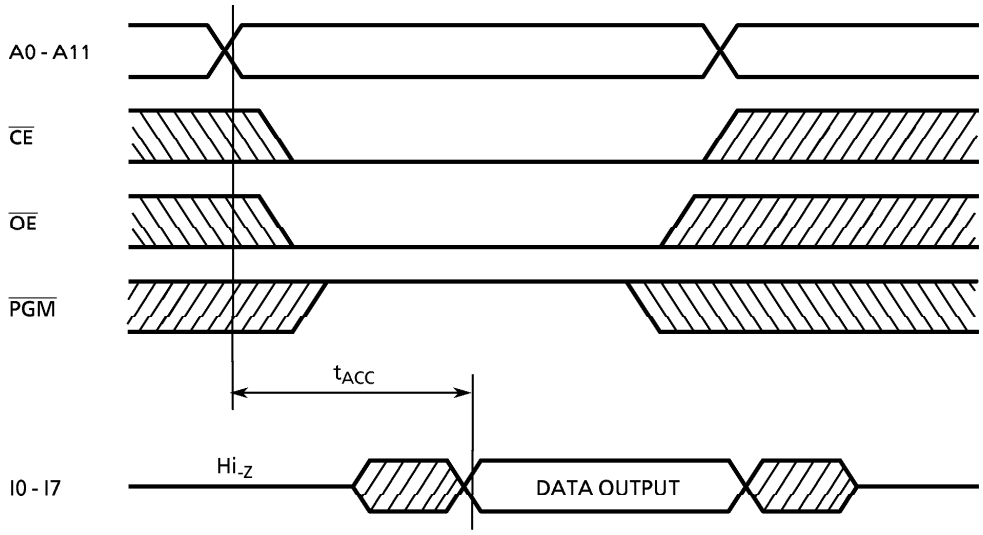
Recommended oscillating conditions of the 47P440V are equal to the 47C440B's.

DC/AC CHARACTERISTICS

(V_{SS} = 0V)

(1) Read Operation

PARAMETER	SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT
Output Level High Voltage	V_{IH4}		V_{CC} × 0.8	–	V_{CC}	V
Output Level Low Voltage	V_{IL4}		0	–	V_{CC} × 0.1	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
Programming Voltage	V_{PP}					
Address Access Time	t_{ACC}	V_{CC} = 5.0 ± 0.25V	–	–	350	ns



(2) High Speed Programming Operation

PARAMETER	SYBOL	CONDITION	Min.	Typ.	Max.	UNIT
Input High Voltage	V_{IH4}		$V_{CC} \times 0.8$	–	V_{CC}	V
Input Low Voltage	V_{IL4}		0	–	$V_{CC} \times 0.1$	V
Supply Voltage	V_{CC}		4.75	–	6.0	V
V_{PP} Power Supply Voltage	V_{PP}		12.0	12.5	13.0	V
Programming Pulse Width	t_{PW}	$V_{CC} = 6.0 \pm 0.25V$	0.95	1.0	1.05	ms