



# LB1894M

## 3-Phase Brushless Motor Driver for CD-ROM Spindle Motors

### Overview

The LB1894M is a 3-phase brushless motor driver for use in CD-ROM spindle motors.

### Function and Features

- 3-phase bipolar brushless motor driver.
- Voltage linear drive, enabling the external capacitance to be reduced.
- Thermal shutdown circuit built-in.
- Overcurrent protection circuit built-in.
- V-type control amplifier built-in.
- 2-step switching control gain.
- Control gain switchable using operational amplifier.

### Specifications

#### Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC1 \text{ max}}$		20	V
	$V_{CC2 \text{ max}}$		7.0	V
Output supply current	$V_{OU, V, W}$		22	V
Output current	$I_{OUT}$		1.5	A
Allowable power dissipation	$P_d \text{ max}$		1.05	W
Operating temperature	$T_{opr}$		-20 to +75	$^\circ\text{C}$
Storage temperature	$T_{stg}$		-55 to +150	$^\circ\text{C}$

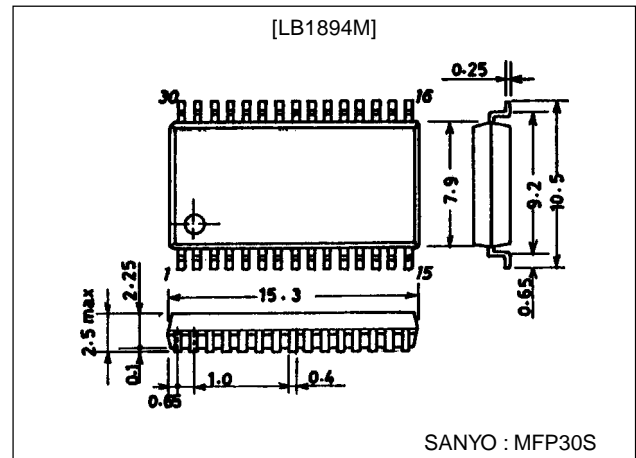
#### Allowable Operating Ranges at $T_a = 25^\circ\text{C}$

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC1}$		5 to 18	V
	$V_{CC2}$		4.3 to 6.5	V

### Package Dimensions

unit:mm

#### 3073A-MFP30S



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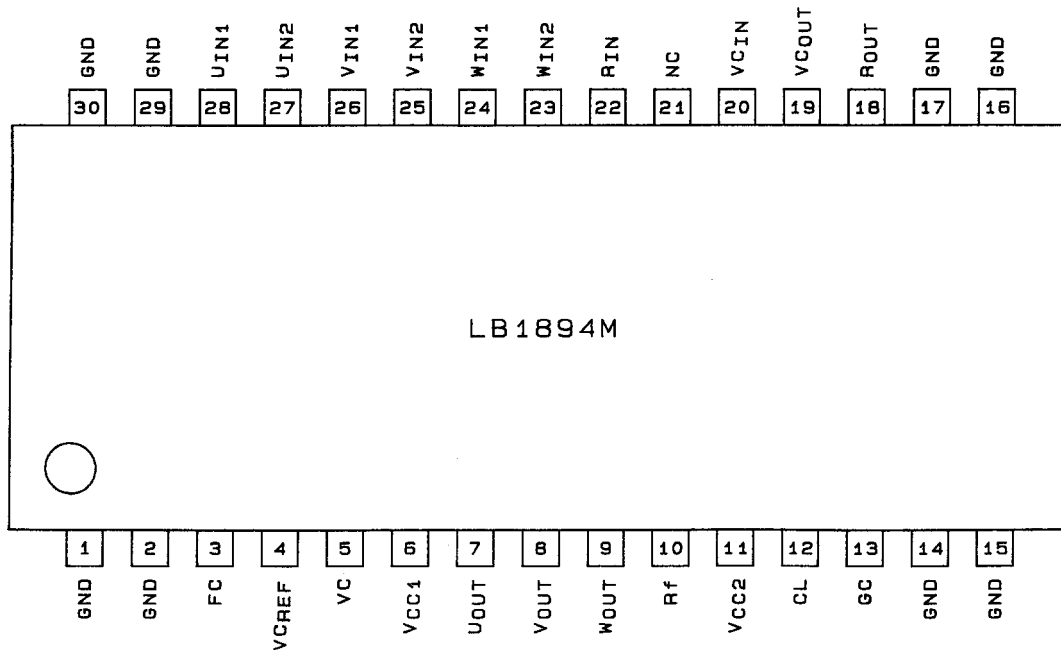
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## Electrical Characteristics at Ta = 25°C, VCC1=12V, VCC2=5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I <sub>CC 1</sub>	VC=V <sub>CCREF</sub> , R <sub>L</sub> =∞		17	30	mA
	I <sub>CC 2</sub>	VC=V <sub>CCREF</sub>		6.5	9.5	mA
[Driver stage]						
Output saturation voltage	V <sub>O(sat)1</sub>	I <sub>OUT</sub> =0.5A, sink+source		1.6	2.2	V
	V <sub>O(sat)2</sub>	I <sub>OUT</sub> =1.0A, sink+source		2.0	3.0	V
Output transistor blocking voltage	V <sub>O(sus)</sub>	I <sub>OUT</sub> =20mA, design value	20			V
Output rest voltage	V <sub>OQ</sub>	VC=V <sub>CCREF</sub>	5.7	6.0	6.3	V
Hall amplifier input offset voltage	V <sub>H offset</sub>		-5		+5	mV
Hall amplifier input bias current	I <sub>H bias</sub>			1	5	μA
Hall amplifier common-mode input voltage range	V <sub>Hch</sub>		1.3		2.2	V
Hall amplifier input-output voltage gain	G <sub>VHO</sub>		42	45	48	dB
[Control stage]						
Control-output drive gain	G <sub>VCO1</sub>	High gain, GC=high	32	35	38	dB
	G <sub>VCO2</sub>	Low gain, GC=low	26	29	32	dB
Control-output channel difference	ΔG <sub>VCO</sub>		-2		+2	dB
Control rising threshold voltage	V <sub>CTH</sub>	V <sub>CCREF</sub> =2.5V, V <sub>OUT</sub> =0.1Vp-p	2.35		2.65	V
Control rising threshold voltage width	ΔV <sub>CTH</sub>	V <sub>CCREF</sub> =2.5V, V <sub>OUT</sub> =0.1Vp-p	50		150	mV
Gain control switching high-level voltage	V <sub>GC</sub>		4		5	V
Gain control switching low-level voltage	V <sub>GCL</sub>	Inputs are low level when left open	0		+2	V
[Op-amplifiers]						
Op-amplifier input offset voltage	V <sub>FG offset</sub>		-8		+8	mV
Open-loop voltage gain	G <sub>VFG</sub>	f=1kHz		60		dB
Source output saturation voltage	V <sub>FG OU</sub>	I <sub>O</sub> =-2mA	3.7			V
Sink output saturation voltage	V <sub>FG OD</sub>	I <sub>O</sub> =2mA			1.3	V
Common-mode signal rejection	CHR	Design value		80		dB
Op-amplifier common-mode input voltage range	V <sub>FG CH</sub>	V <sub>CCREF</sub> =1.5V to V <sub>CC2</sub> , design value	0		+3.5	V
Phase margin	φ <sub>M</sub>	Design value		20		deg
[Thermal shutdown]						
Thermal shutdown operating temperature	TSD	Design value	150	180	210	°C
TSD hysteresis	ΔTSD	Design value		15		°C

## Pin Assignment



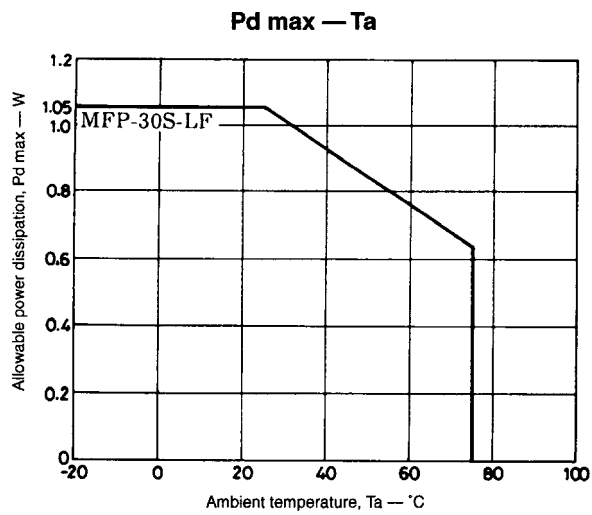
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(Top view)

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## Truth Table

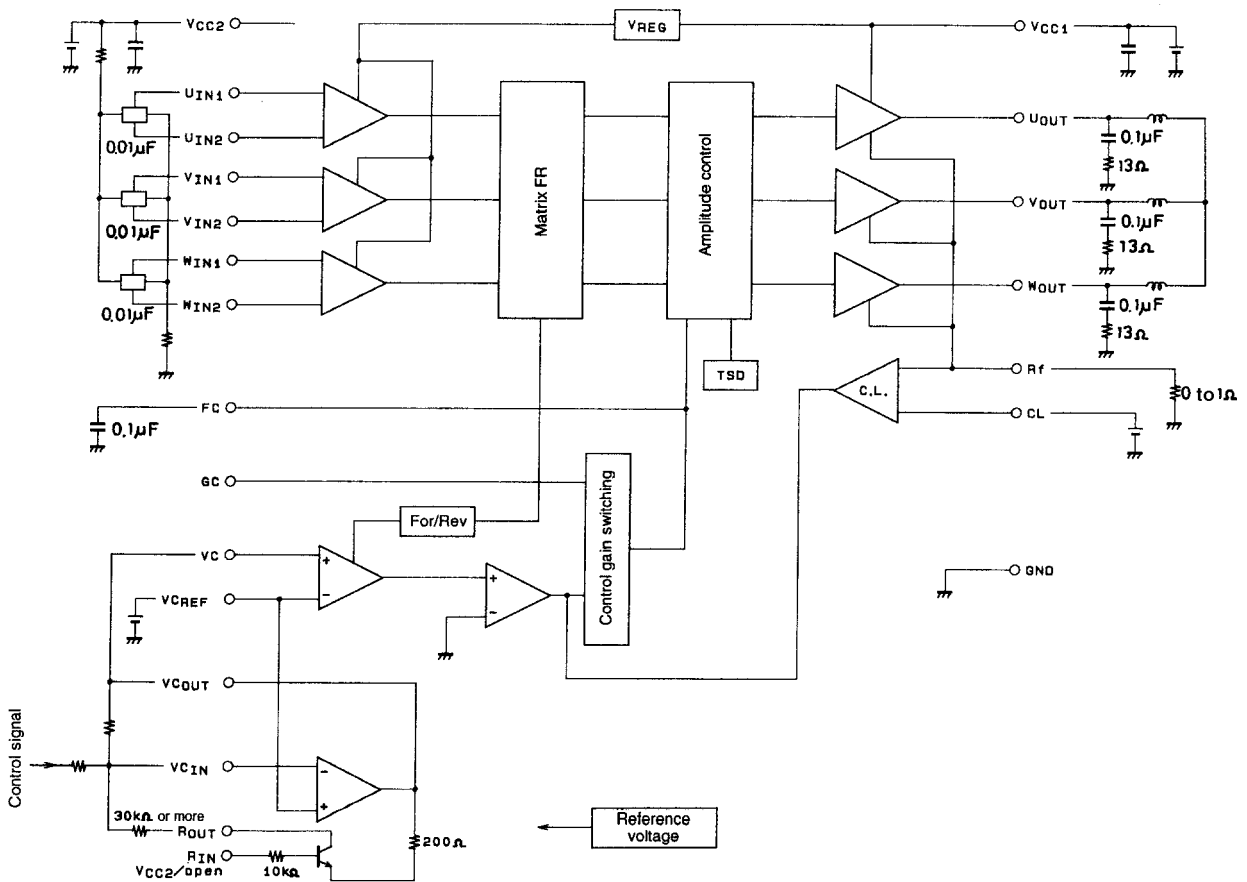
	Source→Sink	Hall Input			Control VC
		U <sub>IN</sub>	V <sub>IN</sub>	W <sub>IN</sub>	
1	W-phase → V-phase	HIGH	HIGH	LOW	HIGH
	V-phase → W-phase				LOW
2	W-phase → U-phase	HIGH	LOW	LOW	HIGH
	U-phase → W-phase				LOW
3	V-phase → W-phase	LOW	LOW	HIGH	HIGH
	W-phase → V-phase				LOW
4	U-phase → V-phase	LOW	HIGH	LOW	HIGH
	V-phase → U-phase				LOW
5	V-phase → U-phase	HIGH	LOW	HIGH	HIGH
	U-phase → V-phase				LOW
6	U-phase → W-phase	LOW	HIGH	HIGH	HIGH
	W-phase → U-phase				LOW

An input is considered to be HIGH when  $U_{IN1} > U_{IN2}$ ,  $V_{IN1} > V_{IN2}$ , and  $W_{IN1} > W_{IN2}$  by 0.2V more, and is considered to be LOW when  $U_{IN1} > U_{IN2}$ ,  $V_{IN1} > V_{IN2}$ , and  $W_{IN1} > W_{IN2}$  by 0.2V or less.



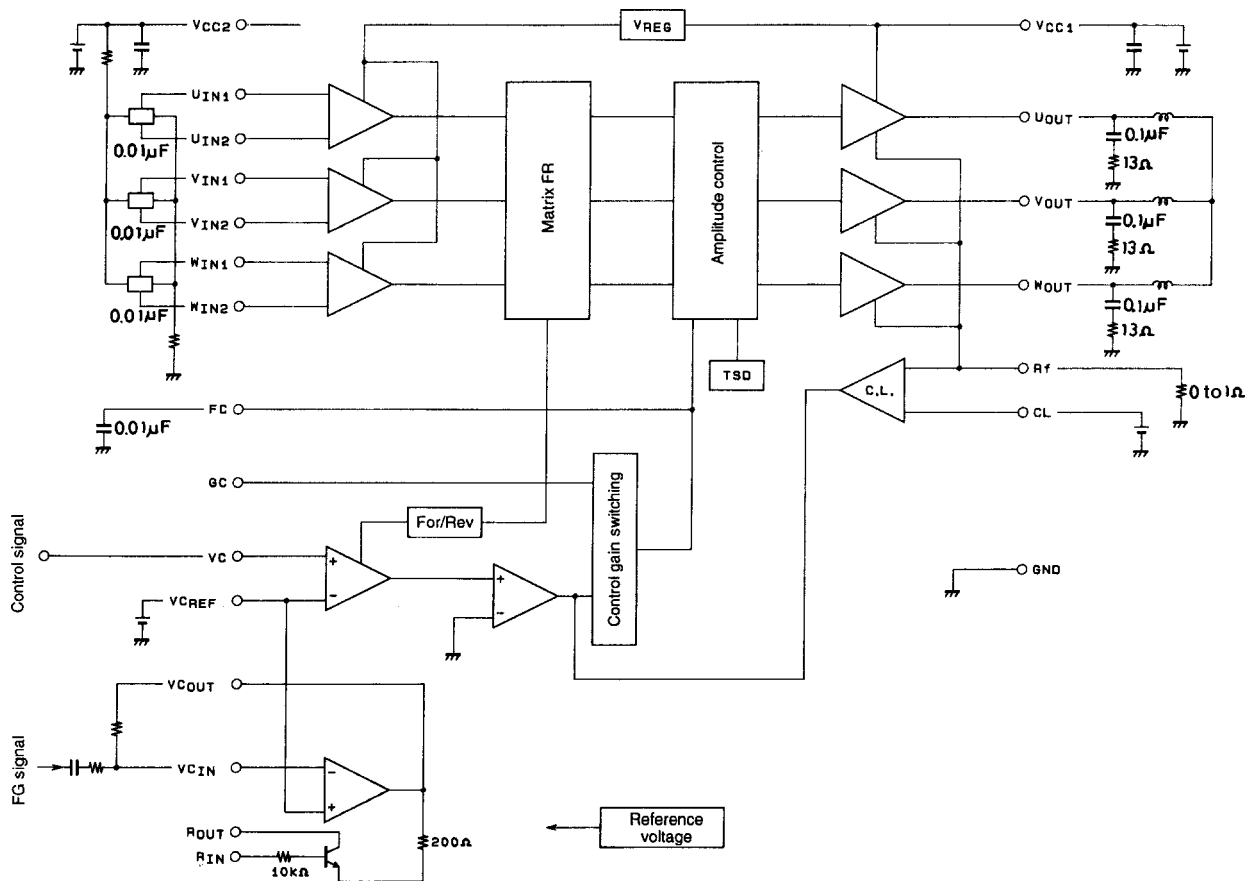
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## Block Diagram 1



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## Block Diagram 2



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## Pin Functions

Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
1, 2, 14, 15, 16, 17, 29, 30	FRAME (GND)			<ul style="list-style-type: none"> <li>Ground connection for all circuit except the outputs.</li> </ul>
3	FC			<ul style="list-style-type: none"> <li>Connect a capacitor between this pin and ground to reduce the control input-output gain frequency response and to stop the oscillator.</li> </ul>
4	V <sub>CREF</sub>	1.5V min V <sub>CC2</sub> max		<ul style="list-style-type: none"> <li>Speed control pins.</li> <li>Pin 4 voltage determines the control start voltage.</li> <li>Pin 5 voltage is used to control the output voltage (voltage control method).</li> </ul>
5	VC	0V min V <sub>CC2</sub> max		
6	V <sub>CC1</sub>	5 to 18V		<ul style="list-style-type: none"> <li>Output-stage supply pin.</li> </ul>
7 8 9	U <sub>OUT</sub> V <sub>OUT</sub> W <sub>OUT</sub>			<ul style="list-style-type: none"> <li>Output pins.</li> </ul>
10	R <sub>f</sub>			<ul style="list-style-type: none"> <li>Output transistor ground.</li> <li>A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection.</li> </ul>
11	V <sub>CC2</sub>	4.3 to 6.5V		<ul style="list-style-type: none"> <li>Supply for all circuits except the output stage.</li> <li>This supply should be kept stable to prevent ripple and noise from entering this pin.</li> </ul>

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Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
12	CL	0V min $V_{CC2}$ max		<ul style="list-style-type: none"> <li>When the voltage on Rf pin becomes equal to the voltage on pin 12 (CL), the current limiter operates. The pin 12 (CL) voltage is determined externally. If the current limiter is not used, it should be connected to <math>V_{CC2}</math></li> </ul>
13	GC	0V min $V_{CC2}$ max		<ul style="list-style-type: none"> <li>Control input gain switching pin. 35dB is selected when pin 13 (GC) is HIGH (4 to 5), and 29dB is selected when pin 13 (GC) is LOW (0 to 2V) or open for a value <math>V_{CC2}=5V</math>.</li> </ul>
18	$R_{OUT}$			<ul style="list-style-type: none"> <li>A resistor connected between this pin and pin 20 (<math>V_{CIN}</math>) enables pin 22 switching between HIGH level and open to switch the op-amplifier gain.</li> </ul>
19	$V_{COUT}$			<ul style="list-style-type: none"> <li>Op-amplifier output pin. This op-amplifier can be used for : 1. Control gain changing, or 2. FG amplifier.</li> </ul>
22	$R_{IN}$			<ul style="list-style-type: none"> <li>When this pin goes HIGH, the resistor connected between pins 18 and 20 is connected in parallel with the op-amplifier feedback resistor to switch the gain.</li> </ul>
20	$V_{CIN}$	0V min 3.5V max ( $V_{CC2}=5V$ )		<ul style="list-style-type: none"> <li>Op-amplifier inverting input pin. The op-amplifier non-inverting input is connected to pin 4 <math>V_{CREF}</math></li> </ul>

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Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
23 24	$W_{IN2}$ $W_{IN1}$	1.3V min 2.2V max		<ul style="list-style-type: none"> <li>W-phase Hall element input pins. Logic HIGH is represented by <math>W_{IN1} &gt; W_{IN2}</math>.</li> </ul>
25 26	$V_{IN2}$ $V_{IN1}$			<ul style="list-style-type: none"> <li>V-phase Hall element input pins. Logic HIGH is represented by <math>V_{IN1} &gt; V_{IN2}</math>.</li> </ul>
27 28	$U_{IN2}$ $U_{IN1}$			<ul style="list-style-type: none"> <li>U-phase Hall element input pins. Logic HIGH is represented by <math>U_{IN1} &gt; U_{IN2}</math>.</li> </ul>

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