Ordering number:EN4948A

Monolithic Digital IC

LB1894M

3-Phase Brushless Motor Driver for CD-ROM Spindle Motors

Overview

The LB1894M is a 3-phase brushless motor driver for use in CD-ROM spindle motors.

Function and Features

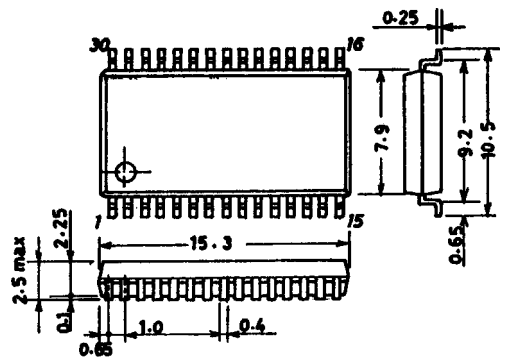
- 3-phase bipolar brushless motor driver.
- Voltage linear drive, enabling the external capacitance to be reduced.
- Thermal shutdown circuit built-in.
- Overcurrent protection circuit built-in.
- V-type control amplifier built-in.
- 2-step switching control gain.
- Control gain switchable using operational amplifier.

Package Dimensions

unit:mm

3073A-MFP30S

[LB1894M]



SANYO : MFP30S

Specifications

Absolute Maximum Ratings at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC}1$ max		20	V
	$V_{CC}2$ max		7.0	V
Output supply current	$V_{OU, V, W}$		22	V
Output current	I_{OUT}		1.5	A
Allowable power dissipation	Pd max		1.05	W
Operating temperature	Topr		–20 to +75	˚C
Storage temperature	Tstg		–55 to +150	˚C

Allowable Operating Ranges at Ta = 25˚C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	$V_{CC}1$		5 to 18	V
	$V_{CC}2$		4.3 to 6.5	V

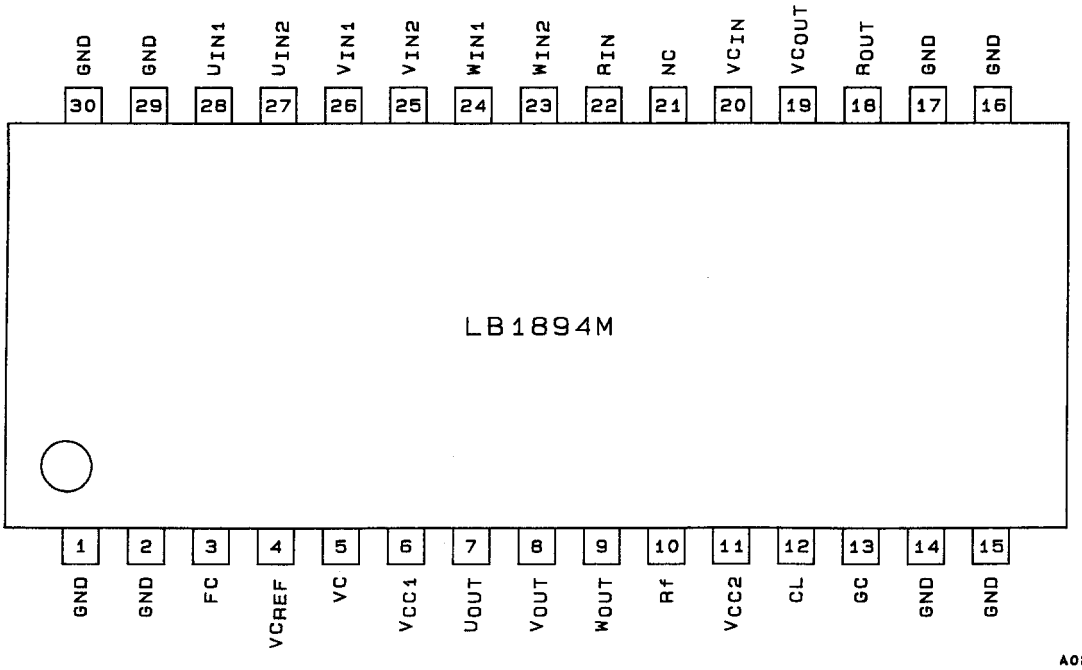
SANYO Electric Co.,Ltd. Semiconductor Bussiness Headquaters

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

Electrical Characteristics at Ta = 25˚C, $V_{CC}1$=12V, $V_{CC}2$=5V

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Supply current	I_{CC} 1	VC=VC_{REF}, R_L=∞		17	30	mA
	I_{CC} 2	VC=VC_{REF}		6.5	9.5	mA
[Driver stage]						
Output saturation voltage	$V_{O(sat)}1$	I_{OUT}=0.5A, sink+source		1.6	2.2	V
	$V_{O(sat)}2$	I_{OUT}=1.0A, sink+source		2.0	3.0	V
Output transistor blocking voltage	$V_{O(sus)}$	I_{OUT}=20mA, design value	20			V
Output rest voltage	V_{OQ}	VC=VC_{REF}	5.7	6.0	6.3	V
Hall amplifier input offset voltage	$V_{H\ offset}$		–5		+5	mV
Hall amplifier input bias current	$I_{H\ bias}$			1	5	µA
Hall amplifier common-mode input voltage range	V_{Hch}		1.3		2.2	V
Hall amplifier input-output voltage gain	G_{VHO}		42	45	48	dB
[Control stage]						
Control-output drive gain	$G_{VCO}1$	High gain, GC=high	32	35	38	dB
	$G_{VCO}2$	Low gain, GC=low	26	29	32	dB
Control-output channel difference	ΔG_{VCO}		–2		+2	dB
Control rising threshold voltage	VC_{TH}	VC_{REF}=2.5V, V_{OUT}=0.1Vp-p	2.35		2.65	V
Control rising threshold voltage width	ΔVC_{TH}	VC_{REF}=2.5V, V_{OUT}=0.1Vp-p	50		150	mV
Gain control switching high-level voltage	V_{GCH}		4		5	V
Gain control switching low-level voltage	V_{GCL}	Inputs are low level when left open	0		+2	V
[Op-amplifiers]						
Op-amplifier intput offset voltage	$V_{FG\ offset}$		–8		+8	mV
Open-loop voltage gain	G_{VFG}	f=1kHz		60		dB
Source output saturation voltage	$V_{FG\ OU}$	I_O=–2mA	3.7			V
Sink output saturation voltage	$V_{FG\ OD}$	I_O=2mA			1.3	V
Common-mode signal rejection	CHR	Design value		80		dB
Op-amplifier common-mode input voltage range	$V_{FG\ CH}$	VC_{REF}=1.5V to V_{CC}2, design value	0		+3.5	V
Phase margin	ϕM	Design value		20		deg
[Thermal shutdown]						
Thermal shutdown operating temperature	TSD	Design value	150	180	210	˚C
TSD hysteresis	ΔTSD	Design value		15		˚C

Pin Assignment

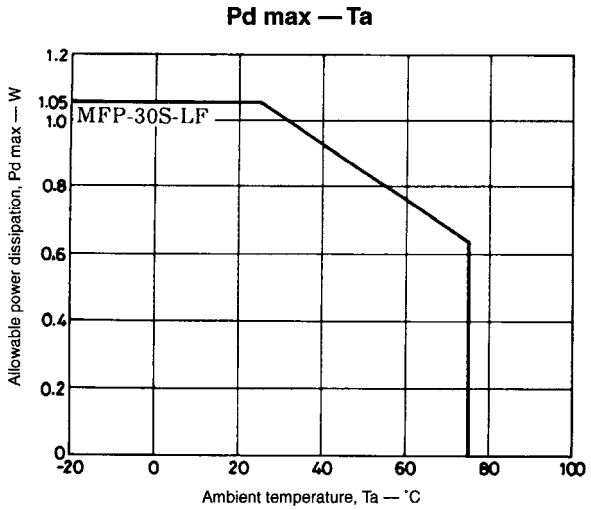


(Top view)

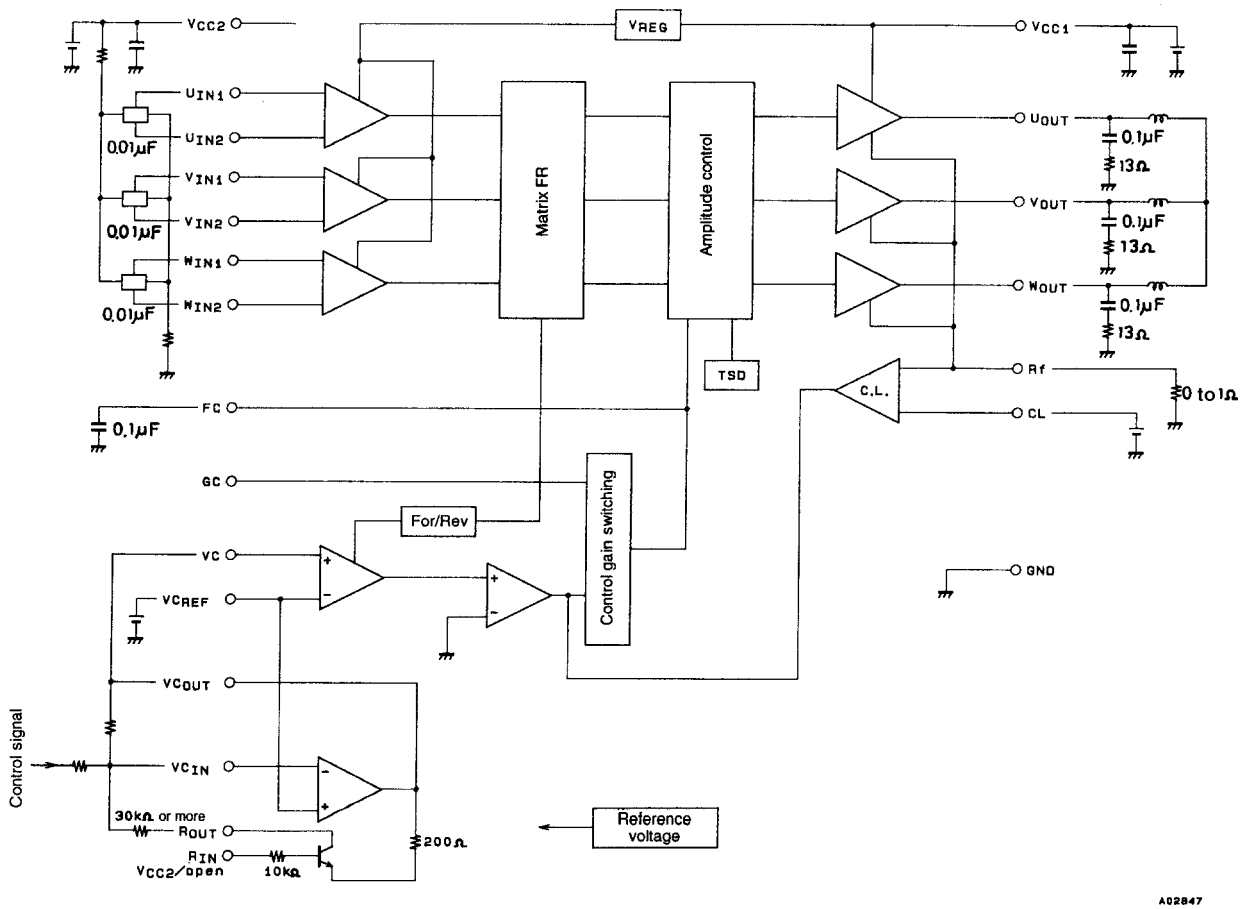
Truth Table

	Source→Sink	Hall Input			Control VC
		U_{IN}	V_{IN}	W_{IN}	
1	W-phase →V-phase	HIGH	HIGH	LOW	HIGH
	V-phase →W-phase				LOW
2	W-phase →U-phase	HIGH	LOW	LOW	HIGH
	U-phase →W-phase				LOW
3	V-phase →W-phase	LOW	LOW	HIGH	HIGH
	W-phase →V-phase				LOW
4	U-phase →V-phase	LOW	HIGH	LOW	HIGH
	V-phase →U-phase				LOW
5	V-phase →U-phase	HIGH	LOW	HIGH	HIGH
	U-phase →V-phase				LOW
6	U-phase →W-phase	LOW	HIGH	HIGH	HIGH
	W-phase →U-phase				LOW

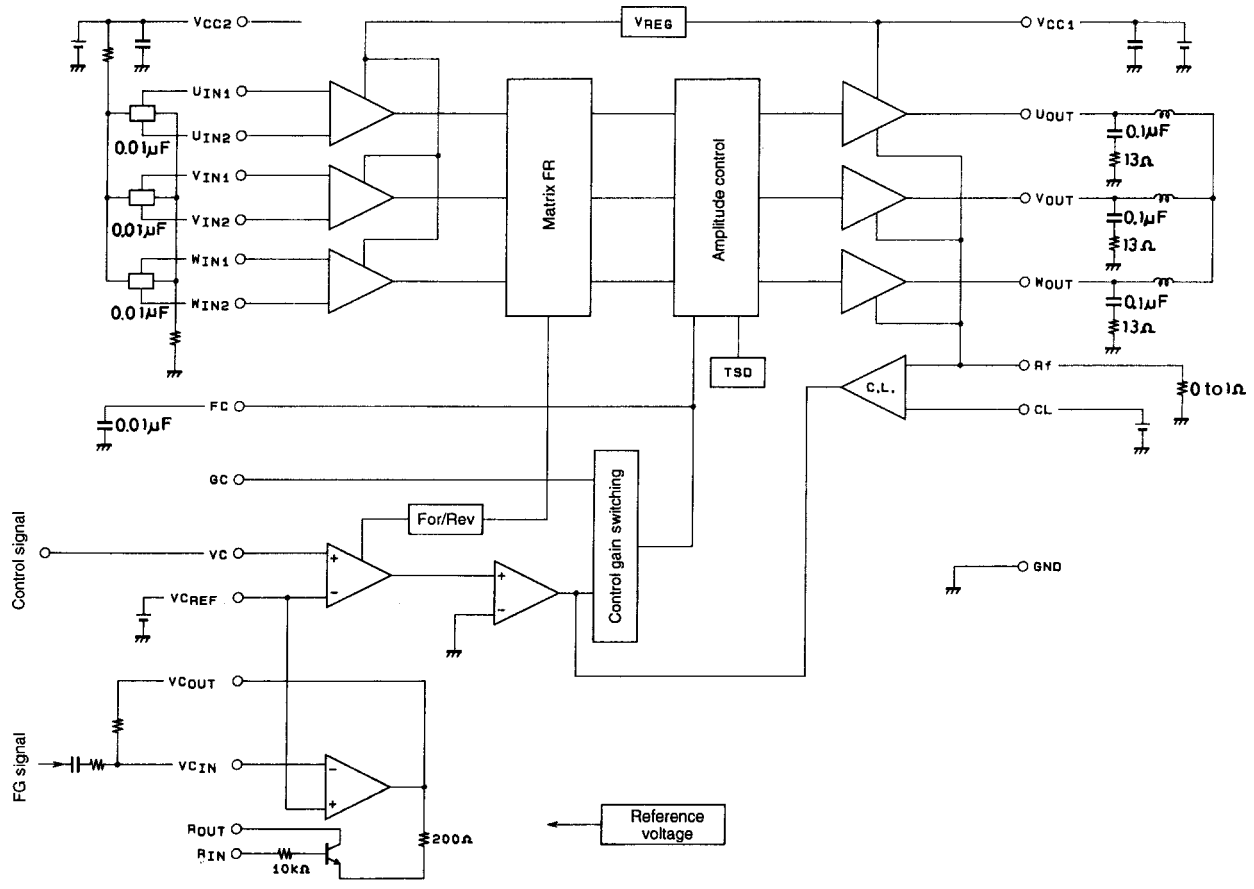
An input is considered to be HIGH when $U_{IN}1 > U_{IN}2$, $V_{IN}1 > V_{IN}2$, and $W_{IN}1 > W_{IN}2$ by 0.2V more, and is considered to be LOW when $U_{IN}1 > U_{IN}2$, $V_{IN}1 > V_{IN}2$, and $W_{IN}1 > W_{IN}2$ by 0.2V or less.



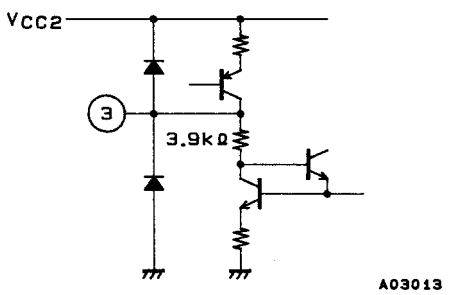
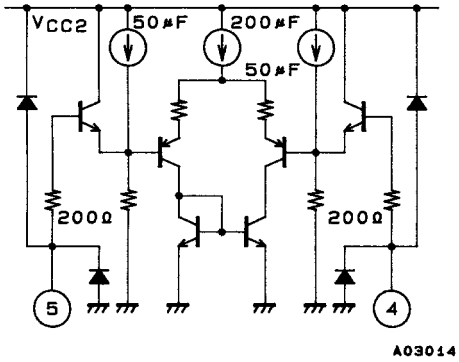
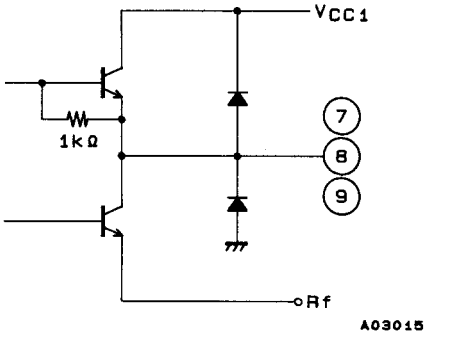
Block Diagram 1



Block Diagram 2



Pin Functions

Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
1, 2, 14, 15, 16, 17, 29, 30	FRAME (GND)			• Ground connection for all circuit except the outputs.
3	FC			• Connect a capacitor between this pin and ground to reduce the control input-output gain frequency response and to stop the oscillator.
4	VC_{REF}	1.5V min $V_{CC}2$ max		• Speed control pins. Pin 4 voltage determines the control start voltage. Pin 5 voltage is used to control the output voltage (voltage control method).
5	VC	0V min $V_{CC}2$ max		
6	$V_{CC}1$	5 to 18V		• Output-stage supply pin.
7 8 9	U_{OUT} V_{OUT} W_{OUT}			• Output pins.
10	Rf			• Output transistor ground. A resistor can be connected between this pin and GND to sense the output current as a voltage drop to provide for overcurrent protection.
11	$V_{CC}2$	4.3 to 6.5V		• Supply for all circuits except the output stage. This supply should be kept stable to prevent ripple and noise from sntering this pin.

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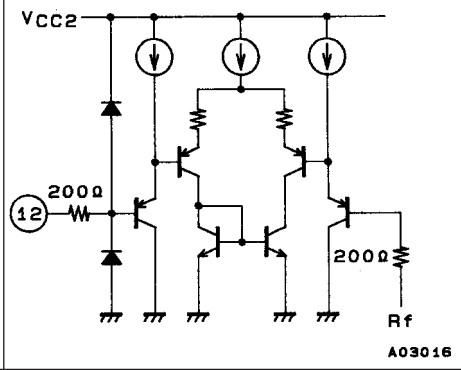
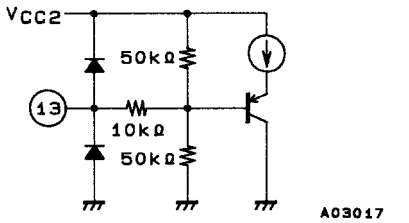
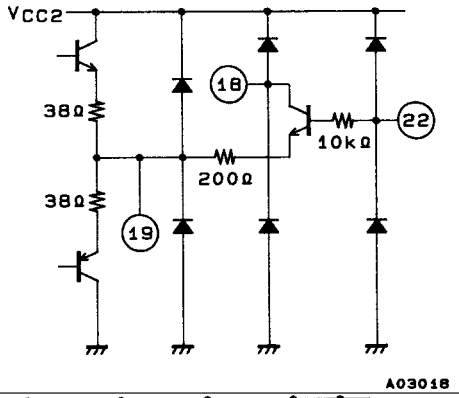
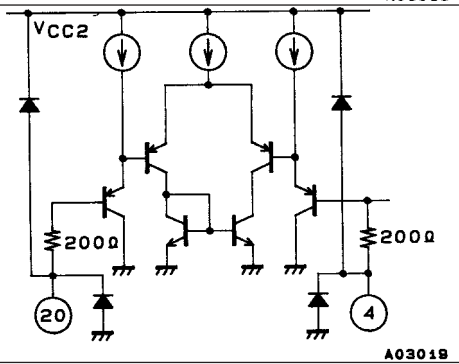
Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
12	CL	0V min $V_{CC}2$ max		• When the voltage on Rf pin becomes equal to the voltage on pin 12 (CL), the current limiter operates. The pin 12 (CL) voltage is determined externally. If the current limiter is not used, it should be connected to $V_{CC}2$
13	GC	0V min $V_{CC}2$ max		• Control input gain switching pin. 35dB is selected when pin 13 (GC) is HIGH (4 to 5), and 29dB is selected when pin 13 (GC) is LOW (0 to 2V) or open for a value $V_{CC}2$=5V.
18	R_{OUT}			• A resistor connected between this pin and pin 20 (VC_{IN}) enables pin 22 switching between HIGH level and open to switch the op-amplifier gain.
19	VC_{OUT}			• Op-amplifier output pin. This op-amplifier can be used for : 1. Control gain changing, or 2. FG amplifier.
22	R_{IN}			• When this pin goes HIGH, the resistor connected between pins 18 and 20 is connected in parallel with the op-amplifier feedback resistor to switch the gain.
20	VC_{IN}	0V min 3.5V max ($V_{CC}2$=5V)		• Op-amplifier inverting input pin. The op-amplifier non-inverting input is connected to pin 4 VC_{REF}

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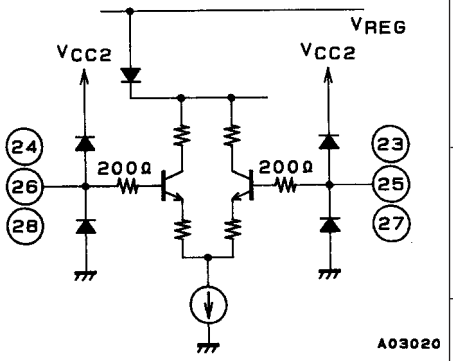
Pin No.	Symbol	Pin voltage	Equivalent circuit	Function
23 24	W_{IN} 2 W_{IN} 1	1.3V min 2.2V max		• W-phase Hall element input pins. Logic HIGH is represented by $W_{IN}1 > W_{IN}2$.
25 26	V_{IN} 2 V_{IN} 1			• V-phase Hall element input pins. Logic HIGH is represented by $V_{IN}1 > V_{IN}2$.
27 28	U_{IN} 2 U_{IN} 1			• U-phase Hall element input pins. Logic HIGH is represented by $U_{IN}1 > U_{IN}2$.