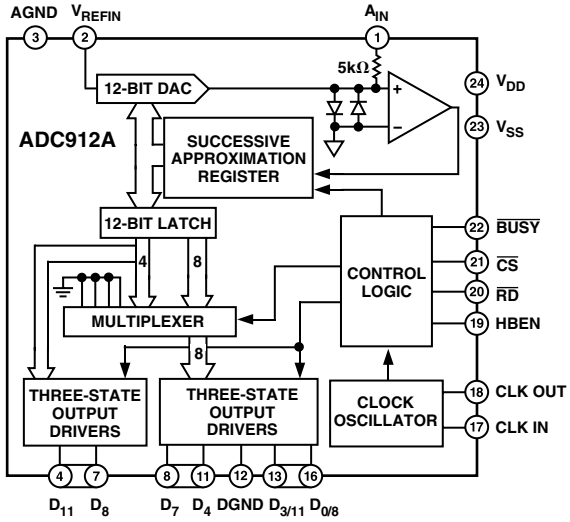
CMOS Microprocessor-Compatible 12-Bit A/D Converter

ADC912A

FEATURES
- Low Cost
- Low Transition Noise between Code
- 12-Bit Accurate
  - ±1/2 LSB Nonlinearity Error over Temperature
  - No Missing Codes at All Temperatures
- 10 μs Conversion Time
- Internal or External Clock
- 8- or 16-Bit Data Bus Compatible
- Improved ESD Resistant Design
- Latchup Resistant Epi-CMOS Processing
- Low 95 mW Power Consumption
- Space-Saving 24-Lead 0.3" DIP, or 24-Lead SOIC

APPLICATIONS
- Data Acquisition Systems
- DSP System Front End
- Process Control Systems
- Portable Instrumentation

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADC912A is a monolithic 12-bit accurate CMOS A/D converter. It contains a complete successive-approximation A/D converter built with a high-accuracy D/A converter, a precision bipolar transistor high-speed comparator, and successive-approximation logic including three-state bus interface for logic compatibility. The accuracy of the ADC912A results from the addition of precision bipolar transistors to Analog Devices' advanced-oxide isolated silicon-gate CMOS process. Particular attention was paid to the reduction of transition noise between adjacent codes achieving a 1/6 LSB uncertainty. The low noise design produces the same digital output for dc analog inputs not located at a transition voltage, see Figures 1 and 2. NPN digital output transistors provide excellent bus interface timing, 125 ns access and bus disconnect time which results in faster data transfer without the need for wait states. An external 1.25 MHz clock provides a 10 μs conversion time.

In stand-alone applications an internal clock can be used with external crystal.

An external negative five-volt reference sets the 0 V to 10 V input range. Plus 5 V and minus 12 V power supplies result in 95 mW of total power consumption.

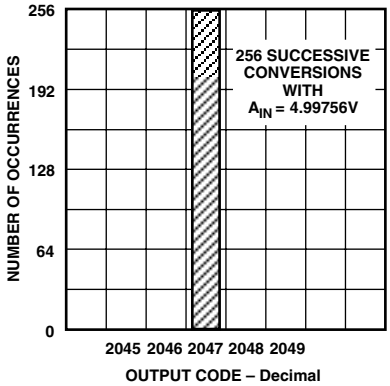


Figure 1. Code Repetition

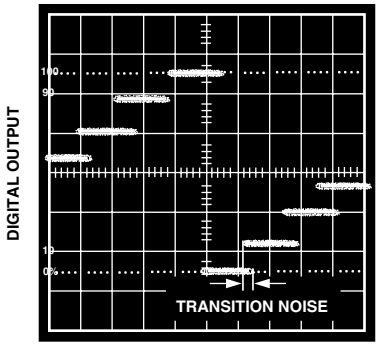


Figure 2. Transition Noise Cross Plot

REV. B

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ADC912A–SPECIFICATIONS (V_{DD} = +5 V ± 5%, V_{SS} = –11.4 V to –15.75 V, V_{REFIN} = –5 V, Analog Input 0 V to 10 V; External f_{CLK} = 1.25 MHz; –40°C to +85°C applies to ADC912A/F unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
STATIC ACCURACY						
Integral Nonlinearity	INL		–1		+1	LSB
Differential Nonlinearity	DNL		–1		+1	LSB
Offset Error	V_{ZSE}	V_{DD} = +5 V, V_{SS} = –12 V	–5		+5	LSB
Gain Error	G_{FSE}	V_{DD} = +5 V, V_{SS} = –12 V	–6		+6	LSB
Full-Scale Tempco[1]	TCG_{FS}			5	15	ppm/°C
ANALOG INPUT						
Input Voltage Range	V_{IN}		0		10	V
Input Current Range	I_{IN}		0		3	mA
POWER SUPPLIES						
Positive Supply Current	I_{DD}	V_{DD} = +5 V[2]		5	7	mA
Negative Supply Current	I_{SS}	V_{SS} = –12 V[2]		3	5	mA
Power Consumption	P_{DISS}	V_{DD} = +5 V[2], V_{SS} = –12 V[2]		70	95	mW
Power Supply Rejection Ratio	PSRR+	ΔV_{DD} = ±5%, A_{IN} = 10 V		1/2	4	LSB
	PSRR–	ΔV_{SS} = ±5%, A_{IN} = 10 V		1/2	4	LSB
DIGITAL INPUTS						
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4			V
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN			0.8	V
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN			±1	µA
Digital Input Capacitance	C_{IN}	Digital Inputs, $\overline{CS}$, $\overline{RD}$, HBEN, CLKIN		7	10	pF
DIGITAL OUTPUTS						
Logic Input High Voltage	V_{OH}	I_{SOURCE} = 0.2 mA	4			V
Logic Input Low Voltage	V_{OL}	I_{SINK} = 1.6 mA			0.4	V
Three-State Output Leakage	I_{OZ}	D_{11}–$D_{0/8}$			10	µA
Digital Input Capacitance	C_{OUT}	D_{11}–$D_{0/8}$[1]		8	15	pF
DYNAMIC PERFORMANCE						
Conversion Time	TC	f_{CLK} = 1.25 MHz[3]				
		Synchronous Clock			10.4	µs
		Asynchronous Clock	10.4		11.2	µs

NOTES
[1]Guaranteed by design.
[2]Converter inactive; $\overline{CS}$, $\overline{RD}$ = High, A_{IN} = 10 V.
[3]See Synchronizing Start Conversion information in Converter Operation Details. Typicals (typ) are median values measured at 25 °C. See Typical Performance Characteristics for additional information.

Specifications subject to change without notice.

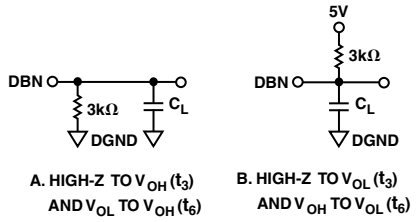


Figure 3. Load Circuits for Access Time

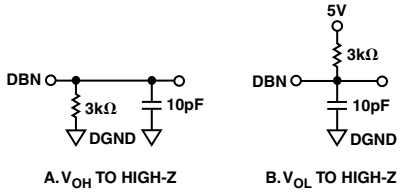


Figure 4. Load Circuits for Output Float Delay

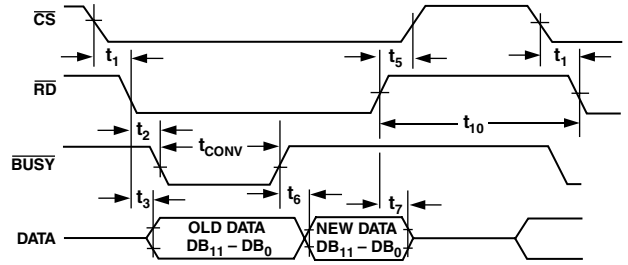
TIMING CHARACTERISTICS[1, 2] (V_{DD} = +5 V ± 5%, V_{SS} = –11.4 V to –15.75 V, V_{REFIN} = –5 V, Analog Input 0 V to 10 V; External f_{CLK} = 1.25 MHz; –40°C to +85°C applies to ADC912A/F unless otherwise noted. See Figures 5 to 8.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_1		0			ns
$\overline{RD}$ to $\overline{BUSY}$ Propagation Delay	t_2				150	ns
Data Access Time after READ	t_3[3]	C_L = 100 pF		65	125	ns
Read Pulsewidth	t_4[3]		90			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_5		0			ns
New Data Valid after $\overline{BUSY}$	t_6[3]	C_L = 100 pF		–30	0	ns
Bus Disconnect Time	t_7		20	60	90	ns
HBEN to $\overline{RD}$ Setup Time	t_8		20			ns
HBEN to $\overline{RD}$ Hold Time	t_9		20			ns
Delay between Successive Read Operations	t_{10}		350	250		ns

NOTES
[1]Guaranteed by design.
[2]All input control signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of 5 V) and timed from a voltage level of 1.6 V.
[3]t_3, t_4, and t_6 are measured with the load circuits of Figure 3 and timed for and output to cross 0.8 V or 2.4 V.
[4]t_7 is the time required for the data lines to change 0.5 V when loaded with the circuits of Figure 4.

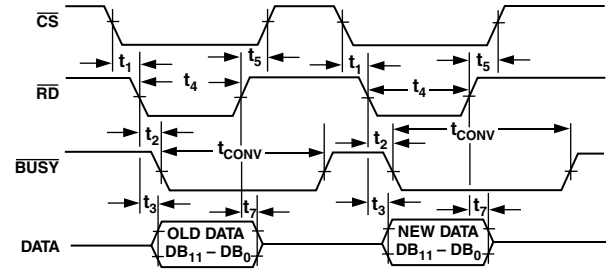
Specifications subject to change without notice.

TIMING DIAGRAMS



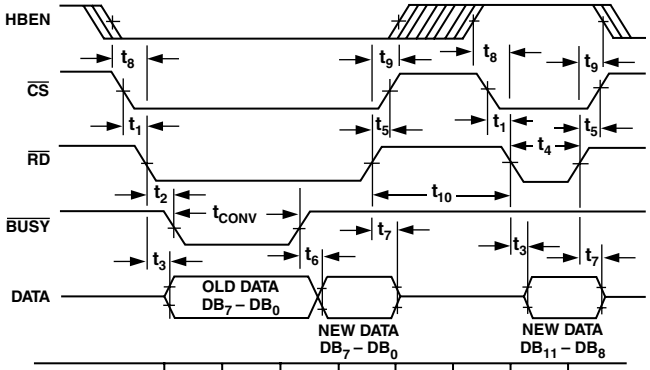
DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Figure 5. Parallel Read Timing Diagram, Slow-Memory Mode (HBEN = LOW)



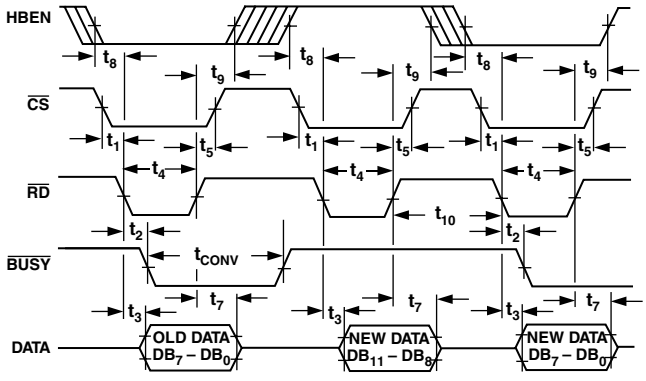
DATA OUTPUTS	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ (OLD DATA)	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Figure 7. Parallel Read Timing Diagram, ROM Mode (HBEN = LOW)



DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8

Figure 6. Two-Byte Read Timing Diagram, Slow-Memory Mode



DATA OUTPUTS	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
FIRST READ (OLD DATA)	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
SECOND READ	LOW	LOW	LOW	LOW	DB_{11}	DB_{10}	DB_9	DB_8
THIRD READ	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0

Figure 8. Two-Byte Read Timing Diagram, ROM Mode

ABSOLUTE MAXIMUM RATINGS
(T_A = 25°C, unless otherwise noted)

V_{DD} to DGND . . . . . –0.3 V to +7 V
V_{SS} to DGND . . . . . +0.3 V to –7 V
V_{REFIN} to DGND . . . . . V_{SS} to V_{DD}
AGND to DGND . . . . . –0.3 V to V_{DD} + 0.3 V
A_{IN} to AGND . . . . . –15 V to +15 V
Digital Input Voltage to DGND,
Pins 17, 19–21 . . . . . –0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to DGND,
Pins 4–11, 13–16, 18, 22 . . . . . –0.3 V to V_{DD} + 0.3 V
Operating Temperature Range
Extended Industrial: ADC912A/F . . . . . –40°C to +85°C
Storage Temperature . . . . . –65°C to +150°C
Lead Temperature (Soldering, 10 sec) . . . . . 300°C
Maximum Junction Temperature (T_J max) . . . . . 150°C
Package Power Dissipation . . . . . (T_J max–T_A)/θ_{JA}
Thermal Resistance θ_{JA}
Plastic DIP . . . . . 57°C/W
SOIC-24 . . . . . 70°C

ORDERING GUIDE

Model	Temperature Range	INL (LSB)	Package Description	Package Option
ADC912AFP	–40°C to +85°C	±1	24-Lead Narrow-Body Plastic	N-24
ADC912AFS	–40°C to +85°C	±1	24-Lead Wide-Body SOIC	R-24

Table I. Analog Input to Digital Output Code Conversion

	Analog Input Voltage		Output Code*
	0 V to 10 V	–10 V to +10 V	DB_{11} (MSB) DB_0 (LSB)
+FS – 1 LSB	9.9976	9.99951	1 1 1 1 1 1 1 1 1 1 1 1
+FS – 1 1/2 LSB	9.9964	9.9927	1 1 1 1 1 1 1 1 1 1 1 ϕ
Midscale + 1/2 LSB	5.0012	0.0024	1 0 0 0 0 0 0 0 0 0 0 ϕ
Midscale	5.0000	0.0000	1 0 0 0 0 0 0 0 0 0 0 0
–FS + 1/2 LSB	0.0012	–9.9976	0 0 0 0 0 0 0 0 0 0 0 ϕ
–FS	0.0000	–10.000	0 0 0 0 0 0 0 0 0 0 0 0

*The symbol"ϕ" indicates a 0 or 1 with equal probability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADC912A features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

WAFER TEST LIMITS (@ V_{DD} = +5 V, V_{SS} = –12 V or –15 V, V_{REF} = –5 V, A_{IN} = 0 V to 10 V, and T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	ADC912AG Limit	Unit
Integral Nonlinearity	INL		±1	LSB max
Differential Nonlinearity	DNL		±1	LSB max
Offset Error	V_{ZSE}	Guaranteed by Design	±8	LSB max
Gain Error	G_{FSE}		±8	LSB max
Analog Input Resistance	R_{AIN}		4/6	kΩ min/max
Logic Input High Voltage	V_{INH}	$\overline{CS}$, $\overline{RD}$, HBEN	2.4	V min
Logic Input Low Voltage	V_{INL}	$\overline{CS}$, $\overline{RD}$, HBEN	0.8	V max
Logic Input Current	I_{IN}	$\overline{CS}$, $\overline{RD}$, HBEN	±1	µA max
Logic Output High Voltage	V_{OH}	I_{SOURCE} = 0.2 mA	4	V min
Logic Output Low Voltage	V_{OL}	I_{SINK} = 1.6 mA	0.4	V max
Positive Supply Current	I_{DD}	V_{DD} = +5 V, $\overline{CS}$ = $\overline{RD}$ = V_{DD}, A_{IN} = +10 V	7	mA max
Negative Supply Current	I_{SS}	V_{SS} = –12 V, $\overline{CS}$ = $\overline{RD}$ = V_{DD}, A_{IN} = +10 V	5	mA max

NOTE
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

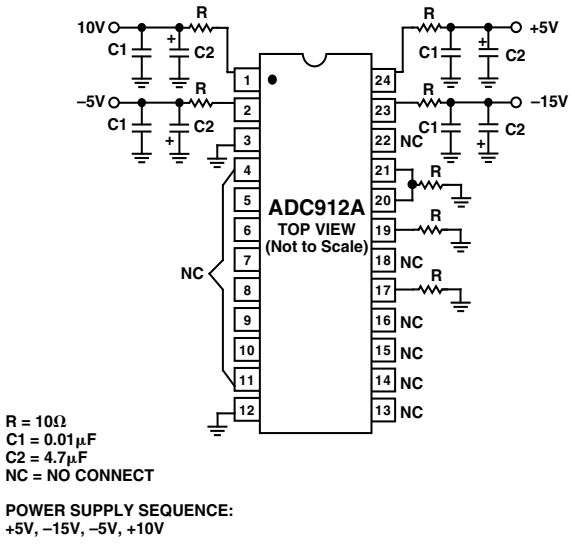


Figure 9. Burn-In Circuit

PIN FUNCTION DESCRIPTIONS

Pin	Mnemonic	Description
1	AIN	Analog Input. 0 V to 10 V.
2	VREFIN	Voltage Reference Input. Requires external –5 V reference.
3	AGND	Analog Ground.
4 . . . 11	D_{11} . . . D_4	Three-state data outputs become active when $\overline{CS}$ and $\overline{RD}$ are brought low.
13 . . . 16	$D_{3/11}$ . . . $D_{0/8}$	Individual pin function is dependent upon High Byte Enable (HBEN) input.

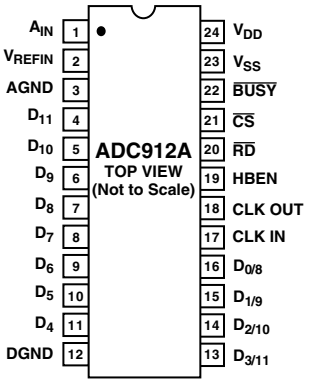
DATA BUS OUTPUT, $\overline{CS}$ and $\overline{RD}$ = LOW

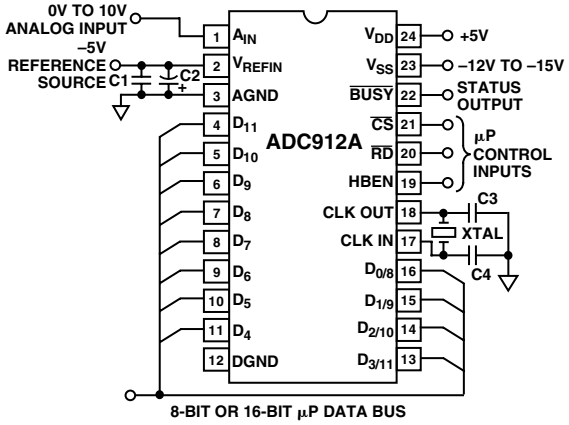
	Pin 4	Pin 5	Pin 6	Pin 7	Pin 8	Pin 9	Pin 10	Pin 11	Pin 13	Pin 14	Pin 15	Pin 16
Mnemonic*	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	$D_{3/11}$	$D_{2/10}$	$D_{1/9}$	$D_{0/8}$
HBEN = LOW	DB_{11}	DB_{10}	DB_9	DB_8	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
HBEN = HIGH	DB_{11}	DB_{10}	DB_9	DB_8	Low	Low	Low	Low	DB_{11}	DB_{10}	DB_9	DB_8

*D_{11} . . . $D_{0/8}$ are the ADC data output pins.
DB_{11} . . . DB_0 are the 12-bit conversion results. DB_{11} is the MSB.

12	DGND	Digital Ground.
17	CLK IN	Clock Input Pin. An external TTL-compatible clock may be applied to this pin. Alternatively a crystal or ceramic resonator may be connected between CLK IN (Pin 17) and CLK OUT (Pin 18).
18	CLK OUT	Clock Output Pin. An inverted CLK IN signal appears at CLK OUT when an external clock is used. See CLK IN (Pin 17) description for crystal (resonator).
19	HBEN	High Byte Enable Input. Its primary function is to multiplex the 12 bits of conversion data onto the lower D_7 . . . $D_{0/8}$ outputs (4 MSBs or 8 LSBs). See pin description 4 . . . 11 and 13 . . . 16. Also disables conversion start when HBEN is high.
20	$\overline{RD}$	READ Input. This active LOW signal, in conjunction with $\overline{CS}$, is used to enable the output data three state drivers and initiates a conversion if CS and HBEN are low.
21	$\overline{CS}$	Chip Select Input. This active LOW signal, in conjunction with $\overline{RD}$, is used to enable the output data three-state drivers and initiates a conversion if $\overline{RD}$ and HBEN are low.
22	$\overline{BUSY}$	$\overline{BUSY}$ output indicates converter status. $\overline{BUSY}$ is LOW during conversion.
23	V_{SS}	Negative Supply, –12 V or –15 V.
24	V_{DD}	Positive Supply, +5 V.

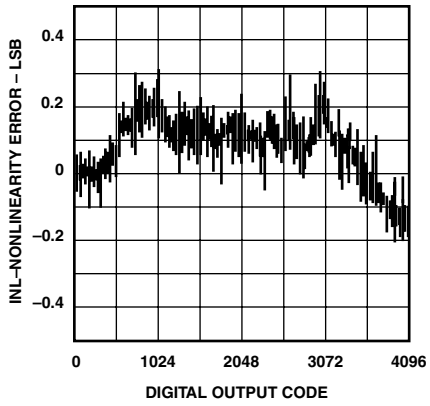
PIN CONFIGURATION



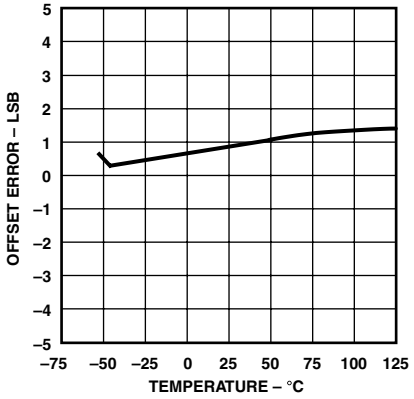


XTAL = 1MHz, C1 = 0.1 µF, C3 = 10 µF
C3, C4 = 30pF TO 100pF DEPENDING ON XTAL CHOSEN

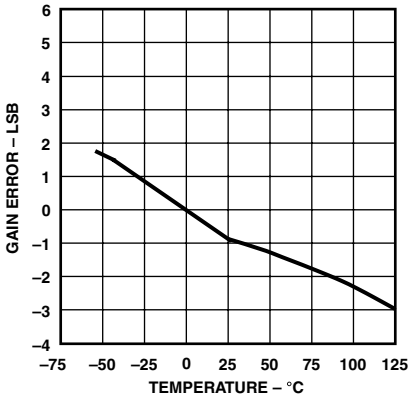
Figure 10. Basic Connection Diagram



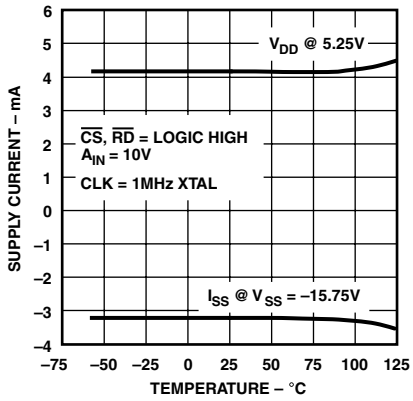
TPC 1. Nonlinearity Error vs. Digital Output Code



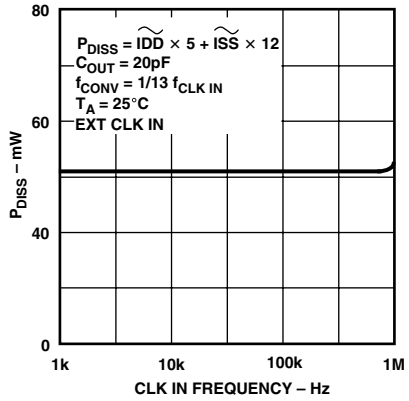
TPC 2. Offset Error vs. Temperature



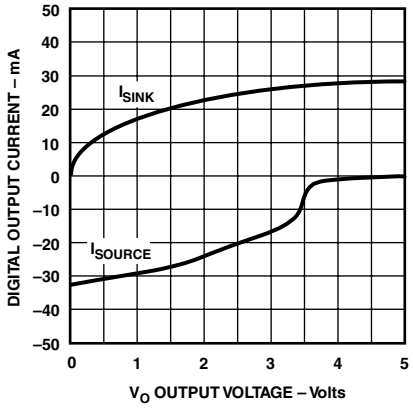
TPC 3. Gain Error vs. Temperature



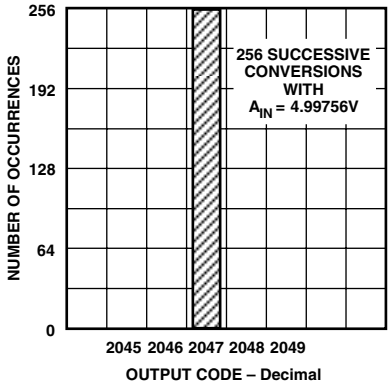
TPC 4. Supply Current vs. Temperature



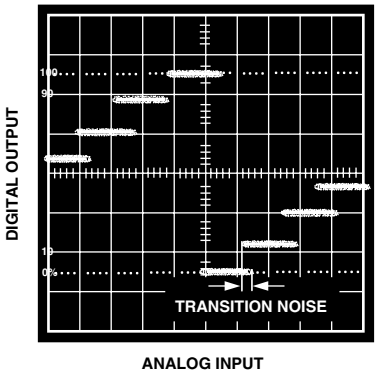
TPC 5. Power Dissipation vs. CLK IN Frequency



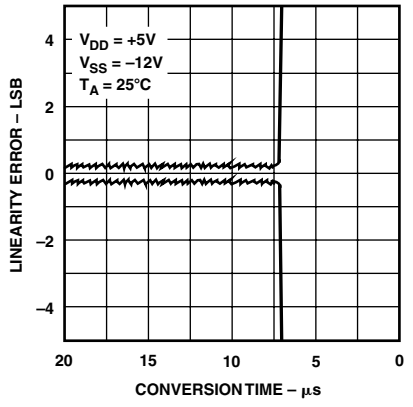
TPC 6. Digital Output Current vs. Output Voltage



TPC 7. Code Repetition



TPC 8. Transition Noise Cross Plot



TPC 9. Linearity Error vs. Conversion Time

CIRCUIT CHARACTERISTICS

The characteristic curves provide more complete static and dynamic accuracy information necessary for repetitive sampling applications often used in DSP processing. One of the important characteristic curves provided displays integral nonlinearity error (INL) versus output code with a typical value of ±1/4 LSB. Another very important characteristic associated with INL is the transition noise shown in the transition noise cross plot. The ADC912A offers extremely small, ±1/6 LSB, transition noise which maintains the system signal-to-noise ratio in DSP processing applications. Code repetition plots show the precision internal comparator of the ADC912A making the same decision every time for dc input voltages. Code repetition along with no missing codes assures proper performance when the ADC912A is used in servo-control systems.

CONVERTER OPERATION DETAILS

The $\overline{CS}$, $\overline{RD}$, and HBEN digital inputs control the start of conversion. A high-to-low on both $\overline{CS}$ and $\overline{RD}$ initiate a conversion sequence. The HBEN high-byte-enable input must be low or coincident with the read $\overline{RD}$ input edge. The start of conversion resets the internal successive approximation register (SAR) and enables the three-state outputs. See Figure 11. The busy line is active low during the conversion process.

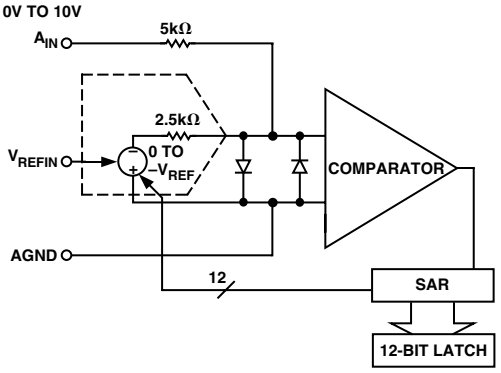


Figure 11. Simplified Analog Input Circuitry of ADC912A

During conversion, the SAR sequences the internal voltage output DAC from the most significant bit (MSB) to the least significant bit (LSB). The analog input connects to the comparator via a 5 kΩ resistor. The DAC, which has a 2.5 kΩ output resistance, connects to the same comparator input. The comparator, performing a zero crossing detection, tests the addition of successively weighted bits from the DAC output versus the analog input signal. The MSB decision occurs 200 ns after the second positive edge of the CLK IN following conversion initiation. The remaining 11-bit trials occur after the next 11 positive CLK IN edges. Once a conversion cycle is started it cannot be stopped or restarted, without upsetting the remaining bit decisions. Every conversion cycle must have 13 negative and positive CLK IN edges. At the end of conversion the comparator input voltage is zero. The SAR contains the 12-bit data word representing the analog input voltage. The BUSY line returns to logic high, signaling end of conversion. The SAR transfers the new data to the 12-bit latch.

SYNCHRONIZING START CONVERSION

Aligning the negative edge of $\overline{RD}$ with the rising edge of CLK IN provides synchronization of the internal start conversion signal to other system devices for sampling applications.

When the negative edge of $\overline{RD}$ is aligned with the positive edge of CLK IN, the conversion will take 10.4 microseconds. The minimum setup time between the negative edge of CLK IN and the negative edge of $\overline{RD}$ is 180 ns. Without synchronization the conversion time will vary from 12.5 to 13.5 clock cycles. See Figure 12.

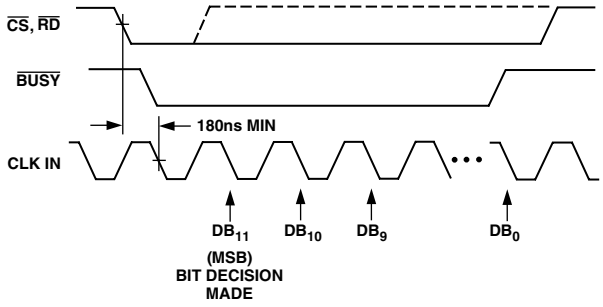


Figure 12. External Clock Input Synchronization

POWER ON INITIALIZATION

During system power-up the ADC912A comes up in a random state. Once the clock is operating or an external clock is applied, the first valid conversion begins with the application of a high-to-low transition on both $\overline{CS}$ and $\overline{RD}$. The next 13 negative clock edges complete the first conversion, producing valid data at the digital outputs. This is important in battery-operated systems where power supplies are shut down between measurement times.

DRIVING THE ANALOG INPUT

During conversion, the internal DAC output current modulates the analog input current at the CLK IN frequency of 1.25 MHz. The analog input to the ADC912A must not change during the conversion process. This requires an external buffer with low output impedance at 1.25 MHz. Suitable devices meeting this requirement include the OP27, OP42, and the SMP-11.

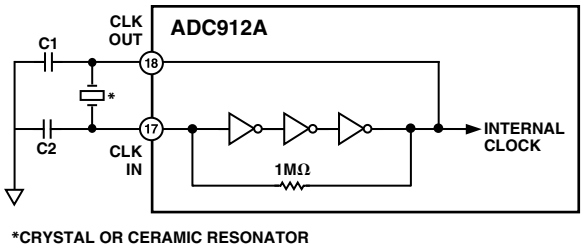


Figure 13. ADC912A Simplified Internal Clock Circuit

INTERNAL CLOCK OSCILLATOR

Figure 13 shows the ADC912A internal clock circuit. The clock oscillates at the external crystal or ceramic resonator frequency. The 1.25 MHz crystal or ceramic resonator connects between the CLK IN (Pin 17) and the CLK OUT (Pin 18). Capacitance values (C1, C2) depend on the crystal or ceramic resonator manufacturer. The crystal vendors should be qualified due to variations in C1 and C2 values required from vendor to vendor. Typical values range from 30 pF to 100 pF.

EXTERNAL CLOCK INPUT

A TTL compatible signal connected to CLK IN provides proper converter clock operation. No connection is necessary to the CLK OUT pin. The duty cycle of the external clock input can vary from 45% to 55%. Figure 12 shows the important waveforms.

EXTERNAL REFERENCE

A low output resistance, negative five volt reference is necessary. The external reference should be able to supply 3 mA of reference current. A bypass capacitor is necessary on the reference input lead to minimize system noise as the internal DAC switches. The reference input to the internal DAC is code dependent requiring anywhere from zero to 3 mA. The reference voltage tolerance has a direct influence on A/D converter full-scale voltage, and the maximum input full-scale voltage equals $2 \times -V_{REF}$. The ADC912A is designed for ratiometric operation, but operation using reference voltages between –5.00 V and 0 V will result in degraded linearity performance. Integral linearity is fully tested and guaranteed for references of –5 V. Figure 14 provides a good –5 V reference that does not require precision resistors.

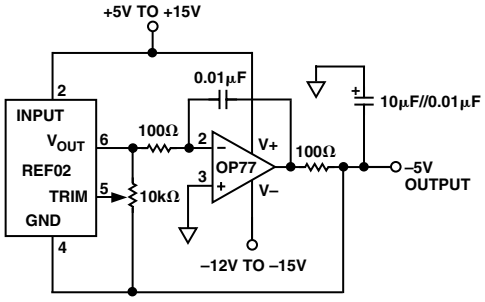


Figure 14. –5 V Reference

UNIPOLAR ANALOG INPUT OPERATION

Figure 15 shows the ideal input/output characteristic for the 0 V to 10 V input range of the ADC912A. The designed output code transitions occur midway between successive integer LSB values (i.e., 0.5 LSB, 1.5 LSBs, 2.5 LSBs . . . FS – 1.5 LSBs). The output code is natural binary with 1 LSB = FS/4096 = (10/4096) V = 2.44 mV. The maximum full-scale input voltage is (10 × 4095/4096) V = 9.9976 V.

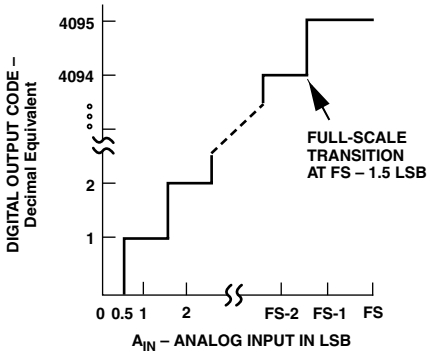


Figure 15. Ideal ADC912A Input/Output Transfer Characteristic

OFFSET AND FULL-SCALE ERROR ADJUSTMENT, UNIPOLAR OPERATION

For applications where absolute accuracy is important, offset and full-scale errors can be adjusted to zero. Figure 16 shows the extra components required for full-scale error adjustment. Zero offset is achieved by adjusting the null offset of the op amp driving A_{IN}.

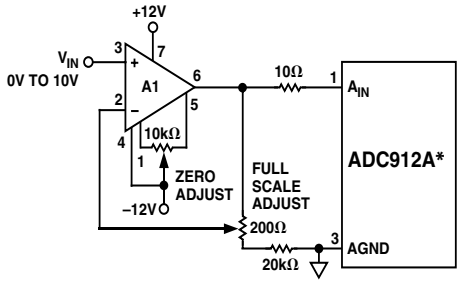
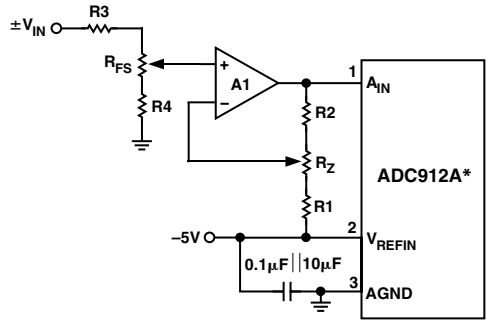


Figure 16. Unipolar 0 V to 10 V Operation

Adjust the zero scale first by applying 1.22 mV (equivalent to 0.5 LSB input) to V_{IN}. Adjust the op amp offset control until the digital output toggles between 0000 0000 0000 and 0000 0000 0001. The next step is adjustment of full scale. Apply 9.9963 V (equivalent to FS – 1.5 LSB) to V_{IN} and adjust R1 until the digital output toggles between 1111 1111 1110 and 1111 1111 1111.

BIPOLAR ANALOG INPUT OPERATION

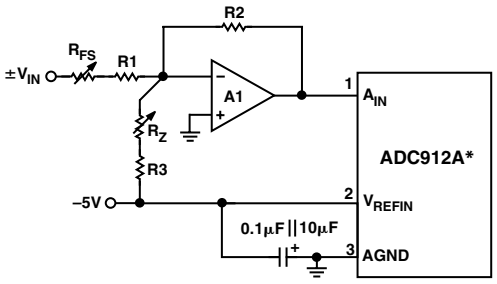
Bipolar analog input operation is achieved with an external amplifier providing an analog offset. Figures 17 and 18 show two circuit topologies that result in different digital-output coding. In Figure 17, offset binary coding is produced when the external amplifier is connected in the inverting mode. Figure 19 shows the ideal transfer characteristics for both the inverting and noninverting configurations given in Figures 17 and 18.



R1 = R2 = 20kΩ
SEE TABLE II FOR VALUES OF R3, R4, R_Z, AND R_{FS}
A1: OP27 LOWEST NOISE, OP42 BEST BANDWIDTH
*EXTRA PINS OMITTED FOR CLARITY

Figure 17. Noninverting Bipolar Analog Input Operation

The scaling resistors chosen in bipolar input applications should be from the same manufacturer to obtain good resistor tracking performance over temperature. When potentiometers are used for absolute adjustment, 0.1% tolerance resistors should still be used as shown in Figures 17 and 18 to minimize temperature coefficient errors.



SEE TABLE III FOR VALUES OF R1, R2, R3, R4, R_Z, AND R_{FS}
A1: OP27 LOWEST NOISE, OP42 BEST BANDWIDTH
*EXTRA PINS OMITTED FOR CLARITY

Figure 18. Inverting Bipolar Analog Input

Calibration of the bipolar analog input circuits (Figures 17 and 18) should begin with zero adjustment first. Apply a +1/2 LSB analog input to A_{IN}, (see Tables II and III) and adjust R_Z until the successive digital output codes flicker between the following codes:

For noninverting, Figure 17	1000 0000 0000
	1000 0000 0001
For inverting, Figure 18	0111 1111 1111
	0111 1111 1110

Next, adjust full scale by applying a FS–3/2 LSB analog input to A_{IN}, (see Tables II and III) and adjust R_{FS} until the successive digital output codes flicker between the following codes:

For Noninverting, Figure 17	1111 1111 1110
	1111 1111 1111
For Inverting, Figure 18	0000 0000 0001
	0000 0000 0000

Table II. Resistor and Potentiometer Values Required for Figure 17

V_{IN} Range V	R3 kΩ	R4 kΩ	R_Z kΩ	R_{FS} kΩ	1/2 LSB mV	FS/2–3/2 LSB V
±2.5	0	40.2	0.5	0.5	0.61	2.49817
±5.0	20.0	19.8	0.5	1.0	1.22	4.99634
±10.0	29.8	10.0	0.5	0.5	2.44	9.99268

Table III. Resistor and Potentiometer Values Required for Figure 18

V_{IN} Range V	R1 kΩ	R2 kΩ	R3 kΩ	R_Z kΩ	R_{FS} kΩ	1/2 LSB mV	FS/2–3/2 LSB V
±2.5	20.0	41.2	40.2	2	1	0.61	2.49817
±5.0	20.0	20.5	20.0	1	1	1.22	4.99634
±10.0	20.0	10.5	10.2	0.5	1	2.44	9.99268

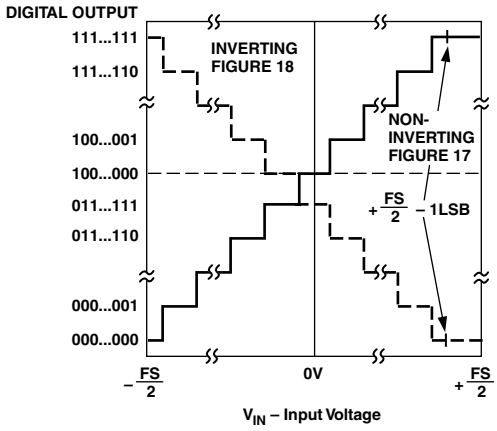


Figure 19. Ideal Input/Output Transfer Characteristics for Bipolar Input Circuits

MICROPROCESSOR INTERFACING

The ADC912A has self-contained logic for both 8-bit and 16-bit data bus interfacing. The output data can be formatted into either a 12-bit parallel word for a 16-bit data bus or an 8-bit data word pair for an 8-bit data bus. Data is always right justified, i.e., LSB is the most right-hand bit in a 16-bit word. For a two-byte read, only data outputs $D_7 \ldots D_{0/8}$ are used. Byte selection is governed by the HBEN input which controls an internal digital multiplexer. This multiplexes the 12 bits of conversion data onto the lower $D_7 \ldots D_{0/8}$ outputs (4 MSBs or 8 LSBs) where it can be read in two read cycles. The 4 MSBs always appear on $D_{11} \ldots D_8$ whenever the three-state output drivers are turned on. See Figure 20.

Two A/D conversion modes of operation are available for both data bus sizes: the ROM mode and the Slow-Memory mode.

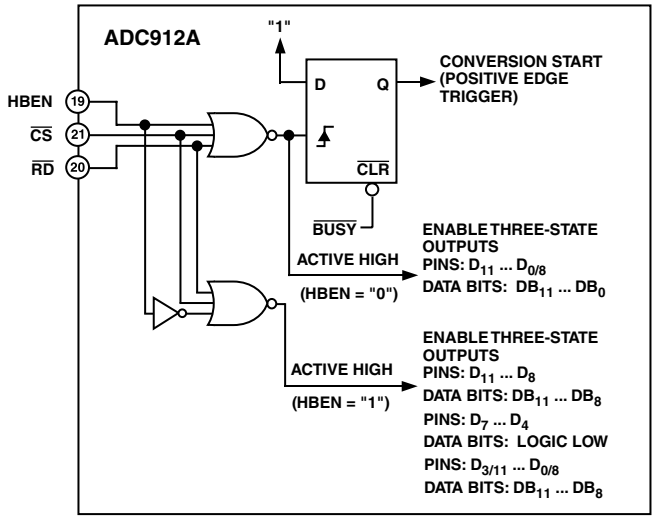


Figure 20. Internal Logic for Control Inputs $\overline{CS}$, $\overline{RD}$, and HBEN

In the ROM mode each READ instruction obtains new, valid data, assuming the minimum timing requirements are satisfied. However, since the data output from a current READ instruction was generated from a conversion initiated by a previous READ operation, the current data may be out-of-date. To be sure of obtaining up-to-date data, READ instructions may be coded in pairs (with some NOPs between them); use only the data from the second READ in each pair. The first READ starts the conversion, the second READ gets the results.

The Slow-Memory mode is the simplest. It is the method of choice where compact coding is essential, or where software bugs are a hazard. In this mode, a single READ instruction will initiate a data conversion, interrupt the microprocessor until completion (WAIT states are introduced), then read the results. If the system throughput tolerates WAIT states, and the hardware is correct, then the Slow-Memory mode is virtually immune to subsequent software modifications. Placing the microprocessor in the WAIT state has an additional advantage of quieting the digital system to reduce noise pickup in the analog conversion circuitry. The 12-bit parallel Slow-Memory mode provides the fastest analog sampling rate combined with digital data transfer rate for sampled-data systems.

PARALLEL READ, SLOW-MEMORY MODE (HBEN = LOW)

Figure 5 shows the timing diagram and data bus status for Parallel Read, Slow-Memory Mode. $\overline{CS}$ and $\overline{RD}$ going low triggers a conversion and the ADC912A acknowledges by taking $\overline{BUSY}$ low. Data from the previous conversion appears on the three-state data outputs. $\overline{BUSY}$ returns high at the end of conversion, when the output latches have been updated, and the conversion result is placed on data outputs $D_{11} \ldots D_{0/8}$.

TWO-BYTE READ, SLOW-MEMORY MODE

For a two-byte read only the eight data outputs $D_7 \ldots D_{0/8}$ are used. Conversion start procedure and data output status for the first read operation is identical to Parallel Read, Slow-Memory Mode. See Figure 6, Timing Diagram and Data Bus Status. At the end of conversion, the low data byte ($DB_7 \ldots DB_0$) is read from the A/D converter. A second READ operation with HBEN high places the high byte on data outputs $D_{3/11} \ldots D_{0/8}$ and disables conversion start. Note the 4 MSBs also appear on data outputs $D_{11} \ldots D_8$ during these two READ operations.

PARALLEL READ, ROM MODE (HBEN = LOW)

A conversion is started with a READ operation. The 12 bits of data from the previous conversion are available on data outputs $D_{11} \ldots D_{0/8}$ (see Figure 7). This data may be disregarded if not required. A second READ operation reads the new data ($DB_{11} \ldots DB_0$) and starts another conversion. A delay at least as long as the ADC912A conversion time must be allowed between READ operations. If a READ takes place prior to the end of 13 CLKS of the ADC conversion, the remaining bits not yet tested will be invalid.

TWO-BYTE READ, ROM MODE

For a two-byte read only the data outputs $D_7 \ldots D_{0/8}$ are used. Conversion is started in the same way with a READ operation and the data output status is the same as the Parallel Read, ROM Mode. See Figure 8, Two-Byte Read Timing Diagram, ROM Mode. Two more READ operations are required to obtain the new conversion result. A delay equal to the ADC912A conversion time must be allowed between conversion start and places the high byte (4 MSBs) on data outputs $D_{3/11} \ldots D_{0/8}$. A third READ operation accesses the low data byte ($DB_7 \ldots DB_0$) and starts another conversion. The 4 MSBs also appear on data outputs $D_{11} \ldots D_8$ during all three read operations above.

CIRCUIT LAYOUT GUIDELINES

As with any high-speed A/D converters, good circuit layout practice is essential. Wire-wrap boards are not recommended due to stray pickup of the high-frequency digital noise. A PC board offers the best results. Digital and analog grounds should be separated even if they are ground planes instead of ground traces. Do not lay digital traces adjacent to high-impedance analog traces. Avoid digital layouts that radiate high-frequency clock signals; i.e., do not lay out digital signal lines and ground returns in the shape of a loop antenna. Shield the analog input if it comes from a different PC board source. Set up a single point ground at AGND (Pin 3) of the ADC912A; tie all other analog grounds to this point. Also tie the logic power supply ground, but no other digital grounds, to this point (see Figure 21). Low impedance analog and digital power supply common returns are essential to low noise operation of the ADC. Their trace widths should be as wide as possible. Good power supply bypass capacitors located near the ADC package ensure quiet operation. Place a 10 µF capacitor in parallel with a 0.01 µF ceramic capacitor across V_{DD} to ground and V_{SS} to ground (near Pin 3).

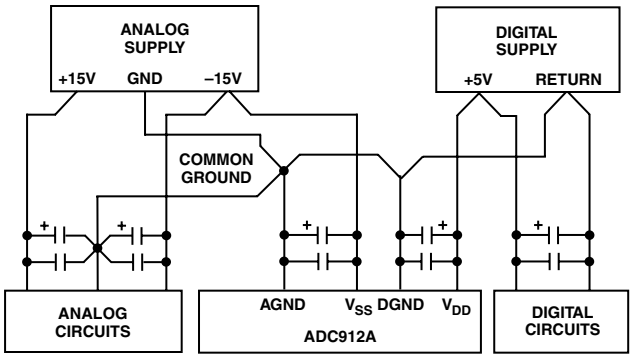


Figure 21. Power Supply Grounding

In applications where the ADC912A data outputs and control signals are connected to a continuously active microprocessor bus, it is possible to get LSB level errors in conversion results. These errors are due to a feedthrough from the microprocessor to the internal comparator. The problem can be minimized by forcing the microprocessor into a WAIT state during conversion (see Slow-Memory microprocessor interfacing). An alternate method is isolation of the data bus with three-state buffers, such as the 74HC541.

INTERFACING TO THE TMS32010 DSP PROCESSOR

Figure 22 shows an ADC912A to TMS32010 interface. The ADC912A is operating in the ROM mode. The interface is designed for the maximum TMS32010 clock frequency of 20 MHz.

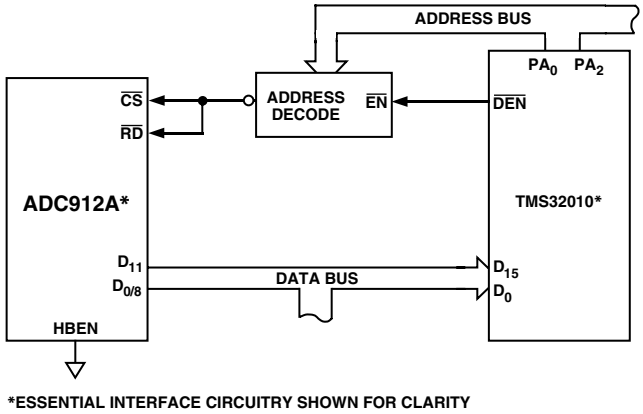


Figure 22. ADC912A to TMS32010 DSP Processor Interface

The ADC912A is mapped at a user-selected port address (PA). The following I/O instruction starts a conversion and reads the previous conversion into the data memory:

IN DATA, PA PA = Port Address

DATA = Data Memory Location

When conversion is complete, a second I/O instruction reads the new data into the data memory and starts another conversion. Sufficient A/D conversion time must be allowed between I/O instructions. The very first data read after system power-up should be discarded.

USING WAIT STATES

The TMS32020 DSP processor has the added capability of WAIT states. This feature simplifies the hardware required for slow memory devices by extending the microprocessor bus access time. Figure 23 shows an ADC912A to TMS32020 interface using one WAIT state to guarantee data interface at the full 20 MHz clock frequency. This WAIT state extends the bus access time by 200 ns. In this circuit the ADC912A operated in the ROM mode where each input instruction (IN DATA, PA) takes the previous conversion result and stores it in memory. The next input instruction must be delayed for the length of the A/D conversion time so that a new conversion result can be read.

SLOW-MEMORY MODE OPERATION USING WAIT STATES

The WAIT state feature of the TMS32020 can also be used to operate the ADC912A in the Slow-Memory mode. This is accomplished by driving the clock input of the 7474 flip-flop in Figure 23, from the BUSY output of the ADC912A, instead of the CLK OUT 1 of the TMS32020. Once a conversion has started the READY input of the TMS32020 is not released until the ADC912A completes its 12-bit A/D conversion. This stops the TMS32020 during the conversion process reducing microprocessor system noise generation. Another advantage for the system software is the single instruction IN MEM, PA used to start, process, and read the results of the A/D conversion. This makes the software code more transportable between systems operating at different clock speeds. The disadvantage is some loss in instruction processing time.

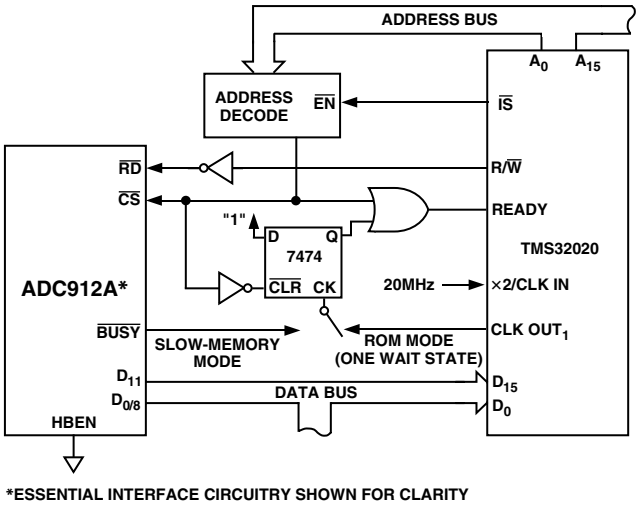
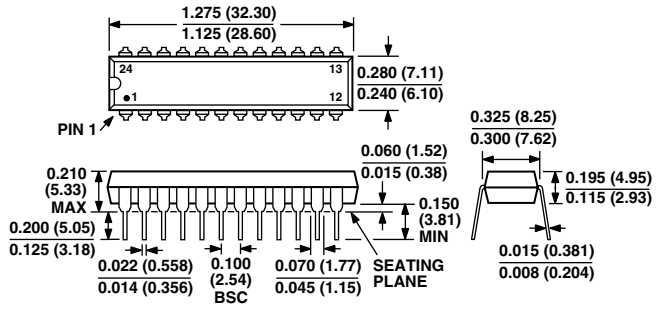


Figure 23. ADC912A to TMS32020 Interface Using Wait States

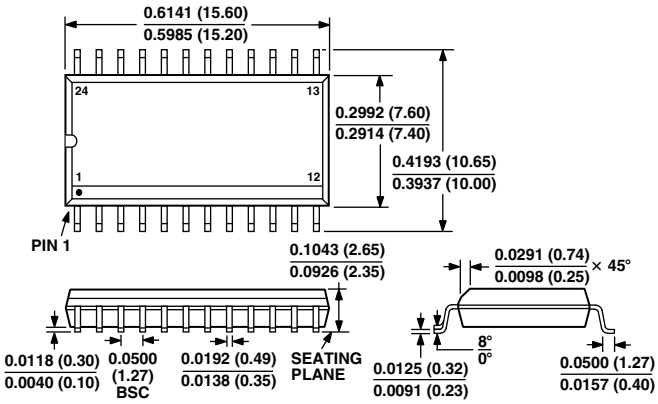
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

24-Lead Narrow Body Plastic DIP Package
(N-24)



24-Lead Wide Body SOIC Package
(R-24)



Revision History–ADC912A

Location	Page
Data Sheet changed from REV. A to REV. B.	
Changes to General Description	1
Changes to Static Accuracy section of Specification page	2
Edits to Timing Characteristics	3
Edits to Absolute Maximum Ratings	4
Changes to Ordering Guide	4

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