TEMIC
Semiconductors

Si9804DY

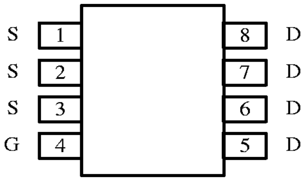
N-Channel Reduced Q_g, Fast Switching MOSFET

Product Summary

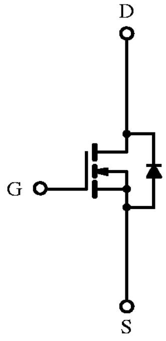
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
25	0.023 @ V_{GS} = 4.5 V	±7.8
	0.030 @ V_{GS} = 3.0 V	±6.8

High-Efficiency
PWM Optimized

SO-8



Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_A = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	25	V
Gate-Source Voltage		V_{GS}	±12	
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	±7.8	A
	T_A = 70°C		±6.2	
Pulsed Drain Current (10 μs Pulse Width)		I_{DM}	±40	
Continuous Source Current (Diode Conduction)[a]		I_S	±2.1	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	2.5	W
	T_A = 70°C		1.6	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	–55 to 150	°C

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient[a]	R_{thJA}	50	°C/W

Notes
a. Surface Mounted on FR4 Board, t ≤ 10 sec.

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Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\ \mu A$	0.6			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 12$ V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 25$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 25$ V, $V_{GS} = 0$ V, $T_J = 55°C$			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 4.5$ V	40			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 7.8$ A		0.018	0.023	Ω
		$V_{GS} = 3.0$ V, $I_D = 6.8$ A		0.022	0.030	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 10$ V, $I_D = 7.8$ A		25		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 2.1$ A, $V_{GS} = 0$ V		0.71	1.2	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 7.8$ A		13.5	20	nC
Gate-Source Charge	Q_{gs}			2.4		
Gate-Drain Charge	Q_{gd}			4.2		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 10\ \Omega$ $I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_G = 6\ \Omega$		16	30	ns
Rise Time	t_r			30	60	
Turn-Off Delay Time	$t_{d(off)}$			46	90	
Fall Time	t_f			18	35	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 2.1$ A, di/dt = 100 A/µs		80	120	

Notes
- a. Guaranteed by design, not subject to production testing.
- b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.

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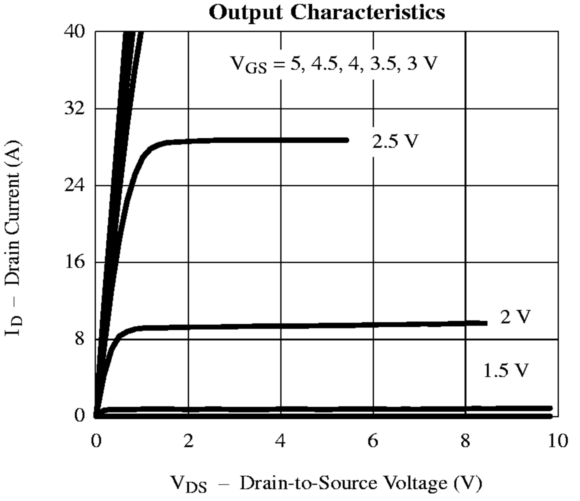
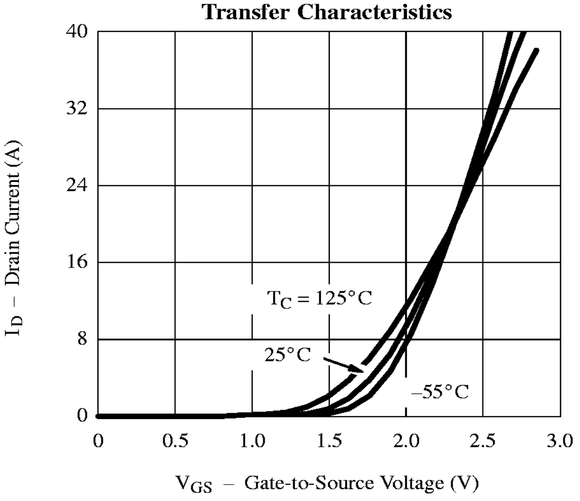
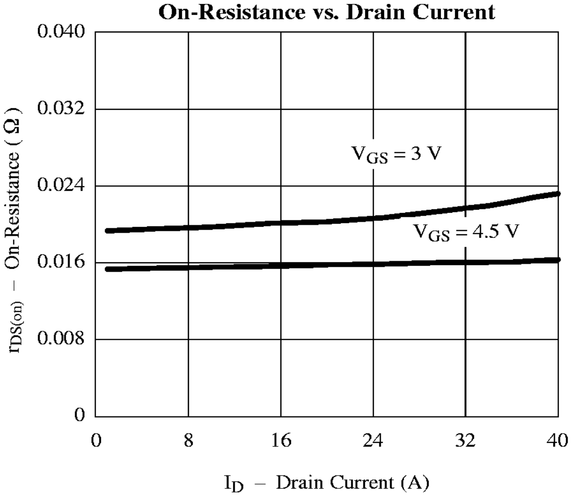
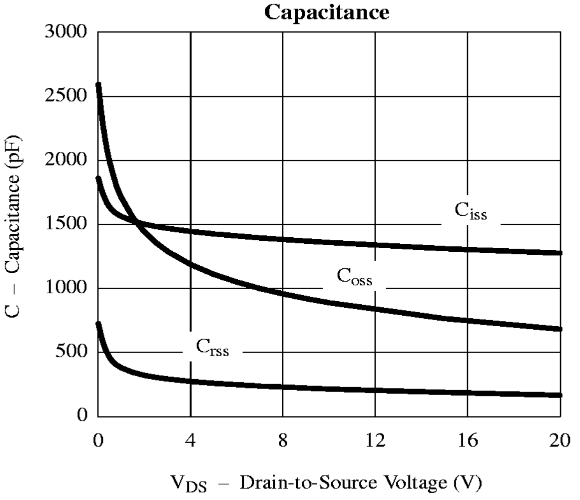
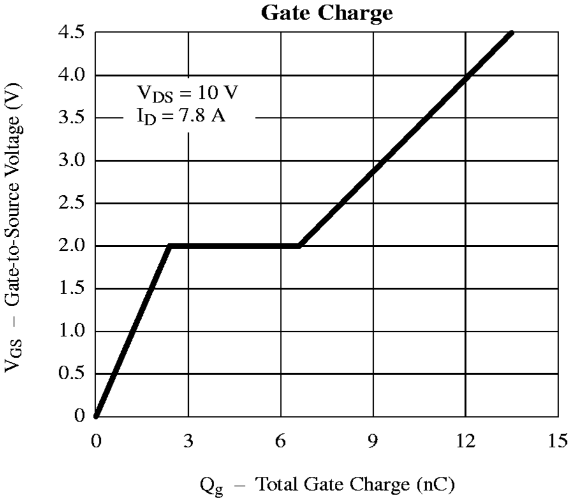
Typical Characteristics (25°C Unless Otherwise Noted)

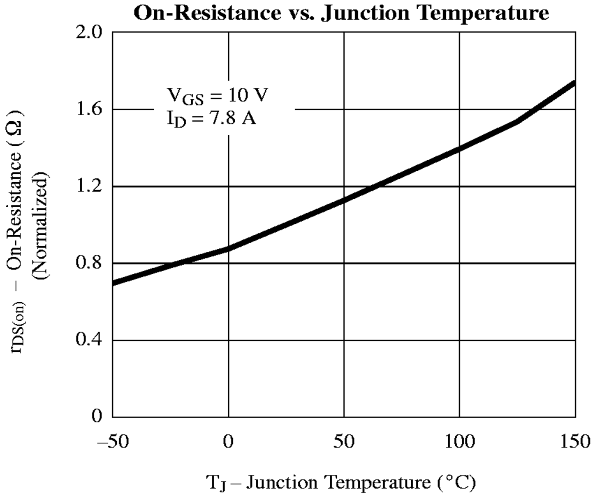












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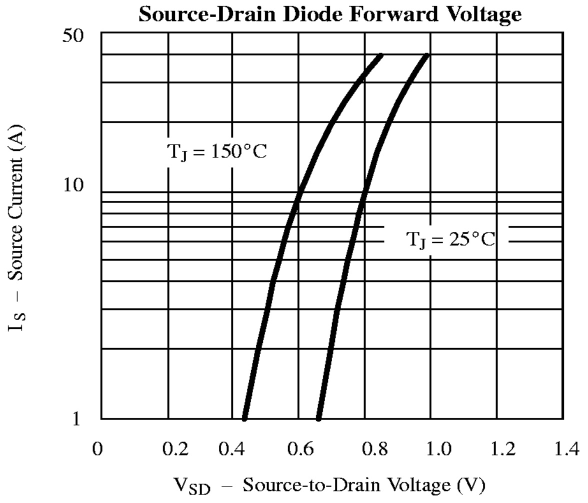
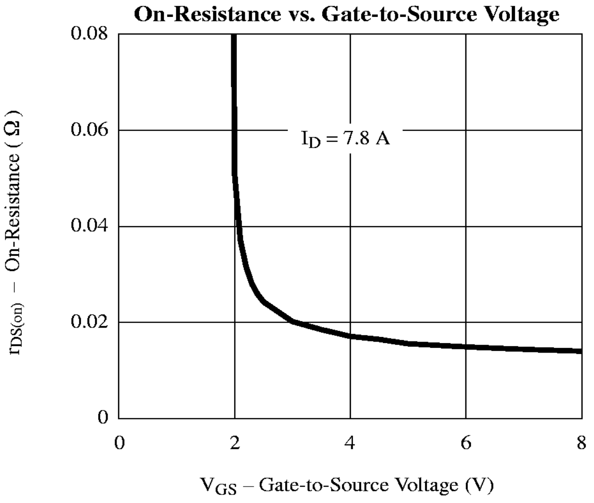
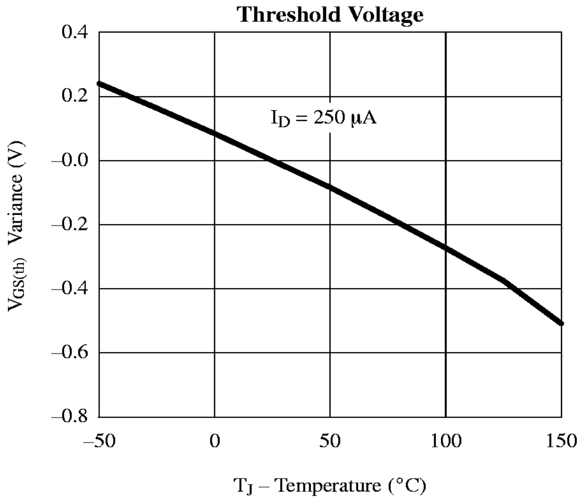
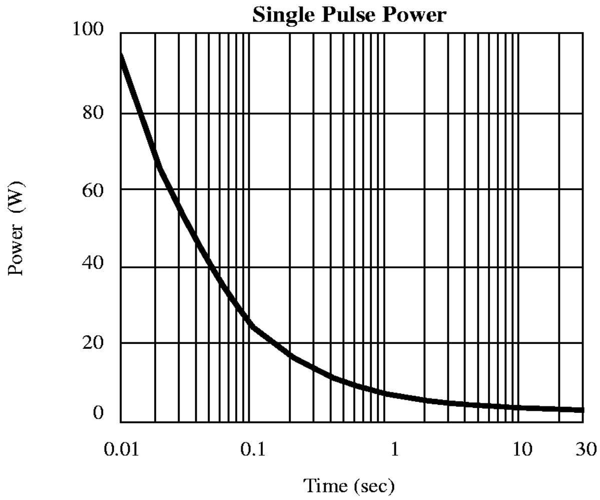
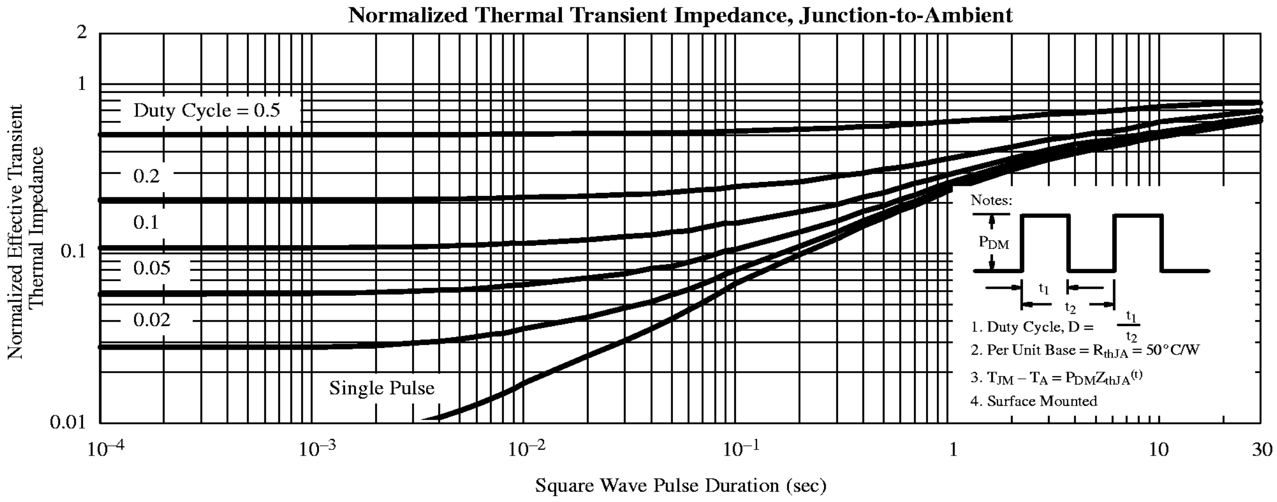
Typical Characteristics (25°C Unless Otherwise Noted)


Source-Drain Diode Forward Voltage


On-Resistance vs. Gate-to-Source Voltage


Threshold Voltage


Single Pulse Power


Normalized Thermal Transient Impedance, Junction-to-Ambient

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