19-3028; Rev 1; 2/04

MAXIM

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

General Description

The MAX1123 is a monolithic 10-bit, 210Msps analog-to-digital converter (ADC) optimized for outstanding dynamic performance at high IF frequencies up to 500MHz. The product operates with conversion rates of up to 210Msps while consuming only 460mW.

At 210Msps and an input frequency of 100MHz, the MAX1123 achieves a spurious-free dynamic range (SFDR) of 74.5dBc. Its excellent signal-to-noise ratio (SNR) of 57.4dB at 10MHz remains flat (within 1.5dB) for input tones up to 500MHz. This makes the MAX1123 ideal for wideband applications such as digital predistortion in cellular base-station transceiver systems.

The MAX1123 requires a single 1.8V supply. The analog input is designed for either differential or single-ended operation and can be AC- or DC-coupled. The ADC also features a selectable on-chip divide-by-2 clock circuit, which allows the user to apply clock frequencies as high as 420MHz. This helps to reduce the phase noise of the input clock source. A differential LVDS sampling clock is recommended for best performance. The converter's digital outputs are LVDS compatible, and the data format can be selected to be either two's complement or offset binary.

The MAX1123 is available in a 68-pin QFN with exposed paddle (EP) and is specified over the industrial (-40°C to +85°C) temperature range.

For pin-compatible, lower and higher speed versions of the MAX1123, refer to the MAX1122 (170Msps) and the MAX1124 (250Msps) data sheets. For a higher speed, pin-compatible 8-bit version of the MAX1123, refer to the MAX1121 data sheet.

Applications

Wireless and Wired Broadband Communication

Cable-Head End Systems

Digital Predistortion Receivers

Communications Test Equipment

Radar and Satellite Subsystems Antenna Array Processing

Features

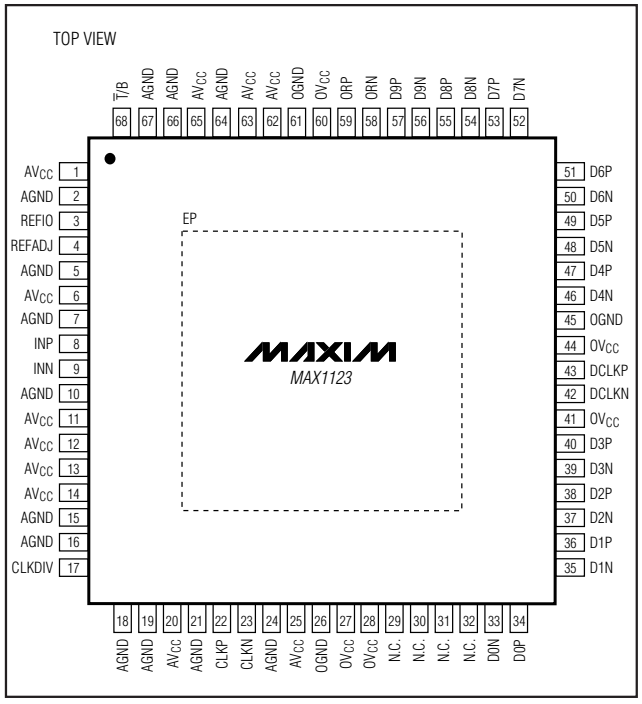
- **210Msps Conversion Rate**
- **SNR = 57.4dB/56dB at f_{IN} = 100MHz/500MHz**
- **SFDR = 74.5dBc/62.6dBc at f_{IN} = 100MHz/500MHz**
- **NPR = 53.6dB at f_{NOTCH} = 28.8MHz**
- **Single 1.8V Supply**
- **460mW Power Dissipation at 210Msps**
- **On-Chip Track-and-Hold and Internal Reference**
- **On-Chip Selectable Divide-by-2 Clock Input**
- **LVDS Digital Outputs with Data Clock Output**
- **Evaluation Kit Available (Order MAX1124EVKIT)**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX1123EGK	-40°C to +85°C	68 QFN-EP*

**EP = Exposed paddle.*

Pin Configuration



1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

ABSOLUTE MAXIMUM RATINGS

AV_{CC} to AGND .....-0.3V to +2.1V
OV_{CC} to OGND .....-0.3V to +2.1V
AGND to OGND .....-0.3V to +0.3V
Analog Inputs to AGND .....-0.3V to (AV_{CC} + 0.3V)
Digital Inputs to AGND.....-0.3V to (AV_{CC} + 0.3V)
REF, REFADJ to AGND.....-0.3V to (AV_{CC} + 0.3V)
Digital Outputs to OGND.....-0.3V to (OV_{CC} + 0.3V)
ESD on All Pins (Human Body Model).....±2000V

Continuous Power Dissipation (T_A = +70°C)
68-Pin QFN (derate 41.7mW/°C above +70°C) 3333mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-60°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Maximum Current into Any Pin.....50mA

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210MHz, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω ±1%, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥25°C guaranteed by production test, <25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC ACCURACY							
Resolution				10			Bits
Integral Nonlinearity	INL	(Note 1)		-2	±0.4	+2	LSB
Differential Nonlinearity	DNL	No missing codes (Note 1)		-1.0	±0.3	+1.5	LSB
Transfer Curve Offset	V_{OS}	(Note 1)	T_A ≥ +25°C	-25		+25	LSB
			(Note 2)	-37		+37	
Offset Temperature Drift					±20		µV/°C
ANALOG INPUTS (INP, INN)							
Full-Scale Input Voltage Range	V_{FS}	(Note 1)		1100	1250	1375	mV_{P-P}
Full-Scale Range Temperature Drift					130		ppm/°C
Common-Mode Input Range	V_{CM}				1.38 ±0.18		V
Input Capacitance	C_{IN}				3		pF
Differential Input Resistance	R_{IN}			3.00	4.3	6.25	kΩ
Full-Power Analog Bandwidth	FPBW	Figure 8			600		MHz
REFERENCE (REFIO, REFADJ)							
Reference Output Voltage	V_{REFIO}			1.18	1.24	1.30	V
Reference Temperature Drift					90		ppm/°C
REFADJ Input High Voltage	V_{REFADJ}	Used to disable the internal reference		AV_{CC} - 0.3			V
SAMPLING CHARACTERISTICS							
Maximum Sampling Rate	f_{SAMPLE}			210			MHz
Minimum Sampling Rate	f_{SAMPLE}				20		MHz

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210MHz, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω ±1%, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥25°C guaranteed by production test, <25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Duty Cycle		Set by clock management circuit		40 to 60		%
Aperture Delay	t_{AD}			350		ps
Aperture Jitter	t_{AJ}			0.21		ps_{RMS}
CLOCK INPUTS (CLKP, CLKN)						
Differential Clock Input Amplitude		(Note 2)	200	500		mV_{P-P}
Clock Input Common-Mode Voltage Range				1.15 ±0.2		V
Clock Differential Input Resistance	R_{CLK}			11 ± 25%		kΩ
Clock Differential Input Capacitance	C_{CLK}			5		pF
DYNAMIC CHARACTERISTICS (at -0.5dBFS)						
Signal-to-Noise Ratio	SNR	f_{IN} = 10MHz, T_A ≥ +25°C	56	57.5		dB
		f_{IN} = 100MHz, T_A ≥ +25°C	55.5	57.1		
		f_{IN} = 180MHz		57		
		f_{IN} = 500MHz		56		
Signal-to-Noise and Distortion	SINAD	f_{IN} = 10MHz, T_A ≥ +25°C	55.5	57.4		dB
		f_{IN} = 100MHz, T_A ≥ +25°C	55	57		
		f_{IN} = 180MHz		56.5		
		f_{IN} = 500MHz		55		
Spurious-Free Dynamic Range	SFDR	f_{IN} = 10MHz, T_A ≥ +25°C	63	77		dBc
		f_{IN} = 100MHz, T_A ≥ +25°C	61	72		
		f_{IN} = 180MHz		66.3		
		f_{IN} = 500MHz		62.5		
Worst Harmonics (HD2 or HD3)		f_{IN} = 10MHz		-77		dBc
		f_{IN} = 100MHz		-72		
		f_{IN} = 180MHz		-66.3		
		f_{IN} = 500MHz		-62.5		
Two-Tone Intermodulation Distortion	IMD_{100}	f_{IN1} = 99MHz at -7dBFS, f_{IN2} = 101MHz at -7dBFS		-75		dBc
	IMD_{500}	f_{IN1} = 498.5MHz at -7dBFS, f_{IN2} = 502.5MHz at -7dBFS		-58		
LVDS DIGITAL OUTPUTS (D0P/N–D9P/N, DCLKP/N)						
Differential Output Voltage	$\|V_{OD}\|$		250		400	mV

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

ELECTRICAL CHARACTERISTICS (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210MHz, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω ±1%, C_L = 5pF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. ≥25°C guaranteed by production test, <25°C guaranteed by design and characterization. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Offset Voltage	OV_{OS}		1.125		1.310	V
LVCMOS DIGITAL INPUTS (CLKDIV, $\overline{T}$/B)						
Digital Input Voltage Low	V_{IL}				0.2 x AV_{CC}	V
Digital Input Voltage High	V_{IH}		0.8 x AV_{CC}			V
TIMING CHARACTERISTICS						
CLK to Data Propagation Delay	t_{PDL}	Figure 4		1.5		ns
CLK to DCLK Propagation Delay	t_{CPDL}	Figure 4		3.01		ns
Data Valid to DCLK Rising Edge	t_{CPDL} - t_{PDL}	Figure 4 (Note 2)	1.23	1.51	1.84	ns
LVDS Output Rise-Time	t_{RISE}	20% to 80%, C_L = 5pF		460		ps
LVDS Output Fall-Time	t_{FALL}	20% to 80%, C_L = 5pF		460		ps
Output Data Pipeline Delay	$t_{LATENCY}$			8		Clock cycles
POWER REQUIREMENTS						
Analog Supply Voltage Range	AV_{CC}		1.7	1.8	1.9	V
Digital Supply Voltage Range	OV_{CC}		1.7	1.8	1.9	V
Analog Supply	I_{AVCC}	f_{IN} = 100MHz		210	280	mA
Digital Supply Current	I_{OVCC}	f_{IN} = 100MHz		45	75	mA
Analog Power Dissipation	P_{DISS}	f_{IN} = 100MHz		460	640	mW
Power-Supply Rejection Ratio (Note 3)	PSRR	Offset		1.6		mV/V
		Gain		1.9		%FS/V

Note 1: Static linearity and offset parameters are computed from a best-fit straight line through the code transition points. The full-scale range is defined as 1023 x slope of the line.

Note 2: Parameter guaranteed by design and characterization; T_A = T_{MIN} to T_{MAX}.

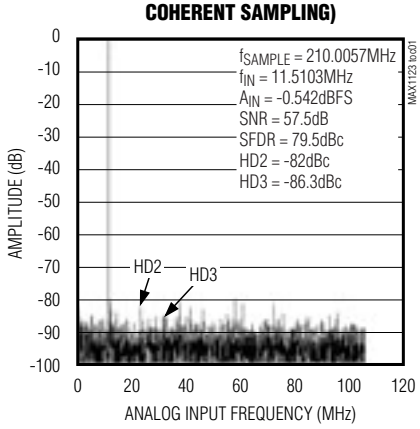
Note 3: PSRR is measured with both analog and digital supplies connected to the same potential.

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

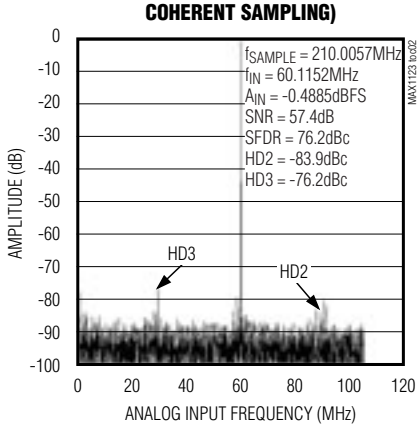
Typical Operating Characteristics

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210.0057MHz, -0.5dBFS; see TOCs for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

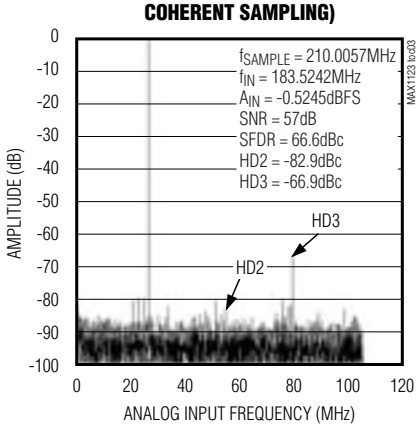
FFT PLOT (8192-POINT DATA RECORD, COHERENT SAMPLING)



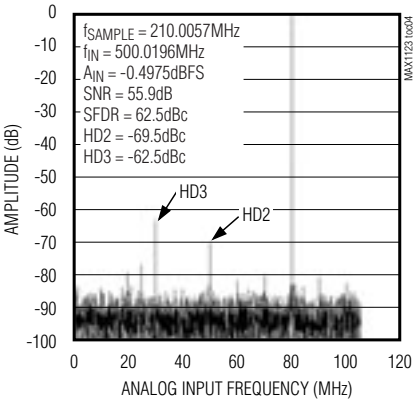
FFT PLOT (8192-POINT DATA RECORD, COHERENT SAMPLING)



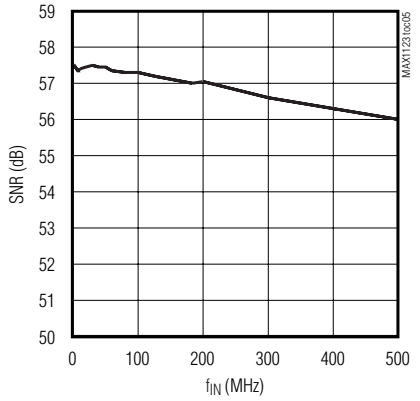
FFT PLOT (8192-POINT DATA RECORD, COHERENT SAMPLING)



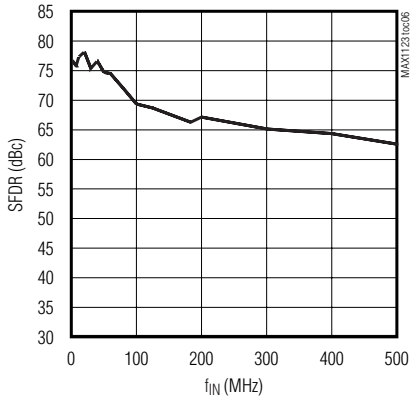
FFT PLOT (8192-POINT DATA RECORD, COHERENT SAMPLING)



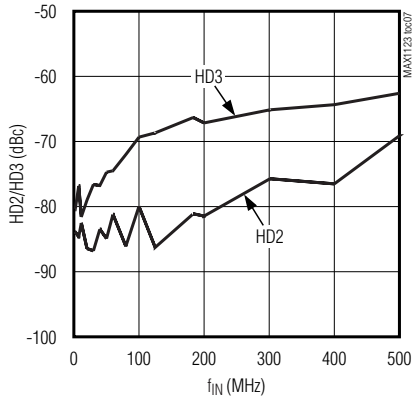
SNR vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 210.0057MHz, A_{IN} = -0.5dBFS)



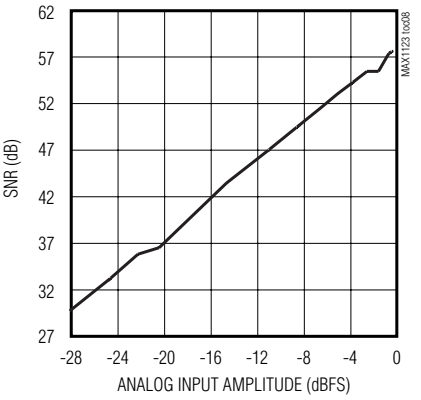
SFDR vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 210.0057MHz, A_{IN} = -0.5dBFS)



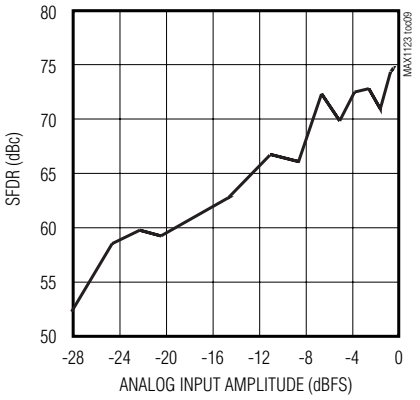
HD2/HD3 vs. ANALOG INPUT FREQUENCY (f_{SAMPLE} = 210.0057MHz, A_{IN} = -0.5dBFS)



SNR vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 210.0057MHz, f_{IN} = 60.0126MHz)



SFDR vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 210.0057MHz, f_{IN} = 60.0126MHz)

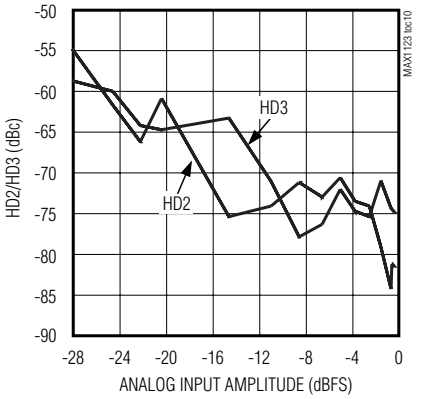


1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

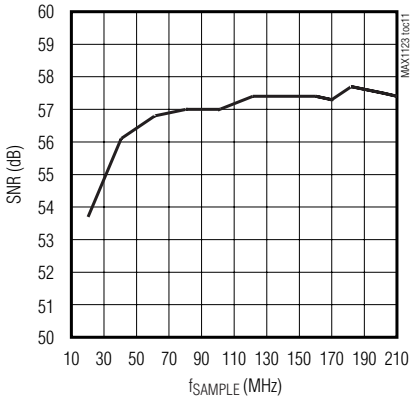
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210.0057MHz, -0.5dBFS; see TOCs for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

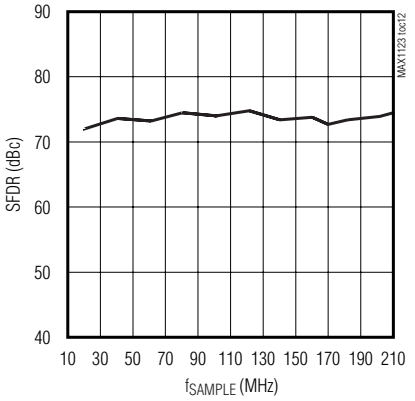
HD2/HD3 vs. ANALOG INPUT AMPLITUDE (f_{SAMPLE} = 210.0057MHz, f_{IN} = 60.0126MHz)



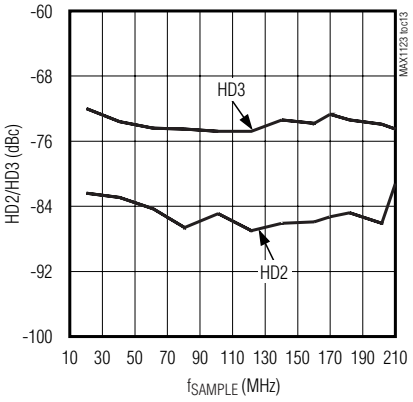
SNR vs. f_{SAMPLE} (f_{IN} = 60.0126MHz, A_{IN} = -0.5dBFS)



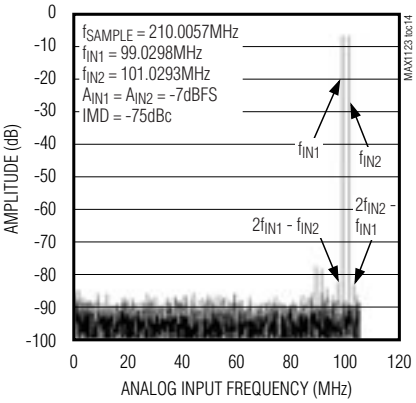
SFDR vs. f_{SAMPLE} (f_{IN} = 60.0126MHz, A_{IN} = -0.5dBFS)



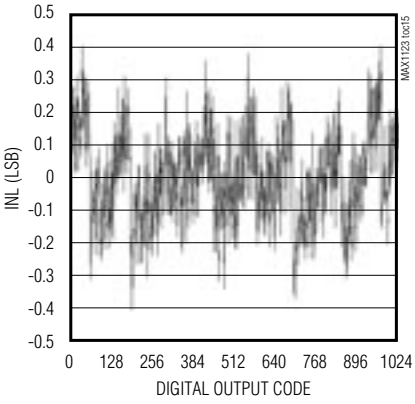
HD2/HD3 vs. f_{SAMPLE} (f_{IN} = 60.0126MHz, A_{IN} = -0.5dBFS)



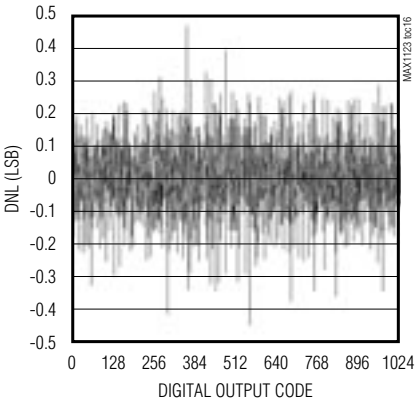
TWO-TONE IMD PLOT (8192-POINT DATA RECORD, COHERENT SAMPLING)



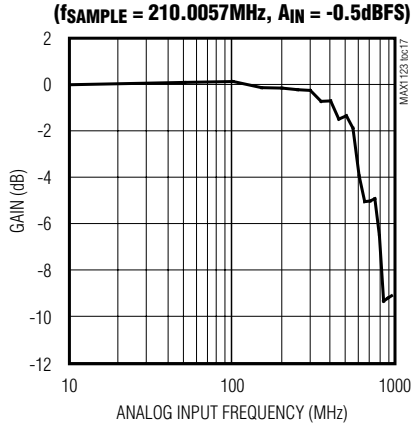
INTEGRAL NONLINEARITY vs. DIGITAL OUTPUT CODE



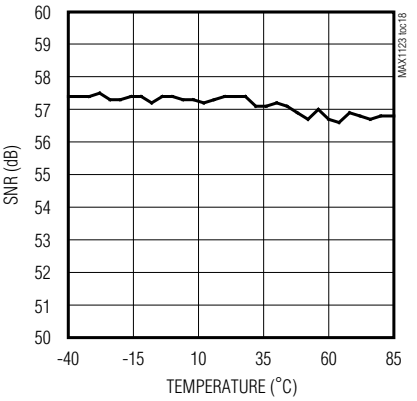
DIFFERENTIAL NONLINEARITY vs. DIGITAL OUTPUT CODE



GAIN BANDWIDTH PLOT (f_{SAMPLE} = 210.0057MHz, A_{IN} = -0.5dBFS)



SNR vs. TEMPERATURE (f_{IN} = 64.9974MHz, f_{SAMPLE} = 210.0428MHz, A_{IN} = -0.5dBFS)

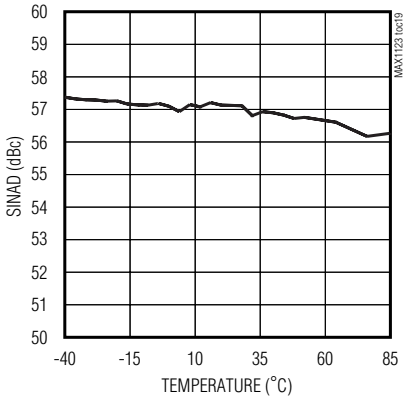


1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

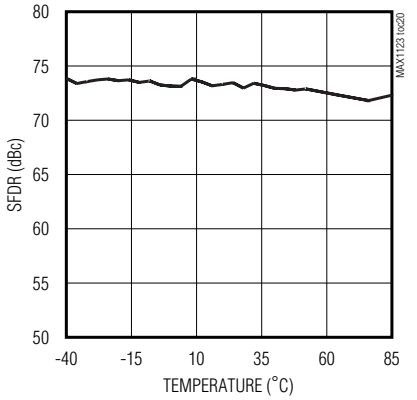
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210.0057MHz, -0.5dBFS; see TOCs for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

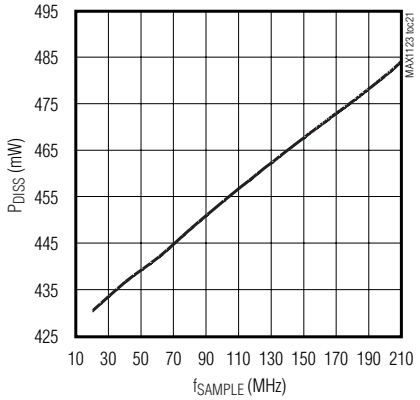
SINAD vs. TEMPERATURE (f_{IN} = 64.9974MHz, f_{SAMPLE} = 210.0428MHz, A_{IN} = -0.5dBFS)



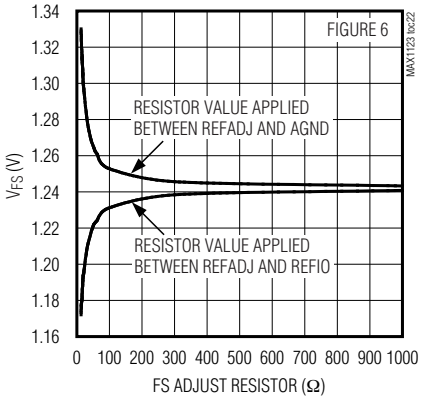
SFDR vs. TEMPERATURE (f_{IN} = 64.9974MHz, f_{SAMPLE} = 210.0428MHz, A_{IN} = -0.5dBFS)



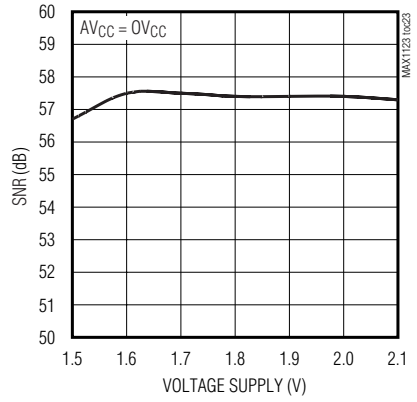
POWER DISSIPATION vs. f_{SAMPLE} (f_{IN} = 60.0126MHz, A_{IN} = -0.5dBFS)



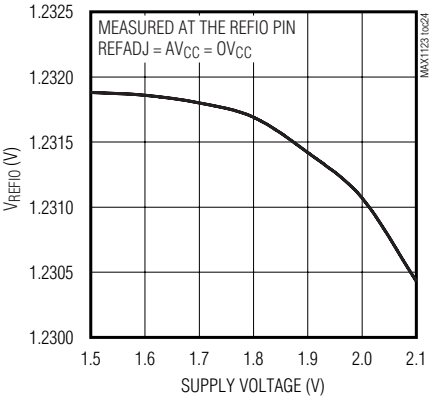
FS VOLTAGE vs. FS ADJUST RESISTOR



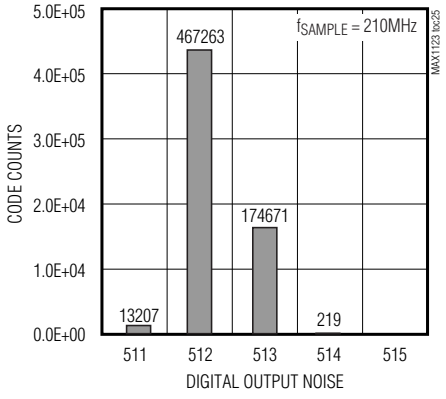
SNR vs. VOLTAGE SUPPLY (f_{IN} = 60.0126MHz, A_{IN} = -0.5dBFS)



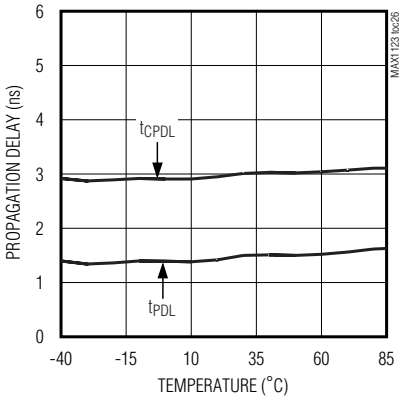
INTERNAL REFERENCE vs. SUPPLY VOLTAGE (f_{SAMPLE} = 210.0057MHz)



NOISE HISTOGRAM (DC INPUT, 256k-POINT DATA RECORD)



PROPAGATION DELAY TIMES vs. TEMPERATURE

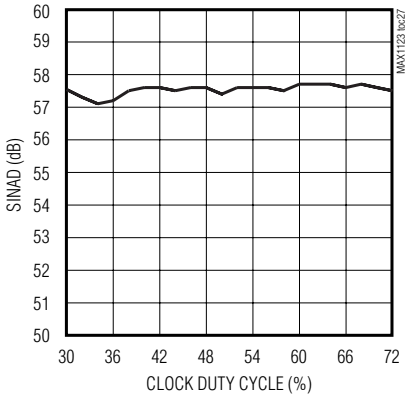


1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

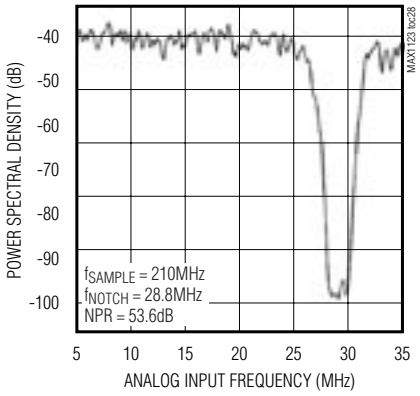
Typical Operating Characteristics (continued)

(AV_{CC} = OV_{CC} = 1.8V, AGND = OGND = 0, f_{SAMPLE} = 210.0057MHz, -0.5dBFS; see TOCs for detailed information on test conditions, differential input drive, differential sine-wave clock input drive, 0.1µF capacitor on REFIO, internal reference, digital output pins differential R_L = 100Ω, T_A = +25°C.)

SINAD vs. CLOCK DUTY CYCLE (f_{IN} = 1.4106MHz, f_{SAMPLE} = 210.0428MHz, A_{IN} = -0.5dBFS)



NOISE POWER RATIO PLOT



Pin Description

PIN	NAME	FUNCTION
1, 6, 11–14, 20, 25, 62, 63, 65	AV_{CC}	Analog Supply Voltage. Bypass each pin with a 0.1µF capacitor for best decoupling results.
2, 5, 7, 10, 15, 16, 18, 19, 21, 24, 64, 66, 67, EP	AGND	Analog Converter Ground. Connect the converter's exposed paddle (EP) to AGND.
3	REFIO	Reference Input/Output. With REFADJ pulled high through a 1kΩ resistor, this I/O port allows an external reference source to be connected to the MAX1123. With REFADJ pulled low through the same 1kΩ resistor, the internal 1.23V bandgap reference is active.
4	REFADJ	Reference-Adjust Input. REFADJ allows for full-scale range adjustments by placing a resistor or trim potentiometer between REFADJ and AGND (decreases FS range) or REFADJ and REFIO (increases FS range). If REFADJ is connected to AV_{CC} through a 1kΩ resistor, the internal reference can be overdriven with an external source connected to REFIO. If REFADJ is connected to AGND through a 1kΩ resistor, the internal reference is used to determine the full-scale range of the data converter.
8	INP	Positive Analog Input Terminal
9	INN	Negative Analog Input Terminal
17	CLKDIV	Clock Divider Input. This LVCMOS-compatible input controls which speed the converter's digital outputs are updated. CLKDIV has an internal pulldown resistor. CLKDIV = 0: ADC updates digital outputs at one-half the input clock rate. CLKDIV = 1: ADC updates digital outputs at the input clock rate.
22	CLKP	True Clock Input. This input requires an LVDS-compatible input level to maintain the converter's excellent performance.
23	CLKN	Complementary Clock Input. This input requires an LVDS-compatible input level to maintain the converter's excellent performance.

Pin Description (continued)

PIN	NAME	FUNCTION
26, 45, 61	OGND	Digital Converter Ground. Ground connection for digital circuitry and output drivers.
27, 28, 41, 44, 60	OV_{CC}	Digital Supply Voltage. Bypass with a 0.1µF capacitor for best decoupling results.
29–32	N.C.	No Connection. Do not connect to these pins.
33	D0N	Complementary Output Bit 0 (LSB)
34	D0P	True Output Bit 0 (LSB)
35	D1N	Complementary Output Bit 1
36	D1P	True Output Bit 1
37	D2N	Complementary Output Bit 2
38	D2P	True Output Bit 2
39	D3N	Complementary Output Bit 3
40	D3P	True Output Bit 3
42	DCLKN	Complementary Clock Output. This output provides an LVDS-compatible output level and can be used to synchronize external devices to the converter clock. There is a 2.1ns delay between CLKP and DCLKP.
43	DCLKP	True Clock Output. This output provides an LVDS-compatible output level and can be used to synchronize external devices to the converter clock. There is a 2.1ns delay between CLKN and DCLKN.
46	D4N	Complementary Output Bit 4
47	D4P	True Output Bit 4
48	D5N	Complementary Output Bit 5
49	D5P	True Output Bit 5
50	D6N	Complementary Output Bit 6
51	D6P	True Output Bit 6
52	D7N	Complementary Output Bit 7
53	D7P	True Output Bit 7
54	D8N	Complementary Output Bit 8
55	D8P	True Output Bit 8
56	D9N	Complementary Output Bit 9 (MSB)
57	D9P	True Output Bit 9 (MSB)
58	ORN	Complementary Output for Out-of-Range Control Bit. If an out-of-range condition is detected, bit ORN flags this condition by transitioning low.
59	ORP	True Output for Out-of-Range Control Bit. If an out-of-range condition is detected, bit ORP flags this condition by transitioning high.
68	$\overline{T}$/B	Two's Complement or Binary Output Format Selection. This LVCMOS-compatible input controls the digital output format of the MAX1123. $\overline{T}$/B has an internal pulldown resistor. $\overline{T}$/B = 0: Two's complement output format $\overline{T}$/B = 1: Binary output format

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

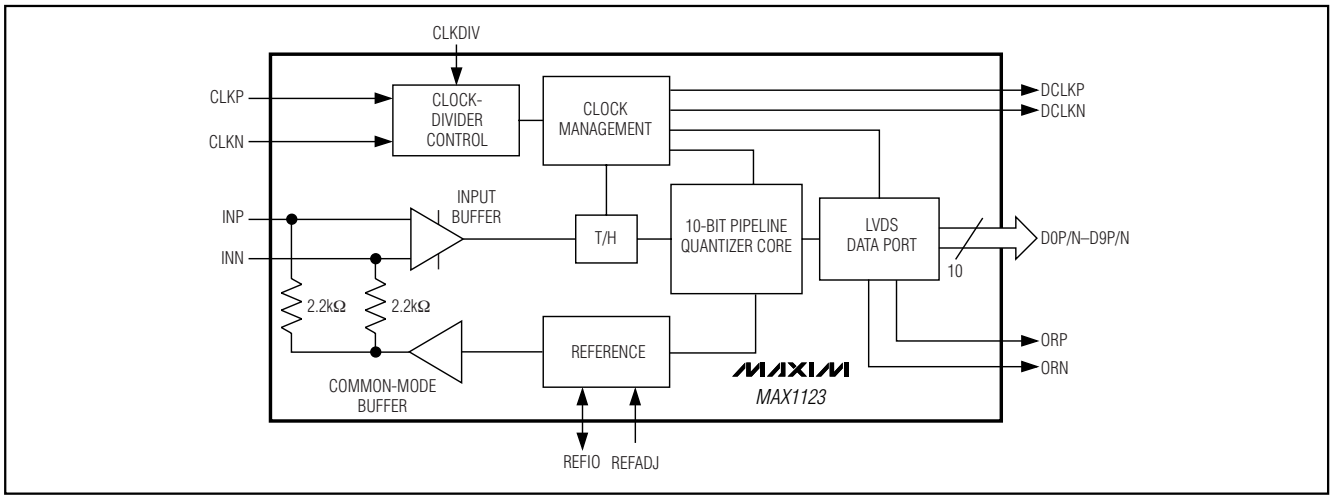


Figure 1. MAX1123 Block Diagram

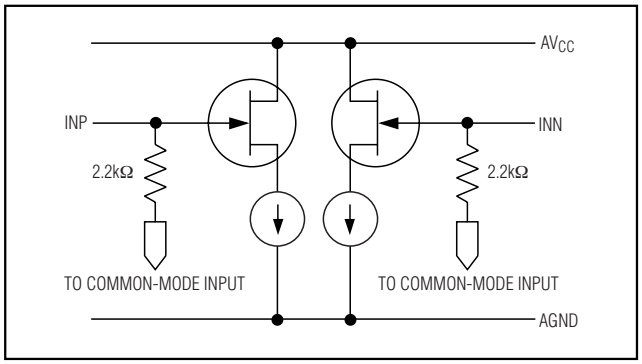


Figure 2. Simplified Analog Input Architecture

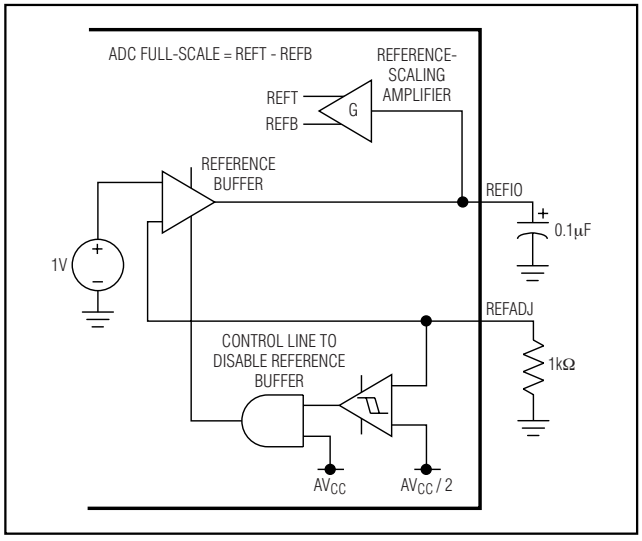


Figure 3. Simplified Reference Architecture

Detailed Description—Theory of Operation

The MAX1123 uses a fully differential, pipelined architecture that allows for high-speed conversion, optimized accuracy and linearity, while minimizing power consumption and die size.

Both positive (INP) and negative/complementary analog input terminals (INN) are centered around a common-mode voltage of 1.4V, and accept a differential analog input voltage swing of ±0.3125V each, resulting in a typical differential full-scale signal swing of $1.25V_{P-P}$.

INP and INN are buffered prior to entering each track-and-hold (T/H) stage and are sampled when the differential sampling clock signal transitions high. A 2-bit ADC following the first T/H stage then digitizes the signal, and controls a 2-bit digital-to-analog converter (DAC). Digitized and reference signals are then subtracted, resulting in a fractional residue signal that is amplified before it is passed on to the next stage through another T/H amplifier. This process is repeated until the applied input signal has successfully passed through all stages of the 10-bit quantizer. Finally, the digital outputs of all stages are combined and corrected for in the digital correction logic to generate the final output code. The result is a 10-bit parallel digital output word in user-selectable two's complement or binary output formats with LVDS-compatible output levels. See Figure 1 for a more detailed view of the MAX1123 architecture.

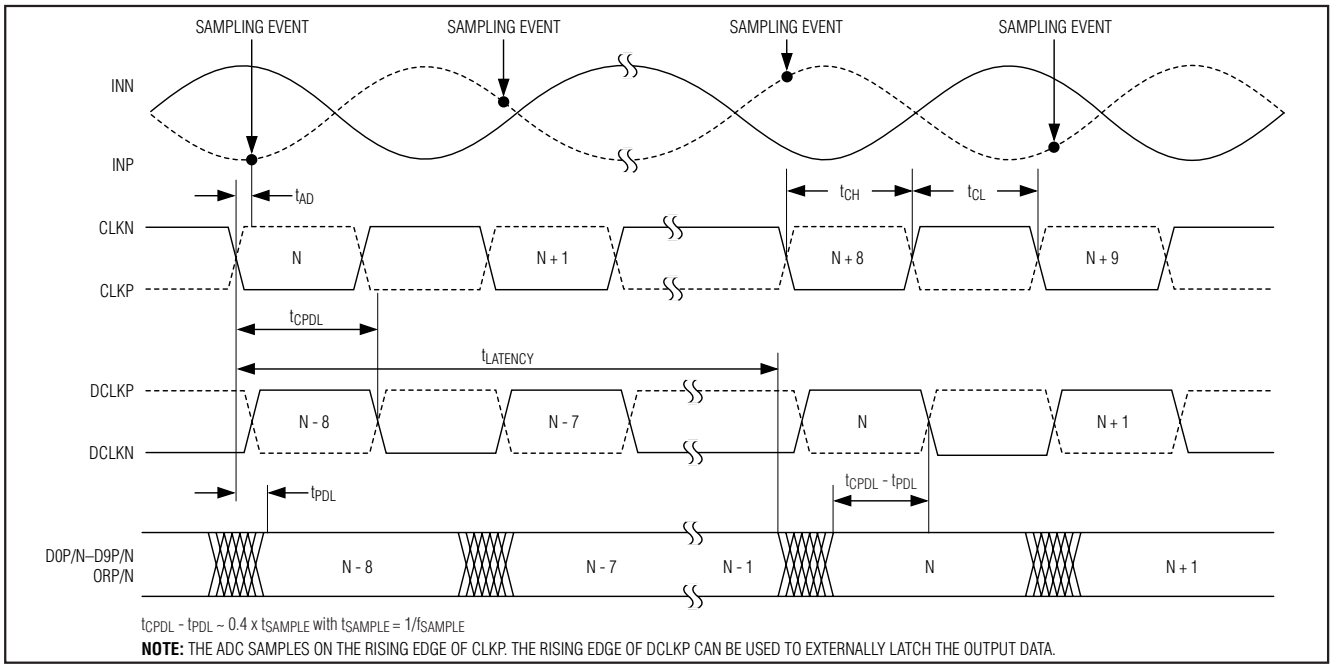


Figure 4. System and Output Timing Diagram

Analog Inputs (INP, INN)

INP and INN are the fully differential inputs of the MAX1123. Differential inputs usually feature good rejection of even-order harmonics, which allows for enhanced AC performance as the signals are progressing through the analog stages. The MAX1123 analog inputs are self-biased at a common-mode voltage of 1.4V and allow a differential input voltage swing of $1.25V_{P-P}$. Both inputs are self-biased through 2.2kΩ resistors, resulting in a typical differential input resistance of 4.4kΩ. It is recommended to drive the analog inputs of the MAX1123 in AC-coupled configuration to achieve best dynamic performance. See the *AC-Coupled Analog Inputs* section for a detailed discussion of this configuration.

On-Chip Reference Circuit

The MAX1123 features an internal 1.23V bandgap reference circuit (Figure 3), which, in combination with an internal reference-scaling amplifier, determines the full-scale range of the MAX1123. Bypass REFIO with a 0.1µF capacitor to AGND. To compensate for gain errors or increase the ADC's full-scale range, the voltage of this bandgap reference can be indirectly adjusted by adding an external resistor (e.g., 100kΩ trim potentiometer) between REFADJ and AGND or REFADJ and REFIO. See the *Applications Information* section for a detailed description of this process.

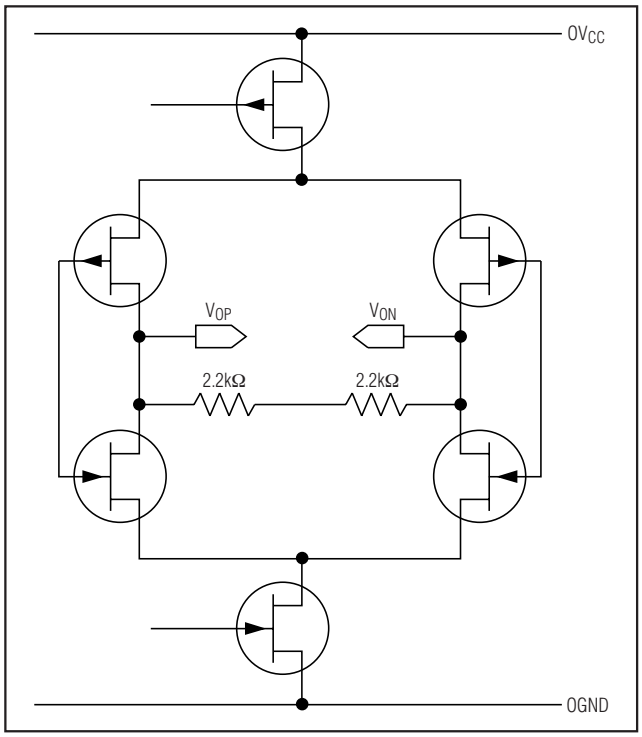


Figure 5. Simplified LVDS Output Architecture

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

Table 1. MAX1123 Digital Output Coding

INP ANALOG VOLTAGE LEVEL	INN ANALOG VOLTAGE LEVEL	OUT-OF-RANGE ORP (ORN)	BINARY DIGITAL OUTPUT CODE (D9–D0)	TWO'S COMPLEMENT DIGITAL OUTPUT CODE (D9–D0)
> V_{CM} + 0.3125V	< V_{CM} - 0.3125V	1 (0)	11 1111 1111 (exceeds positive full scale, OR set)	01 1111 1111 (exceeds positive full scale, OR set)
V_{CM} + 0.3125V	V_{CM} - 0.3125V	0 (1)	11 1111 1111 (represents positive full scale)	01 1111 1111 (represents positive full scale)
V_{CM}	V_{CM}	0 (1)	10 0000 0000 or 01 1111 1111 (represents midscale)	00 0000 0000 or 11 1111 1111 (represents midscale)
V_{CM} - 0.3125V	V_{CM} + 0.3125V	0 (1)	00 0000 0000 (represents negative full scale)	10 0000 0000 (represents negative full scale)
< V_{CM} - 0.3125V	> V_{CM} + 0.3125V	1 (0)	00 0000 0000 (exceeds negative full scale, OR set)	10 0000 0000 (exceeds negative full scale, OR set)

Clock Inputs (CLKP, CLKN)

Designed for a differential LVDS clock input drive, it is recommended to drive the clock inputs of the MAX1123 with an LVDS-compatible clock to achieve the best dynamic performance. The clock signal source must be a high-quality, low phase noise to avoid any degradation in the noise performance of the ADC. The clock inputs (CLKP, CLKN) are internally biased to 1.2V, accept a differential signal swing of $0.2V_{P-P}$ to $1.0V_{P-P}$ and are usually driven in AC-coupled configuration. See the *Differential, AC-Coupled Clock Input* in the *Applications Information* section for more circuit details on how to drive CLKP and CLKN appropriately. Although not recommended, the clock inputs also accept a single-ended input signal.

The MAX1123 also features an internal clock management circuit (duty-cycle equalizer) that ensures that the clock signal applied to inputs CLKP and CLKN is processed to provide a 50% duty cycle clock signal, which desensitizes the performance of the converter to variations in the duty cycle of the input clock source. Note that the clock duty-cycle equalizer cannot be turned off externally and requires a minimum clock frequency of >20MHz to work appropriately and according to data sheet specifications.

Clock Outputs (DCLKP, DCLKN)

The MAX1123 features a differential clock output, which can be used to latch the digital output data with an external latch or receiver. Additionally, the clock output can be used to synchronize external devices (e.g., FPGAs) to the ADC. DCLKP and DCLKN are differential outputs with LVDS-compatible voltage levels. There is a 2.1ns delay time between the rising (falling) edge of CLKP (CLKN) and the rising edge of DCLKP (DCLKN). See Figure 4 for timing details.

Divide-by-2 Clock Control (CLKDIV)

The MAX1123 offers a clock control line (CLKDIV), which supports the reduction of clock jitter in a system. Connect CLKDIV to OGND to enable the ADC's internal divide-by-2 clock divider. Data is now updated at one-half the ADC's input clock rate. CLKDIV has an internal pulldown resistor and can be left open for applications that only operate with update rates one-half of the converter's sampling rate. Connecting CLKDIV to OV_{CC} allows data to be updated at the speed of the ADC input clock.

System Timing Requirements

Figure 4 depicts the relationship between the clock input and output, analog input, sampling event, and data output. The MAX1123 samples on the rising (falling) edge of CLKP (CLKN). Output data is valid on the next rising (falling) edge of the DCLKP (DCLKN) clock, but has an internal latency of eight clock cycles.

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

Digital Outputs (D0P/N–D9P/N, DCLKP/N, ORP/N) and Control Input T/B

The digital outputs D0P/N–D9P/N, DCLKP/N, and ORP/N are LVDS compatible, and data on D0P/N–D9P/N is presented in either binary or two's complement format (Table 1). The T/B control line is an LVCMOS-compatible input, which allows the user to select the desired output format. Pulling T/B low outputs data in two's complement and pulling it high presents data in offset binary format on the 10-bit parallel bus. T/B has an internal pulldown resistor and may be left unconnected in applications using only two's complement output format. All LVDS outputs provide a typical voltage swing of 0.4V around a common-mode voltage of approximately 1.2V, and must be terminated at the far end of each transmission line pair (true and complementary) with 100Ω. The LVDS outputs are powered from a separate power supply, which can be operated between 1.7V and 1.9V.

The MAX1123 offers an additional differential output pair (ORP, ORN) to flag out-of-range conditions, where out of range is above positive or below negative full scale. An out-of-range condition is identified with ORP (ORN) transitioning high (low).

Note: Although differential LVDS reduces single-ended transients to the supply and ground planes, capacitive loading on the digital outputs should still be kept as low as possible. Using LVDS buffers on the digital outputs of the ADC when driving off-board may improve overall performance and reduce system timing constraints.

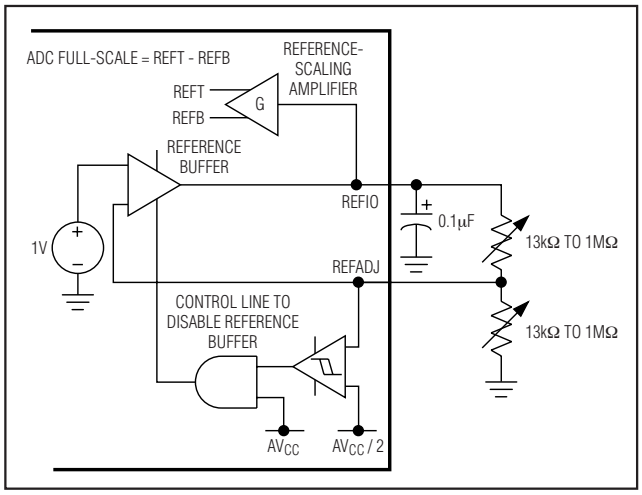


Figure 6. Circuit Suggestions to Adjust the ADC's Full-Scale Range

Applications Information

Full-Scale Range Adjustments Using the Internal Bandgap Reference

The MAX1123 supports a full-scale adjustment range of 10% (±5%). To decrease the full-scale range, an external resistor value ranging from 13kΩ to 1MΩ may be added between REFADJ and AGND. A similar approach can be taken to increase the ADCs full-scale range. Adding a variable resistor, potentiometer, or

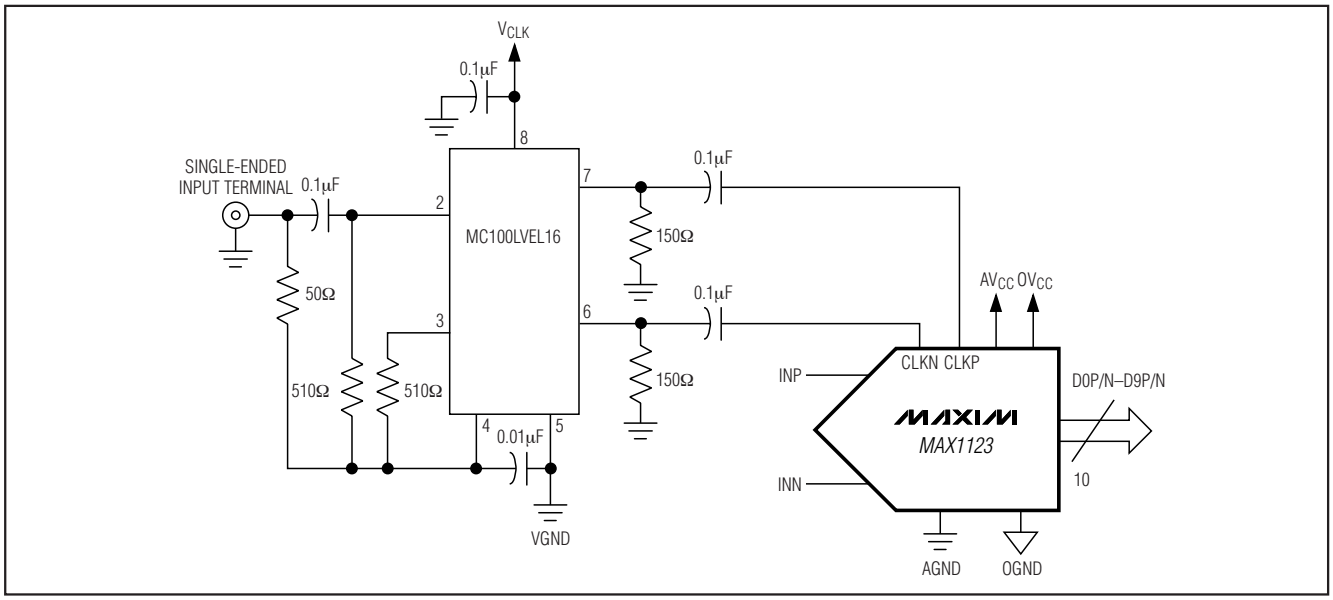


Figure 7. Differential, AC-Coupled, PECL-Compatible Clock Input Configuration

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

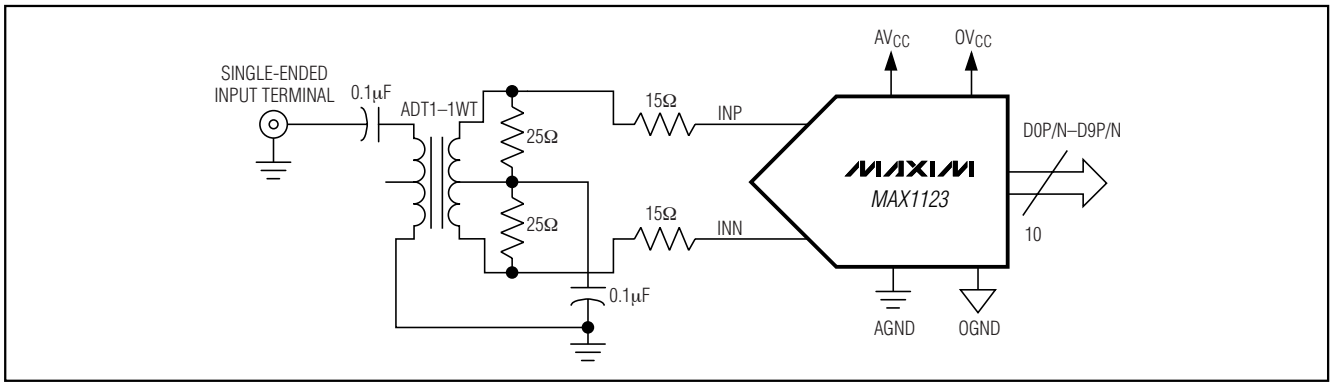


Figure 8. Transformer-Coupled Analog Input Configuration with Secondary-Side Termination

predetermined resistor value between REFADJ and REFIO increases the full-scale range of the data converter. Figure 6 shows the two possible configurations and their impact on the overall full-scale range adjustment of the MAX1123. Do not use resistor values of less than 13kΩ to avoid instability of the internal gain regulation loop for the bandgap reference.

Differential, AC-Coupled, PECL-Compatible Clock Input

The preferred method of clocking the MAX1123 is differentially with LVDS- or PECL-compatible input levels. To accomplish this, a 50Ω reverse-terminated clock signal source with low phase noise is AC-coupled into a fast differential receiver such as the MC100LVEL16 (Figure 7). The receiver produces the necessary PECL output levels to drive the clock inputs of the data converter.

Differential, AC-Coupled Analog Input

An RF transformer provides an excellent solution to convert a single-ended source signal to a fully differential signal, required by the MAX1123 for optimum dynamic performance. In general, the MAX1123 provides the best SFDR and THD with fully differential input signals and it is not recommended to drive the ADC inputs in single-ended configuration. In differential input mode, even-order harmonics are usually lower since INP and INN are balanced, and each of the ADC inputs only requires half the signal swing compared to a single-ended configuration.

Figure 8 depicts a secondary-side termination of the 1:1 transformer into two separate 25Ω loads. Terminating the transformer in this fashion reduces the potential effects of transformer parasitics. The source impedance combined with the shunt capacitance provided by a PC board and the ADC's parasitic capacitance reduce the combined bandwidth to approximately 550MHz.

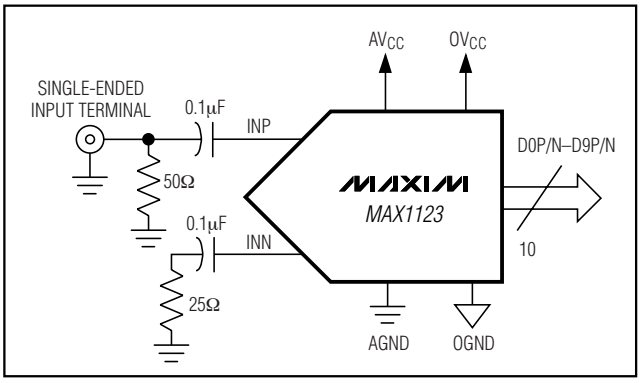


Figure 9. Single-Ended AC-Coupled Analog Input Configuration

Single-Ended, AC-Coupled Analog Input

Although not recommended, the MAX1123 can be used in single-ended mode (Figure 9). Analog signals can be AC-coupled to the positive input INP through a 0.1µF capacitor and terminated with a 50Ω resistor to AGND. The negative input should be 25Ω reverse-terminated and AC grounded with a 0.1µF capacitor.

Grounding, Bypassing, and Board Layout Considerations

The MAX1123 requires board layout design techniques suitable for high-speed data converters. This ADC provides separate analog and digital power supplies. The analog and digital supply voltage pins accept input voltage ranges of 1.7V to 1.9V. Although both supply types can be combined and supplied from one source, it is recommended to use separate sources to cut down on performance degradation caused by digital switching currents, which can couple into the analog supply network. Isolate analog and digital supplies (AV_{CC} and

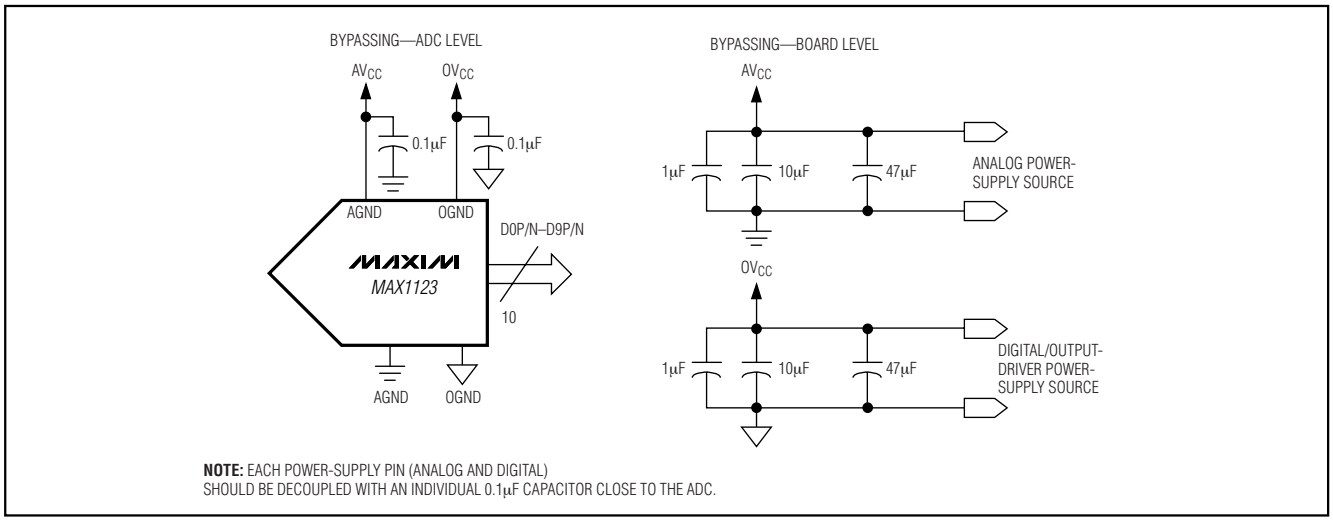


Figure 10. Grounding, Bypassing, and Decoupling Recommendations for the MAX1123

OV_{CC}) where they enter the PC board with separate networks of ferrite beads and capacitors to their corresponding grounds (AGND, OGND).

To achieve optimum performance, provide each supply with a separate network of a 47µF tantalum capacitor in parallel with 10µF and 1µF ceramic capacitors. Additionally, the ADC requires each supply pin to be bypassed with separate 0.1µF ceramic capacitors (Figure 10). Locate these capacitors directly at the ADC supply pins or as close as possible to the MAX1123. Choose surface-mount capacitors, which are preferably located on the same side as the converter, to save space and minimize the inductance.

Multilayer boards with separated ground and power planes produce the highest level of signal integrity. Consider the use of a split ground plane arranged to match the physical location of analog and digital ground on the ADC's package. The two ground planes should be joined at a single point so the noisy digital ground currents do not interfere with the analog ground plane. A major concern with this approach are the dynamic currents that may need to travel long distances before they are recombined at a common source ground, resulting in large and undesirable ground loops. Ground loops can add to digital noise by coupling back to the analog front end of the converter, resulting in increased spur activity and a decreased noise performance.

Alternatively, all ground pins could share the same ground plane, if the ground plane is sufficiently isolated from any noisy, digital systems ground. To minimize the effects of digital noise coupling, ground return vias can be positioned throughout the layout to divert digital switching currents away from the sensitive analog sections of the ADC. This does not require additional ground splitting, but can be accomplished by placing substantial ground connections between the analog front end and the digital outputs.

The MAX1123 is packaged in a 68-pin QFN-EP package (package code: G6800-4), providing greater design flexibility, increased thermal efficiency, and optimized AC performance of the ADC. **The EP must be soldered down to AGND.**

In this package, the data converter die is attached to an EP lead frame with the back of this frame exposed at the package bottom surface, facing the PC board side of the package. This allows a solid attachment of the package to the PC board with standard infrared (IR) flow soldering techniques.

Note that thermal efficiency is not the key factor, since the MAX1123 features low-power operation. The exposed pad is the key element to ensure a solid ground connection between the DAC and the PC board's analog ground layer.

Considerable care must be taken, when routing the digital output traces for a high-speed, high-resolution data converter. It is essential to keep trace lengths at a minimum and place minimal capacitive loading—less than 5pF—on any digital trace to prevent coupling to sensitive analog sections of the ADC. It is recommended to run the LVDS output traces as differential lines with 100Ω characteristic impedance from the ADC to the LVDS load device.

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

Static Parameter Definitions

Integral Nonlinearity (INL)

Integral nonlinearity is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best straight-line fit or a line drawn between the end points of the transfer function, once offset and gain errors have been nullified. However, the static linearity parameters for the MAX1123 are measured using the histogram method with an input frequency of 10MHz.

Differential Nonlinearly (DNL)

Differential nonlinearity is the difference between an actual step width and the ideal value of 1 LSB. A DNL error specification of less than 1 LSB guarantees no missing codes and a monotonic transfer function. The MAX1123's DNL specification is measured with the histogram method based on a 10MHz input tone.

Dynamic Parameter Definitions

Aperture Jitter

Figure 11 depicts the aperture jitter (t_{AJ}), which is the sample-to-sample variation in the aperture delay.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of the sampling clock and the instant when an actual sample is taken (Figure 11).

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of the full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{dB[max]} = 6.02_{dB} \times N + 1.76_{dB}$$

In reality, other noise sources such as thermal noise, clock jitter, signal phase noise, and transfer function nonlinearities are also contributing to the SNR calculation and should be considered when determining the SNR in ADC.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is computed by taking the ratio of the RMS signal to all spectral components excluding the fundamental and the DC offset. In case of the MAX1123, SINAD is computed from a curve fit.

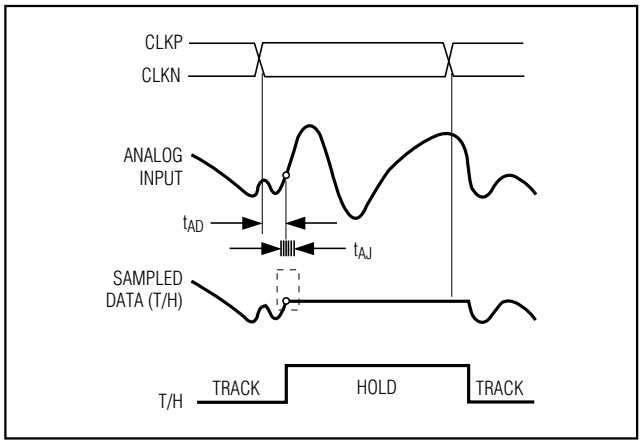


Figure 11. Aperture Jitter/Delay Specifications

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the carrier frequency (maximum signal component) to the RMS value of the next-largest noise or harmonic distortion component. SFDR is usually measured in dBc with respect to the carrier frequency amplitude or in dBFS with respect to the ADC's full-scale range.

Two-Tone Intermodulation Distortion (IMD)

The two-tone IMD is the ratio expressed in decibels of either input tone to the worst 3rd-order (or higher) intermodulation products. The individual input tone levels are at -7dB full scale.

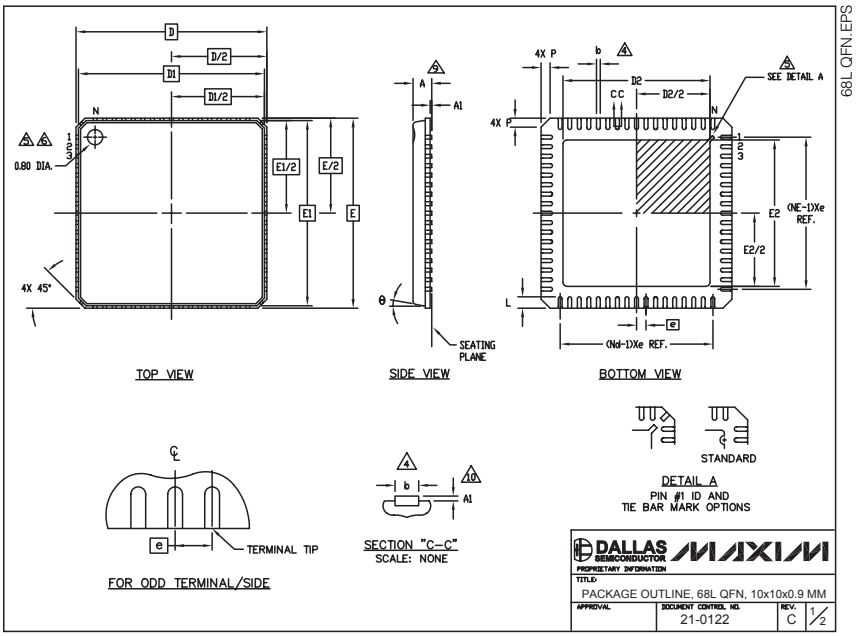
Pin-Compatible Higher Speed/ Lower Resolution Versions

PART	RESOLUTION (Bits)	SPEED GRADE (Msps)
MAX1122	10	170
MAX1124	10	250
MAX1121	8	250

1.8V, 10-Bit, 210Msps Analog-to-Digital Converter with LVDS Outputs for Wideband Applications

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



SYMBOL	COMMON DIMENSIONS			NOTE
	MIN.	NOM.	MAX.	
A	–	0.90	1.00	
A1	0.00	0.01	0.05	11
b	0.18	0.23	0.30	4
D		10.00 BSC		
D1		9.75 BSC		
e		0.50 BSC		
E		10.00 BSC		
E1		9.75 BSC		
L	0.50	0.60	0.65	
N		68		3
Nd		17		3
Ne		17		3
θ	0		12°	
P	0	0.42	0.60	

1. DIE THICKNESS ALLOWABLE IS .012 INCHES MAXIMUM.
2. DIMENSIONING & TOLERANCES CONFORM TO ASME Y14.5M. – 1994.
3. N IS THE NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X-DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y-DIRECTION.
4. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20 AND 0.25mm FROM TERMINAL TIP.
5. THE PIN #1 IDENTIFIER MUST BE LOCATED ON THE TOP SURFACE OF THE PACKAGE BY USING INDENTATION MARK OR OTHER FEATURE OF PACKAGE BODY. DETAILS OF PIN #1 IDENTIFIER IS OPTIONAL, BUT MUST BE LOCATED WITHIN ZONE INDICATED.
6. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
7. ALL DIMENSIONS ARE IN MILLIMETERS.
8. PACKAGE WARPAGE MAX 0.10mm.
9. APPLIES TO EXPOSED SURFACE OF PADS AND TERMINALS
10. APPLIES ONLY TO TERMINALS.
11. MEETS JEDEC MO-220.

EXPOSED PAD VARIATIONS						
	D2			E2		
PKG CODE	MIN	NOM	MAX	MIN	NOM	MAX
G6800-2	7.55	7.70	7.85	7.55	7.70	7.85
G6800-4	5.65	5.80	5.95	5.65	5.80	5.95

DALLAS SEMICONDUCTOR
PROPRIETARY INFORMATION
MAXIM
TITLE:
PACKAGE OUTLINE, 68L QFN, 10x10x0.9 MM
APPROVAL
DOCUMENT CONTROL NO.
21-0122
REV.
C
1/2