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*Microprocessor and Memory
Technologies Group*

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Product Brief

Integrated Portable System Processor: DragonBall™

Focusing on system prerequisites, the M68328 addresses the rigorous demands of the emerging portable digital assistant (PDA) market. The high-level of smart on-chip integration minimizes system complexity and reduces the number of components, resulting in compact implementations, low power consumption, and, most importantly, delivers cost-efficient system performance.

Bundled in a 144-pin thin plastic package, the M68328 (known as DragonBall™) is powered by Motorola's M68EC000 HCMOS static core (Figure 1). Combine this processor with the many well-established M68K tool sets, and the DragonBall is positioned for rapid deployment.

Low power consumption was a key design consideration of the M68328, typically drawing 20 milliamps when clocked at 16MHz. Power dissipation can be regulated dynamically by controlling the internal processor frequency without altering the processor status. Operation at 125KHz will typically draw 1 milliamp. In addition, a sleep mode can power down active circuits in the processor, halting instruction execution, and reducing power to less than 20 microamps. The M68328 is well-suited for extended-life battery-powered applications for uncompromising performance.

The M68328 is the only integrated member of the 68K Family to accommodate an LCD controller, thus eliminating the need for dedicated display memory and providing handwriting-recognition functionality. In addition, the M68328 provides key functionality that is applicable across many applications. Modules such as real-time clock (RTC), pulse-width modulation (PWM), timers, master/slave serial peripheral interface (SPI), universal asynchronous receiver transmitter (UART), and the system integration module (SIM28) provide more flexibility and resources to help engineers design efficient and innovative products.

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

■■■■■■■■■■ **SEMICONDUCTOR PRODUCT INFORMATION** ■■■■■■■■■■

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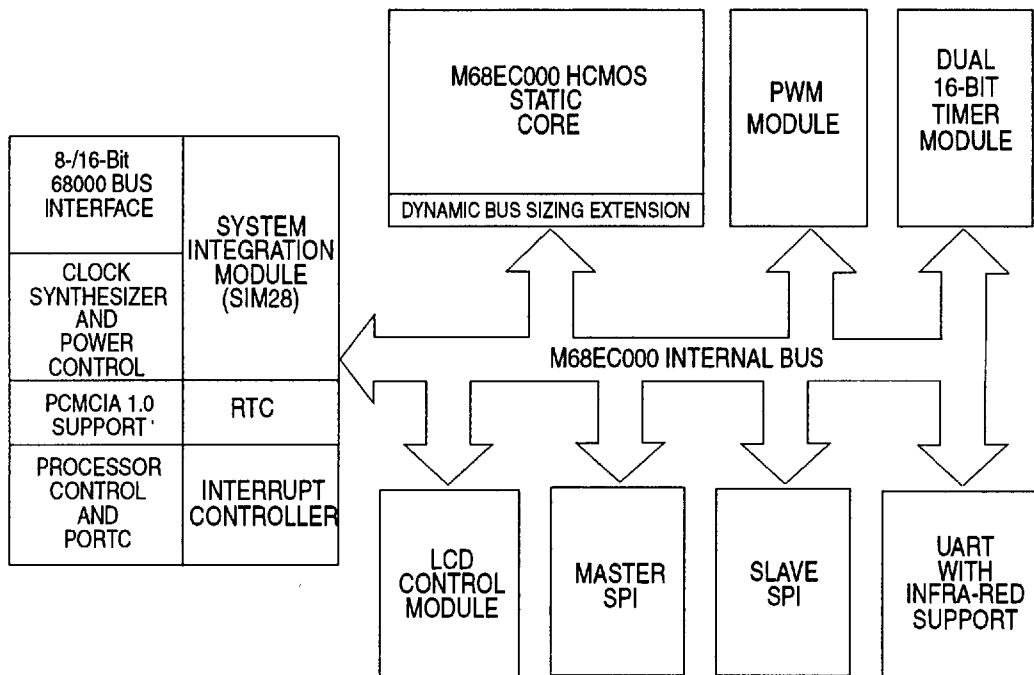


Figure 1. M68328 Block Diagram

KEY FEATURES

The primary features of the M68328 are as follows:

- M68EC000 Static Core Processor
 - 100% Compatibility With M68000 and M68EC000 Processors
 - 32-Bit External and Internal Address Bus Capable of 4G Bytes of Address Space
 - 16-Bit On-Chip Data Bus for M68000 Bus Operations
 - Static Design Allows Processor Clock to be Stopped Providing Dramatic Power Savings\
- External Interface with Dynamic Bus Sizing for 8-Bit and 16-Bit Data Ports
- System Integration Module (SIM28), Incorporating Functions Relegated to External Array Logic
 - System Configuration, Programmable Address Mapping
 - Glueless Interface to SRAM, EPROM, FLASH Memory
 - 16 Programmable Peripheral Chip Selects with Wait-State Generation Logic
 - Interrupt Controller with 13 Flexible Inputs
 - Programmable Interrupt Vector Response for On-Chip Peripheral Modules
 - Hardware Watchdog Timer
 - Software Watchdog Timer
 - Low-Power Controls for Operation
 - Up to 76-Bit Individually Programmable Parallel I/O Ports
 - PCMCIA 1.0 Support

- UART
 - Supports IrDA-Compliant Physical Layer Protocol
 - 8-Byte FIFOs on Rx and Tx
- Two Separated Serial Peripheral Interface Ports (Master and Slave)
 - Support for External POCSAG Decoder (Slave)
 - Support for Digitizer from A/D Input or EEPROM (Master)
- Dual Channel 16-Bit General Purpose Counter/timer
 - Multimode Operation, Independent Capture/Compare Registers
 - Automatic Interrupt Generation
 - 240ns Resolution At 16-MHz System Clock
 - Each Timer Has an Input and an Output Pin for Capture and Compare
- Pulse-Width Modulation Output for Sound Generation
 - Programmable Frame Rate
 - 16-Bit programmable
 - Supports Motor Control
- Real-Time Clock
 - 24-Hour Time
 - 1 Programmable Alarm
- Power Management
 - 3.3-V Operation
 - a. 20 milliamps When Clock Operates at 16 MHz (Full)
 - b. 1 milliamp When Clock Operates at 125KHz (Doze)
 - c. 20 microamps in Low Power Stop (Sleep)
 - Fully Static HCMOS Technology
 - Programmable Clock Synthesizer for Full Frequency Control
 - Low Power Stop Capabilities
 - Modules can be Individually Shut down
 - Lowest Power Mode Control (Shut Down CPU and Peripherals)
- LCD Control Module
 - Software-Programmable Screen Size to Support Single (Non-Split) Monochrome/ STN Panels
 - Capable of Direct Driving Common LCD Drivers/Modules from Motorola and other LCD Drive Manufacturers
 - Support Up to 4 Grey Levels
 - Utilize System Memory as Display Memory
- IEEE 1149.1 Boundary Scan Test Access Port (JTAG)
- Operation from DC to 16 MHz (Processor Clock)
- 3.3V ± 0.3V Operating Voltages
- Compact 144-Lead Thin-Plastic-Quad-Flat-Pack (TQFP) Package

SYSTEM INTEGRATION MODULE

The M68328 system integration module (SIM28) controls the system start-up, initialization, configuration, and the external bus with minimal glue logic. The memory interfaces gluelessly with the SRAM, EPROM as well as PCMCIA 1.0 memory cards. Using the chip-select logic, wait states are programmable. The hardware and software watchdog timers perform system protection functions. The interrupt controller accepts and resolves

the priority from internal modules and external generated interrupts. It also handles the masking and wake-up selection control for power control. The low-power logic can control the CPU power dissipation by altering the frequency or stopping it altogether. The SIM28 can configure the pin to let users select either dedicated I/O or parallel I/O, thereby increasing the number of available I/O ports by reclaiming the dedicated function when not in use.

System Configuration

The M68328 system configuration logic consists of a system control register (SCR) to configure operation of the following functions:

- System Status and Control Logic
- Register Double Mapping
- Bus Error Generation Control
- Protection of the Module Control Registers from Access by User Programs

VCO/PLL Clock Synthesizer

The clock synthesizer can operate with either an external crystal or an external oscillator for reference, using the internal phase-locked loop (PLL) and voltage-controlled oscillator (VCO), or an external clock can directly drive the clock signal at the operating frequency.

Chip Select Logic

The M68328 provides 16 programmable general-purpose chip-select signals. For a given chip-select block, users may choose whether the chip-select allows read-only or both read-and-write access; whether the chip-select should match only one function code value or all values; whether a \overline{DTACK} is automatically generated for this chip-select and after how many wait states (from zero to six) the \overline{DTACK} will be generated.

External Bus Interface

The external bus interface handles information transfer between the internal M68EC000 core and the memory, peripherals, or other processing elements in the external address space. It consists of a 16-bit 68000 bus interface for internal data transfer and a selectable 8-bit or 16-bit interface for external data transfer.

Interrupt Controller

The interrupt controller accepts and prioritizes both internal and external interrupt requests and generates a vector number during the CPU interrupt-acknowledge cycle. Interrupt nesting is also provided so that an interrupt service routine of a lower priority interrupt may be suspended by a higher priority interrupt request. The on-chip interrupt controller has the following features:

- Prioritized Interrupt Sources (Internal and External)
- A Fully Nested Interrupt Environment
- Programmable Vector Generation
- Interrupt Masking
- Wake-up Interrupt Masking

Parallel General-Purpose I/O Ports

The M68328 supports up to 76-bit general-purpose I/O ports, which can be configured as general-purpose I/O pins or as dedicated peripheral interface pins of the on-chip modules.

Each port pin can be independently programmed as a general-purpose I/O pin, even when other pins related to the same on-chip peripheral are used as dedicated pins. If all the pins for a particular peripheral are configured as general-purpose I/O, the peripheral will still operate normally, though this is useful only in the case of the RTC and timer modules.

Software Watchdog

A software watchdog timer protects against system failures by providing a means to escape from unexpected input conditions, external events, or programming errors. Once started, the software watchdog timer must be cleared by software on a regular basis so that it never reaches its time-out value. Upon reaching the time-out value, the timer assumes that a system failure has occurred, and the software watchdog logic resets or interrupts the M68EC000 core.

Low-Power Stop Logic

Available power-saving techniques include: turning off unused peripherals, reducing processor clock speed, disabling the processor altogether, or a combination of these.

LCD Controller

- Interfaces with Monochrome STN LCD Modules
- Up to 4 Levels of Gray Scale through Frame Rate Control
- Utilize System RAM for Display Memory
- Screen Refresh through DMA

UART and Infrared Communication Support

The UART supports standard asynchronous serial communications at normal baud rates and is compatible with IrDA physical communication protocol.

Real Time Clock

The real-time clock in the M68328 is driven by a 32.76kHz or 38.4kHz crystal that is the same as the clock synthesizer clock source. It provides an interrupt for alarm purposes.

JTAG Test Access Port

To aid in system diagnostics, the M68328 includes dedicated user-accessible test logic that is fully compliant with the IEEE 1149.1 standard for boundary-scan testability, often referred to as JTAG (Joint Test Action Group).

ORDERING INFORMATION

Table 1 identifies the packages and operating frequencies available for the M68328.


Table 1. M68328 Package/Frequency Availability

Package Type	V _{CC}	Frequency (MHz)	Temperature	Order Number	Samples Order
144-Lead TQFP	3.3V	16	0°C to 70°C	XC68328PV16V	SPAK 328
144-Lead TQFP	3.3V	16	-40°C to 85°C	Available 1Q96	SPAKCV

The documents listed in Table 2 contain detailed information on the M68328. These documents may be obtained from the Literature Distribution Centers at the addresses listed at the bottom of this page.

Table 2. Documentation

Document Title	Order Number	Contents
MC68328 User's Manual	MC68328UM/AD	LDC Stocking est. 2Q95
M68000 Family Programmer's Reference Manual	M68000PM/AD	M68000 Family Instruction Set

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