TEF6701HL

Car radio tuner front-end for digital IF

Rev. 01 — 16 November 2004 Product data sheet

1. General description

The TEF6701HL is a single chip car radio tuner for AM, FM standard, FM In-Band On-Channel Digital Audio Broadcast (IBOC DAB) and weather band providing gain controlled output of FM IF and AM IF2 for a car IF DSP IC (e.g. SAA7724H) including the following functions:

- AM double conversion tuner for LW/MW/SW (31 m, 41 m and 49 m bands) with IF1 = 10.7 MHz and IF2 = 450 kHz
- FM single conversion tuner to an IF frequency of 10.7 MHz with integrated image rejection for US FM, Europe FM, Japan FM, East Europe FM and weather band reception; all bands can be selected using high side or low side Local Oscillator (LO) injection
- Tuning system includes VCO, crystal oscillator and PLL synthesizer on one chip.

2. Features

- FM mixer for conversion of FM RF (64 MHz to 108 MHz and US weather band) to an IF of 10.7 MHz; the mixer provides inherent image rejection and can be switched from low injection to high injection Local Oscillator (LO) via the I²C-bus; two different mixer conversion gains can be selected via the I²C-bus
- AGC PIN diode drive circuit for FM RF AGC; AGC detection at FM mixer input; the AGC PIN diode drive can be activated via the I²C-bus as a local function for search tuning; AGC threshold is a programmable and keyed function switchable via the I²C-bus
- Digital alignment circuit for bus controlled matching of oscillator tuning voltage to FM antenna tank circuit tuning voltage
- Buffer output for weather band flag
- FM IF linear amplifier with high dynamic input range; amplifier gain can be switched to two different positions via the I²C-bus
- FM IF AGC with multiplexed inputs for FM and In-Band On-Channel Digital Audio Broadcast (IBOC DAB)
- Buffer amplifier for FM IBOC DAB IF bypassing second IF filter can be activated via I²C-bus
- AM mixer 1 for conversion of AM RF to AM IF1 10.7 MHz
- AM RF PIN diode drive circuit and RF JFET conductance control by AGC cascode drive circuit; AGC threshold detection at AM mixer 1 and IF2 AGC input; threshold is programmable via the I²C-bus
- AM noise blanker with blanking at AM IF2; AM noise blanker can be deactivated via the I²C-bus
- AM mixer 2 for conversion of AM IF1 to AM IF2 450 kHz

- AM IF2 AGC
- Multiplexer to output AM IF2 AGC and FM IF AGC to a car IF DSP IC (e.g. SAA7724H)
- AM/FM RF AGC monitor output
- Level detector for AM and FM with temperature compensated output voltage; starting point and slope of level output is programmable via the I^2C-bus
- IF counter for AM IF2 and FM IF
- LC tuner oscillator providing mixer frequencies for FM mixer and AM mixer 1
- Crystal oscillator providing mixer frequencies for AM mixer 2 and reference for synthesizer PLL, IF count and timing for Radio Data System (RDS) update
- Fast synthesizer PLL tuning system with local control for inaudible RDS updating
- Timing function for RDS update algorithm and control signal output for a car IF DSP IC (e.g. SAA7724H)
- Three hardware programmable I^2C-bus addresses; pin BUSENABLE; two software controlled flag outputs
- Several test modes for fast IC and system tests.

3. Quick reference data

Table 1: Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DDA(n)}$	analog supply voltages 1 to 4 and 6		8	8.5	9	V
V_{DDA5}	analog supply voltage 5		4.75	5	5.25	V
V_{DDD}	digital supply voltage		4.75	5	5.25	V
$I_{DDA(n)}$	sum of analog supply currents 1 to 4 and 6	FM Japan mode	42	55	71	mA
		AM mode	32	43	56	mA
I_{DDA5}	analog supply current 5	FM Japan mode	7.5	10	12	mA
		AM mode	14	18.5	23	mA
I_{DDD}	digital supply current	FM Japan mode	25	32	39.5	mA
		AM mode	21	26	32	mA
$f_{AM(ant)}$	AM input frequency	LW	0.144	-	0.288	MHz
		MW	0.522	-	1.710	MHz
		SW	5.73	-	9.99	MHz
$f_{FM(ant)}$	FM input frequency		64	-	108	MHz
$f_{FM(WB)(ant)}$	FM weather band input frequency		162.4	-	162.55	MHz
T_{amb}	ambient temperature		–40	-	+85	°C
AM overall system parameters; see Figure 8						
$g_{m(conv)}$	AM mixer 1 conversion transconductance $\frac{I_{IF1}}{V_{RF}}$		3.9	5.2	6.5	$\frac{mA}{V}$
F_{AMMIX1}	noise figure of AM mixer 1		-	4.5	7.1	dB

Table 1: Quick reference data *...continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IP3	3rd-order input intercept point	R_L = 2.6 kΩ (AC load between output pins); Δf = 300 kHz	135	138	-	dBμV
$g_{m(conv)}$	AM mixer 2 conversion transconductance $\frac{I_{IF2}}{V_{IF1}}$		3.2	4.3	5.4	$\frac{mA}{V}$
ΔAGC	AM IF2 amplifier gain control range $\frac{V_{IFstop}}{V_{IFstart}}$		52	-	-	dB
FM overall system parameters; see Figure 8						
FM mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{IF}}{V_{RF}}$	MIXGAIN = 0	8.5	12.5	18	$\frac{mA}{V}$
		MIXGAIN = 1	17	25	36	$\frac{mA}{V}$
$F_{FMmixer}$	noise figure of FM mixer	MIXGAIN = 0	-	3.5	4.6	dB
		MIXGAIN = 1	-	2.4	-	dB
IP3	3rd-order input intercept point	MIXGAIN = 0	113	117	-	dBμV
		MIXGAIN = 1	-	108	-	dBμV
FM amplifier						
G_{IFAMP}	FM IF amplifier gain $\frac{V_{FMIFAMPOUT}}{V_{IFAMPIN-IFAMPDEC}}$	R_L = 330 Ω; $V_{IFAMPIN-IFAMPDEC}$ = 1 mV				
		IFGAIN = 0	-	10.5	-	dB
		IFGAIN = 1	-	14	-	dB
$G_{IBOCAMP}$	FM IBOC amplifier gain	IBOC = 1	-	8	-	dB
$IP3_{IF}$	3rd-order input intercept point	IFGAIN = 0	-	123	-	dBμV
		IFGAIN = 1	-	119	-	dBμV
$IP3_{IBOC}$	3rd-order input intercept point IBOC mode	IBOC = 1	-	123	-	dBμV
F_{IFAMP}	noise figure of FM IF amplifier	IFGAIN = 0	-	10	-	dB
		IFGAIN = 1	-	8.3	-	dB
$F_{IBOCAMP}$	noise figure of FM IBOC amplifier	IBOC = 1	-	7	-	dB
ΔAGC	FM IF amplifier gain control range $\frac{V_{IFstop}}{V_{IFstart}}$		59	-	-	dB

4. Ordering information

Table 2: Ordering information

Type number	Package		
	Name	Description	Version
TEF6701HL	LQFP64	plastic low profile quad flat package; 64 leads; body 10 × 10 × 1.4 mm	SOT314-2

5. Block diagram

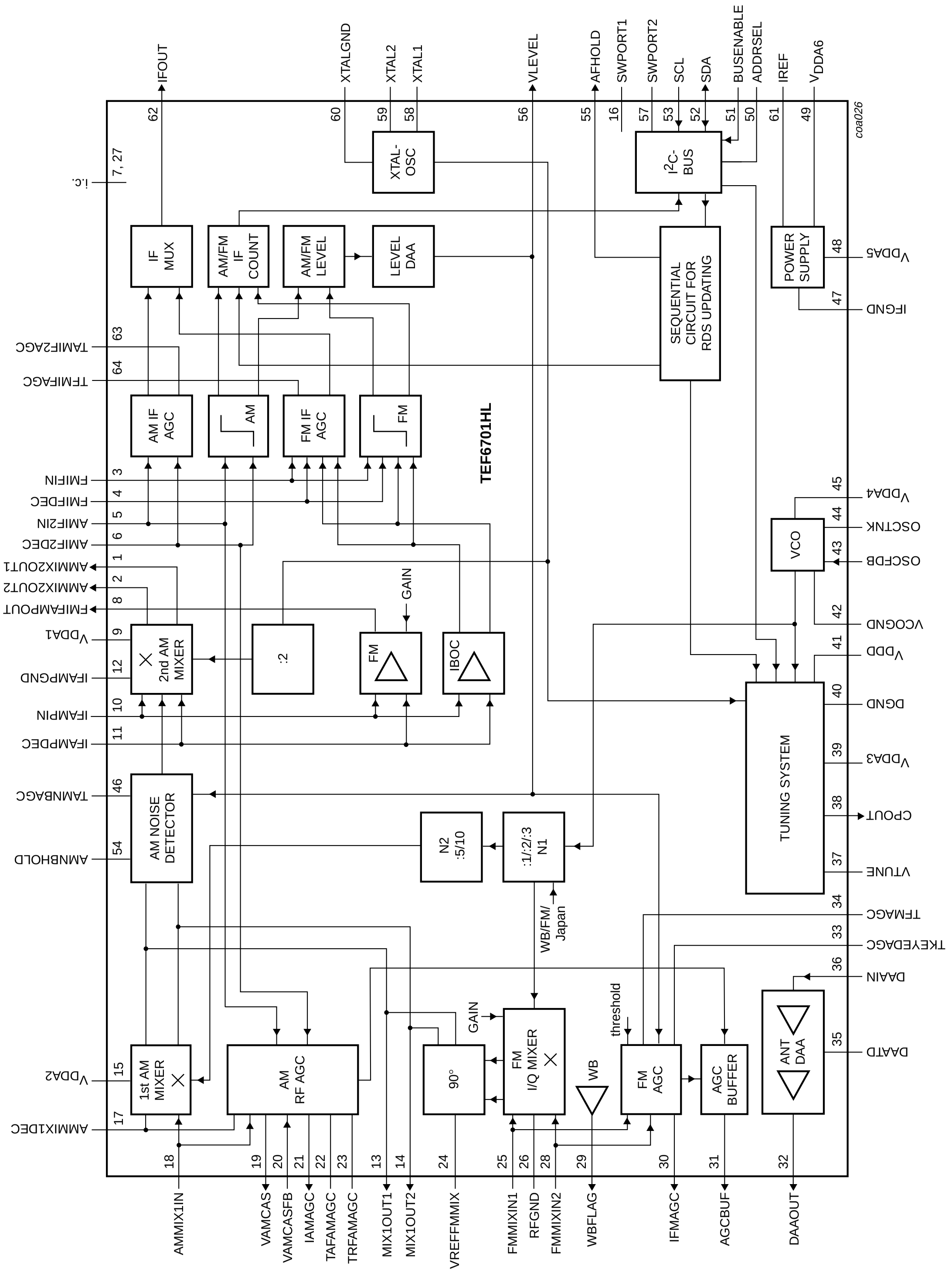


Fig 1. Block diagram.

6. Pinning information

6.1 Pinning

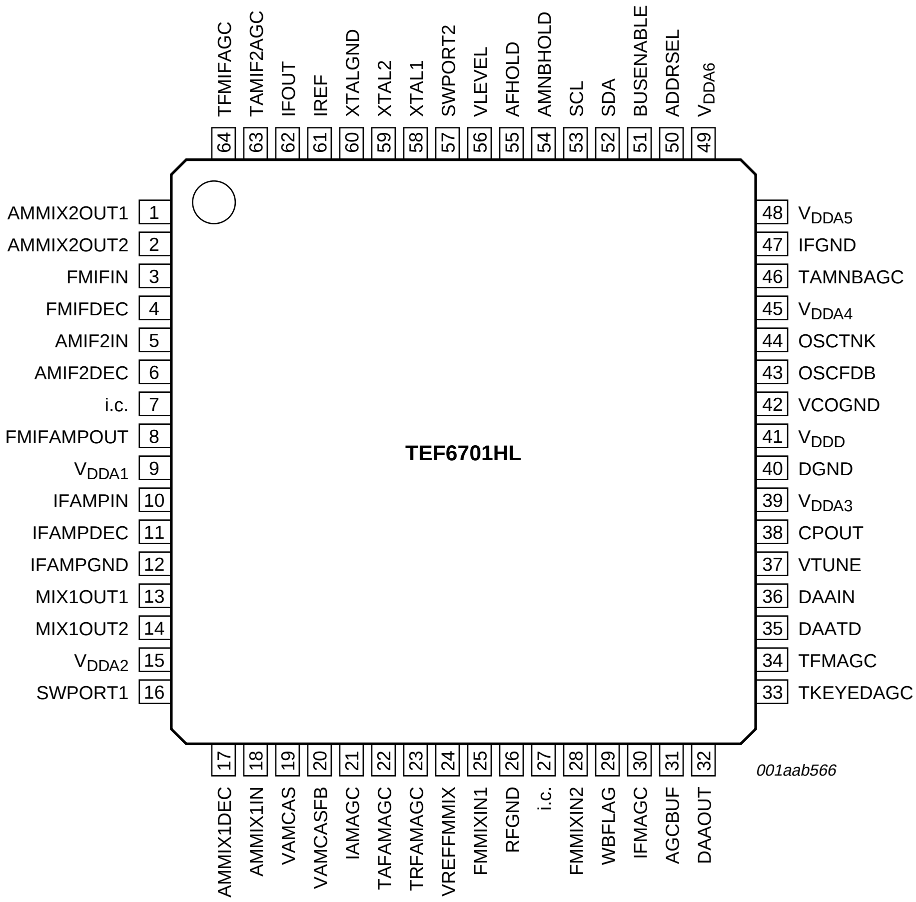


Fig 2. Pin configuration.

6.2 Pin description

Table 3: Pin description

Symbol	Pin	Description
AMMIX2OUT1	1	2nd AM mixer output 1 (450 kHz)
AMMIX2OUT2	2	2nd AM mixer output 2 (450 kHz)
FMIFIN	3	FM IF AGC and FM level detector input
FMIFDEC	4	FM IF AGC and FM level detector decoupling
AMIF2IN	5	AM IF2 AGC and AM level detector input (450 kHz)
AMIF2DEC	6	AM IF2 AGC and AM level detector decoupling
i.c.	7	internally connected
FMIFAMPOUT	8	FM IF amplifier output (10.7 MHz)
V_{DDA1}	9	analog supply voltage 1 (8.5 V) for FM IF amplifier

Table 3: Pin description *…continued*

Symbol	Pin	Description
IFAMPIN	10	FM IF amplifier and AM mixer 2 input (10.7 MHz)
IFAMPDEC	11	FM IF amplifier and AM mixer 2 decoupling
IFAMPGND	12	ground for FM IF amplifier
MIX1OUT1	13	FM mixer and AM mixer 1 IF output 1 (10.7 MHz)
MIX1OUT2	14	FM mixer and AM mixer 1 IF output 2 (10.7 MHz)
V_{DDA2}	15	analog supply voltage 2 (8.5 V) for FM and AM RF
SWPORT1	16	software programmable port 1
AMMIX1DEC	17	AM mixer 1 decoupling
AMMIX1IN	18	AM mixer 1 input
VAMCAS	19	output for AM RF cascode AGC
VAMCASFB	20	feedback input for AM RF cascode AGC
IAMAGC	21	PIN diode drive current output of AM front-end AGC
TAFAMAGC	22	AF time constant of AM front-end AGC
TRFAMAGC	23	RF time constant of AM front-end AGC
VREFFMMIX	24	reference voltage for FM RF mixer
FMMIXIN1	25	FM mixer input 1
RFGND	26	RF ground
i.c.	27	internally connected
FMMIXIN2	28	FM mixer input 2
WBFLAG	29	buffered weather band flag output
IFMAGC	30	PIN diode drive current output of FM front-end AGC
AGCBUF	31	monitor current output of FM and AM front-end AGC
DAAOUT	32	output of digital auto alignment circuit for antenna tank circuit
TKEYEDAGC	33	time constant of keyed FM front-end AGC
TFMAGC	34	time constant of FM front-end AGC
DAATD	35	temperature compensation diode of digital auto alignment circuit for antenna tank circuit
DAAIN	36	input of digital auto alignment circuit for antenna tank circuit
VTUNE	37	VCO tuning voltage
CPOUT	38	charge pump output
V_{DDA3}	39	analog supply voltage 3 (8.5 V) for tuning PLL
DGND	40	digital ground
V_{DDD}	41	digital supply voltage (5 V)
VCOGND	42	VCO ground
OSCFDB	43	VCO feedback input
OSCTNK	44	VCO tank circuit
V_{DDA4}	45	analog supply voltage 4 (8.5 V) for VCO
TAMNBAGC	46	AGC time constant for AM IF noise blanker
IFGND	47	IF AGC ground
V_{DDA5}	48	analog supply voltage 5 (5 V) for on-chip power supply
V_{DDA6}	49	analog supply voltage 6 (8.5 V) for on-chip power supply

Table 3: Pin description ...*continued*

Symbol	Pin	Description
ADDRSEL	50	hardware address select for I^2C-bus
BUSENABLE	51	enable input for I^2C-bus
SDA	52	I^2C-bus data line input and output
SCL	53	I^2C-bus clock line input
AMNBHOLD	54	AM noise blanker threshold
AFHOLD	55	AF hold flag output for a car IF DSP IC (e.g. SAA7724H)
VLEVEL	56	level voltage output for AM and FM
SWPORT2	57	software programmable port 2
XTAL1	58	crystal oscillator 1
XTAL2	59	crystal oscillator 2
XTALGND	60	crystal oscillator ground
IREF	61	reference current for power supply
IFOUT	62	multiplexer output for FM IF AGC and AM IF2 AGC
TAMIF2AGC	63	time constant for AM IF2 AGC
TFMIFAGC	64	time constant for FM IF AGC

7. Functional description

7.1 FM I/Q mixer

The FM quadrature mixer converts FM RF (64 MHz to 162.55 MHz) to an IF of 10.7 MHz. The FM mixer provides inherent image rejection and high RF sensitivity. The image rejection can be switched from low injection Local Oscillator (LO) to high injection LO via the I^2C-bus. The mixer gain can be increased by 6 dB via the I^2C-bus. In this case the threshold of the FM keyed AGC has to be lowered by 6 dB to prevent the mixer from being overloaded.

The mixer is capable of tuning the:

- US FM and US IBOC DAB from 87.9 MHz to 107.9 MHz
- US weather FM from 162.4 MHz to 162.55 MHz
- Europe FM from 87.5 MHz to 108 MHz
- Japan FM from 76 MHz to 91 MHz
- East Europe FM from 64 MHz to 74 MHz.

7.2 Buffer output for weather band flag

The buffer output (pin WBFLAG) is HIGH for weather band mode.

7.3 VCO

The varactor tuned LC oscillator provides the local oscillator signal for both FM and AM mixer 1. It has a frequency range from 159.9 MHz to 248.2 MHz.

7.4 Crystal oscillator

The crystal oscillator provides a 20.5 MHz signal that is used for:

- Reference frequency for frequency synthesizer PLL
- Local oscillator for AM mixer 2
- Reference frequency for the IF counter
- Timing signal for the RDS update algorithm.

7.5 PLL

The fast synthesizer PLL tuning system with local control is used for inaudible RDS updating.

7.6 DAA

To reduce the number of manual alignments in production, the following I^2C-bus controlled Digital Auto Alignment (DAA) functions are included:

- FM RF DAA
  - 7-bit DAA circuitry for the conversion of the VCO tuning voltage to a controlled alignment voltage for the FM antenna tank circuit.
- FM and AM level DAA
  - Level DAA circuitry for alignment of slope (3-bit) and starting point (5-bit) of the level curve.

7.7 FM keyed AGC

The AGC threshold is programmable and the keyed AGC function is switchable via the I^2C-bus. AGC detection occurs at the input of the FM mixer. If the keyed AGC function is activated, the AGC is keyed only by the narrow-band level. The AGC PIN diode drive can be activated via the I^2C-bus as a local function for search tuning. The AGC sources a constant 10 mA current into the FM PIN diode in AM mode.

7.8 FM IF amplifier

The FM IF amplifier provides 10.5 dB or 14 dB gain, selectable via the I^2C-bus with high linearity over a wide dynamic range. In IBOC DAB mode (activated via the I^2C-bus) FM IF is buffered and directly fed to FM IF AGC, bypassing the second FM ceramic filter.

7.9 FM IF AGC

This is a linear FM IF AGC amplifier with multiplexed inputs for FM standard and FM IBOC DAB. The gain controlled FM IF is output by the multiplexed FM IF/AM IF2 buffer for a car IF DSP IC (e.g. SAA7724H).

7.10 AM tuner including mixer 1 and mixer 2

The AM tuner is realized in a double conversion technique and is capable of selecting LW, MW and SW bands.

AM mixer 1 converts AM RF to an IF1 of 10.7 MHz, while AM mixer 2 converts IF1 of 10.7 MHz to an IF2 of 450 kHz:

- LW from 144 kHz to 288 kHz
- MW from 522 kHz to 1710 kHz (US AM band)
- SW from 5.73 MHz to 9.99 MHz (including the 31 m, 41 m and 49 m bands).

7.11 AM RF AGC

The AM wideband AGC in front of the AM mixer 1 is realized first by a cascoded NPN transistor, which controls the transconductance of the RF amplifier JFET with 10 dB of AGC range. An AM PIN diode stage with 30 dB of AGC range is also available. The minimum JFET drain source voltage is controlled by a DC feedback loop (pin VAMCASFB) in order to limit the cascode AGC range to 10 dB. If the cascode AGC is not required, a simple RF AGC loop is possible by using only a PIN diode. In some conditions, noise behavior will increase. In this case pins VAMCAS and VAMCASFB have to be left open-circuit. In FM mode, the cascode switches off the JFET bias current to reduce the total power consumption. The PIN diode is biased by 1 mA in FM mode.

The AGC detection points for AM RF AGC are at the AM mixer 1 input (threshold programmable via the I^2C-bus) and the IF2 AGC input (fixed threshold).

7.12 AM noise blanker

The detection point for the AM noise blanker is the output stage of AM mixer 1, while blanking is realized at the output of mixer 2.

7.13 AM IF2 AGC

This is a linear AM IF2 AGC amplifier. The gain controlled AM IF2 is output via the multiplexed FM IF/AM IF2 buffer to a car IF DSP IC (e.g. SAA7724H).

7.14 FM IF and AM IF2 buffer

This buffers and multiplexes AM IF2 and FM IF to pin IFOUT.

7.15 FM and AM level detector

The FM and AM level detectors provide the temperature compensated output voltage. The starting points and slopes of the level detector outputs are programmable via the I^2C-bus.

7.16 FM/AM RF AGC buffer

The output (open-collector) sinks a current which in AM mode is proportional to the voltage at pin TRFAMAGC and in FM mode proportional to the RF level detector voltage (pin TFMAGC) inside the FM AGC.

8. I²C-bus protocol

8.1 I²C-bus specification

SDA and SCL HIGH and LOW levels are specified according to a 3.3 V I²C-bus. The bus pins tolerate also thresholds of a 5 V bus.

The standard I²C-bus specification is expanded by the following definitions.

IC addresses:

- 1st IC address C2H: 1100001 R/$\overline{W}$
- 2nd IC address C0H: 1100000 R/$\overline{W}$
- 3rd IC address C4H: 1100010 R/$\overline{W}$.

Structure of the I²C-bus logic: slave transceiver with auto increment.

Subaddresses are not used.

The second I²C-bus address can be selected by connecting pin ADDRSEL via a 120 kΩ resistor to GND. The third I²C-bus address can be selected by connecting pin ADDRSEL via a 33 kΩ resistor to GND.

The maximum bit rate for this device is 100 kbit/s.

The I²C-bus interface is extended with an enable input (pin BUSENABLE). If pin BUSENABLE is HIGH the communication with the device is active; if pin BUSENABLE is LOW the signals on the I²C-bus are ignored so that higher bit rates (> 100 kbit/s) can be used to communicate with other devices on the same I²C-bus. The enable signal must not change while bus communication takes place.

The data hold time $t_{HD;DAT}$ must be at least 1 μs.

No default settings at power-on reset. I²C-bus transmission is required to program the IC.

8.1.1 Data transfer

Data sequence: address, byte 0, byte 1, byte 2, byte 3, byte 4, byte 5 and byte 6.

The data transfer has to be in this order. The LSB of the address being logic 0 indicates a write operation.

Bit 7 of each byte is considered the MSB and has to be transferred as the first bit of the byte.

The data becomes valid at the output of the internal latches with the acknowledge of each byte. A STOP condition after any byte can shorten transmission times.

When writing to the transceiver by using the STOP condition before completion of the whole transfer:

- The remaining bytes will contain the old information
- If the transfer of a byte is not completed, this byte is lost and the previous information is available.

8.1.2 Frequency setting

For new frequency setting, in both AM and FM mode, the programmable divider is enabled by setting bit PRESET to logic 1. To select a frequency, two I^2C-bus transmissions are necessary:

- First: bit PRESET = 1
- Second: bit PRESET = 0.

8.1.3 Restriction of the I^2C-bus characteristic

At –40 °C the start of the acknowledge bit after transmitting the slave address exceeds the general requirement of $t_{HD;DAT}$ < 3.45 µs. The start of acknowledge is $t_{ST;ACK}$ < 4.1 µs over the full temperature range from –40 °C to +85 °C. This will not influence the overall system performance, because the required set-up time $t_{SU;DAT}$ > 250 ns is fulfilled at any condition.

8.2 I^2C-bus protocol

8.2.1 Data transfer mode and IC address

Table 4: Write mode

S [1]	address (write)	A [2]	data byte(s)	A [2]	P [3]

[1] S = START condition.

[2] A = acknowledge.

[3] P = STOP condition.

Table 5: Read mode

S [1]	address (read)	A [2]	data byte 0	NA [3]	P [4]

[1] S = START condition.

[2] A = acknowledge.

[3] NA = no acknowledge.

[4] P = STOP condition.

Table 6: IC address byte

Address	IC address [1]							Mode [2]
1	1	1	0	0	0	0	1	$R/\overline{W}$
2	1	1	0	0	0	0	0	$R/\overline{W}$
3	1	1	0	0	0	1	0	$R/\overline{W}$

[1] Pin ADDRSEL left open-circuit activates first IC address; R_{ext} = 120 kΩ at pin ADDRSEL to ground activates second IC address; R_{ext} = 33 kΩ at pin ADDRSEL to ground activates third IC address.

[2] Read or write bit:
0 = write operation to TEF6701HL
1 = read operation from TEF6701HL.

8.2.2 Write mode: data byte 0

Table 7: Format of data byte 0

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
AF	PLL14	PLL13	PLL12	PLL11	PLL10	PLL9	PLL8

Table 8: Description of data byte 0 bits

Bit	Symbol	Description
7	AF	**Alternative frequency.** If AF = 0, then normal operation. If AF = 1, then AF (RDS) update mode.
6 to 0	PLL[14:8]	**Setting of programmable counter of synthesizer PLL.** Upper byte of PLL divider word.

8.2.3 Write mode: data byte 1

Table 9: Format of data byte 1

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL7	PLL6	PLL5	PLL4	PLL3	PLL2	PLL1	PLL0

Table 10: Description of data byte 1 bits

Bit	Symbol	Description
7 to 0	PLL[7:0]	**Setting of programmable counter of synthesizer PLL.** Lower byte of PLL divider word.

8.2.4 Write mode: data byte 2

Table 11: Format of data byte 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PRESET	DAA6	DAA5	DAA4	DAA3	DAA2	DAA1	DAA0

Table 12: Description of data byte 2 bits

Bit	Symbol	Description
7	PRESET	**Preset.** If PRESET = 0, then programmable divider and antenna DAA locked. If PRESET = 1, then writing to programmable divider and antenna DAA enabled.
6 to 0	DAA[6:0]	**Setting of antenna digital auto alignment.**

8.2.5 Write mode: data byte 3

Table 13: Format of data byte 3

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IFMT	FREF2	FREF1	FREF0	IFPR	BND1	BND0	AMFM

Table 14: Description of data byte 3 bits

Bit	Symbol	Description
7	IFMT	**IF measuring time.** If IFMT = 0, then IF measuring time is 20 ms. If IFMT = 1, then IF measuring time is 2 ms.
6 to 4	FREF[2:0]	**Reference frequency for synthesizer.** These 3 bits determine the reference frequency, see Table 15.
3	IFPR	**IF counter prescaler ratio.** If IFPR = 0, then IF prescaler ratio is 100. If IFPR = 1, then IF prescaler ratio is 10.
2 and 1	BND[1:0]	**Band switch.** These 2 bits select the frequency in AM and FM mode, see Table 16 and Table 17.
0	AMFM	**AM or FM switch.** If AMFM = 0, then FM mode. If AMFM = 1, then AM mode.

Table 15: Reference frequency setting

FREF2	FREF1	FREF0	f_{ref} (kHz)
0	0	0	100
1	0	0	50
0	1	0	25
1	1	0	20
0	0	1	10
1	0	1	10
0	1	1	10
1	1	1	10

Table 16: FM band selection bits

BND1	BND0	Frequency band	VCO divider	Charge pump current
0	0	FM standard	2	130 µA + 3 mA
0	1	FM Japan	3	130 µA + 3 mA
1	0	FM East Europe	3	1 mA
1	1	FM weather	1	300 µA

Table 17: AM band selection bits [1]

BND1	BND0	Frequency band	VCO divider	Charge pump current
0	X	AM SW	10	1 mA
1	X	AM LW/MW	20	1 mA

[1] X = don't care.

8.2.6 Write mode: data byte 4

Table 18: Format of data byte 4

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KAGC	AGC1	AGC0	LODX	FMINJ	IBOC	IFGAIN	MIXGAIN

Table 19: Description of data byte 4 bits

Bit	Symbol	Description
7	KAGC	**Keyed FM AGC.** If KAGC = 0, then keyed FM AGC is off. If KAGC = 1, then keyed FM AGC is on.
6 and 5	AGC[1:0]	**Wideband AGC.** These 2 bits set the start value of wideband AGC. For AM, see Table 20 and for FM, see Table 21.
4	LODX	**Local or distance.** If LODX = 0, then distance mode is on. If LODX = 1, then local mode is on.
3	FMINJ	**FM mixer image rejection.** If FMINJ = 0, then low injection. If FMINJ = 1, then high injection.
2	IBOC	**FM IBOC mode.** If IBOC = 0, then IBOC buffer amplifier is off. If IBOC = 1, then IBOC buffer amplifier is on.
1	IFGAIN	**IF amplifier gain.** If IFGAIN = 0, then G_{IFAMP} = 10.5 dB. If IFGAIN = 1, then G_{IFAMP} = 14 dB.
0	MIXGAIN	**FM mixer gain.** If MIXGAIN = 0, then the FM mixer gain is nominal. If MIXGAIN = 1, then the FM mixer gain is +6 dB.

Table 20: Setting of wideband AGC for AM (m = 0.3)

AGC1	AGC0	AM mixer 1 input voltage (peak value) (mV)
0	0	530
0	1	420
1	0	290
1	1	150

Table 21: Setting of wideband AGC for FM

AGC1	AGC0	FM RF mixer input voltage (RMS value) (mV)
1	1	3
1	0	6
0	1	9
0	0	12

8.2.7 Write mode: data byte 5

Table 22: Format of data byte 5

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0

Table 23: Description of data byte 5 bits

Bit	Symbol	Description
7 to 3	LST[4:0]	**Setting of level DAA starting point.** These 5 bits determine the offset of the level detector output voltage.
2 to 0	LSL[2:0]	**Setting of level DAA slope.** These 3 bits determine the steepness of the level detector output voltage.

Table 24: Standard setting of data byte 5 bits

Setting of level DAA starting point					Setting of level DAA slope		
LST4	LST3	LST2	LST1	LST0	LSL2	LSL1	LSL0
1	0	0	0	0	1	0	0

8.2.8 Write mode: data byte 6

Table 25: Format of data byte 6

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SWPORT2	SWPORT1	AMNB	-	-	-	-	-

Table 26: Description of data byte 6 bits

Bit	Symbol	Description
7	SWPORT2	**Software programmable port 2.** If SWPORT2 = 0, then pin SWPORT2 is inactive (high-impedance). If SWPORT2 = 1, then pin SWPORT2 is active (pull down to ground).
6	SWPORT1	**Software programmable port 1.** If SWPORT1 = 0, then pin SWPORT1 is inactive (high-impedance). If SWPORT1 = 1, then pin SWPORT1 is active (pull down to ground).
5	AMNB	**AM noise blanker.** If AMNB = 0, then the AM noise blanker is off. If AMNB = 1, then the AM noise blanker is on.
4 to 0	-	These 5 bits are not used and should be set to logic 0.

8.2.9 Read mode: data byte 0

Table 27: Format of first data byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IFC7	IFC6	IFC5	IFC4	IFC3	IFC2	IFC1	IFC0

Table 28: Description of data byte 0 bits

Bit	Symbol	Description
7 to 0	IFC[7:0]	**IF counter result.** These bits contain the least significant eight bits of the IF counter result.

9. Internal circuitry

Table 29: Equivalent pin circuits

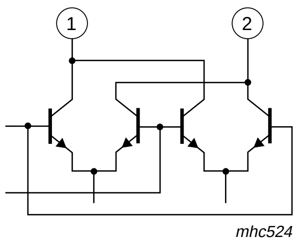
Symbol	Pin	Equivalent circuit
AMMIX2OUT1	1	
AMMIX2OUT2	2	

Table 29: Equivalent pin circuits *...continued*

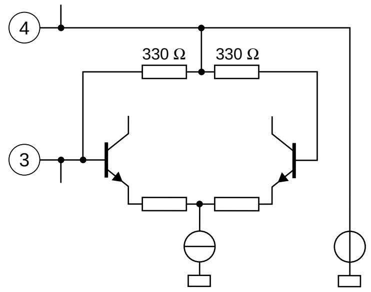
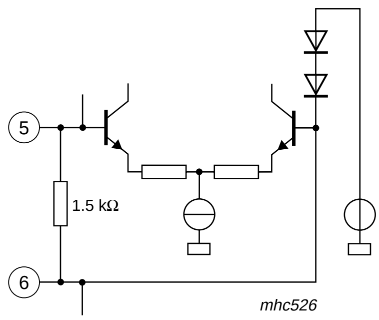
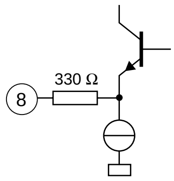
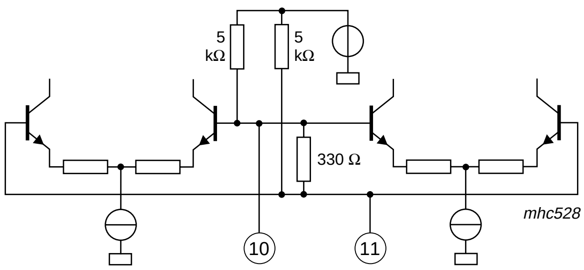
Symbol	Pin	Equivalent circuit
FMIFIN	3	 mhc525
FMIFDEC	4	
AMIF2IN	5	 mhc526
AMIF2DEC	6	
i.c.	7	
FMIFAMPOUT	8	 mhc527
V_{DDA1}	9	
IFAMPIN	10	 mhc528
IFAMPDEC	11	
IFAMPGND	12	

Table 29: Equivalent pin circuits *...continued*

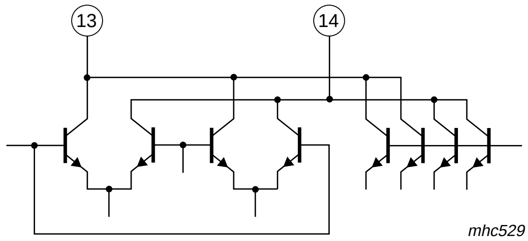
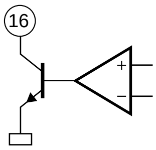
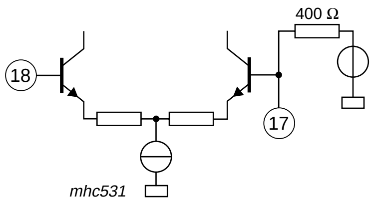
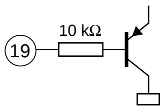
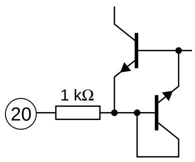
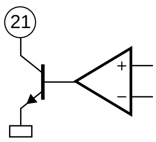
Symbol	Pin	Equivalent circuit
MIX1OUT1	13	 mhc529
MIX1OUT2	14	
V_{DDA2}	15	
SWPORT1	16	 mhc530
AMMIX1DEC	17	 mhc531
AMMIX1IN	18	
VAMCAS	19	 mhc532
VAMCASFB	20	 mhc533
IAMAGC	21	 mhc539

Table 29: Equivalent pin circuits *…continued*

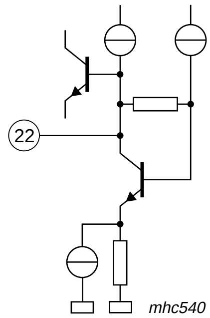
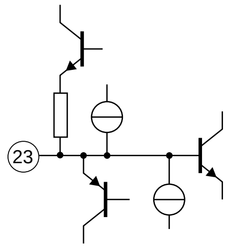
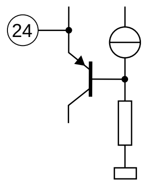
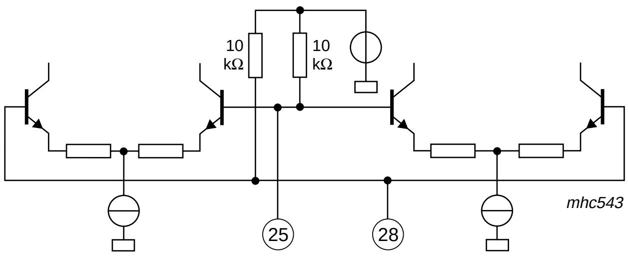
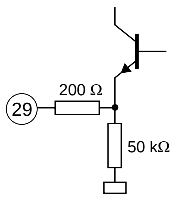
Symbol	Pin	Equivalent circuit
TAFAMAGC	22	 *mhc540*
TRFAMAGC	23	 *mhc541*
VREFFMMIX	24	 *mhc542*
FMMIXIN1	25	 *mhc543*
FMMIXIN2	28	
RFGND	26	
i.c.	27	
WBFLAG	29	 *mhc534*

Table 29: Equivalent pin circuits *...continued*

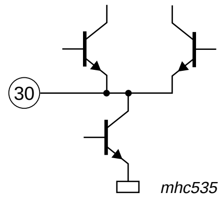
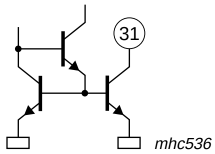
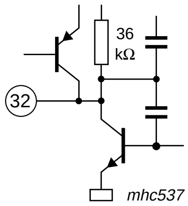
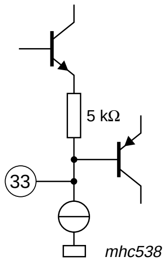
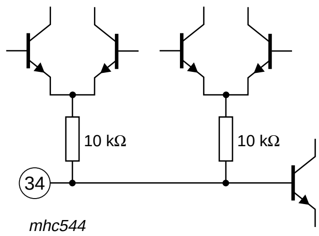
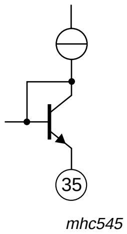
Symbol	Pin	Equivalent circuit
IFMAGC	30	
AGCBUF	31	
DAAOUT	32	
TKEYEDAGC	33	
TFMAGC	34	
DAATD	35	

Table 29: Equivalent pin circuits *...continued*

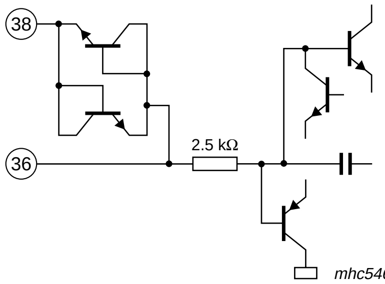
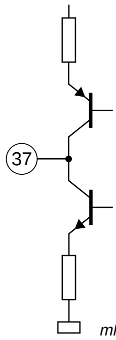
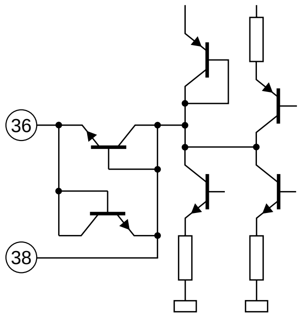
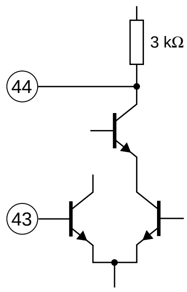
Symbol	Pin	Equivalent circuit
DAAIN	36	 *mhc546*
VTUNE	37	 *mhc547*
CPOUT	38	 *mhc548*
V_{DDA3}	39	
DGND	40	
V_{DDD}	41	
VCOGND	42	
OSCFDB	43	
OSCTNK	44	 *mhc549*

Table 29: Equivalent pin circuits *…continued*

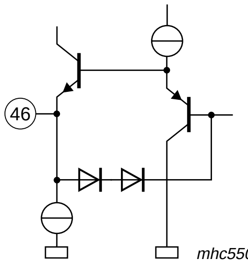
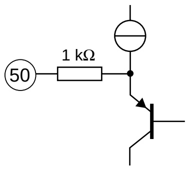
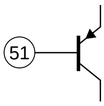
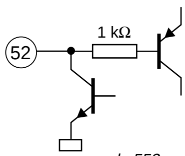
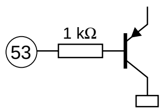
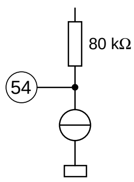
Symbol	Pin	Equivalent circuit
V_{DDA4}	45	
TAMNBAGC	46	 *mhc550*
IFGND	47	
V_{DDA5}	48	
V_{DDA6}	49	
ADDRSEL	50	 *mhc551*
BUSENABLE	51	 *mhc552*
SDA	52	 *mhc553*
SCL	53	 *mhc554*
AMNBHOLD	54	 *mhc555*

Table 29: Equivalent pin circuits *…continued*

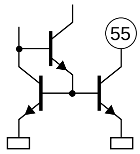
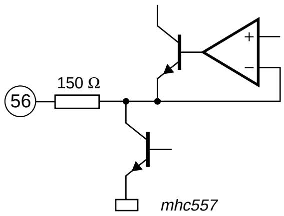
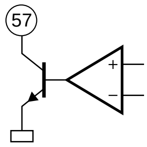
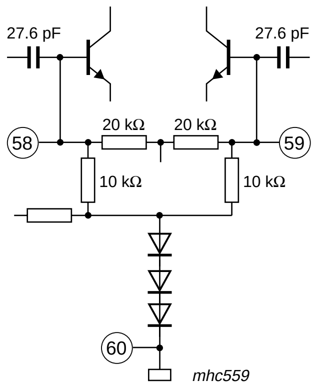
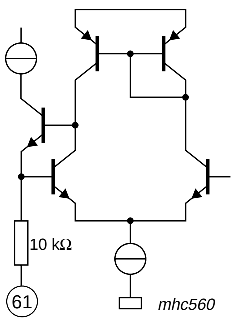
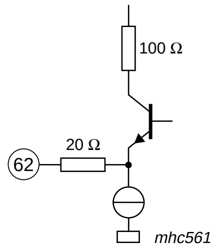
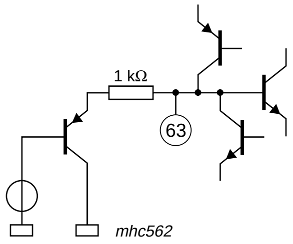
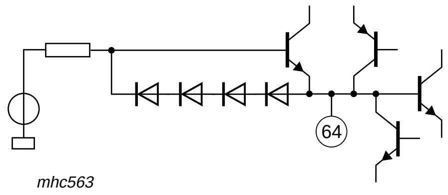
Symbol	Pin	Equivalent circuit
AFHOLD	55	 *mhc556*
VLEVEL	56	
SWPORT2	57	 *mhc558*
XTAL1	58	 *mhc559*
XTAL2	59	
XTALGND	60	
IREF	61	 *mhc560*

Table 29: Equivalent pin circuits *…continued*

Symbol	Pin	Equivalent circuit
IFOUT	62	
TAMIF2AGC	63	
TFMIFAGC	64	

10. Limiting values

Table 30: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA1}	analog supply voltage 1 for FM IF amplifier		[1]	–0.3	+10	V
V_{DDA2}	analog supply voltage 2 for FM and AM RF		[1]	–0.3	+10	V
V_{DDA3}	analog supply voltage 3 for tuning PLL		[1]	–0.3	+10	V
V_{DDA4}	analog supply voltage 4 for VCO		[1]	–0.3	+10	V
V_{DDA5}	analog supply voltage 5 for on-chip power supply			–0.3	+6.5	V
V_{DDA6}	analog supply voltage 6 for on-chip power supply		[1]	–0.3	+10	V
V_{DDD}	digital supply voltage			–0.3	+6.5	V
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
V_{es}	electrostatic handling voltage		[2]	–200	+200	V
			[3]	–2000	+2000	V

[1] To avoid damages and wrong operation it is necessary to keep all 8.5 V supply voltages at a higher level than any 5 V supply voltage. This is also necessary during power-on and power-down sequences. Precautions have to be provided in such a way that interferences can not pull down the 8.5 V supply below the 5 V supply.

[2] Machine model (R = 0 Ω, C = 200 pF).

[3] Human body model (R = 1.5 kΩ, C = 100 pF).

11. Thermal characteristics

Table 31: Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	58	K/W

12. Static characteristics

Table 32: Static characteristics

$V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5$ V; $V_{DDA5} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltage						
$V_{DDA(n)}$	analog supply voltages 1 to 4 and 6		8	8.5	9	V
V_{DDA5}	analog supply voltage 5		4.75	5	5.25	V
V_{DDD}	digital supply voltage		4.75	5	5.25	V
Supply current in FM mode						
I_{DDA1}	analog supply current 1 for FM IF amplifier	IBOC mode	-	7.9	-	mA
		no IBOC mode	-	8.9	-	mA
I_{DDA2}	analog supply current 2 for RF		4.7	5.7	6.7	mA
I_{DDA3}	analog supply current 3 for tuning PLL		-	4	-	mA
I_{DDA4}	analog supply current 4 for VCO		5.2	6.5	7.8	mA

Table 32: Static characteristics *…continued*

V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA5}	analog supply current 5 for on-chip power supply	Europe/US band	-	6.4	-	mA
		Japan/East Europe band	7.5	10	12	mA
I_{DDA6}	analog supply current 6 for on-chip power supply		-	20.5	-	mA
I_{DDD}	digital supply current	Europe/US band	20	25	31	mA
		Japan/East Europe band	25	32	39.5	mA
$I_{MIX1OUT1}$	bias current of FM mixer output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of FM mixer output 2		4.8	6	7.2	mA
Supply current in AM mode						
I_{DDA1}	analog supply current 1 for AM mixer 2		-	140	-	µA
I_{DDA2}	analog supply current 2 for RF		-	2.6	-	mA
I_{DDA3}	analog supply current 3 for tuning PLL		-	2.2	-	mA
I_{DDA4}	analog supply current 4 for VCO		5	6.5	8	mA
I_{DDA5}	analog supply current 5 for on-chip power supply		14	18.5	23	mA
I_{DDA6}	analog supply current 6 for on-chip power supply		-	16.7	-	mA
I_{DDD}	digital supply current		21	26	32	mA
$I_{MIX1OUT1}$	bias current of AM mixer 1 output 1		4.8	6	7.2	mA
$I_{MIX1OUT2}$	bias current of AM mixer 1 output 2		4.8	6	7.2	mA
$I_{AMMIX2OUT1}$	bias current of AM mixer 2 output 1		3.6	4.5	5.4	mA
$I_{AMMIX2OUT2}$	bias current of AM mixer 2 output 2		3.6	4.5	5.4	mA
On-chip power supply reference current generator: pin IREF						
$V_{o(ref)}$	output reference voltage		4	4.25	4.5	V
R_o	output resistance		-	10	-	kΩ
$I_{o(source)(max)}$	maximum output source current		–100	-	+100	nA

13. Dynamic characteristics

Table 33: Dynamic characteristics

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5$ V; $V_{DDA5} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Voltage controlled oscillator						
f_{osc}	oscillator frequency		159.9	-	248.2	MHz
C/N	carrier-to-noise ratio	$f_{osc} = 200$ MHz; $\Delta f = 10$ kHz; B = 1 Hz	-	97	-	dBc
RR	ripple rejection $\frac{\Delta f_{osc}}{f_{osc}}$	$f_{ripple} = 100$ Hz; $V_{DDA4(ripple)} = 100$ mV; $f_{osc} = 200$ MHz	92	99	-	dB
Crystal oscillator						
f_{xtal}	crystal frequency		-	20.5	-	MHz
C/N	carrier-to-noise ratio	$f_{xtal} = 20.5$ MHz; $\Delta f = 10$ kHz	-	112	-	$\frac{dBc}{\sqrt{Hz}}$
Circuit inputs: pins XTAL1, XTAL2 and XTALGND [1]						
V_{xtal}	crystal voltage		80	100	160	mV
V_{XTAL1}, V_{XTAL2}	DC bias voltage		1.7	2.1	2.5	V
R_i	real part of input impedance	$V_{XTAL1} - V_{XTAL2} = 1$ mV	–250	-	-	Ω
C_i	input capacitance		8	10	12	pF
Synthesizer						
Programmable divider						
N_{prog}	programmable divider ratio		512	-	32767	
ΔN_{step}	programmable divider step size		-	1	-	
Charge pump: pin CPOUT						
$I_{sink(cp1)l}$	low charge pump 1 peak sink current	FM weather band mode; 0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} > f_{ref} \times N_{prog}$	-	300	-	µA
$I_{source(cp1)l}$	low charge pump 1 peak source current	FM weather band mode; 0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} < f_{ref} \times N_{prog}$	-	–300	-	µA
$I_{sink(cp1)h}$	high charge pump 1 peak sink current	0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} > f_{ref} \times N_{prog}$				
		AM mode	-	1	-	mA
		FM East Europe band	-	1	-	mA
$I_{source(cp1)h}$	high charge pump 1 peak source current	0.4 V < V_{CPOUT} < 7.6 V; $f_{VCO} < f_{ref} \times N_{prog}$				
		AM mode	-	–1	-	mA
		FM East Europe band	-	–1	-	mA
$I_{sink(cp2)}$	charge pump 2 peak sink current	FM standard or FM Japan mode; $f_{VCO} > f_{ref} \times N_{prog}$; 0.3 V < V_{CPOUT} < 7.1 V	-	130	-	µA

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6}$ = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{source(cp2)}$	charge pump 2 peak source current	FM standard or FM Japan mode; $f_{VCO} < f_{ref} \times N_{prog}$; 0.3 V < V_{CPOUT} < 7.1 V		-	−130	-	µA
Charge pump: pin VTUNE							
$I_{sink(cp3)}$	charge pump 3 peak sink current	FM standard or FM Japan mode; $f_{VCO} > f_{ref} \times N_{prog}$; 0.4 V < V_{VTUNE} < 7.6 V		-	3	-	mA
$I_{source(cp3)}$	charge pump 3 peak source current	FM standard or FM Japan mode; $f_{VCO} < f_{ref} \times N_{prog}$; 0.4 V < V_{VTUNE} < 7.6 V		-	−3	-	mA
Antenna Digital Auto Alignment (DAA)							
DAA input: pin DAAIN							
$I_{bias(cp)}$	charge pump buffer input bias current	V_{DAAIN} = 0.4 V to 8 V		−10	-	+10	nA
$V_{i(cp)}$	charge pump buffer input voltage			0	-	8.5	V
DAA output: pin DAAOUT							
$V_{o(AM)}$	DAA output voltage in AM mode	I_{DAAOUT} < 100 µA		-	-	0.3	V
$V_{o(FM)}$	DAA output voltage in FM mode	V_{DAATD} = 0.45 V					
		minimum value; data byte 2 = 1000 0000 (n = 0); V_{DAAIN} = 0.5 V		-	-	0.5	V
		data byte 2 = 1010 1010 (n = 42); V_{DAAIN} = 2 V		1.2	1.4	1.6	V
		data byte 2 = 1101 0101 (n = 85); V_{DAAIN} = 2 V	[2]	2.3	2.6	2.9	V
		data byte 2 = 1000 0000 (n = 0); V_{DAAIN} = 4 V	[2]	0.4	0.65	1	V
		data byte 2 = 1100 0000 (n = 64); V_{DAAIN} = 4 V		3.8	4	4.2	V
		maximum value; data byte 2 = 1111 1111 (n = 127); V_{DAAIN} = 4.7 V		8	-	8.5	V
$V_{o(n)}$	DAA output noise voltage	data byte 2 = 1100 0000 (n = 64); FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; B = 300 Hz to 22 kHz		-	30	100	µV
$\Delta V_{o(T)}$	DAA output voltage variation with temperature	T_{amb} = −40 °C to +85 °C; data byte 2 = 1100 0000 (n = 64)		−8	-	+8	mV
$\Delta V_{o(step)}$	DAA step accuracy	FM mode; n = 0 to 127; V_{DAAOUT} = 0.5 V to 8 V; V_{DAAIN} = 2 V; V_{DAATD} = 0.45 V	[3]	$0.5V_{LSB}$	V_{LSB}	$1.5V_{LSB}$	mV

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1}$ = $V_{AMMIX2OUT2}$ = $V_{MIX1OUT1}$ = $V_{MIX1OUT2}$ = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see *Figure 8**; all AC values are given in RMS; unless otherwise specified.*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$\Delta V_{o(sink)}$	DAA output voltage variation caused by sink current	V_{DAAIN} = 4 V; I_{DAAOUT} = 50 µA	[3]	$-V_{LSB}$	-	$+V_{LSB}$	mV
$\Delta V_{o(source)}$	DAA output voltage variation caused by source current	V_{DAAIN} = 4 V; I_{DAAOUT} = –50 µA	[3]	$-V_{LSB}$	-	$+V_{LSB}$	mV
t_{st}	DAA output settling time	V_{DAAOUT} = 0.2 V to 8.25 V; C_L = 270 pF		-	20	30	µs
RR	ripple rejection $\frac{V_{DAAOUT}}{V_{DDA3}}$	data byte 2 = 1010 1011 (n = 43); FM mode; V_{DAAIN} = 4 V; V_{DAATD} = 0.45 V; f_{ripple} = 100 Hz; $V_{DDA3(ripple)}$ = 100 mV		-	65	-	dB
C_L	DAA output load capacitance			-	-	270	pF
DAA temperature compensation: pin DAATD							
I_{source}	compensation diode source current	V_{DAATD} = 0.2 V to 1.2 V		–50	–40	–30	µA
TC_{source}	temperature coefficient of compensation diode source current	V_{DAATD} = 0.2 V to 1.2 V; T_{amb} = –40 °C to +85 °C		–300	-	+300	$\frac{10^{-6}}{K}$
IF counter (FM IF or AM IF2 counter)							
N_{IF}	IF counter length for AM and FM			-	8	-	bit
AM mode							
V_{sen}	sensitivity voltage (pin AMIF2IN to AMIF2DEC)	m = 0		-	30	70	µV
N	counter result (decimal)	$V_{AMIF2IN-AMIF2DEC}$ = 200 µV					
		period = 2 ms		-	132	-	
		period = 20 ms		-	40	-	
FM mode							
V_{sen}	sensitivity voltage (pin FMIFIN to FMIFDEC)			-	60	100	µV
N	counter result (decimal)	period = 2 ms; $V_{FMIFIN-FMIFDEC}$ = 100 µV					
		prescaler ratio = 10		-	92	-	
		prescaler ratio = 100		-	214	-	
		period = 20 ms; $V_{FMIFIN-FMIFDEC}$ = 100 µV					
		prescaler ratio = 10		-	152	-	
		prescaler ratio = 100		-	92	-	

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6}$ = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I²C-bus address select: pin ADDRSEL						
R_L	load resistance to ground	1st I²C-bus address	1	-	-	MΩ
		2nd I²C-bus address	108	120	132	kΩ
		3rd I²C-bus address	29.7	33	36.3	kΩ
I²C-bus enable: pin BUSENABLE						
V_{IL}	LOW-level input voltage		–0.3	-	+1	V
V_{IH}	HIGH-level input voltage		2	-	V_{DDD} + 0.3	V
Software programmable ports: pins SWPORT1 and SWPORT2						
$I_{sink(max)}$	maximum sink current	bit SWPORT1 = 1	1	-	1.6	mA
		bit SWPORT2 = 1	1	-	1.6	mA
Weather band flag: pin WBFLAG						
$I_{source(max)}$	maximum source current	R = 560 Ω	–6	–5	–4	mA
$R_{i(shunt)}$	internal shunt resistance to ground		-	50	-	kΩ
$V_{o(FM)(max)}$	maximum output voltage for FM mode	measured with respect to pin RFGND	0	-	0.2	V
$V_{o(WB)}$	output voltage for weather band mode	measured with respect to pin RFGND	4	-	5	V
AM signal channel						
AM RF AGC: pins AMMIX1IN and AMMIX1DEC						
$V_{i(RF)(p)}$	RF input voltage for wideband AGC start level (peak value)	m = 0.3; f_{AF} = 1 kHz				
		AGC[1:0] = 00	375	530	750	mV
		AGC[1:0] = 01	300	420	590	mV
		AGC[1:0] = 10	210	290	410	mV
		AGC[1:0] = 11	110	150	210	mV
AM IF AGC stage inputs: pins AMIF2IN and AMIF2DEC						
$V_{i(IF2)}$	IF2 input voltage	AGC start level				
		m = 0	0.09	0.12	0.19	V
		m = 0.8	0.07	0.10	0.14	V
AM RF AGC PIN diode drive: pin IAMAGC						
$I_{sink(max)}$	maximum AGC sink current	V_{IAMAGC} = 2.8 V	9	14	18	mA
I_{sink}	AGC sink current	FM mode; V_{IAMAGC} = 2.8 V	1	1.5	2	mA
R_o	output resistance	I_{IAMAGC} = 1 µA	0.5	-	-	MΩ
C_o	output capacitance		-	5	7	pF
AM RF AGC cascode stage: pin VAMCAS						
V_{cas}	cascode voltage	$V_{AMMIX1IN-AMMIX1DEC}$ below threshold; maximum gain	4.5	5	5.5	V
I_{cas}	cascode transistor base current capability		100	-	-	µA
$I_{cas(off)}$	cascode transistor base off current	FM mode	-	-	100	nA

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1}$ = $V_{AMMIX2OUT2}$ = $V_{MIX1OUT1}$ = $V_{MIX1OUT2}$ = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM RF AGC cascode stage: pin VAMCASFB						
$V_{cas(FB)}$	cascode voltage	$V_{AMMIX1IN-AMMIX1DEC}$ above threshold; minimum gain	0.2	0.28	0.35	V
$I_{cas(FB)}$	cascode feedback sense current		0	0.4	1	μA
AM RF AGC transconductance buffer: pin AGCBUF [4]						
$g_{m(buf)}$	buffer transconductance $\frac{\Delta I_{AGCBUF}}{\Delta V_{TRFAMAGC}}$	AM mode; $\Delta V_{TRFAMAGC}$ = 50 mV to 0.4 V	0.85	1.1	1.35	mS
$I_{sink(max)}$	maximum sink current	AM mode; open-collector; $\Delta V_{TRFAMAGC}$ = 0.8 V	450	500	560	μA
$I_{source(max)}$	maximum source current	AM mode; $\Delta V_{TRFAMAGC}$ < 50 mV	-	-	−30	μA
$V_{o(n)}$	buffer output noise voltage	AM mode; $V_{DDA2} - V_{AGCBUF}$ = 1 V (voltage across external pull-up resistor); B = 400 Hz to 20 kHz	-	10	15	μV
AM mixer 1 (IF1 = 10.7 MHz)						
Mixer inputs: pins AMMIX1IN and AMMIX1DEC						
R_i	input resistance		15	25	40	kΩ
C_i	input capacitance		2.5	5	7.5	pF
V_I	DC input voltage		2.3	2.7	3.1	V
$V_{i(max)}$	maximum input voltage	1 dB compression point of AM mixer 1 output; m = 0	500	-	-	mV
Mixer outputs: pins MIX1OUT1 and MIX1OUT2						
R_o	output resistance		100	-	-	kΩ
C_o	output capacitance		-	4	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		12	15	-	V
I_{bias}	mixer bias current	AM mode	4.8	6	7.2	mA
Mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{IF1}}{V_{RF}}$		3.9	5.2	6.5	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		-	-9×10^{-4}	-	K^{-1}

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6}$ = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
IP3	3rd-order intermodulation	R_L = 2.6 kΩ (AC load between output pins); Δf = 300 kHz	135	138	-	dBμV
IP2	2nd-order intermodulation	R_L = 2.6 kΩ (AC load between output pins)	-	170	-	dBμV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 750 Ω; R_L = 2.6 kΩ (AC load between output pins)	-	5.8	8	$\frac{nV}{\sqrt{Hz}}$
F	noise figure of AM mixer 1		-	4.5	7.1	dB
AM mixer 2 (IF2 = 450 kHz)						
Mixer inputs: pins IFAMPIN and IFAMPDEC						
R_i	input resistance		-	330	-	Ω
C_i	input capacitance		-	5	7	pF
V_I	DC input voltage		2.4	2.7	3	V
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of AM mixer 2 output	1.1	1.4	-	V
Mixer outputs: pins AMMIX2OUT1 and AMMIX2OUT2						
R_o	output resistance		50	-	-	kΩ
C_o	output capacitance		-	4	7	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		12	15	-	V
I_{bias}	mixer bias current	AM mode	3.6	4.5	5.4	mA
I_L	mixer leakage current	FM mode	-	-	10	μA
Mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{IF2}}{V_{IF1}}$		3.2	4.3	5.4	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$		-	-9×10^{-4}	-	K^{-1}
IP3	3rd-order intermodulation	R_L = 1.5 kΩ (AC load between output pins); Δf = 300 kHz	134	137	-	dBμV
IP2	2nd-order intermodulation	R_L = 1.5 kΩ (AC load between output pins)	-	170	-	dBμV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; R_L = 1.5 kΩ (AC load between output pins)	-	15	22	$\frac{nV}{\sqrt{Hz}}$
F	noise figure of AM mixer 2		-	16	19.5	dB

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5$ V; $V_{DDA5} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM IF2 AGC stage: pins AMIF2IN and AMIF2DEC						
$G_{AGC(max)}$	maximum AGC amplifier gain	no AGC active	38	41	44	dB
$V_{AGC(start)}$	AGC start voltage (pin IFOUT)	–3 dB below maximum output level; $R_L = 1$ kΩ	93	-	98	dBμV
ΔAGC	AGC range	between start and stop of AGC	52	-	-	dB
THD	total harmonic distortion of IF2 output signal	AM signal; $f_{mod} = 400$ Hz; m = 0.8; $C_{TAMIF2AGC} = 4.7$ μF; $V_{AMIF2IN\text{-}AMIF2DEC} < 0.14$ V	-	-	0.3	%
$V_{i(n)(eq)}$	equivalent input noise voltage	$R_{gen} = 1.5$ kΩ	-	10.5	-	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		1.3	1.5	1.65	kΩ
C_i	input capacitance		-	-	5	pF
AM IF2 AGC stage: pin IFOUT						
$V_{o(rms)}$	AM IF2 output voltage (RMS value)	$R_L = 1$ kΩ; AGC active	63	84	112	mV
t_{st}	AM IF2 AGC settling time	$V_{AMIF2IN} = 10$ mV to 100 mV	-	60	-	ms
		$V_{AMIF2IN} = 100$ mV to 10 mV	-	360	-	ms
		$V_{AMIF2IN} = 140$ μV to 140 mV	-	150	-	ms
		$V_{AMIF2IN} = 140$ mV to 140 μV	-	600	-	ms
AM IF2 level detector output: pin VLEVEL; see Figure 4 [5]						
V_{VLEVEL}	DC output voltage	$V_i = 10$ μV to 1 V	0	-	5	V
		$V_i < 1$ μV; standard setting of level DAA	0.1	0.35	0.8	V
		$V_i = 1.4$ mV; standard setting of level DAA	1.6	2.2	2.8	V
ΔV_{level}	step size for adjustment of level starting point	$V_i = 0$ V; standard setting of level slope	40	53	70	mV
$V_{level(slope)}$	slope of level voltage $\frac{\Delta V_{level}}{\Delta V_{AMIF2IN\text{-}AMIF2DEC}}$	$V_i = 140$ μV to 140 mV; standard setting of level slope	0.8	1	1.2	$\frac{V}{20\ dB}$
ΔV_{step}	step size for adjustment of level slope	$V_i = 1.4$ mV	55	75	95	$\frac{mV}{20\ dB}$
B_{level}	bandwidth of level output voltage	$V_i = 15$ mV; standard setting of level DAA	200	300	-	kHz
R_o	output resistance		-	-	500	Ω
RR	ripple rejection $\frac{V_{VLEVEL}}{V_{DDA6}}$	$V_{DDA6(ripple)} = 100$ mV; $f_{ripple} = 100$ Hz	-	40	-	dB

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6}$ = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
AM noise blanker; AMNB = 1; test signal and test circuit; see Figure 3						
t_{sup}	suppression time	V_{pulse} = 250 mV; V_{VLEVEL} < 1.8 V	6	7.5	10	µs
$f_{trigger}$	trigger sensitivity frequency	V_{pulse} = 200 mV; V_{VLEVEL} < 1.8 V	-	1000	-	Hz
		V_{pulse} = 200 mV; V_{VLEVEL} > 2.2 V	-	-	100	Hz
		V_{pulse} = 20 mV; V_{VLEVEL} < 1.8 V	-	-	100	Hz
$I_{sink(AGC)}$	AM noise blanker AGC sink current	$V_{TAMNBAGC}$ = 3 V	35	50	65	µA
V_{AGC}	AM noise blanker AGC voltage (pin TAMNBAGC)	AM mixer 1 input V_i = 0 V	2	2.4	2.8	V
FM signal channel						
FM RF AGC (FM distance mode; LODX = 0)						
RF input: pins FMMIXIN1 and FMMIXIN2; KAGC = 0						
$V_{i(RF)}$	RF input voltage for start of wideband AGC	AGC[1:0] = 11	-	3	-	mV
		AGC[1:0] = 10	-	6	-	mV
		AGC[1:0] = 01	-	9	-	mV
		AGC[1:0] = 00	-	12	-	mV
FM RF AGC time constant: pin TFMAGC						
R_{source}	source resistance		4	5	6	kΩ
$V_{O(ref)}$	DC output reference voltage	AGC[1:0] = 00; KAGC = 0; $V_{FMMIXIN1\text{-}FMMIXIN2}$ = 0 V	3.6	4.1	4.6	V
FM RF AGC PIN diode drive output: pin IFMAGC						
$I_{sink(max)}$	maximum AGC sink current	V_{IFMAGC} = 2.5 V; $V_{TFMAGC} = V_{O(ref)} - 0.5$ V; AGC[1:0] = 00; KAGC = 0	8	11.5	15	mA
$I_{source(max)}$	maximum AGC source current	V_{IFMAGC} = 2.5 V; $V_{TFMAGC} = V_{O(ref)} + 0.5$ V; AGC[1:0] = 00; KAGC = 0	–15	–11.5	–8	mA
$I_{source(AGC)}$	AGC source current	AM mode	–15	–11.5	–8	mA
		V_{IFMAGC} = 2.5 V; LODX = 1	–4.4	–3.7	–2.7	mA
FM keyed AGC: pin VLEVEL						
V_{th}	threshold voltage for narrow-band AGC	KAGC = 1; $V_{TFMAGC} = V_{O(ref)} + 0.6$ V	0.6	0.75	0.9	V
FM RF AGC transconductance buffer: pin AGCBUF						
$g_{m(buf)}$	buffer transconductance	FM mode; $V_{TFMAGC} = V_{O(ref)}$ to $V_{O(ref)}$ + 80 mV	4	5.3	6.4	mS
$I_{sink(max)}$	maximum sink current	FM mode; open-collector; $V_{TFMAGC} = V_{O(ref)} + 0.15$ V	450	500	560	µA
$I_{source(max)}$	maximum source current	FM mode; $V_{TFMAGC} = V_{O(ref)}$	-	-	–30	µA

Table 33: Dynamic characteristics *…continued*

$V_{AMMIX2OUT1}$ = $V_{AMMIX2OUT2}$ = $V_{MIX1OUT1}$ = $V_{MIX1OUT2}$ = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{o(n)}$	buffer output noise voltage	FM mode; $V_{VDDA2\text{-}AGCBUF}$ = 1 V (voltage across external pull-up resistor); B = 400 Hz to 20 kHz	-	10	15	µV
FM RF mixer						
Reference voltage: pin VREFFMMIX						
V_{ref}	reference voltage	FM mode	6.6	7.3	8	V
		AM mode	2.7	3.1	3.4	V
Inputs: pins FMMIXIN1 and FMMIXIN2						
R_i	input resistance	MIXGAIN = 0	-	3.5	-	kΩ
		MIXGAIN = 1	-	1.8	-	kΩ
C_i	input capacitance		-	5	7	pF
V_{BIAS}	DC bias voltage	FM mode	2.2	2.7	3.2	V
$V_{i(RF)(p)}$	RF input voltage (peak value)	1 dB compression point of FM mixer output				
		MIXGAIN = 0	70	100	-	mV
		MIXGAIN = 1	35	50	-	mV
Outputs: pins MIX1OUT1 and MIX1OUT2						
R_o	output resistance		100	-	-	kΩ
C_o	output capacitance		2	3.5	5	pF
$V_{o(max)(p-p)}$	maximum output voltage (peak-to-peak value)		3	-	-	V
I_{bias}	mixer bias current	FM mode	4.8	6	7.2	mA
FM mixer						
$g_{m(conv)}$	conversion transconductance $\frac{I_{IF}}{V_{RF}}$	MIXGAIN = 0	8.5	12.5	18	$\frac{mA}{V}$
		MIXGAIN = 1	17	25	36	$\frac{mA}{V}$
$g_{m(conv)(T)}$	conversion transconductance variation with temperature $\frac{\Delta g_{m(conv)}}{g_{m(conv)} \times \Delta T}$	MIXGAIN = 0	-	-1×10^{-3}	-	K^{-1}
F	noise figure	MIXGAIN = 0	-	3.5	4.6	dB
		MIXGAIN = 1	-	2.4	-	dB
IP3	3rd-order intermodulation	MIXGAIN = 0	113	117	-	dBµV
		MIXGAIN = 1	-	108	-	dBµV

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5$ V; $V_{DDA5} = 5$ V; $V_{DDD} = 5$ V; $T_{amb} = 25$ °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
IRR	image rejection ratio	FMINJ = 1	[6]				
		$f_{RFwanted}$ = 87.5 MHz; $f_{RFimage}$ = 108.9 MHz		25	30	-	dB
		data byte 3 = X010X110; $f_{RFwanted}$ = 162.475 MHz; $f_{RFimage}$ = 183.875 MHz		22	30	-	dB
$V_{i(n)(eq)}$	equivalent input noise voltage (pin FMMIXIN1 to FMMIXIN2)	R_{gen} = 200 Ω; R_L = 2.6 kΩ					
		MIXGAIN = 0		-	2.9	3.1	$\frac{nV}{\sqrt{Hz}}$
		MIXGAIN = 1		-	2.6	-	$\frac{nV}{\sqrt{Hz}}$
$R_{gen(opt)}$	optimum generator resistance			-	200	-	Ω
FM IF amplifier (IBOC = 0)							
G	gain	R_L = 330 Ω; V_i = 1 mV	[7]				
		IFGAIN = 0		-	10.5	-	dB
		IFGAIN = 1		-	14	-	dB
F	noise figure	IFGAIN = 0		-	10	-	dB
		IFGAIN = 1		-	8.3	-	dB
IP3	3rd-order intermodulation	IFGAIN = 0		-	123	-	dBμV
		IFGAIN = 1		-	119	-	dBμV
Inputs: pins IFAMPIN and IFAMPDEC							
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of FM IF amplifier output voltage					
		IFGAIN = 0		400	-	-	mV
		IFGAIN = 1		250	-	-	mV
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω					
		IFGAIN = 0		-	8	10	$\frac{nV}{\sqrt{Hz}}$
		IFGAIN = 1		-	6.5	10	$\frac{nV}{\sqrt{Hz}}$
$V_{I(IFAMP)}$	DC voltage IF amplifier input	FM mode		2.2	2.7	3.2	V
R_i	input resistance			270	330	390	Ω
C_i	input capacitance			-	5	7	pF
Output: pin FMIFAMPOUT							
$V_{o(max)(p)}$	maximum output voltage (peak value)			1.2	1.5	-	V
$V_{O(IFAMP)}$	DC voltage IF amplifier output	FM mode		3	3.5	4	V

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1}$ = $V_{AMMIX2OUT2}$ = $V_{MIX1OUT1}$ = $V_{MIX1OUT2}$ = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6} = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_o	output resistance		270	330	390	Ω
C_o	output capacitance		-	5	7	pF
IBOC amplifier (IBOC = 1)						
G	gain		-	8	-	dB
IP3	3rd-order intermodulation		-	123	-	dBμV
Inputs: pins IFAMPIN and IFAMPDEC						
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω	-	5.2	10	$\frac{nV}{\sqrt{Hz}}$
$V_{i(max)(p)}$	maximum input voltage (peak value)	1 dB compression point of FM IF amplifier output voltage	420	-	-	mV
FM IF AGC						
G_{AGC}	small signal AGC amplifier gain $\frac{V_{IFOUT}}{V_{FMIFIN-FMIFDEC}}$	linear range: $V_{FMIFIN-FMIFDEC}$ = 25 μV to 1 mV; no AGC active	-	28.5	-	dB
ΔAGC	AGC range		59	-	-	dB
IP3	3rd-order intermodulation	$V_{FMIFIN-FMIFDEC}$ = 95 dBμV	-	121	-	dBμV
t_{st}	FM IF AGC settling time	V_{FMIFIN} = 1 mV to 10 mV	-	2	-	ms
		V_{FMIFIN} = 10 mV to 1 mV	-	1	-	ms
Inputs: pins FMIFIN and FMIFDEC						
$V_{i(IF)}$	IF input voltage for IF AGC start level	start of AGC	-	65	-	dBμV
$V_{i(max)(p)}$	maximum input voltage (peak value)		-	1.6	-	V
$V_{i(n)(eq)}$	equivalent input noise voltage	R_{gen} = 330 Ω; no AGC active	-	7	-	$\frac{nV}{\sqrt{Hz}}$
R_i	input resistance		270	330	390	Ω
C_i	input capacitance		-	5	7	pF
Output: pin IFOUT						
V_O	FM IF output voltage	R_L = 1 kΩ; AGC active	89	94	99	dBμV
FM IF level detector output: pin VLEVEL; see Figure 5 [8]						
V_{VLEVEL}	DC output voltage	V_i = 10 μV to 1 V	0	-	5	V
		V_i < 1 μV; standard setting of level DAA	0.1	0.35	0.8	V
		V_i = 1 mV; standard setting of level DAA	1.4	2	2.4	V
ΔV_{level}	step size for adjustment of level starting point	LSL[2:0] = 100	40	53	70	mV
$V_{level(slope)}$	slope of level voltage $\frac{\Delta V_{level}}{\Delta V_i}$	V_i = 1 mV to 300 mV; standard setting of level slope	0.8	1	1.2	$\frac{V}{20\ dB}$

Table 33: Dynamic characteristics *...continued*

$V_{AMMIX2OUT1} = V_{AMMIX2OUT2} = V_{MIX1OUT1} = V_{MIX1OUT2} = V_{DDA1} = V_{DDA2} = V_{DDA3} = V_{DDA4} = V_{DDA6}$ = 8.5 V; V_{DDA5} = 5 V; V_{DDD} = 5 V; T_{amb} = 25 °C; see Figure 8; all AC values are given in RMS; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_{step}	step size for adjustment of level slope	V_i = 1 mV	55	75	95	$\frac{mV}{20\ dB}$
B_{level}	bandwidth of level output voltage	V_i = 10 mV; standard setting of level DAA	200	300	-	kHz
I_{source}	output source current	$V_{level(ref)}$ − 60 mV; V_i = 1 mV	-	-	−300	μA
I_{sink}	output sink current	$V_{level(ref)}$ + 25 mV; V_i = 1 mV	50	-	-	μA
R_o	output resistance		-	-	500	Ω
RR	ripple rejection $\frac{V_{VLEVEL}}{V_{DDA6}}$	$V_{DDA6(ripple)}$ = 100 mV; f_{ripple} = 100 Hz	-	40	-	dB
FM IF/AM IF2 buffer						
Output: pin IFOUT						
$Z_{L(min)}$	minimum load impedance for IF multiplexer/buffer		1	-	-	kΩ
$V_{o(max)(p)}$	maximum output voltage (peak value)		-	-	750	mV
RDS update						
Output: pin AFHOLD; see Figure 6						
$I_{sink(max)}$	maximum sink current	after first bus transmission with AF = 1; V_o = 0.5 V	1	1.2	1.4	mA

[1] Measured between pins XTAL1 and XTAL2.

[2] DAA conversion gain formula: $V_{DAAOUT} = \left[2 \times \left(0.75 \times \frac{n}{128} + 0.125\right) \times (V_{DAAIN} + V_{DAATD})\right] - V_{DAATD}$; where n = 0 to 127.

[3] $V_{LSB} = V_{DAAOUT(n+1)} - V_{DAAOUT(n)}$

[4] The AM AGC transconductance buffer delivers a sink current which is proportional to the voltage change at pin TRFAMAGC.

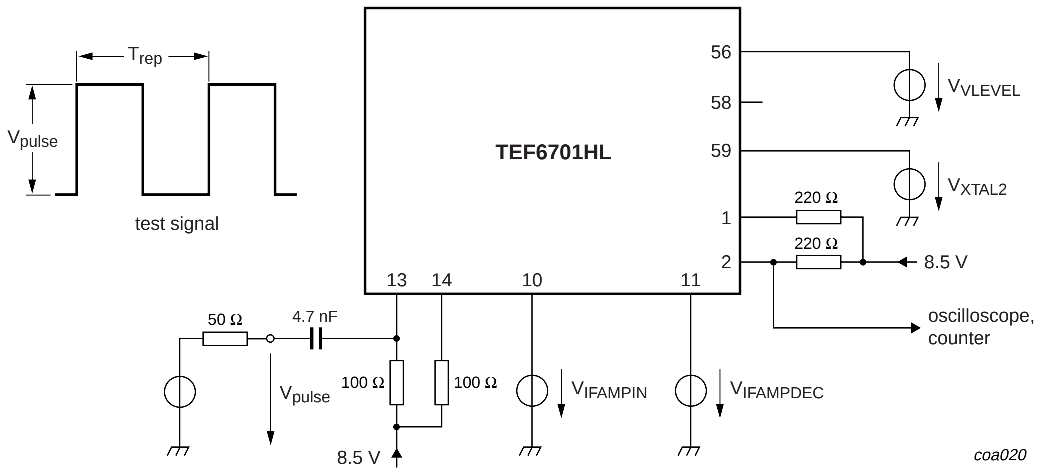
$$\Delta V_{TRFAMAGC} = V_{TRFAMAGC} - V_{TRFAMAGC}\Big|_{(V_{AMMIX1IN} - V_{AMMIX1DEC}) < 10\ mV}$$

[5] Input parameters of AM IF2 measured between pins AMIF2IN and AMIF2DEC.

[6] Image rejection ratio: $IRR = \frac{V_{(MIX1OUT1\text{-}MIX1OUT2)wanted}}{V_{(MIX1OUT1\text{-}MIX1OUT2)image}}$

[7] Input parameters of FM IF amplifier measured between pins IFAMPIN and IFAMPDEC.

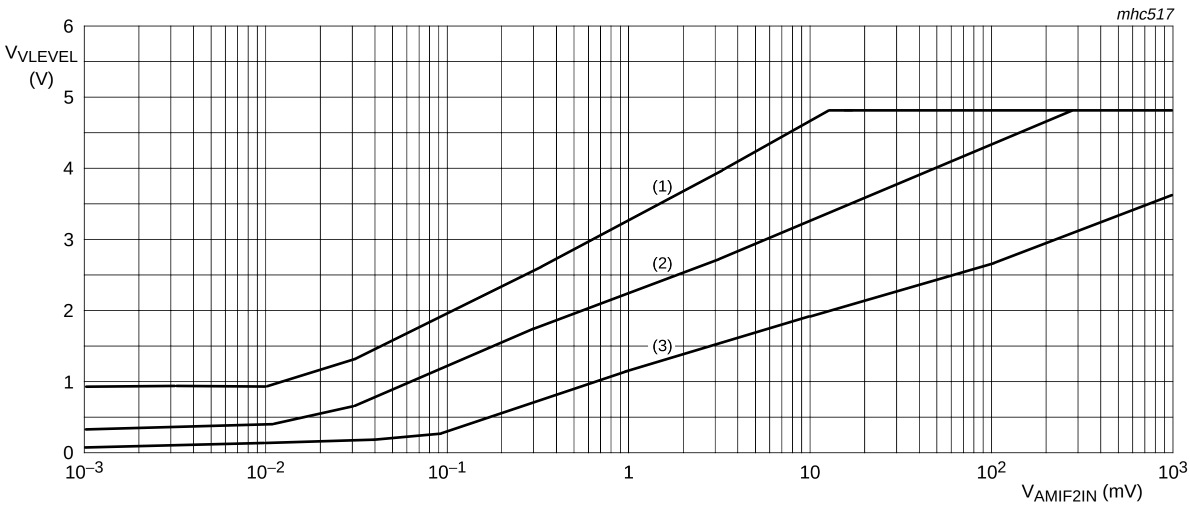
[8] Input parameters of FM IF level detector measured between pins FMIFIN and FMIFDEC.



Test signal: T_{rep} = 2 ms, t_r < 50 ns, t_f < 50 ns and duty factor 50 %.

V_{XTAL2} = 3 V; $V_{IFAMPIN}$ = 4 V and $V_{IFAMPIN\text{-}IFAMPDEC}$ = 0.2 V.

Fig 3. Test circuit for AM noise blanker.

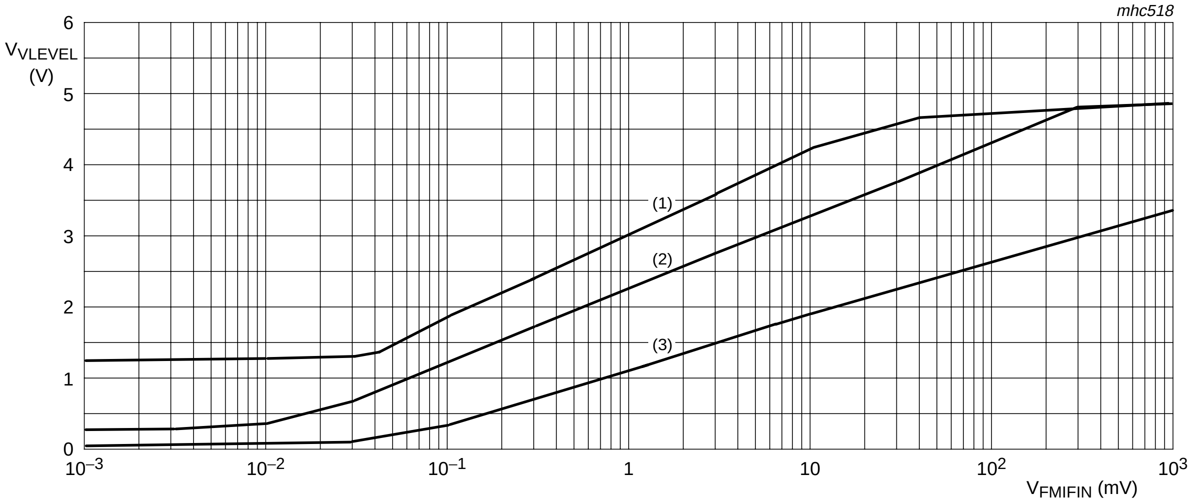


(1) Level DAA setting byte 5 = FFH.

(2) Level DAA setting byte 5 = 84H (standard setting).

(3) Level DAA setting byte 5 = 00H.

Fig 4. AM level output voltage (DAA) as a function of AM level circuit input voltage.

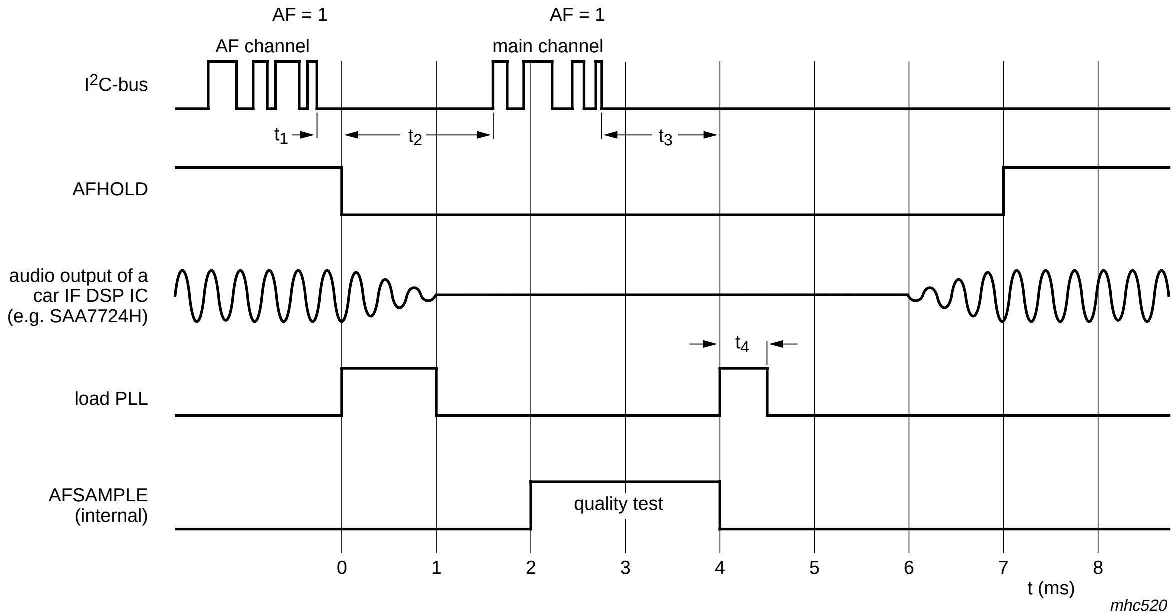


(1) Level DAA setting byte 5 = FFH.

(2) Level DAA setting byte 5 = 84H (standard setting).

(3) Level DAA setting byte 5 = 00H.

Fig 5. FM level output voltage (DAA) as a function of FM level circuit input voltage.



AFHOLD signal is used to hold the quality information for signal processing of the main channel during the alternative frequency jumps. PLL registers are loaded during load PLL = 1, but actual frequency jumps take place at the falling edge of this signal. IF counting is carried out during AFSAMPLE = 1. 10 µs after falling edge of AFSAMPLE result is valid for AF and remains valid until read by microcontroller. Quality tests in a car IF DSP IC (e.g. SAA7724H) should take place 2 ms after falling edge of AFHOLD.

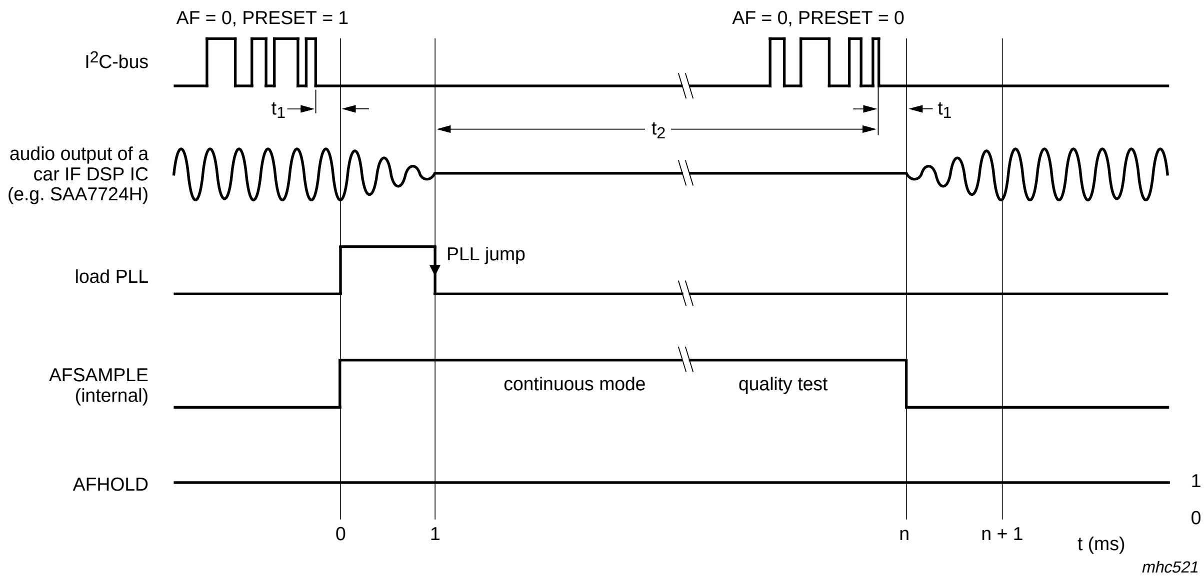
t_1 is the internal TEF6701HL clock related logic delay: 100 µs.

t_2 should be > 1.1 ms to ensure correct loading of PLL for the main channel.

t_3 should be > 0 to ensure inaudible update.

t_4 = 500 µs.

Fig 6. Inaudible AF update timing diagram.



t_1 is the internal TEF6701HL clock related logic delay: 100 µs.

t_2 should be greater than the required PLL tuning time for the given band (FM: $t_2 > 1$ ms; AM: $t_2 > 20$ ms).

Fig 7. Preset mode timing diagram.

14. Application information

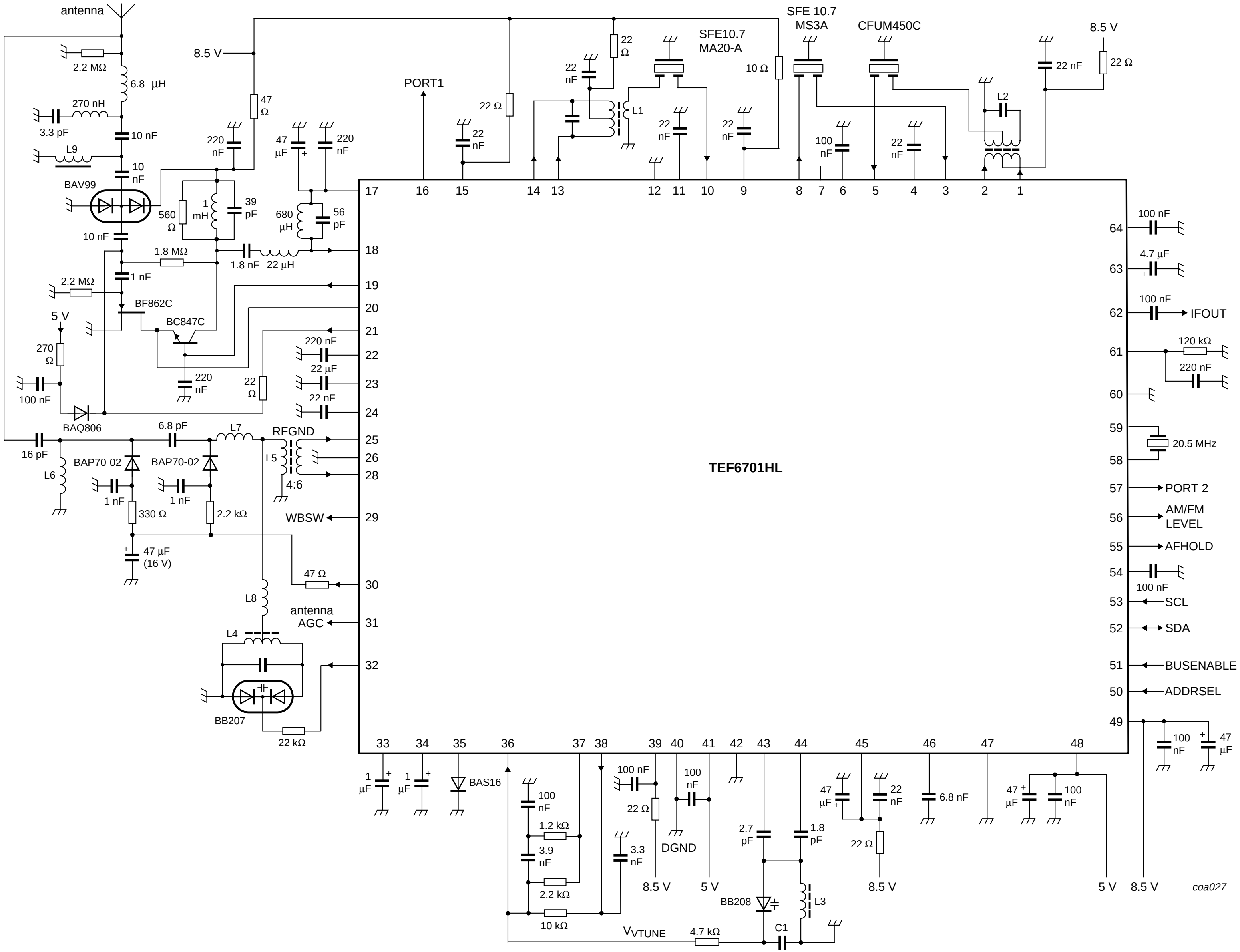
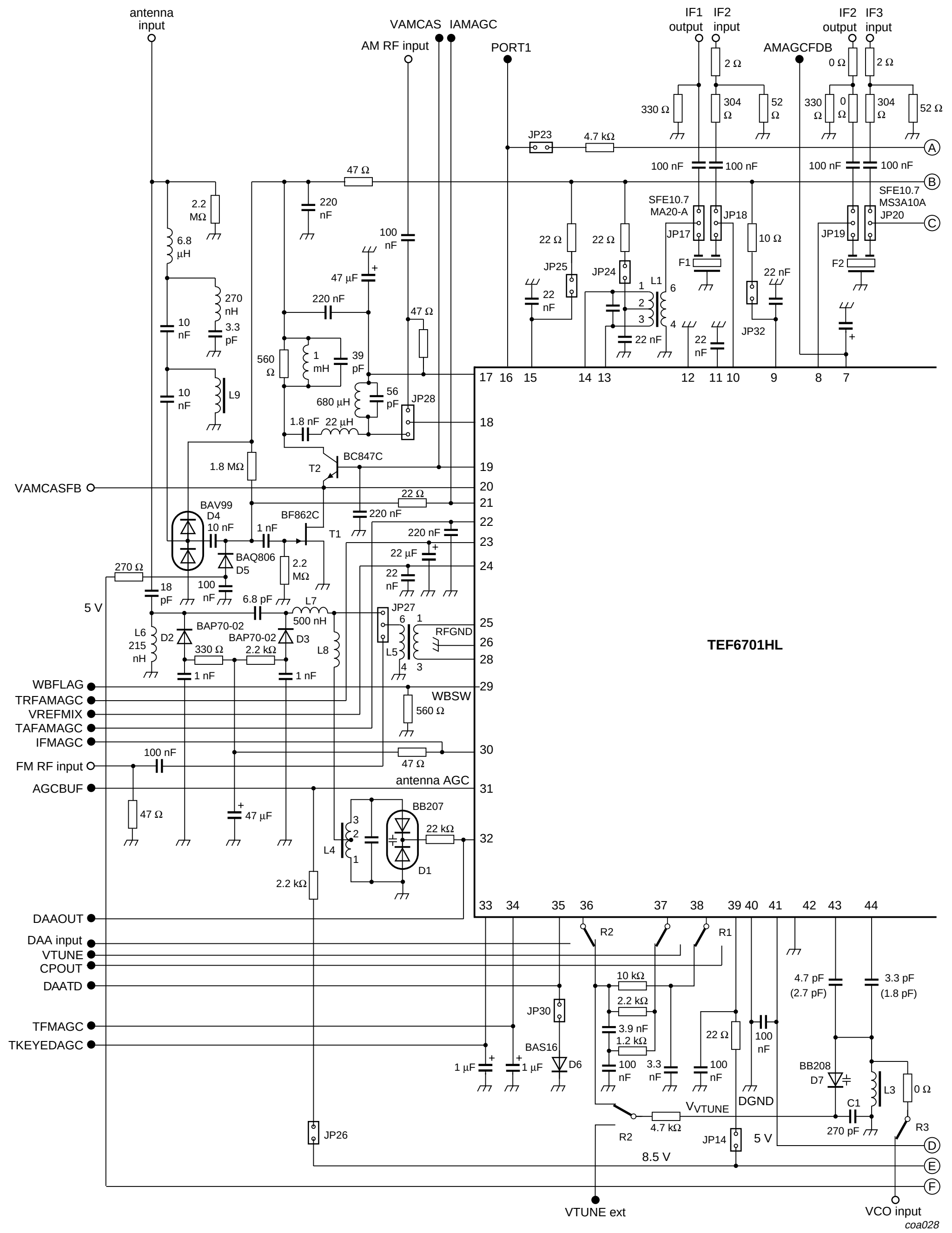


Fig 8. Application diagram.

Table 34: List of components

Symbol	Parameter	Type	Manufacturer
C1	capacitor for VCO tuning	270 pF; type NP0	
L1	10.7 MHz IF coil	P7 PSG P826RC 5134N=S	TOKO
L2	450 kHz IF coil	P7PSGAE-5078D=S	TOKO
L3	oscillator coil	E543SNAS-02010	TOKO
L4	FM image rejection	611SNS-1066Y	TOKO
L5	FM input transformer	369INS-3076X	TOKO
L6	FM antenna coil	LQN1HR50; 215 nH	MURATA
L7	PIN diode bias	LQN1HR21; 500 nH	MURATA
L8	connection image reject	wire 10 mm/printed coil	
L9	AM input	388BN-1211Z	TOKO
D1	double varicap diode	BB207	Philips
D2	silicon PIN diode	BAP70-02	Philips
D3	silicon PIN diode	BAP70-02	Philips
D4	high-speed double diode	BAV99	Philips
D5	AM PIN diode	BAQ806	Philips
D6	high-speed diode	BAS16	Philips
D7	varicap diode	BB208	Philips
T1	N-channel junction FET	BF862C	Philips
T2	NPN general purpose transistor	BC847C	Philips
F1	ceramic filter	10.7 MHz	MURATA
F2	ceramic filter	10.7 MHz	MURATA
F3	ceramic filter	450 kHz	MURATA
	crystal 20.5 MHz	LN-G102-587	NDK

15. Test information



For list of components see Table 34.

Fig 9. Test circuit (continued in Figure 10).

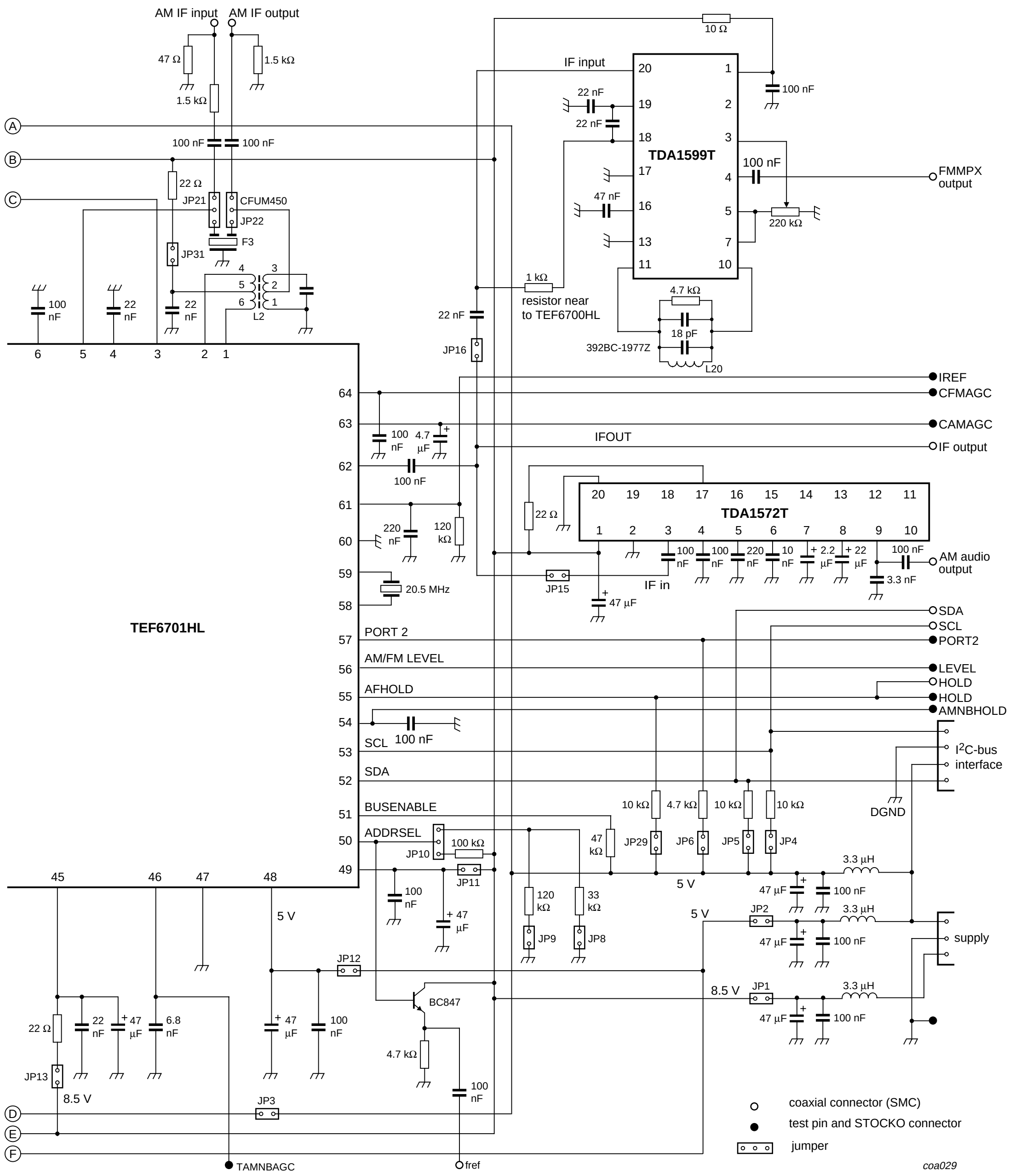


Fig 10. Test circuit (continued from Figure 9).

Table 35: DC operating points

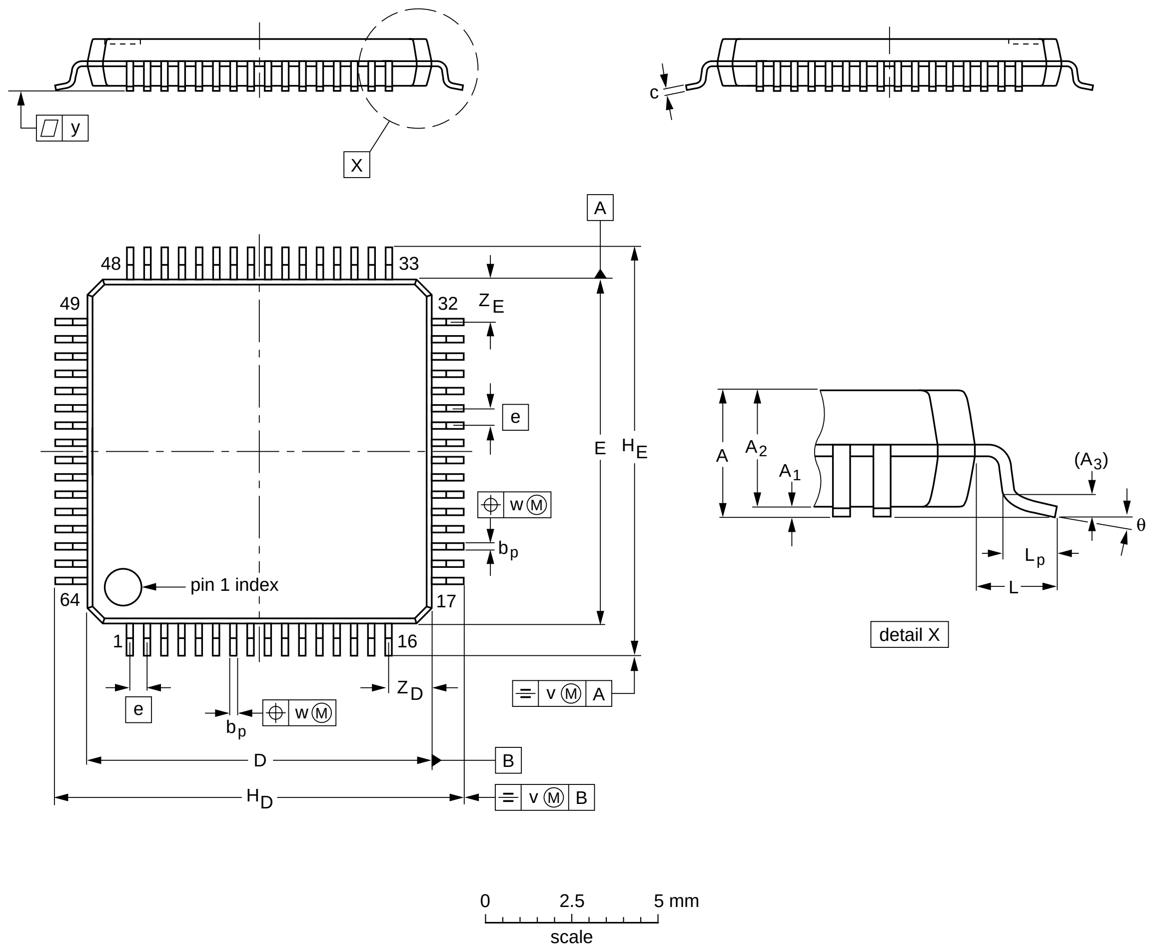
Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
AMMIX2OUT1	1	external 8.5			external 8.5		
AMMIX2OUT2	2	external 8.5			external 8.5		
FMIFIN	3	-	3.3	-	-	3.3	-
FMIFDEC	4	-	3.3	-	-	3.3	-
AMIF2IN	5	-	3	-	floating		
AMIF2DEC	6	-	3	-	floating		
i.c.	7	-	5.6	-	-	5.6	-
FMIFAMPOUT	8	-	8.1	-	-	4	-
V_{DDA1}	9	external 8.5			external 8.5		
IFAMPIN	10	-	2.9	-	-	2.7	-
IFAMPDEC	11	-	2.9	-	-	2.7	-
IFAMPGND	12	external 0			external 0		
MIX1OUT1	13	external 8.5			external 8.5		
MIX1OUT2	14	external 8.5			external 8.5		
V_{DDA2}	15	external 8.5			external 8.5		
SWPORT1	16	open-collector			open-collector		
AMMIX1DEC	17	-	2.8	-	floating		
AMMIX1IN	18	external biasing			floating		
VAMCAS	19	-	4.8	-	0	0.1	0.2
VAMCASFB	20	-	4.1	-	0	0.1	1
IAMAGC	21	7.1 (external biasing)			external biasing		
TAFAMAGC	22	-	0.3	-	0 (no WB)	0.3 (no WB)	0.5 (no WB)
TRFAMAGC	23	-	2.9	-	floating		
VREFFMMIX	24	-	3.2	-	-	7.3	-
FMMIXIN1	25	-	1.65	-	-	2.75	-
RFGND	26	external 0			external 0		
i.c.	27	external 0			external 0		
FMMIXIN2	28	-	1.65	-	-	2.75	-
WBFLAG	29	0			4 (WB)	4.5 (WB)	5 (WB)
					- (FM)	< 0.5 (FM)	- (FM)
IFMAGC	30	5 (external biasing)			0.1 (external biasing)	-	4 (external biasing)
AGCBUF	31	8.5 (external biasing)			8.5 (external biasing)		
DAAOUT	32	-	0.2	0.3	0.2	-	8.25
TKEYEDAGC	33	floating			1	-	7
TFMAGC	34	7.8	8.3	8.8	-	4	-
DAATD	35	floating		1.5	0.2	-	1.5
DAAIN	36	0	-	8.5	0	-	8.5
VTUNE	37	0	-	8.5	0	-	8.5

Table 35: DC operating points *...continued*

Symbol	Pin	Unloaded DC voltage (V)					
		AM mode			FM mode		
		Min	Typ	Max	Min	Typ	Max
CPOUT	38	0	-	8.5	0	-	8.5
V_{DDA3}	39	external 8.5			external 8.5		
DGND	40	external 0			external 0		
V_{DDD}	41	external 5			external 5		
VCOGND	42	external 0			external 0		
OSCFDB	43	2.2	2.8	3.4	2.2	2.8	3.4
OSCTNK	44	5	6.1	7.2	5	6.1	7.2
V_{DDA4}	45	external 8.5			external 8.5		
TAMNBAGC	46	-	2.4	-	floating		
IFGND	47	external 0			external 0		
V_{DDA5}	48	external 5			external 5		
V_{DDA6}	49	external 8.5			external 8.5		
ADDRSEL	50	-	3.6	-	-	3.6	-
BUSENABLE	51	external biasing			external biasing		
SDA	52	external biasing			external biasing		
SCL	53	external biasing			external biasing		
AMNBHOLD	54	4.3	4.6	5.1	8	8.4	-
AFHOLD	55	open-collector			open-collector		
VLEVEL	56	0	-	5	0	-	5
SWPORT2	57	open-collector			open-collector		
XTAL1	58	1.7	2.1	2.5	1.7	2.1	2.5
XTAL2	59	1.7	2.1	2.5	1.7	2.1	2.5
XTALGND	60	external 0			external 0		
IREF	61	4	4.25	4.5	4	4.25	4.5
IFOUT	62	-	2.5	-	-	4.6	-
TAMIF2AGC	63	-	4	-	-	4.2	-
TFMIFAGC	64	-	5	-	-	4.8	-

16. Package outline

LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm **SOT314-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				~~00-01-19~~ 03-02-25

Fig 11. Package outline SOT314-2 (LQFP64).

17. Soldering

17.1 Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *Data Handbook IC26; Integrated Circuit Packages* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering can still be used for certain surface mount ICs, but it is not suitable for fine pitch SMDs. In these situations reflow soldering is recommended.

17.2 Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement. Driven by legislation and environmental forces the worldwide use of lead-free solder pastes is increasing.

Several methods exist for reflowing; for example, convection or convection/infrared heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 seconds and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 °C to 270 °C depending on solder paste material. The top-surface temperature of the packages should preferably be kept:

- below 225 °C (SnPb process) or below 245 °C (Pb-free process)
  - for all BGA, HTSSON..T and SSOP..T packages
  - for packages with a thickness ≥ 2.5 mm
  - for packages with a thickness < 2.5 mm and a volume ≥ 350 mm^3 so called thick/large packages.
- below 240 °C (SnPb process) or below 260 °C (Pb-free process) for packages with a thickness < 2.5 mm and a volume < 350 mm^3 so called small/thin packages.

Moisture sensitivity precautions, as indicated on packing, must be respected at all times.

17.3 Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;

– smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

The footprint must incorporate solder thieves at the downstream end.

- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time of the leads in the wave ranges from 3 seconds to 4 seconds at 250 °C or 265 °C, depending on solder material applied, SnPb or Pb-free respectively.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

17.4 Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 seconds to 5 seconds between 270 °C and 320 °C.

17.5 Package related soldering information

Table 36: Suitability of surface mount IC packages for wave and reflow soldering methods

Package [1]	**Soldering method**	
	Wave	**Reflow** [2]
BGA, HTSSON..T [3], LBGA, LFBGA, SQFP, SSOP..T [3], TFBGA, VFBGA, XSON	not suitable	suitable
DHVQFN, HBCC, HBGA, HLQFP, HSO, HSOP, HSQFP, HSSON, HTQFP, HTSSOP, HVQFN, HVSON, SMS	not suitable [4]	suitable
PLCC [5], SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended [5] [6]	suitable
SSOP, TSSOP, VSO, VSSOP	not recommended [7]	suitable
CWQCCN..L [8], PMFP [9], WQCCN..L [8]	not suitable	not suitable

[1] For more detailed information on the BGA packages refer to the *(LF)BGA Application Note* (AN01026); order a copy from your Philips Semiconductors sales office.

[2] All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods*.

[3] These transparent plastic packages are extremely sensitive to reflow soldering conditions and must on no account be processed through more than one soldering cycle or subjected to infrared reflow soldering with peak temperature exceeding 217 °C ± 10 °C measured in the atmosphere of the reflow oven. The package body peak temperature must be kept as low as possible.

[4] These packages are not suitable for wave soldering. On versions with the heatsink on the bottom side, the solder cannot penetrate between the printed-circuit board and the heatsink. On versions with the heatsink on the top side, the solder might be deposited on the heatsink surface.

[5] If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.

[6] Wave soldering is suitable for LQFP, QFP and TQFP packages with a pitch (e) larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.

[7] Wave soldering is suitable for SSOP, TSSOP, VSO and VSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

[8] Image sensor packages in principle should not be soldered. They are mounted in sockets or delivered pre-mounted on flex foil. However, the image sensor package can be mounted by the client on a flex foil by using a hot bar soldering process. The appropriate soldering profile can be provided on request.

[9] Hot bar soldering or manual soldering is suitable for PMFP packages.

18. Revision history

Table 37: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
TEF6701HL_1	20041116	Product data sheet	-	9397 750 13471	-

19. Data sheet status

Level	Data sheet status [1]	Product status [2] [3]	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
II	Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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