T-42-11-09

FUJITSU

UHB SERIES 1.5μ CMOS GATE ARRAYS

MB62XXXX
MB60XXXX

September 1988
Edition 1.1

DESCRIPTION

The UHB series of 1.5-micron CMOS gate arrays is a highly integrated low-power, ultra high-speed product family that derives its enhanced performance and increased user flexibility from the use of a system-proven, dual-column gate structure and 2-layer metal interconnect technology. The unique dual-column gate structure increases density and speed performance, as well as gate utilization.

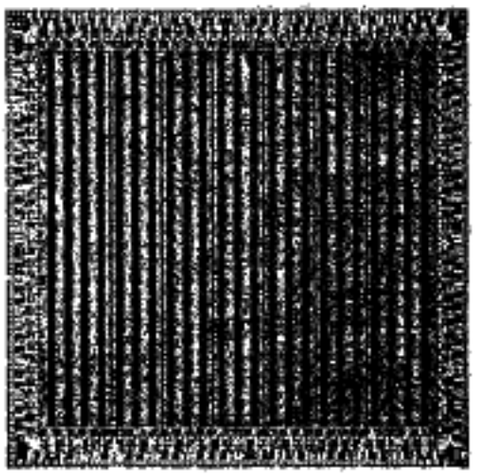
Internal high-drive clock buffers minimize clock skew across the chip while internal bus performance and integrity is assured by incorporating 3-state transmission gate logic underneath the routing channels. The high-drive output buffers provide highly symmetrical output waveforms.

FEATURES

- High-density silicon gate CMOS technology
  - 330 to 12,000 usable gates
  - 90% maximum utilization fully autorouted
- Ultra high speed
  - typical 0.9 ns gate delay
  - narrow delay variation
- High sink current capability
  - 3.2 mA, 8 mA, 12 mA, and 24 mA options available
  - selectable edge rate control
- Low-skew clock signal distribution
  - High-performance clock drivers
  - Hierarchical clock distribution
  - Frequency-dependent clock routing
- Automatic test pattern generation for 8K gates and up
  - complete family of scan design macros available
- 2-column gate structure enhances macro performance
- High-performance internal 3-state bus
  - buried cells within the routing channels ensure high density and reliable performance
- Proven 1.5-micron 2-layer metal technology
- Highest pin-to-gate count commercially available
  - 60 logic I/O for 336 gates
  - 222 logic I/O for 1200 gates
- Input buffers incorporating pull-up/pull-down resistance
- Built-in feedback resistors for oscillators
- User-defined hierarchy-driven placement

Device Name	Utilizable Gates[1]	Maximum Signal Pins[2]
C-330UHB	336 gates	60
C-630UHB	630 gates	66
C-830UHB	830 gates	76
C-1200UHB	1233 gates	92
C-1700UHB	1724 gates	106
C-2200UHB	2220 gates	123
C-3000UHB	3066 gates	148
C-4100UHB	4174 gates	163
C-6000UHB	6000 gates	163
C-8700UHB	8768 gates	188
C-12000UHB	12734 gates	220

1. Gates available for logic (exclusive of I/O usage).
2. Maximum signal pin numbers depend on the output drive requirements and the package selected.



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PRODUCT FAMILY DESCRIPTIONS

Device Name	Part Number	2-Input Gate Equivalent Complexity	Maximum Signal Pins	Total Number of Basic Cells on Chip
C-330UHB	MB625xxx	336 gates	60	610 gates
C-530UHB	MB624xxx	530 gates	66	840 gates
C-830UHB	MB623xxx	830 gates	76	1176 gates
C-1200UHB	MB622xxx	1233 gates	92	1680 gates
C-1700UHB	MB621xxx	1724 gates	108	2232 gates
C-2200UHB	MB620xxx	2220 gates	123	2800 gates
C-3000UHB	MB606xxx	3066 gates	148	3744 gates
C-4100UHB	MB606xxx	4174 gates	163	4888 gates
C-6000UHB	MB604xxx	6000 gates	163	6978 gates
C-8700UHB	MB603xxx	8768 gates	186	9720 gates
C-12000UHB	MB602xxx	12734 gates	220	13728 gates

Notes: 1. Typical device gate speed, with F/O=2, for a 2-input NAND gate, is 0.9 ns.
2. A basic cell is equivalent to a 2-input gate.
3. Basic cells on chip are also used for I/O buffer function.
4. The maximum signal pin numbers depend on the output drive requirements and the package selection.

AC CHARACTERISTICS

BEST/WORST CASE MULTIPLIERS FOR PROPAGATION DELAYS

Propagation delays characteristic of a gate array are a function of several factors, including operating temperature, supply voltage, fanout loading, interconnection routing metal, process variation, input transition time, and input signal polarity. Temperature and supply voltage factors affecting propagation delays in the UHB CMOS family of gate arrays are given in the table below.

Temperature Range	Pre-Layout Simulation				Post-Layout Simulation			
	V_{DD} = 5V± 5%		V_{DD} = 5V±10%		V_{DD} = 5V± 5%		V_{DD} = 5V±10%	
	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case	Best Case	Worst Case
1. 0 – 70°C	0.35	1.65	0.30	1.75	0.40	1.60	0.35	1.70
2. -20 – 70°C	0.35	1.65	0.25	1.75	0.35	1.60	0.30	1.70
3. -40 – 70°C	0.25	1.65	0.20	1.75	0.30	1.60	0.25	1.70
4. -40 – 85°C	0.25	1.75	0.20	1.85	0.30	1.70	0.25	1.80

1. = commercial temperature range

4. = industrial temperature range

Constants for calculating the delays due to process variation, fanout loading, interconnection routing metal, transition time, and signal polarity are given for each unit cell in the UHB Unit Cell Library. Delays using these factors are calculated for a representative selection of unit cells and are shown in the Propagation Delays table on the following page.

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REPRESENTATIVE PROPAGATION DELAYS

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS Gate Array).
Typical values are indicated. Worst case multipliers are applied to typical values. Smaller arrays can exhibit significantly greater speed.

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition	Propagation Delays (in ns)					
				NDI (Fan-out)					
				1	2	4	8	16	32
Inverter	V1N	1	t_{PLH}, t_{PHL}	0.88 0.67	1.51 1.04	2.38 1.62	3.53 2.18	5.19 3.11	8.09 4.74
Power 2-Input NAND	N2K	2	t_{PLH}, t_{PHL}	0.66 0.68	.99 .97	1.41 1.34	1.99 1.85	2.83 2.58	4.27 3.85
Power 16-Input NAND	N0B	11	t_{PLH}, t_{PHL}	1.82 3.69	2.15 3.93	2.67 4.25	3.15 4.69	3.99 5.31	5.43 6.40
Power 2-Input NOR	R2K	2	t_{PLH}, t_{PHL}	0.95 0.67	1.53 0.91	2.27 1.23	3.29 1.67	4.75 2.29	7.28 3.06
Power Exclusive OR	X2B	4	t_{PLH}, t_{PHL}	1.72 1.62	2.05 2.03	2.47 2.29	3.06 2.66	3.89 3.18	5.33 4.06
3-wide 2-AND 6-Input AND-OR Inverter (A→Y)	D36	3	t_{PLH}, t_{PHL}	1.76 1.22	2.93 1.80	4.41 2.54	6.45 3.58	9.37 5.02	4.43 7.65
2-wide 2-OR 4-Input OR-AND-Inverter (A→X)	G24	2	t_{PLH}, t_{PHL}	1.54 1.20	2.73 1.78	4.27 2.62	6.39 3.64	9.40 5.00	14.65 7.53
Power 2-AND 8-Wide Multiplexer (A→X)	T2B	11	t_{PLH}, t_{PHL}	2.41 1.66	2.74 1.83	3.16 2.04	3.74 2.33	4.58 2.75	6.02 3.47
Power Clock Buffer	K2B	3	t_{PLH}, t_{PHL}	1.30 1.38	1.57 1.58	1.90 1.83	2.30 2.13	2.81 2.51	3.61 3.11
Scan 8-bit D FF with Clock Inhibit and 2:1 Data Multiplexer (CK,IH→Q)	SHK	88	t_{PLH}, t_{PHL}	5.22 4.82	5.87 5.29	6.72 5.77	7.89 6.43	9.55 7.36	12.45 8.99
Non-Scan D FF with Reset (CK→Q)	FDO	7	t_{PLH}, t_{PHL}	2.51 2.14	3.16 2.55	4.01 3.06	5.18 3.81	6.84 4.85	9.74 6.66
Non-Scan Power D FF with Clear (CK→Q)	FD5	8	t_{PLH}, t_{PHL}	2.17 1.89	2.50 2.10	2.92 2.35	3.50 2.73	4.34 3.25	5.78 4.15
Non-Scan 4-bit Binary Synchronous Up Counter (CI→CO)	C43	48	t_{PLH}, t_{PHL}	2.18 1.10	2.83 1.43	3.68 1.85	4.85 2.43	6.51 3.27	9.41 4.71
Non-Scan 4-bit Binary Synchronous Up Counter (CI→CO)	C45	48	t_{PLH}, t_{PHL}	2.52 1.68	3.22 2.05	4.12 2.53	5.36 3.19	7.13 4.12	10.21 5.75

Note: Delays for inter-block wiring are not included

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REPRESENTATIVE PROPAGATION DELAYS (Continued)

Calculations are representative of unit cells in the C12000UHB (UHB 12000-Gate CMOS Gate Array).
Typical values are indicated. Worst case multipliers are applied to typical values.

Unit Cell Function	Unit Cell Name	Equivalent Gate Count	Input Transition	Propagation Delays (in ns)					
				NDI (Fan-out)					
				1	2	4	8	16	32
Non-Scan 4-bit Binary Synchronous Up/Down Counter (DU→CO)	C47	68	t_{PLH}, t_{PHL}	2.87 3.30	3.32 3.63	3.90 4.05	4.70 4.63	5.85 5.47	7.84 6.91
4-bit Binary Full Adder with Fast Carry (CI→S1)	A4H	48	t_{PLH}, t_{PHL}	1.97 2.13	2.67 2.71	4.04 3.45	5.65 4.47	7.93 5.93	11.92 8.48
4:1 Selector (S5→X)	T5A	5	t_{PLH}, t_{PHL}	1.39 1.12	2.33 1.77	3.56 2.62	5.23 3.79	7.62 5.46	11.79 8.35
4-bit Shift Register with Synchronous Load	FS2	30	t_{PLH}, t_{PHL}	2.90 3.46	3.55 3.83	4.40 4.31	5.57 4.97	7.23 5.90	10.13 7.53
9-bit Odd Parity Generator/Checker	PO9	22	t_{PLH}, t_{PHL}	5.76 6.00	6.43 6.33	7.28 6.75	8.45 7.33	10.11 8.17	13.01 9.61
4-wide 2:1 Data Selector (A→X)	P24	12	t_{PLH}, t_{PHL}	1.24 0.97	1.57 1.14	1.99 1.35	2.57 1.64	3.41 2.06	4.65 2.78
4-bit Magnitude Comparator (IS→OG)	MC4	42	t_{PLH}, t_{PHL}	3.17 2.60	4.36 2.93	5.90 3.35	8.02 3.93	11.03 4.77	16.28 6.21
4-bit Bus Driver (A→X)	B41	9	t_{PLH}, t_{PHL}	1.99 1.87	2.48 2.29	3.06 2.78	3.76 3.39	4.64 4.14	6.04 5.34
Input Buffer (Inverter)	I1B	5	t_{PLH}, t_{PHL}	1.84 1.78	2.11 2.05	2.44 2.36	2.84 2.78	3.35 3.29	4.15 4.09
Clock Input Buffer (Inverter)	IKB	4	t_{PLH}, t_{PHL}	2.49 1.94	2.63 2.08	2.79 2.24	2.99 2.44	3.24 2.69	3.64 3.09
				Output Buffer Load in pF					
				12	25	50	100	200	400
Output Buffer (True)	O2B	2	t_{PLH}, t_{PHL}	2.37 3.24	3.10 4.85	4.50 7.85	7.30 14.15	12.90 26.55	24.10 51.35
Power Output Buffer (True)	O2L	2	t_{PLH}, t_{PHL}	2.53 2.47	3.02 3.01	3.94 4.03	5.79 6.08	9.49 10.18	16.89 18.38
3-State Output Buffer (True)	O4T	4	t_{PLH}, t_{PHL}	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.52	13.62 28.52	24.82 54.52
Power 3-State Output Buffer (True)	O4W	4	t_{PLH}, t_{PHL}	3.48 4.68	3.97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92
3-State Output and Input Buffer (True)	H6T	8	t_{PLH}, t_{PHL}	3.09 4.08	3.82 5.77	5.22 9.02	8.02 15.57	13.62 28.52	24.82 54.52
Power 3-State Output and Input Buffer (True)	H6W	8	t_{PLH}, t_{PHL}	3.48 4.68	3.97 5.30	4.92 6.47	6.82 8.82	10.62 13.52	18.22 22.92

Note: Delays for inter-block wiring are not included

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DC CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS[1]

Rating		Symbol	Minimum	Maximum	Unit
Supply Voltage		V_{DD}	V_{SS}[2] −0.5	6.0	V
Input Voltage		V_I	V_{SS}[2] −0.5	V_{DD}+0.5	V
Output Voltage		V_O	V_{SS}[2] −0.5	V_{DD}+0.5	V
Output Current[3]	I_{OL}=3.2mA	I_{OS}	−40	+40	mA
	I_{OL}=8mA		−40	+80	
	I_{OL}=12mA		−60	+120	
	I_{OL}=24mA		−80	+160	
Storage Temperature	Ceramic Plastic	T_{stg}	−65 −40	+150 +125	°C
Temperature Under Bias	Ceramic Plastic	T_{bias}	−40 −25	+125 +85	°C

Notes: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to the conditions as detailed in the operation sections of the data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Vss = 0V.
3. Only one output at a time may be shorted for more than one second.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply Voltage	V_{DD}	4.75	5.0	5.25	V
Input High Voltage for TTL Input	V_{IH}	2.2	–	–	V
Input Low Voltage for TTL Input	V_{IL}	–	–	0.8	V
Input High Voltage for CMOS Input	V_{IH}	V_{DD} x 0.7	–	–	V
Input Low Voltage for CMOS Input	V_{IL}	–	–	V_{DD} x 0.3	V
Operating Temperature	T_A	0	–	70	°C

CAPACITANCE (T_A = 25°C, V_{DD} = V_I = 0V, f = 1 MHz)

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Pin Capacitance	C_{IN}	–	–	16	pF
Output Pin Capacitance (I_{OL}=3.2mA, 8mA or 12mA)	C_{OUT}	–	–	16	pF
Output Pin Capacitance (I_{OL}=24mA)	C_{OUT}	–	–	18	pF
I/O Pin Capacitance (I_{OL}=3.2mA, 8mA or 12mA)	$C_{I/O}$	–	–	16	pF
I/O Pin Capacitance (I_{OL}=24mA)	$C_{I/O}$	–	–	23	pF

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DC CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter	Symbol	Condition	Minimum	Typical	Maximum	Unit
Power Supply Current	I_{DDS}	Steady State[1]	0	—	100	µA
Output High Voltage for Normal Output (IOL =3.2mA)	V_{OH}	I_{OH} = -2mA	4.0	—	V_{DD}	V
Output High Voltage for Driver Output (IOL =8mA)	V_{OH}	I_{OH} = -2mA	4.0	—	V_{DD}	V
Output High Voltage for Driver Output (IOL =12mA)	V_{OH}	I_{OH} = -4mA	4.0	—	V_{DD}	V
Output High Voltage for Driver Output (IOL =24mA)	V_{OH}	I_{OH} = -8mA	4.0	—	V_{DD}	V
Output Low Voltage[2] for Normal Output (IOL= 3.2mA)	V_{OL}	I_{OL} = 3.2mA	V_{SS}	—	0.4	V
Output Low Voltage[2] for Driver Output (IOL= 8mA)	V_{OL}	I_{OL} = 8mA	V_{SS}	—	0.4	0V
Output Low Voltage[2] for Driver Output (IOL= 12mA)	V_{OL}	I_{OL} = 12mA	V_{SS}	—	0.4	0V
Output Low Voltage[2] for Driver Output (IOL= 24mA)	V_{OL}	I_{OL} = 24mA	V_{SS}	—	0.4	0V
Input High Voltage for TTL Input	V_{IH}	—	2.2	—	—	V
Input Low Voltage for TTL Input	V_{IL}	—	—	—	0.8	V
Input High Voltage for CMOS Input	VIH	—	V_{DD} x 0.7	—	—	V
Input Low Voltage for CMOS Input	V_{IL}	—	—	—	V_{DD} x 0.3	V
Schmitt Trigger CMOS Input[3] Positive-going Threshold Negative-going Threshold Hysteresis	V_{T+} V_{T-} $V_{T+} - V_{T-}$	— — V_{IL} to V_{IH} V_{IH} to V_{IL}	 2.5 0.7 1.1	 3.3 1.4 1.9	 4.0 2.0 2.7	 V V V
Schmitt Trigger TTL Input[3] Positive-going Threshold Negative-going Threshold Hysteresis	V_{T+} V_{T-} $V_{T+} - V_{T-}$	— — V_{IL} to V_{IH} V_{IH} to V_{IL}	 1.4 0.8 0.4	 1.9 1.3 0.6	 2.5 1.8 0.7	 V V V
Input Pull-up/Pull-down Resistor	RP	$V_{IH} = V_{DD}$ $V_{IL} = V_{SS}$	25	50	100	kΩ
Input Leakage Current	I_{LI}	V_I = 0 - V_{DD}	-10	—	10	µA
Input Leakage Current (3-state)	I_{LZ}	V_I = 0 - V_{DD}	-10	—	10	µA

Notes: 1.$V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$
2.With certain restrictions on pin assignment
3.These values for reference only

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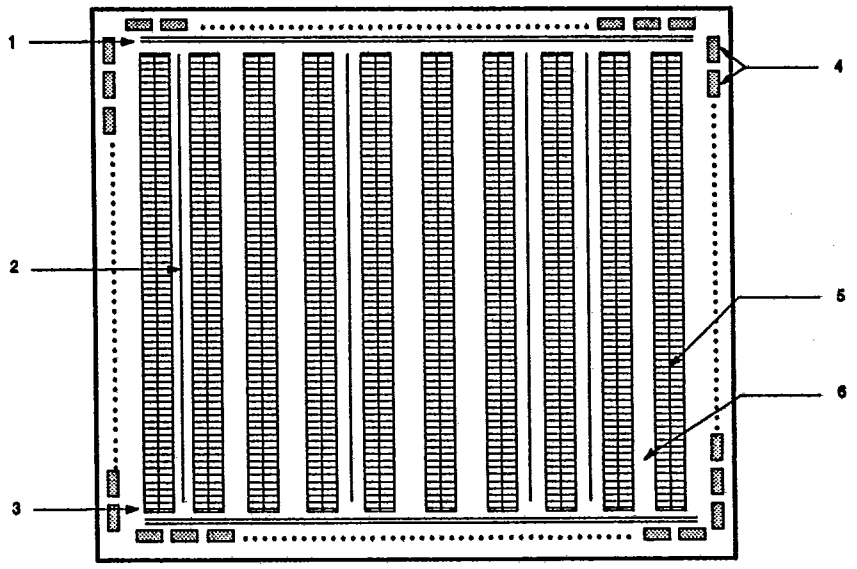
ARRAY ARCHITECTURE

The typical UHB chip is composed of double columns of CMOS gates (basic cells) separated by dedicated wiring channels. A basic cell consists of a pair of N-channel and a pair of P-channel transistors interconnected by polysilicon gate control terminals. Groups of basic cells are interconnected by custom metalization into unit cells. Fujitsu unit cells provide a wide range of standard logic functions such as exclusive OR gates, flip-flops, buffers, and counters. The UHB Series CMOS Gate Array family includes over 250 different unit cells. These unit cells are the building blocks from which complex designs are constructed.

The spaces between the double columns of basic cells are occupied by channels for custom metalization. Nearly half of these wiring channels contain transmission gates that implement internal 3-state buses. Bus terminators located at the ends of the double columns of cells maintain the last value to be sent through the bus to ensure proper operation under all conditions.

The I/O cells around the perimeter of the matrix of cells are composed of internal cells with input protection networks and the potential to be configured as input buffers, clock input buffers, output buffers, power output buffers, or bidirectional buffers.



Typical Chip Layout, Double Column Structure

1. Dedicated Clock Network – for high frequency clocks
2. 3-state Bus Logic – located in wiring channels
3. Bus Terminators – prevent floating state on buses
4. Driver Transistors and I/O Protection Networks – provide high I/O count
5. Double Columns – for optional macro utilization and speed
6. Wiring Channel Area – for metalization between unit cells

DESIGN COMPONENTS

DESIGNING WITH THE UHB PRODUCT FAMILY

To implement logic functions, the designer builds up the elements of the circuit from unit cells. Simple unit cells are used hierarchically to build higher level functions until the logic is completely defined. Fujitsu offers a complete line of standard logic functions in the unit cell library.

Soft macros are used to implement large super-cell functions such as expandable ALU's and multipliers.

I/O BUFFERS

Each UHB I/O buffer around the perimeter of the array consists of an input protection network and large N-channel and P-channel transistors capable of supplying the standard 3.2-mA, 8-mA, and 12-mA output currents. Two of these large transistor pairs may be connected in parallel, using high-output-current macros, to obtain 24-mA drive. One of the I/O pads whose output transistors have been used for the 24-mA high-current option may still be used as an input.

Input I/O buffers convert external TTL levels to internal CMOS levels or may receive CMOS level signals directly. Output I/O buffers are totem pole and may drive either CMOS and TTL levels, depending on their AC and DC loads. Any of the pins except the dedicated power and ground pads can be designed to be an input buffer, an input buffer with pull-up/pull-down resistance, a clock input buffer, an output buffer, a high-drive output buffer, an output buffer with noise limiting resistance, a 3-state output buffer, a bi-directional buffer, or a Schmitt trigger input buffer. There are some restrictions on the location of 24-mA buffers.

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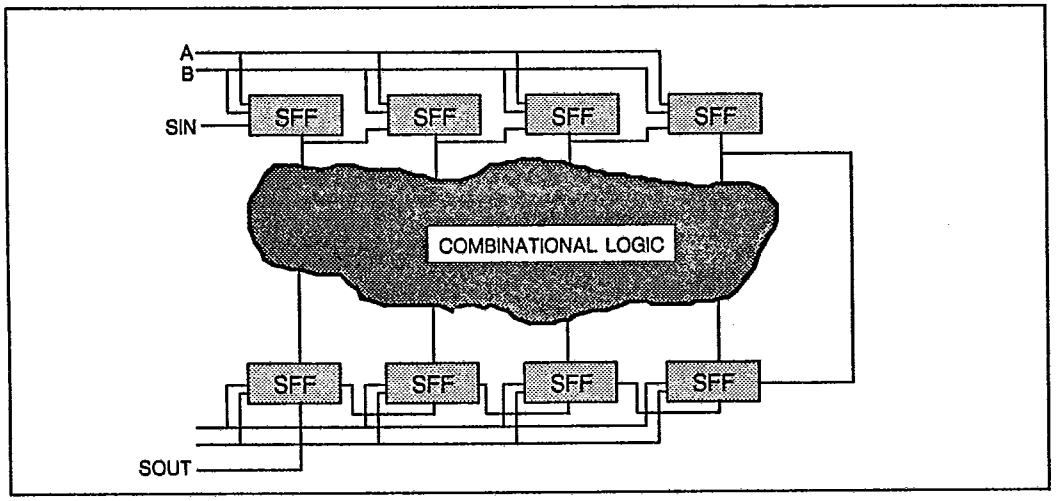
INPUT CLOCK DRIVERS

The large output I/O transistor pair is used in a high-drive input clock driver for high fanout applications within the array. This allows the designer to fully utilize the high speed capabilities of the UHB technology.

TESTING UHB DEVICES

Two options are available for testing UHB designs: (1) the standard designer-supplied test patterns and test vectors (in Fujitsu's FTDL format) and (2) the use of scan cells combined with Automatic Test Generation (ATG) performed by Fujitsu computers for additional diagnostic test patterns. If the designer has designed with scan cells and other scan logic elements, Fujitsu will complete the scan test program generation.

Regardless of the selected test option, it is the responsibility of the designer to furnish Fujitsu with enough test patterns to guarantee that the submitted design completely performs its intended logic functions. These patterns include the designer's test function of each I/O pin.



Diagramatic Representation of Design Structure for Scan Testing

VDD and VSS REQUIREMENTS

Each UHB Series gate array device has two options for each package type, both supporting a different number of power and ground pins. The number of power and ground pins required depends on the number of simultaneously switching outputs used in the design. Simultaneously switching outputs (SSOs) are output signals that change from H to L or L to H or from Z to H or Z to L within a 20-ns window (including possible skew).

Multiple outputs that switch at the same time can cause noise on V_{DD} and V_{SS} lines and affect the performance of a device. Therefore, to achieve maximum reliability, Fujitsu limits the number of SSOs per V_{DD} pin according to the table below. The maximum number of SSOs per pin is determined by a representative value specified for the driving capability of each type of output. The total representative value of all SSOs used in a design must not exceed 80 per V_{SS} pin. For example, 11 normal 3.2-mA outputs with edge rate control, four 12-mA outputs, or three 24-mA outputs per V_{SS} pin may be SSOs.

Output Drive Type	Representative Value per Output
Normal (3.2 mA)	10
High Drive (12 mA)	20
Normal (3.2 mA) with Edge Rate Control	7
High Drive (12 mA) with Edge Rate Control	14
High Drive (24 mA) with Edge Rate Control	26

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ESTIMATION OF POWER DISSIPATION

In order to select a suitable ASIC package and determine system cooling requirements and system power supply requirements, the designer needs to estimate the power dissipation of the circuit.

Power dissipation calculation in CMOS technologies is complicated by the fact that transient currents involved in charging and discharging capacitances dominate the total power dissipation.

Fujitsu has simplified the calculation of power dissipation by studying a long history of designs to determine what typical circuit activity constitutes, and by observing the power dissipation characteristics of individual gates as they operate. These parameters are summarized below and are incorporated into the worksheet that follows.

$P_{d(in)}$ = 0.073mW/MHz

$P^{d(out)}$ = 0.025mW/pF

$P^{d(seq)}$ = 0.20mW/MHz

$P^{d(comb)}$ = 0.033mW/MHz

$C^{V}(5V \pm 5\%)$ = 1.11

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The example below assumes a system clock frequency (f) of 25 MHz for a circuit of 2700 gates with 90 inputs and 50 outputs, all outputs loaded at 20 pF. The circuit activity, that is, the maximum number of internal gates, inputs, and outputs that are simultaneously active, is 20%. The mix of sequential to combinational gates is 1:5 (20%).

Note: P is in units of mW/MHz, except $P_{d(out)}$, which is in mW/MHz/pF.

1.0 I/O AC POWER CALCULATION

1.1 Number of inputs 90 x freq 25/2 x $P_{D(in)}$ x 20% = 16.43 mW

1.2 Number of outputs 50 x freq[1] 25/4 x load 20F x $P_{D(out)}$ x 20% = 31.25 mW

1.3 Total I/O AC (transient) Power ..... P_{AC} = 47.68 mW

2.0 I/O DC POWER CALCULATION

2.1 Number of 3.2 mA outputs[2] 34 x (0.15 x (I_{OL} + I_{OH})) = 26.52 mW

2.2 Number of 8 mA outputs 16 x (0.15 (I_{OL} + I_{OH})) = 24 mW

2.3 Number of 12 mA outputs 0 x (0.15 (I_{OL} + I_{OH})) = 0 mW

2.4 Number of 24 mA outputs 0 x (0.15 (0.15 x (I_{OL} + I_{OH})) = 0 mW

2.5 Total I/O DC (steady state) Power ..... P_{DC} = 50.52 mW

3.0 INTERNAL GATE POWER CALCULATION

3.1 Number of used gates 2700 x % seq. 20% x freq 25/8 X $P_{D(seq)}$ = 337.5 mW

3.2 Number of used gates 2700 x % comb. 80% x freq[3] 25/20 X $P_{D(comb)}$ = 89.1 mW

3.3 Total Internal Gate Transient Power ..... P_{INT} = 426.6 mW

4.0 TOTAL CHIP ESTIMATED POWER DISSIPATION

4.1 P_t (typical) = P_{AC} 47.68 mW + P_{DC} 50.52 mW + P_{INT} 426.6 mW = 524.8 mW

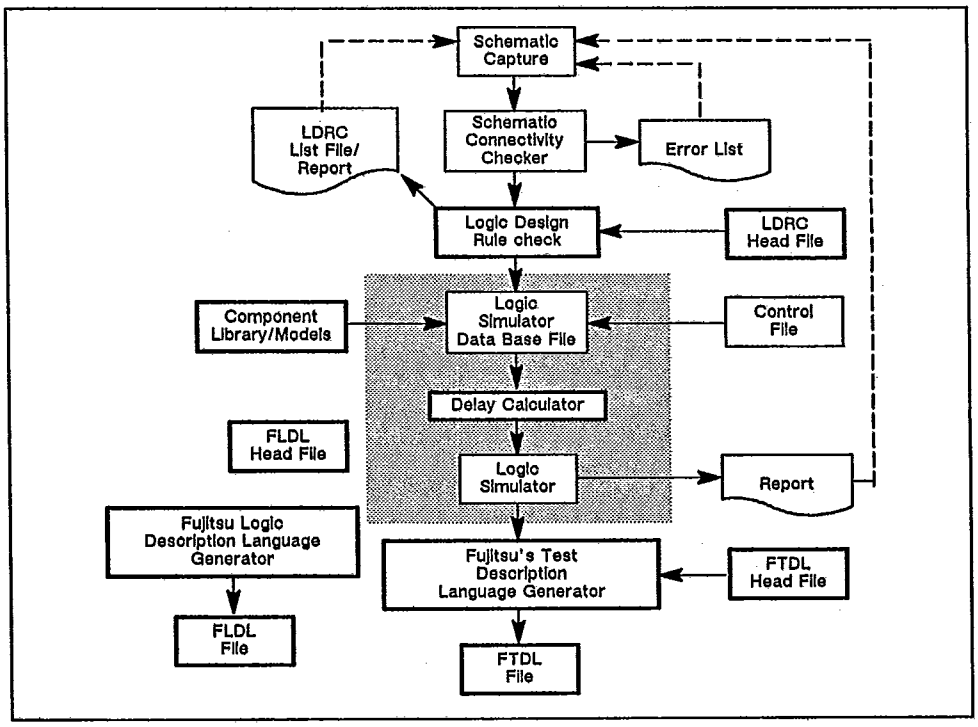
4.2 P_D(worst case) = P_t = 524.8 mW x C_V 1.11 = 582.5 mW = .6W W

Notes: 1. It is assumed that outputs will toggle at one fourth the frequency of the system clock on the average.
2. The (I_{OL} + I_{OH}) term assumes outputs are symmetrically high and low
3. It is assumed that only 20% of the combinational gates are simultaneously active, and at a frequency of one fourth the clock frequency.

WORKSTATION DESIGN FLOW

Fujitsu ASICs customers have a choice of four popular CAE design packages (Daisy, Mentor, Valid, and HP 9000) plus Fujitsu's own new Sun-based workstation software (ViewCAD) for schematic capture and design implementation. The design flow process is summarized in the diagram below. The boxes outlined in bold indicate Fujitsu-supplied software that integrates with standard CAE software to produce the data files necessary to implement a design. The design process flowchart is somewhat simpler for the Fujitsu (ViewCAD) software because ViewCAD was written specifically for Fujitsu's high-reliability design process.

A design logic file and a test data file, known as Fujitsu Logic Design Language (FTDL) and Fujitsu Test Design Language (FTDL), are the ultimate result of the workstation design process.



Workstation Design Process

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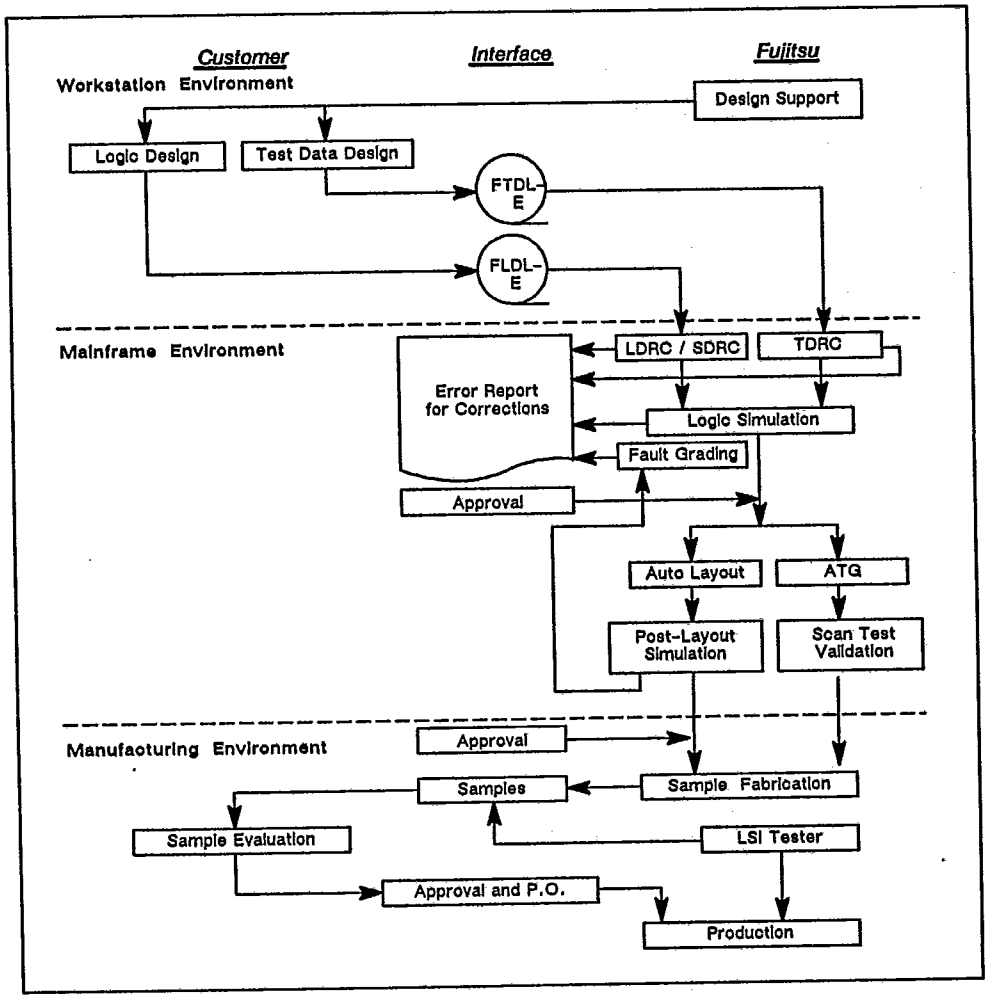
DESIGN IMPLEMENTATION FLOW

After the workstation design process is complete, the FLDL and FTDL files are transferred to the mainframe environment at one of Fujitsu's Technical Resource Centers. There, the FLDL file is checked by the Logic Design Rule Check (LDRC) and a pre-layout simulation is made using the test data generated in FTDL. Then, after automated layout takes place, simulation is run to validate the LSI function.

When the design data is validated, the design files are sent to the prototype manufacturing area where mask sets are fabricated and engineering sample devices are manufactured for test and approval. After the engineering samples are fully tested and signed off, full production can begin.



Post-Design Process

FUNCTIONAL INDEX OF UNIT CELL LIBRARY

Note: The load unit (ℓu) is a normalized loading unit of capacitance representing the input load of an inverter without metal interconnection.

Inverter and Buffer Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (ℓu)**	**Polarity**
V1N	Inverter	1	18	Neg
V2B	Power Inverter	1	36	Neg
V1L	Double Power Inverter	2	55	Neg
B1N	True Buffer	1	18	Pos
BD3	True Delay Buffer (> 5ns)	5	18	Pos
BD4	Delay Cell (> 4ns)	4	6	Pos
BD5	Delay Cell (>10ns)	9	18	Pos
BD6	Delay Cell (>22ns)	17	18	Pos
Clock Buffer Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (ℓu)**	**Polarity**
K1B	True Clock Buffer	2	36	Pos
K2B	Power Clock Buffer	3	55	Pos
K3B	Gated Clock (AND) Buffer	2	36	Pos
K4B	Gated Clock (OR) Buffer	2	36	Pos
K5B	Gated Clock (NAND) Buffer	3	36	Neg
KAB	Block Clock (OR) Buffer	3	55	Pos
KBB	Block Clock (OR x 10) Buffer	30	55	Pos
NAND Family				
Unit Cell Name	**Description**	**Basic Cells**	**Drive (ℓu)**	
N2N	2-Input NAND	1	18	
N2B	Power 2-Input NAND	3	36	
N2K	Fast Power 2-Input NAND	2	36	
N3N	3-Input NAND	2	14	
N3B	Power 3-Input NAND	3	36	
N4N	4-Input NAND	2	10	
N4B	Power 4-Input NAND	4	36	
N6B	Power 6-Input NAND	5	36	
N8B	Power 8-Input NAND	6	36	
N9B	Power 9-Input NAND	8	36	
NCB	Power 12-Input NAND	10	36	
NGB	Power 16-Input NAND	11	36	
N3K	Fast Power 3-Input NAND	3	36	
N4K	Fast Power 4-Input NAND	4	36	

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FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

NOR Family				
Unit Cell Name	Description	Basic Cells	Drive (ℓu)	
R2N	2-Input NOR	1	14	
R2B	Power 2-Input NOR	3	36	
R2K	Power 2-Input NOR	2	36	
R3N	3-Input NOR	2	10	
R3B	Power 3-Input NOR	3	36	
R3K	Power 3-Input NOR	3	36	
R4N	4-Input NOR	2	6	
R4B	Power 4-Input NOR	4	36	
R4K	Power 4-Input NOR	4	36	
R6B	Power 6-Input NOR	5	36	
R8B	Power 8-Input NOR	6	36	
R9B	Power 9-Input NOR	8	36	
RCB	Power 12-Input NOR	10	36	
RGB	Power 16-Input NOR	11	36	

AND Family				
Unit Cell Name	Description	Basic Cells	Drive (ℓu)	
N2P	Power 2-Input AND	2	36	
N3P	Power 3-Input AND	3	36	
N4P	Power 4-Input AND	3	36	
N8P	Power 8-Input AND	6	36	

OR Family				
Unit Cell Name	Description	Basic Cells	Drive (ℓu)	
R2P	Power 2-Input OR	2	36	
R3P	Power 3-Input OR	3	36	
R4P	Power 4-Input OR	3	36	
R8P	Power 8-Input OR	6	36	

Exclusive NOR/OR Family (EXOR/EXNOR)				
Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Polarity
X1N	Exclusive NOR	3	18	Neg
X1B	Power Exclusive NOR	4	36	Neg
X2N	Exclusive OR	3	14	Pos
X2B	Power Exclusive OR	4	36	Neg
X3N	3-Input Exclusive NOR	5	14	Neg
X3B	Power 3-Input Exclusive NOR	6	36	Neg
X4N	3-Input Exclusive OR	5	14	Pos
X4B	Power 3-Input Exclusive OR	6	36	Pos

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

AND-OR-Inverter Family (AOI)

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	
D23	2 AND into 2 NOR AOI	2	14	
D14	3 AND into 2 NOR AOI	2	14	
D24	2, 2 AND into 2 NOR AOI	2	14	
D34	2 AND into 3 NOR AOI	2	10	
D36	3, 2 AND into 3 NOR AOI	3	10	
D44	2 OR into 2 AND into 2 NOR AOI	2	10	

Note: AND-OR-Invert unit cells are useful in implementing sum-of-products (SOP) expressions.

OR-AND-Inverter Family (OAI)

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	
G23	2 OR into 2 NAND OAI	2	18	
G14	3 OR into 2 NAND OAI	2	10	
G24	2, 2 OR into 2 NAND OAI	2	10	
G34	2 OR into 3 NAND OAI	2	10	
G44	2 AND into 2 OR into 2 NAND OAI	2	14	

Note: OR-AND-Invert unit cells are useful in implementing product-of-sums (POS) expressions.

Multiplexer Family

Unit Cell Name	Type	Description	Basic Cells	Drive (ℓu)	Function
T24*	4:1	Power 4, 2 ANDs into 4 NOR Multiplexer	6	36	SOP
T26*	6:1	Power 6, 2 ANDs into 6 NOR Multiplexer	10	36	SOP
T28*	8:1	Power 8, 2 ANDs into 8 NOR Multiplexer	11	36	SOP
T32	2:1	Power 2, 3 ANDs into 2 NOR Multiplexer	5	36	SOP
T33*	3:1	Power 3, 3 ANDs into 3 NOR Multiplexer	7	36	SOP
T34*	4:1	Power 4, 3 ANDs into 4 NOR Multiplexer	9	36	SOP
T42	2:1	Power 2, 4 ANDs into 2 NOR Multiplexer	6	36	SOP
T43	3:1	Power 3, 4 ANDs into 3 NOR Multiplexer	10	36	SOP
T44	4:1	Power 4, 4 ANDs into 4 NOR Multiplexer	11	36	SOP
T54	4:1	Power 2, 2-3-4 ANDs into 4 NOR Multiplexer	10	36	SOP
U24*	4:1	Power 4, 2 OR into 4 NAND Multiplexer	6	36	POS
U26*	6:1	Power 6, 2 OR into 6 NAND Multiplexer	9	36	POS
U28*	8:1	Power 8, 2 OR into 8 NAND Multiplexer	11	36	POS
U32	2:1	Power 2, 3 OR into 2 NAND Multiplexer	5	36	POS
U33*	3:1	Power 3, 3 OR into 3 NAND Multiplexer	7	36	POS
U34*	4:1	Power 4, 3 OR into 4 NAND Multiplexer	9	36	POS
U42	2:1	Power 2, 4 OR into 2 NAND Multiplexer	6	36	POS
U43	3:1	Power 3, 4 OR into 3 NAND Multiplexer	9	36	POS
U44	4:1	Power 4, 4 OR into 4 NAND Multiplexer	11	36	POS

* Convenient for typical multiplexer applications

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FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Data Selectors/Multiplexers

Unit Cell Name	Type	Description	Basic Cells	Drive (ℓu)	Selects	Output	Bit Width
P24*	2:1	Data Selector	12	36	S, XS	Q	4
T2E	2:1	Selector	5	18	S	XQ	2
T2F	2:1	Selector	8	18	S	XQ	4
T2B*	2:1	Selector	2	18	S, XS	XQ	1
T2C*	2:1	Selector	4	18	S, XS	XQ	2
T2D*	2:1	Selector	2	14	S, XS	XQ	1
T5A*	4:1	Selector	8	9	S, XS	XQ	1
V3A*	1:2	Selector	2	14	S, XS	XQ	1
V3B*	1:2	Selector	4	14	S, XS	XQ	2

* These are transmission gate devices whose outputs can be tied because they can be inhibited with true/inverted selects.

Decoders

Unit Cell Name	Type	Description	Basic Cells	Drive (ℓu)	Active Level Outputs	Enable	
DE2	2:4	Decoder	5	18	Low	—	
DE3	3:8	Decoder	15	14	Low	—	
DE4	2:4	Decoder	8	14	Low	Low	
DE6	3:8	Decoder	30	18	Low	1 High 2 Low	

Internal Bus Unit Cells

Unit Cell Name	Type	Description	Basic Cells	Drive (ℓu)	Bus Size	Enable	
B41	4-bit Bus Driver		9	36	4 bits	Low	

Notes: 1. The number of B41s used is limited by the chosen array series, as shown in the table below.
2. On-chip buses (managing more than one bus source and/or a bi-directional bus) may be implemented with either multiplexer-type unit cells or bus drivers. While bus drivers impose certain design restrictions, the optimum choice is dictated by the specific design.

Device Name	Maximum B41s
C-330UHB	4
C-530UHB	5
C-830UHB	6
C-1200UHB	8
C-1700UHB	12
C-2200UHB	16
C-3000UHB	21
C-4100UHB	26
C-6000UHB	50

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Data Latch Family

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Enable	Bits	Output	Clear
YL2	Data Latch with TM	5	36	High	1	Q	—
YL4	Data Latch with TM	14	36	High	4	Q	—
LTK	Data Latch	4	18	Low	1	Q, XQ	Async
LTL	Data Latch with Clear	5	18	Low	1	Q, XQ	Async
LTM	Data Latch with Clear	16	18	Low	4	Q, XQ	—
LT1	S-R Latch with Clear	4	18	Low	1	Q, XQ	Async
LT4	Data Latch	14	18	Low	4	Q, XQ	—

Note: Y-type latches incorporate inhibit inputs and transparent mode (TM) to facilitate scan implementation.

Scan Flip-Flop Family (Positive-Edge Triggered)

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Bits	Output	Clear	Preset	Clock Inhibit
SDH*	Scan D FF with 2:1 Multiplex	14	36	1	Q, XQ	Async	—	Yes
SDJ*	Scan D FF with 4:1 Multiplex	15	36	1	Q, XQ	Async	—	Yes
SDK*	Scan D FF with 3:1 Multiplex	16	36	1	Q, XQ	Async	—	Yes
SJH	Scan J-K FF	16	36	1	Q, XQ	Async	—	Yes
SDD*	Scan DFF with 2:1 Multiplex	16	36	1	Q, XQ	Async	Async	Yes
SDA	Scan 1-input D FF	12	36	1	Q, XQ	—	—	Yes
SDB	Scan 1-input D FF	42	36	4	Q, XQ	—	—	Yes
SHA	Scan 1-input D FF	68	18	8	Q, XQ	—	—	Yes
SHB	Scan 1-input D FF	62	18	8	Q	—	—	Yes
SHC	Scan 1-input D FF	62	18	8	XQ	—	—	Yes
SHJ*	Scan D FF with 2:1 Multiplex	78	18	8	Q, XQ	—	—	Yes
SHK*	Scan D FF with 3:1 Multiplex	88	18	8	Q, XQ	—	—	Yes

Note: * Indicates D Flip-Flop with multiplexed inputs.

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FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Non SCAN Flip-Flop Family

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Bits	Outputs	Clear	Preset	Clock Edge
FDN	Non-Scan D FF with Set	7	18	1	Q, XQ	—	Async	Pos
FDM	Non-Scan D F	6	18	1	Q, XQ	—	—	Pos
FDO	Non-Scan D FF with Reset	7	18	1	Q, XQ	Async	—	Pos
FDP	Non-Scan D FF with Set and Reset	8	18	1	Q, XQ	Async	Async	Pos
FDQ	Non-Scan D FF	21	18	4	Q	—	—	Neg
FDR	Non-Scan D FF with Clear	26	18	4	Q	Async	—	Pos
FDS	Non-Scan D FF	20	18	4	Q	—	—	Pos
FD2	Non-Scan Power D FF	7	36	1	Q, XQ	—	—	Neg
FD3	Non-Scan Power D FF with Preset	8	36	1	Q, XQ	—	Async	Neg
FD4	Non-Scan Power D FF with Clear and Preset	9	36	1	Q, XQ	Async	Async	Neg
FD5	Non-Scan Power D FF with Clear	8	36	1	Q, XQ	Async	—	Neg
FJD	Non-Scan Positive Edge Clocked Power J-K FF with Clear	12	36	1	Q, XQ	Async	—	Pos

Note: Synchronous flip-flops my be constructed by adding a simple AND gate (such as N2P) to the input of a flip-flop to create a synchronous clear.

Binary Counter Family

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Bits	Outputs[1]	Load	Clear	Enable	Carry In	Up/ Down
SC7[2]	Scan 4-bit Synchronous Binary Up Counter with Parallel Load	62	36	4	Q, XQ, CO (S)	Sync	—	Low	High	Up
SC8[2]	Scan 4-bit Synchronous Binary Down Counter with Parallel Load	66	36	4	Q, XQ, CO (S)	Sync	—	High	Low	Down
C11[3]	Non-Scan Flip-Flop for Counter	11	18	—	Q, XQ	—	—	—	—	—
C41	Non-Scan 4-bit Binary Asynchronous Counter	24	18	4	Q, (A)	—	Async	—	—	Up
C42	Non-Scan 4-bit Binary Synchronous Counter	32	18	4	Q	—	Async	—	—	Up
C43	Non-Scan 4-bit Binary Synchronous Up Counter	48	18	4	Q, CO(S)	Sync	Async	High	High	Up
C45	Non-Scan Binary Synchronous Up Counter	48	18	4	Q, CO	Sync	Sync	High	High	Up
C47	Non-Scan Binary Synchronous Up/Down Counter	68	18	4	Q, CO	Async	—	Low	Low	Up/Down

Notes: 1. (S), (A) indicate the counter is (S)ynchronous or (A)synchronous.
2. Scan counters include clock inhibit and high drive (C_{DR} = 36 ℓu). For non-Scan counters C_{DR} = 18 ℓu.
3. C11 may by used for purposes other than counters.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Shift Register Family

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Bit Width	Load	Outputs	Clock Polarity
FS1	Serial-In Parallel-out Shift Register	18	16	4	Serial-In only	Q-Parallel	Neg
FS2	Shift Register with Synchronous Load	30	16	4	Sync-High	Q-Parallel	Neg
FS3	Shift Register with Asynchronous Load	34	18	4	Async-Low	Q-Parallel	Pos
SR1	Serial-In Parallel-out Shift Register with Scan	36	36	4	Serial-In only	Q-Parallel	Pos

Datapath Operators (Adder, ALU, Parity)

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Bit Width	Outputs	Carry In
MC4	Magnitude Comparator	42	18(=) 10(<,>)	4	A>B, A=B, A<B	A>B,A=B,ALB
A1A	1-bit Half Adder	5	36	1	S, CO	—
A1N	1-bit Full Adder	8	18	1	S, CO	CI
A2N	2-bit Full Adder	16	14	2	S, CO	CI
A4H	4-bit Binary Full Adder w/Fast Carry	48	18(CO) 14(S)	4	S, CO	CI
PE5	Even Parity Generator/Checker	12	36	5	EVEN, $\overline{ODD}$	—
PO5	Odd Parity Generator/Checker	12	36	5	ODD, $\overline{EVEN}$	—
PE8	Even Parity Generator/Checker	18	18	8	EVEN, $\overline{ODD}$	—
PO8	Odd Parity Generator/Checker	18	18	8	ODD, $\overline{EVEN}$	—
PE9	Even Parity Generator/Checker	22	18	9	EVEN, $\overline{ODD}$	—
PO9	Odd Parity Generator/Checker	22	18	9	ODD, $\overline{EVEN}$	—

Miscellaneous Cells

Unit Cell Name	Description	Basic Cells	Function
Z00	0 Clip	0	Tie to Vss
Z01	1 Clip	0	Tie to VDD

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Input Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (ℓu)	Logic Level	Type	Input/ Output Polarity
I1B	Input Buffer	5	36	TTL	Signal	Invert
I1BU	I1B with Pull-up Resistance	5	36	TTL	Signal	Invert
I1BD	I1B with Pull-down Resistance	5	36	TTL	Signal	Invert
I2B	Input Buffer	4	36	TTL	Signal	True
I2BU	I2B with Pull-up Resistance	4	36	TTL	Signal	True
I2BD	I2B with Pull-down Resistance	4	36	TTL	Signal	True
IKB	Clock Input Buffer	4	72	TTL	Clock	Invert
IKBU	Ikb With Pull-up Resistance	4	72	TTL	Clock	Invert
IKBD	IKB with Pull-down Resistance	4	72	TTL	Clock	Invert
ILB	Clock Input Buffer	6	72	TTL	Clock	True
ILBU	ILB with Pull-up Resistance	6	72	TTL	Clock	True
ILBD	ILB with Pull-down Resistance	6	72	TTL	Clock	True
I1C	CMOS Interface Input Buffer	5	36	CMOS	Signal	Invert
I1CU	I1C with Pull-up Resistance	5	36	CMOS	Signal	Invert
I1CD	I1C with Pull-down Resistance	5	36	CMOS	Signal	Invert
I2C	CMOS Interface Input Buffer	4	36	CMOS	Signal	True
I2CU	I2C with Pull-up Resistance	4	36	CMOS	Signal	True
I2CD	I2C with Pull-down Resistance	4	36	CMOS	Signal	True
I1S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	Invert
I1SU	I1S with Pull-up Resistance	8	18	CMOS	Schmitt	Invert
I1SD	I1S with Pull-down Resistance	8	18	CMOS	Schmitt	Invert
I2S	Schmitt Trigger Input Buffer	8	18	CMOS	Schmitt	True
I2SU	I2S with Pull-up Resistance	8	18	CMOS	Schmitt	True
I2SD	I2S with Pull-down Resistance	8	18	CMOS	Schmitt	True
I1R	Schmitt Trigger Input Buffer	6	18	TTL	Schmitt	Invert
I1RU	I1R with Pull-up Resistance	6	18	TTL	Schmitt	Invert
I1RD	I1R with Pull-down Resistance	6	18	TTL	Schmitt	Invert
I2R	Schmitt Trigger Input Buffer	8	18	TTL	Schmitt	True
I2RU	I2R With Pull-up Resistance	8	18	TTL	Schmitt	True
I2RD	I2R with Pull-down Resistance	8	18	TTL	Schmitt	True

Note: A "U" suffixed to the name of an input buffer indicates pull-up resistance of 50KΩ (typical) and a "D" indicates a pull-down resistance of the equivalent value.

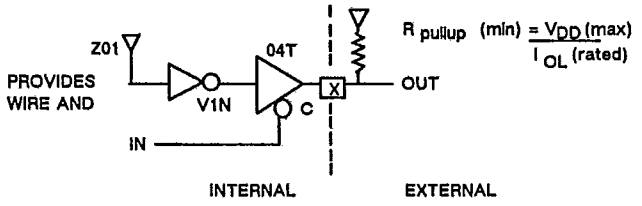
FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Output Buffer Family

Unit Cell Name	Description	Basic Cells	Drive (I_{OL})	Logic[2] Level	Type	Edge Rate Control	Input/ Output Polarity
O1B	Output Buffer	3	3.2mA	TTL/CMOS	Standard	No	Invert
O1L	Power Output Buffer	3	12mA	TTL/CMOS	Standard	No	Invert
O1S	Power Output Buffer	5	12mA	TTL/CMOS	Standard	Yes	Invert
O2B	Output Buffer	2	3.2mA	TTL/CMOS	Standard	No	True
O2L	Power Output Buffer	2	12mA	TTL/CMOS	Standard	No	True
O2S	Power Output Buffer	4	12mA	TTL/CMOS	Standard	Yes	True
O4T[1]	Output Buffer	4	3.2mA	TTL/CMOS	3-state	No	True
O4W[1]	Power 3-state Output Buffer	4	12mA	TTL/CMOS	3-state	No	True
O4S[1]	Power 3-state Output Buffer	5	12mA	TTL/CMOS	3-state	Yes	True
O1R	Output Buffer	5	3.2mA	TTL/CMOS	Standard	Yes	Invert
O2R	Output Buffer	4	3.2mA	TTL/CMOS	Standard	Yes	True
O4R[1]	Output Buffer	5	3.2mA	TTL/CMOS	3-state	Yes	True
O2S2	High Power Output Buffer	6	24mA	TTL/CMOS	Standard	Yes	True
O4S2[1]	High Power Output Buffer	7	24mA	TTL/CMOS	3-state	Yes	True
O1BF	Output Buffer	3	8mA	TTL/CMOS	Standard	No	Invert
O1RF	Output Buffer	5	8mA	TTL/CMOS	Standard	Yes	Invert
O2BF	Output Buffer	2	8mA	TTL/CMOS	Standard	No	True
O2RF	Output Buffer	4	8mA	TTL/CMOS	Standard	Yes	True
O4RF	3-state Output Buffer	5	8mA	TTL/CMOS	3-state	Yes	True
O4TF	3-state Output Buffer	4	8mA	TTL/CMOS	3-state	No	True

Note: 1. While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs.

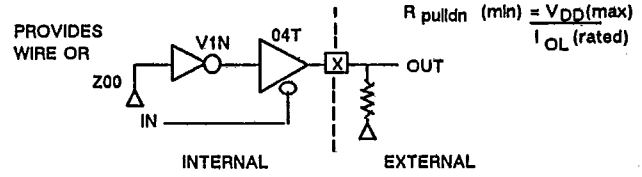
EXAMPLE OF OPEN DRAIN OUTPUT



$$R_{pullup}\ (min) = \frac{V_{DD}\ (max)}{I_{OL}\ (rated)}$$

IN	X	OUT
0	L	L
1	Z	H

EXAMPLE OF OPEN SOURCE OUTPUT



$$R_{pulldn}\ (min) = \frac{V_{DD}\ (max)}{I_{OL}\ (rated)}$$

IN	X	OUT
0	H	H
1	Z	L

Note: 2. Totem pole outputs, such as these buffers have, can drive both TTL and CMOS levels. Voltage margins depend on actual source or sink current (see DC specifications).

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses)

Unit Cell Name	Description	Basic Cells	Drive (IOL)	Logic Level	Edge Rate Control	Input/ Output Polarity
H6T	3-state Output and Input Buffer	8	3.2mA	TTL	No	True
H6TU	H6T with Pull-up Resistance	8	3.2mA	TTL	No	True
H6TD	H6T with Pull-down Resistance	8	3.2mA	TTL	No	True
H6W	Power 3-state Output and Input Buffer	8	12mA	TTL	No	True
H6WU	H6W with Pull-up Resistance	8	12mA	TTL	No	True
H6WD	H6W with Pull-down Resistance	8	12mA	TTL	No	True
H6C	3-state Output and CMOS Interface Input Buffer	8	3.2mA	CMOS	No	True
H6CU	H6C with Pull-up Resistance	8	3.2mA	CMOS	No	True
H6CD	H6C with Pull-down Resistance	8	3.2mA	CMOS	No	True
H6E	Power 3-state Output and CMOS Interface Input Buffer	8	12mA	CMOS	No	True
H6EU	H6E with Pull-up Resistance	8	12mA	CMOS	No	True
H6ED	H6E with Pull-down Resistance	8	12mA	CMOS	No	True
H6S	3-state Output and Schmitt Trigger Input Buffer	12	3.2mA	CMOS	No	True
H6SU	H6S with Pull-up Resistance	12	3.2mA	CMOS	No	True
H6SD	H6S with Pull-down Resistance	12	3.2mA	CMOS	No	True
H6R	3-state Output and Schmitt Trigger Input Buffer	12	3.2mA	TTL	No	True
H6RU	H6R with Pull-up Resistance	12	3.2mA	TTL	No	True
H6RD	H6R with Pull-down Resistance	12	3.2mA	TTL	No	True
H8T	3-state Output and Input Buffer	9	3.2mA	TTL	Yes	True
H8TU	H8T with Pull-up Resistance	9	3.2mA	TTL	Yes	True
H8TD	H8T with Pull-down Resistance	9	3.2mA	TTL	Yes	True
H8W	Power 3-state Output and Input Buffer	9	12mA	TTL	Yes	True
H8WU	H8W with Pull-up Resistance	9	12mA	TTL	Yes	True
H8WD	H8W with Pull-down Resistance	9	12mA	TTL	Yes	True
H8W2	High Power 3-state Output and Input Buffer	11	24mA	TTL	Yes	True
H8W1	H8W2 with Pull-up Resistance	11	24mA	TTL	Yes	True
H8W0	H8W2 with Pull-down Resistance	11	24mA	TTL	Yes	True
H8C	3-state Output Buffer and CMOS Interface Input Buffer	9	3.2mA	CMOS	Yes	True
H8CU	H8C with Pull-up Resistance	9	3.2mA	CMOS	Yes	True
H8CD	H8C with Pull-down Resistance	9	3.2mA	CMOS	Yes	True

Note: A "U" suffixed tol the name of a bidirectional buffer indicates a pull-up resistance of 50Ω (typical) and a "D" indicates a pull-down resistance of the equivalent value.

FUNCTIONAL INDEX OF UNIT CELL LIBRARY (Continued)

Bidirectional I/O Buffers (Buses) continued

Unit Cell Name	Description	Basic Cells	Drive (IOL)	Input Logic Level	Edge Rate Control	Input/ Output Polarity
H8E	Power 3-state Output Buffer and Interface Input Buffer	9	12mA	CMOS	Yes	True
H8EU	H8E with Pull-up Resistance	9	12mA	CMOS	Yes	True
H8ED	H8E with Pull-down Resistance	9	12mA	CMOS	Yes	True
H8E2	High Power 3-state Output and Input Buffer	11	24mA	CMOS	Yes	True
H8E1	H8E2 with Pull-up Resistance	11	24mA	CMOS	Yes	True
H8E0	H8E2 with Pull-down Resistance	11	24mA	CMOS	Yes	True
H8S	3-state Output and Schmitt Trigger Input Buffer	13	3.2mA	CMOS	Yes	True
H8SU	H8S with Pull-up Resistance	13	3.2mA	CMOS	Yes	True
H8SD	H8S with Pull-down Resistance	13	3.2mA	CMOS	Yes	True
H8R	3-state Output and Schmitt Trigger Input Buffer	13	3.2mA	TTL	Yes	True
H8RU	H8R with Pull-up Resistance	13	3.2mA	TTL	Yes	True
H8RD	H8R with Pull-down Resistance	13	3.2mA	TTL	Yes	True
H6TF	3-state Output and Schmitt Trigger Input Buffer	8	8mA	TTL	No	True
H6TFU	H6TF with Pull-up Resistance	8	8mA	TTL	No	True
H6TFD	H6TF with Pull-down Resistance	8	8mA	TTL	No	True
H6CF	3-state Output and Input Buffer	8	8mA	CMOS	No	True
H6CFU	H6CF with Pull-up Resistance	8	8mA	CMOS	No	True
H6CFD	H6CF with Pull-down Resistance	8	8mA	CMOS	No	True
H8TF	3-state Output and Input Buffer	9	8mA	TTL	Yes	True
H8TFU	H8TF with Pull-up Resistance	9	8mA	TTL	Yes	True
H8TFD	H8TF with Pull-down Resistance	9	8mA	TTL	Yes	True
H8CF	3-state Output and Input Buffer	9	8mA	CMOS	Yes	True
H8CFU	H8CF with Pull-up Resistance	9	8mA	CMOS	Yes	True
H8CFD	H8CF with Pull-down Resistance	9	8mA	CMOS	Yes	True

Note: While all outputs are totem-pole type, Open Drain and Open Source types can easily be defined for all 3-state type outputs, which includes all bidirectional buffers.

Oscillator Circuits

Unit Cell Name	Description	Basic Cells	Input Logic Level
HOC	Output Buffer for Oscillator and Input Buffer	8	CMOS
HOCS	Output Buffer for Oscillator and Schmitt Trigger Input Buffer	8	TTL
HOCR	Output Buffer for Oscillator with feedback Resistance	8	CMOS
IT1O	Input Buffer for Oscillator	0	—

1

Availability Characteristics of UHB Gate Array Packages

Dual In-line Packages (Standard DIP)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
DIP-16	DIP-16P-MO2	DIP-16C-C03	1	2	13
	DIP-16P-MO4				
DIP-18	DIP-18P-MO1	DIP-18C-CO1			
	DIP-18P-MO2				
DIP-20	DIP-20P-MO2	DIP-20C-CO2	1	2	17
DIP-20U			1	1	18
DIP-22	DIP-22P-MO2	DIP-22C-C02	2	2	18
	DIP-22P-MO3				
DIP-22U			1	1	20
DIP-24	DIP24P-MO1	DIP-24C-C01	2	2	20
	DIP24P-MO2				
DIP-24U			1	1	22
DIP-28	DIP-28P-M02	DIP-28C-C02	2	2	24
	DIP-28P-M03				
DIP-28U			1	1	26
DIP-40	DIP-40P-M01	DIP-40C-A01	2	4	34
		DIP-40C-A02			
DIP-40U			1	1	38
DIP-42	DIP-42P-MO1	DIP-42C-A01	2	4	36
	DIP-42P-MO2				
DIP-42U			1	1	40
DIP-48	DIP-48P-MO1	DIP-48C-A01	2	4	42
	DIP-48P-MO2				
DIP-48U			1	1	46

Dual In-line Packages (Shrink DIP, 70 mil Pin Pitch)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
DIP-28SH			2	2	24
DIP-28SHU			1	1	26
DIP-42SH			2	4	36
DIP-42SHU			1	1	40
DIP-48SH			2	4	36
DIP-48SHU			1	1	46
DIP-64SH			2	4	58
DIP-64SHU			2	2	60

Subject to Change

Availability Characteristics of UHB Gate Array Packages

Dual In-line Packages (Skinny DIP, 300mil Body Width)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
DIP-22SK			2	2	18
DIP-22SKU			1	1	20
DIP-24SK			2	2	20
DIP-24SKU			1	1	22
DIP-28SK			2	2	24
DIP-28SKU			1	1	26
Flatpack Packages (Dual-Leaded)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
FPT-16	FPT-16P-MO3		1	2	13
FPT-16U			1	1	14
FPT-20	FPT-20P-MO2		1	2	17
FPT-20U			1	1	18
FPT-24	FPT-24-MO2		2	2	20
FPT-24U			1	1	22
FPT-28	FPT-28P-MO1		2	2	24
FPT-28U			1	1	26
Flatpack Packages (Quad-Leaded)					
Pinout Code	Package Code		Number of Vdd	Number of Vss	Available Number of Signal Pins
	Plastic	Ceramic			
FPT-44			2	4	36
FPT-44U			2	2	40
FPT-48	FPT-48P-MO2		2	4	42
FPT-48U			2	2	44
FPT-48 *			2	4	42
FPT-48U *			2	2	44
FPT-64*	FPT-64P-MO1		2	4	58
FPT-64U	FPT-70P-MO1		1	1	62
FPT-80	FPT-80P-MO1		2	6	72
FPT-80U			2	4	74
FPT-100	FPT-100P-MO1		4	8	88
FPT-100U			4	4	92
FPT-120			6	12	102
FPT-120U			4	8	108
FPT-160			8	14	138
FPT-160U			6	12	142

* Small body size.

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Subject to Change

Availability Characteristics of UHB Gate Array Packages

Pinout Code	Package Code		Number # Vdd	Number # Vss	Available Number of Signal Pins
	Plastic	Ceramic			
Pin Grid Arrays (PGA, Thru-Hole, 100mil Pin Pitch)					
PGA-64		PGA-64C-A02	2	4	58
PGA-64U			2	2	60
PGA-88		PGA-88C-A01	4	6	78
PGA-88U			4	4	80
PGA-135			8	12	115
PGA-135U			4	8	127
PGA-179			8	16	155
PGA-179U			8	8	163
PGA-208			12	18	178
PGA-256			16	20	220
Flatpack Packages (Dual-Leaded)					
LCC-28		LCC-28C-A02	2	2	24
LCC-28U			1	1	26
LCC-48		LCC-48C-A01	2	4	42
LCC-48U			1	2	45
LCC-64		LCC-64C-A01	2	4	58
LCC-64U			2	2	60
LCC-68			2	4	62
LCC-68U			2	2	64
LCC-84			4	6	74
LCC-84U			3	4	77
Plastic Leaded Chip Carriers (PLCCs, 50mil Pitch)					
PLCC-28	LCC-28P-M01		2	2	24
PLCC-28U			1	1	26
PLCC-44	LCC-44P-MO1		2	4	38
PLCC-44U			1	2	41
PLCC-68	LCC-68P-M01		2	4	62
PLCC-68U			2	2	64
PLCC-84	LCC-84P-M01		4	6	74
PLCC-84U			2	4	78

Subject to Change

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PACKAGE AVAILABILITY

PACKAGE OPTIONS

		C-330 UHB		C-530 UHB		C-830 UHB		C-1200 UHB		C-1700 UHB		C-2200 UHB		C-3000 UHB		C-4100 UHB		C-6000 UHB		C-8700 UHB		C-12000 UHB	
		C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P	C	P
DIP	16		●																				
	18																						
	20	●	●		●																		
	22	●	●	●	●	●	●		●		●												
	24	●	●	●	●	●	●	●	●		●	●	●										
	28	●	●		●	●	●	●	●	●	●	●	●		●		●						
	40	●	●	●	●	●	●	●	●	●	●	●	●		●		●		●				
	42		●		●		●	●	●	●	●		●	●	●								
	48		●		●	●	●	●	●	●	●	●	●		●		●		●				
SDIP (SHRINK)	28	●	●	●	●	●	●		●		●												
	42		●		●		●	●	●	●	●	●	●		●		●		●				
	48		●		●		●		●		●		●		●		●		●				
	64		●		●		●		●		●		●		●		●		●				
SKDIP (SKINNY)	22		●		●																		
	24																						
	28		●		●																		
FPT with leads on two sides of the package	16		●																				
	20		●																				
	24		●		●		●		●														
	28		●		●		●		●														
FPT with leads on four sides of the package	44		●		●		●		●		●												
	48		●		●	●	●	●	●	●	●	●	●		●								
	48*		●		●		●		●		●												
	64		●		●		●		●		●		●		●		●		●				
	80														●		●		●	○			
	100						●		●	●	●	●	●		●		●		●	○			
	120								●		●		●		●	●	●	●	●	●	●	○	○
	160																					○	○
PLCC	28		●		●		●		●		●		●		●								
	44		●		●		●		●		●		●		●								
	68		●		●		●		●		●		●		●		●		●				
	84										●		●		●		●		●				
PGA	64	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	
	88				●																		
	135																						
	179																						
	208																						
	256																						
LCC	28	●		●		●		●															
	48	●		●		●		●		●		●		●		●							
	64	●		●		●		●		●		●		●		●		●		●			
	68			●		●		●		●		●		●		●		●		●			
	84																						

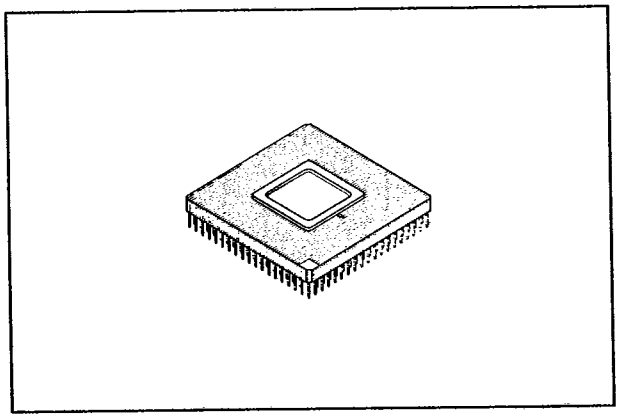
C = Ceramic
P = Plastic

●: available now
○: under development

* = 48-pin FPT, smaller than the other 48 FPT

1

PACKAGE DEMENSIONS



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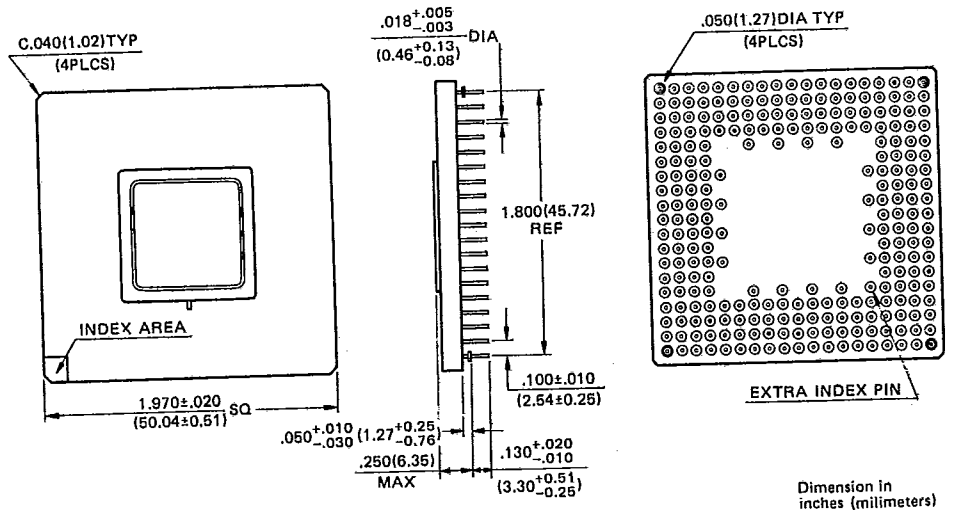
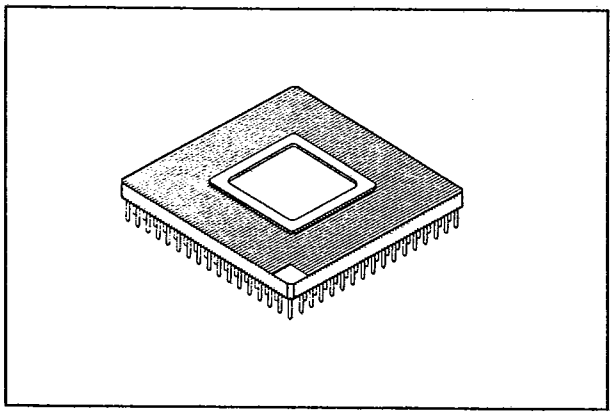
256-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-256C-A03

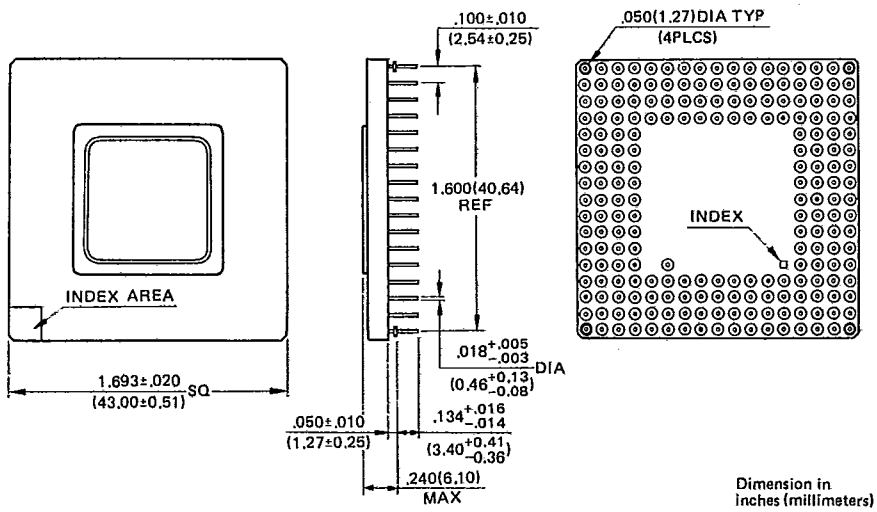


Dimension in inches (milimeters)

PACKAGE DEMENSIONS (Continued)

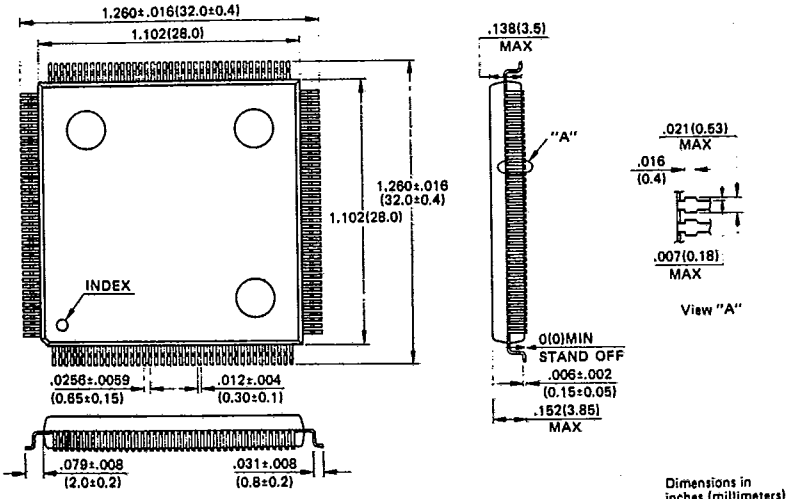


208-LEAD CERAMIC (METAL SEAL) PIN GRID ARRAY PACKAGE
(CASE No.: PGA-208C-A02



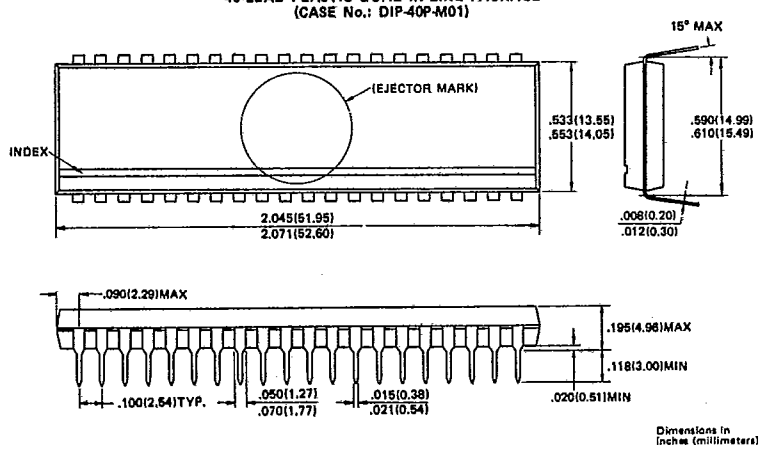
PACKAGE DEMENSIONS (Continued)

160 LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-160P-M01)



Dimensions in inches (millimeters)

40-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-40P-M01)



Dimensions in inches (millimeters)