MYSON TECHNOLOGY

MTV012A

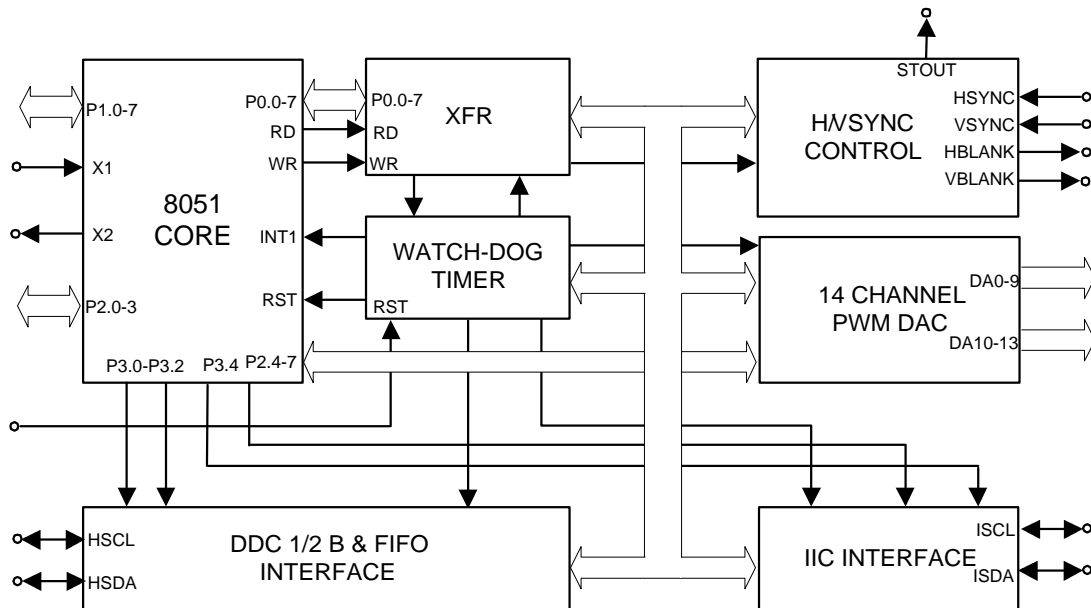## 8051 Embedded CRT Monitor Controller Mask Version

FEATURES

8051 core.
256 bytes internal RAM.
8K bytes program Mask ROM.
14 channels 10V open drain PWM DAC, 10 dedicated channels and 4 channels shared with I/O pin.
20 bi-direction I/O pin, 12 dedicated pin, 4 shared with DAC, 4 shared with DDC/IIC interface.
3 output pins shared with H/V sync output and self test output pins.
SYNC processor for composite sync separation, polarity and frequency check, and polarity adjustment.
Built-in monitor self test pattern generator.
Built-in Low Power Reset circuit.
IIC interface for DDC1/DDC2B and EEPROM, only one EEPROM needed to store DDC1/DDC2B and display mode information.
Watch dog timer with programmable interval.
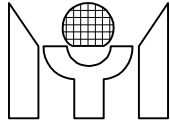40 pin PDIP package.

GENERAL DESCRIPTION

The MTV012A micro controller is an 8051 CPU core-embedded device specially tailored to CRT monitor applications. It includes an 8051 CPU core, 256-byte SRAM, 14 built-in PWM DACs, DDC1/DDC2B interface, 24Cxx series EEPROM interface and an 8K-byte internal program ROM.
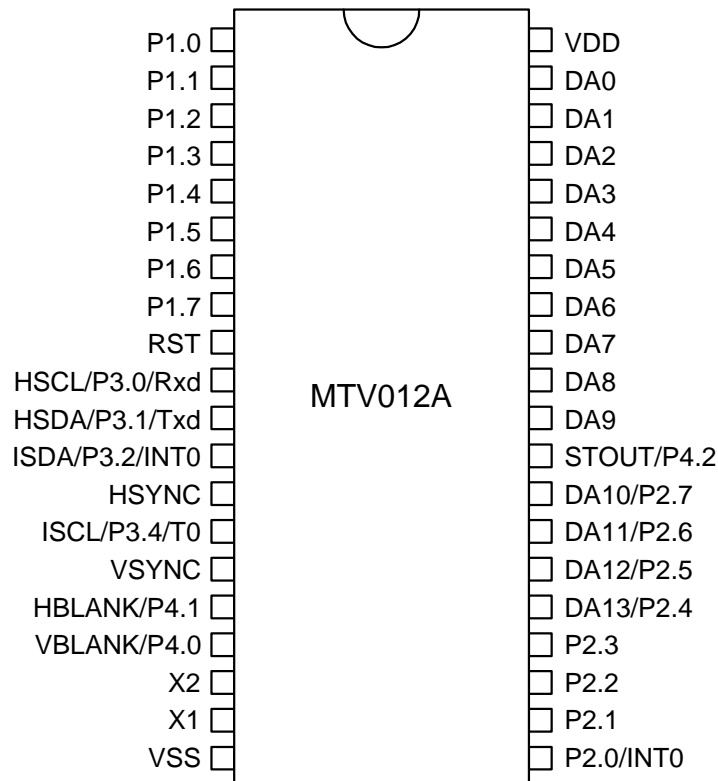
BLOCK DIAGRAM

MYSON TECHNOLOGY

MTV012A

1.0 PIN CONNECTION

```
        P1.0 ⊐           ⊏ VDD
        P1.1 ⊐           ⊏ DA0
        P1.2 ⊐           ⊏ DA1
        P1.3 ⊐           ⊏ DA2
        P1.4 ⊐           ⊏ DA3
        P1.5 ⊐           ⊏ DA4
        P1.6 ⊐           ⊏ DA5
        P1.7 ⊐           ⊏ DA6
         RST ⊐           ⊏ DA7
  HSCL/P3.0/Rxd ⊐  MTV012A  ⊏ DA8
  HSDA/P3.1/Txd ⊐          ⊏ DA9
  ISDA/P3.2/INT0 ⊐         ⊏ STOUT/P4.2
        HSYNC ⊐           ⊏ DA10/P2.7
   ISCL/P3.4/T0 ⊐         ⊏ DA11/P2.6
        VSYNC ⊐           ⊏ DA12/P2.5
  HBLANK/P4.1 ⊐           ⊏ DA13/P2.4
  VBLANK/P4.0 ⊐           ⊏ P2.3
           X2 ⊐           ⊏ P2.2
           X1 ⊐           ⊏ P2.1
          VSS ⊐           ⊏ P2.0/INT0
```

2.0 PIN DESCRIPTION

Name	Type	Pin#	Description
P1.0	I/O	1	General purpose I/O.
P1.1	I/O	2	General purpose I/O.
P1.2	I/O	3	General purpose I/O.
P1.3	I/O	4	General purpose I/O.
P1.4	I/O	5	General purpose I/O.
P1.5	I/O	6	General purpose I/O.
P1.6	I/O	7	General purpose I/O.
P1.7	I/O	8	General purpose I/O.
RST	I	9	Active high reset.
HSCL/P3.0/Rxd	I/O	10	IIC clock / General purpose I/O / Rxd.
HSDA/P3.1/Txd	I/O	11	IIC data / General purpose I/O / Txd.
ISDA/P3.2/INT0	I/O	12	IIC data / General purpose I/O / INT0.
HSYNC	I	13	Horizontal SYNC or composite SYNC.
ISCL/P3.4/T0	I/O	14	IIC clock / General purpose I/O / T0.
VSYNC	I	15	Vertical SYNC.
HBLANK/P4.1	O	16	Horizontal blank / General purpose output.
VBLANK/P4.0	O	17	Vertical blank / General purpose output.
X2	O	18	Oscillator output.
X1	I	19	Oscillator input.
VSS	-	20	Negative power supply.
P2.0/INT0	I/O	21	General purpose I/O / INT0.
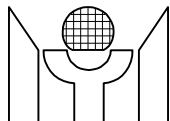
P2.1	I/O	22	General purpose I/O.
P2.2	I/O	23	General purpose I/O.
P2.3	I/O	24	General purpose I/O.
DA13/P2.4	I/O	25	PWM DAC output / General purpose I/O (open-drain).
DA12/P2.5	I/O	26	PWM DAC output / General purpose I/O (open-drain).
DA11/P2.6	I/O	27	PWM DAC output / General purpose I/O (open-drain).
DA10/P2.7	I/O	28	PWM DAC output / General purpose I/O (open-drain).
STOUT/P4.2	O	29	Self-test video output / General purpose output.
DA9	O	30	PWM DAC output (open-drain).
DA8	O	31	PWM DAC output (open-drain).
DA7	O	32	PWM DAC output (open-drain).
DA6	O	33	PWM DAC output (open-drain).
DA5	O	34	PWM DAC output (open-drain).
DA4	O	35	PWM DAC output (open-drain).
DA3	O	36	PWM DAC output (open-drain).
DA2	O	37	PWM DAC output (open-drain).
DA1	O	38	PWM DAC output (open-drain).
DA0	O	39	PWM DAC output (open-drain).
VDD	-	40	Positive power supply.

3.0 FUNCTIONAL DESCRIPTION

1. 8051 CPU Core

MTV012A includes all the 8051 functions with the following exceptions:

1.1 PSEN, ALE, RD and WR pins are disabled. The external RAM access is restricted to XFRs within MTV012A.

1.2 Port0, port3.3 and ports3.5 ~ 3.7 are not general purpose I/O ports. They are dedicated to monitoring control/DAC pins.

1.3 INT1 and T1 input pins are not provided.

1.4 Ports2.4 ~ 2.7 are shared with DAC pins; ports3.0 ~ 3.2 and port3.4 are shared with monitor control pins.

In addition, there are 2 timers, 5 interrupt sources and a serial interface compatible with the standard 8051. The Txd/Rxd (P3.0/P3.1) pins are shared with the DDC interface. INT0/T0 pins are shared with the IIC interface. An extra option can be used to switch the INT0 source from P3.2 to P2.0. This feature maintains an external interrupt source when the IIC interface is enabled.

Note: All registers listed in this document reside in the external RAM area (XFR). For the internal RAM memory map, please refer to the 8051 spec.

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PADMOD	30h (w)	SINT0	X	DDCE	IICE	DA13E	DA12E	DA11E	DA10E

SINT0   = 1   → INT0 source is pin #21.
         = 0   → INT0 source is pin #12.
DDCE   = 1   → Pin #10 is HSCL; pin #11 is HSDA.
         = 0   → Pin #10 is P3.0/Rxd; pin #11 is P3.1/Txd.
IICE   = 1   → Pin #12 is ISDA; pin #14 is ISCL.
         = 0   → Pin #12 is P3.2/(INT0*); pin #14 is P3.4/T0.
DA13E = 1   → Pin #25 is DA13.
         = 0   → Pin #25 is P2.4.
DA12E = 1   → Pin #26 is DA12.
         = 0   → Pin #26 is P2.5.
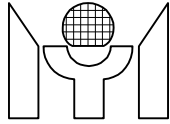
DA11E = 1 $\rightarrow$ Pin #27 is DA11.
     = 0 $\rightarrow$ Pin #27 is P2.6.
DA10E = 1 $\rightarrow$ Pin #28 is DA10.
     = 0 $\rightarrow$ Pin #28 is P2.7.
* SINT0 should be 0 in this case.

2. External Special Function Registers (XFR)

The XFR is a group of registers allocated in the 8051 external RAM area. Most of the registers are used for monitor control or PWM DAC. The program can initialize Ri value and use "MOVX" instruction to access these registers.

3. PWM DAC

Each D/A converter's output pulse width is controlled by an 8-bit register in the XFR. The frequency of these outputs is (Xtal frequency)/253 or (Xtal frequency)/256, selected by DIV253. If DIV253=1, writing FDH/FEH/FFH to the DAC register generates a stable high output. If DIV253=0, the output will pulse low at least once even if the DAC register's content is FFH. Writing 00H to the DAC register generates stable low output.

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
DA0	20h (r/w)	$DA0_{b7}$	$DA0_{b6}$	$DA0_{b5}$	$DA0_{b4}$	$DA0_{b3}$	$DA0_{b2}$	$DA0_{b1}$	$DA0_{b0}$
DA1	21h (r/w)	$DA1_{b7}$	$DA1_{b6}$	$DA1_{b5}$	$DA1_{b4}$	$DA1_{b3}$	$DA1_{b2}$	$DA1_{b1}$	$DA1_{b0}$
DA2	22h (r/w)	$DA2_{b7}$	$DA2_{b6}$	$DA2_{b5}$	$DA2_{b4}$	$DA2_{b3}$	$DA2_{b2}$	$DA2_{b1}$	$DA2_{b0}$
DA3	23h (r/w)	$DA3_{b7}$	$DA3_{b6}$	$DA3_{b5}$	$DA3_{b4}$	$DA3_{b3}$	$DA3_{b2}$	$DA3_{b1}$	$DA3_{b0}$
DA4	24h (r/w)	$DA4_{b7}$	$DA4_{b6}$	$DA4_{b5}$	$DA4_{b4}$	$DA4_{b3}$	$DA4_{b2}$	$DA4_{b1}$	$DA4_{b0}$
DA5	25h (r/w)	$DA5_{b7}$	$DA5_{b6}$	$DA5_{b5}$	$DA5_{b4}$	$DA5_{b3}$	$DA5_{b2}$	$DA5_{b1}$	$DA5_{b0}$
DA6	26h (r/w)	$DA6_{b7}$	$DA6_{b6}$	$DA6_{b5}$	$DA6_{b4}$	$DA6_{b3}$	$DA6_{b2}$	$DA6_{b1}$	$DA6_{b0}$
DA7	27h (r/w)	$DA7_{b7}$	$DA7_{b6}$	$DA7_{b5}$	$DA7_{b4}$	$DA7_{b3}$	$DA7_{b2}$	$DA7_{b1}$	$DA7_{b0}$
DA8	28h (r/w)	$DA8_{b7}$	$DA8_{b6}$	$DA8_{b5}$	$DA8_{b4}$	$DA8_{b3}$	$DA8_{b2}$	$DA8_{b1}$	$DA8_{b0}$
DA9	29h (r/w)	$DA9_{b7}$	$DA9_{b6}$	$DA9_{b5}$	$DA9_{b4}$	$DA9_{b3}$	$DA9_{b2}$	$DA9_{b1}$	$DA9_{b0}$
DA10	2Ah (r/w)	$DA10_{b7}$	$DA10_{b6}$	$DA10_{b5}$	$DA10_{b4}$	$DA10_{b3}$	$DA10_{b2}$	$DA10_{b1}$	$DA10_{b0}$
DA11	2Bh (r/w)	$DA11_{b7}$	$DA11_{b6}$	$DA11_{b5}$	$DA11_{b4}$	$DA11_{b3}$	$DA11_{b2}$	$DA11_{b1}$	$DA11_{b0}$
DA12	2Ch (r/w)	$DA12_{b7}$	$DA12_{b6}$	$DA12_{b5}$	$DA12_{b4}$	$DA12_{b3}$	$DA12_{b2}$	$DA12_{b1}$	$DA12_{b0}$
DA13	2Dh (r/w)	$DA13_{b7}$	$DA13_{b6}$	$DA13_{b5}$	$DA13_{b4}$	$DA13_{b3}$	$DA13_{b2}$	$DA13_{b1}$	$DA13_{b0}$
WDT	80h	WEN	WCLR	CLRDDC	DIV253	X	WDT2	WDT1	WDT0

DA0 (r/w) :   The output pulse width control for DA0.
DA1 (r/w) :   The output pulse width control for DA1.
DA2 (r/w) :   The output pulse width control for DA2.
DA3 (r/w) :   The output pulse width control for DA3.
DA4 (r/w) :   The output pulse width control for DA4.
DA5 (r/w) :   The output pulse width control for DA5.
DA6 (r/w) :   The output pulse width control for DA6.
DA7 (r/w) :   The output pulse width control for DA7.
DA8 (r/w) :   The output pulse width control for DA8.
DA9 (r/w) :   The output pulse width control for DA9.
DA10 (r/w) :   The output pulse width control for DA10.
DA11 (r/w) :   The output pulse width control for DA11.
DA12 (r/w) :   The output pulse width control for DA12.
DA13 (r/w) :   The output pulse width control for DA13.
WDT (w) :   Watchdog timer & special control bit.
    DIV253 = 1 $\rightarrow$ The PWM DAC output frequency is (Xtal frequency)/253.
         = 0 $\rightarrow$ The PWM DAC output frequency is (Xtal frequency)/256.
*1. All D/A converters are centered with value 80h after power-on.
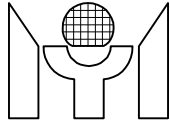
4. H/V SYNC Processing

The H/V SYNC processing block performs the functions of composite signal separation, SYNC input presence check, frequency counting, and polarity detection and control, as well as protection of VBLANK output while VSYNC speeds up to a high DDC communication clock rate. The present and frequency function block treat any pulse shorter than 1 OSC period as noise.

4.1 Composite SYNC Separate
MTV012A continuously monitors the input HSYNC. If the vertical SYNC pulse can be extracted from the input, a CVpre flag is set and the user can select the extracted "CVSYNC" for the source of polarity check, frequency count and VBLANK. The CVSYNC will have a 10-16 us delay compared to the original signal. The delay depends on the OSC frequency and composite mix method.

4.2 H/V Frequency Counter
MTV012A can discriminate between HSYNC/VSYNC frequency and saves the information in XFRs. The 15-bit H counter counts the time of the 64xHSYNC period, but only 11 upper bits are loaded into the HCNTH/HCNTL latch.

The 11-bit output value will be (2/Hfreq) / (1/OSCfreq), updated once per VSYNC/CVSYNC period when VSYNC/CVSYNC is present, or continuously updated when VSYNC/CVSYNC is not present. The 14-bit V counter counts the time between 2 VSYNC pulses, but only 9 upper bits are loaded into the VCNTH/VCNTL latch. The 9-bit output value will be (1/Vfreq) / (512/OSCfreq), updated every VSYNC/CVSYNC period. An extra overflow bit indicates the condition of H/V counter overflow. The VFchg/HFchg interrupt is active when VCNT/HCNT value changes or overflows. Tables 4.2.1 and 4.2.2 show the HCNT/VCNT value under the 8MHz OSC operations.
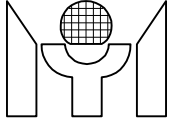
4.2.1 H-Freq Table

H-Freq(KHZ)		Output Value (11 bits)	
		8MHz OSC (hex / dec)	**12MHz OSC (hex / dec)**
1	30	215h / 533	320h / 800
2	31.5	1FBh / 507	2F9h / 761
3	33.5	1DDh /477	2CCh / 716
4	35.5	1C2h / 450	2A4h / 676
5	36.8	1B2h / 434	28Ch / 652
6	38	1A5h / 421	277h / 631
7	40	190h / 400	258h / 600
8	48	14Dh / 333	1F4h / 500
9	50	140h / 320	1E0h / 480
10	57	118h / 280	1A5h / 421
11	60	10Ah / 266	190h / 400
12	64	0FAh / 250	177h / 375
13	100	0A0h / 160	0F0h / 240

*1. The H-Freq output (HF10 - HF0) is valid.
*2. The tolerance deviation is ± 1 LSB.

4.2.2 V-Freq Table

V-Freq(Hz)		Output Value (9 bits)	
		8MHz OSC (hex / dec)	**12MHz OSC (hex / dec)**
1	56.25	115h / 277	1A0h / 416
2	59.94	104h / 260	187h / 391
3	60	104h / 260	186h / 390
4	60.32	103h / 259	184h / 388

5	60.53	102h / 258	183h / 387
6	66.67	0EAh / 234	15Fh / 351
7	70.069	0DEh / 222	14Eh / 334
8	70.08	0DEh / 222	14Eh / 334
9	72	0D9h /217	145h / 325
10	72.378	0D7h / 215	143h / 323
11	72.7	0D6h / 214	142h / 322
12	87	0B3h / 179	10Dh / 269

*1. The V-Freq output (VF8 - VF0) is valid.
*2. The tolerance deviation is ± 1 LSB.

4.3 H/V Present Check

The H present function checks the input HSYNC pulse; the Hpre flag is set when HSYNC is over 10KHz or cleared when HSYNC is under 10Hz. The V present function checks the input VSYNC pulse; the Vpre flag is set when VSYNC is over 40Hz or cleared when VSYNC is under 10Hz. The control bit "PREFS" selects the time base for these functions. The HPRchg interrupt is set when the Hpre value changes. The VPRchg interrupt is set when the Vpre/CVpre values change. However, the CVpre flag interrupt may be disabled when S/W disables the composite function.

### 4.4 H/V Polarity Detection

The polarity functions detect the input HSYNC/VSYNC high and low pulse duty cycle. If the high pulse duration is longer than that of the low pulse, the negative polarity is asserted; otherwise, positive polarity is asserted. The HPLchg interrupt is set when the Hpol value changes. The VPLchg interrupt is set when the Vpol value changes.

4.5 Output HBLANK/VBLANK Control and Polarity Adjustment

HBLANK is the MUX output of HSYNC and the self-test horizontal pattern. The VBLANK is the MUX output of VSYNC, CVSYNC and the self-test vertical pattern. The MUX selection and output polarity are S/W controllable. The VBLANK output is cut off when VSYNC frequency is over 200Hz or 133Hz depends on 8MHz/12MHz OSC selection. HBLANK/VBLANK shares the output pin with P4.1/ P4.0.

4.6 Self-Test Pattern Generator

This generator can generate 4 display patterns for testing purposes: positive cross-hatch, negative cross-hatch, full white and full black (shown in the following figure). It was originally designed to support monitor manufacturers to do a burn-in test, or offer the end-user a reference to check the monitor. The generator's output STOUT shares the output pin with P4.2.
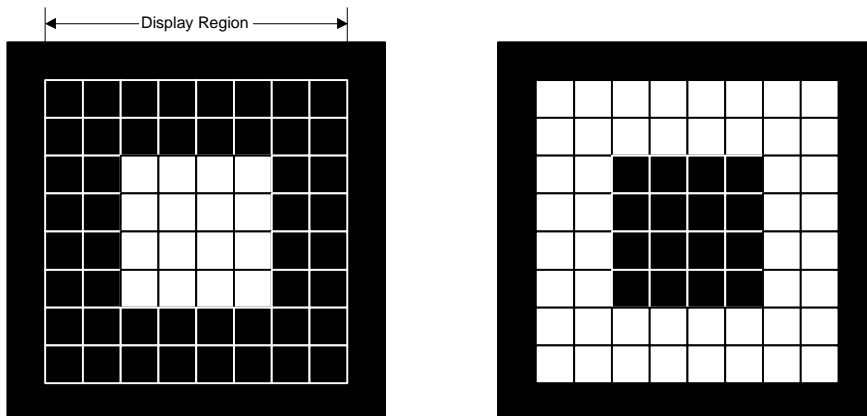
Self-Test Patterns (1)
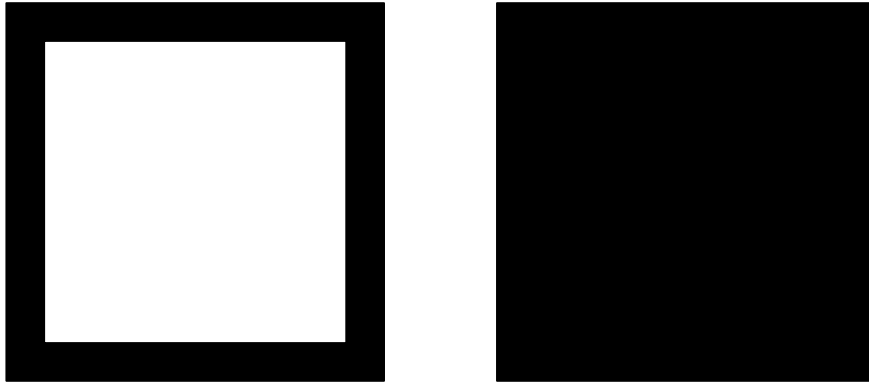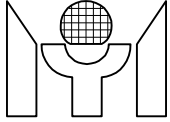
Self-Test Patterns (2)

4.7 H/V Sync Processor Register
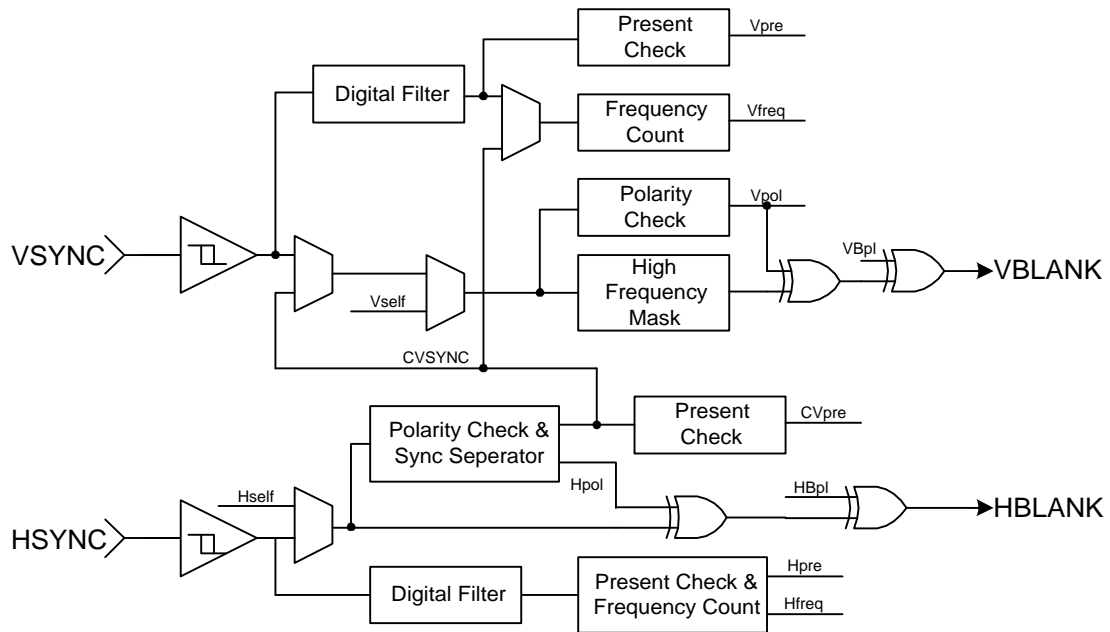
H/V SYNC Processor Block Diagram

reg name	addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
PSTUS	40h (r)	CVpre	X	Hpol	Vpol	Hpre	Vpre	Hoff	Voff
HCNTH	41h (r)	Hovf	X	X	X	X	HF10	HF9	HF8
HCNTL	42h (r)	HF7	HF6	HF5	HF4	HF3	HF2	HF1	HF0
VCNTH	43h (r)	Vovf	X	X	X	X	X	X	VF8
VCNTL	44h (r)	VF7	VF6	VF5	VF4	VF3	VF2	VF1	VF0
PCTR0	40h (w)	C1	C0	HVsel	STOsel	PREFS	HALFV	HBpl	VBpl
PCTR2	42h (w)	X	X	X	Selft	ST_{bsh}	Rt1	Rt0	STF
P4OUT	44h (w)	X	X	X	X	X	P42	P41	P40
INTFLG	50h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	FIFOI	MI
INTEN	60h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EFIFO	EMI

PSTUS (r): The status of polarity, present and static level for HSYNC and VSYNC.

$\quad$ CVpre $\ = 1 \qquad \rightarrow$ The extracted CVSYNC is present.

$\qquad\qquad = 0 \qquad \rightarrow$ The extracted CVSYNC is not present.

$\quad$ Hpol $\ = 1 \qquad \rightarrow$ HSYNC input is positive polarity.
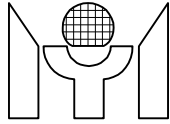
	= 0	→ HSYNC input is negative polarity.
V_{pol}	= 1	→ VSYNC (CVSYNC) is positive polarity.
	= 0	→ VSYNC (CVSYNC) is negative polarity.
H_{pre}	= 1	→ HSYNC input is present.
	= 0	→ HSYNC input is not present.
V_{pre}	= 1	→ VSYNC input is present.
	= 0	→ VSYNC input is not present.
$H_{off}*$	= 1	→ HSYNC input's off-level is high.
	= 0	→ HSYNC input's off-level is low.
$V_{off}*$	= 1	→ VSYNC input's off-level is high.
	= 0	→ VSYNC input's off-level is low.

*H_{off} and V_{off} are valid when H_{pre}=0 or V_{pre}=0.

HCNTH (r) :   H-Freq counter's high bits.

    H_{ovf} = 1 → H-Freq counter overflows; this bit is cleared by H/W when condition removed.

    HF10 - HF8 :   3 high bits of H-Freq counter.

HCNTL (r) :   H-Freq counter's low bits.

VCNTH (r) :   V-Freq counter's high bits.

    V_{ovf} = 1 → V-Freq counter overflows; this bit is cleared by H/W when condition removed.

    VF8 :   High bit of V-Freq counter.

VCNTL (r) :   V-Freq counter's low bits.

PCTR0 (w) :   SYNC processor control register 0.

C1, C0	= 1,1	→ Selects CVSYNC as the polarity, freq and VBLANK source.
	= 1,0	→ Selects VSYNC as the polarity, freq and VBLANK source.
	= 0,0	→ Disables composite function (MTV012 compatible mode).
	= 0,1	→ H/W auto switch to CVSYNC when CVpre=1 and VSpre=0.
HVsel	= 1	→ Pin #16 is P41, pin #17 is P40.
	= 0	→ Pin #16 is HBLANK, pin #17 is VBLANK.
STOsel	= 1	→ Pin #29 is P42.
	= 0	→ Pin #29 is STOUT.
PREFS	= 0	→ Selects 8MHz OSC as H/V present check and self-test pattern time base.
	= 1	→ Selects 12MHz OSC as H/V present check and self-test pattern time base.
HALFV	= 1	→ VBLANK is half frequency output of VSYNC.
HBpl	= 1	→ Negative polarity HBLANK output.
	= 0	→ Positive polarity HBLANK output.
VBpl	= 1	→ Negative polarity VBLANK output.
	= 0	→ Positive polarity VBLANK output.

PCTR2 (w) :   Self-test pattern generator control.

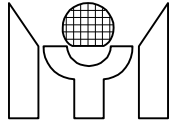|		
S_{elft}	= 1	→ Enables generator.
	= 0	→ Disables generator.
ST_{bsh}	= 1	→ 63.5KHz (horizontal) output selected.
	= 0	→ 31.75KHz (horizontal) output selected.
Rt1,Rt0	= 0,0	→ Positive cross-hatch pattern output.
	= 0,1	→ Negative cross-hatch pattern output.
	= 1,0	→ Full white pattern output.
	= 1,1	→ Full black pattern output.

STF   = 1   → Enables STOUT output.
        = 0   → Disables STOUT output.

P4OUT (w) :   Port 4 data output value.

INTFLG (w) :   Interrupt flag. An interrupt event will set its individual flag, and, if the corresponding interrupt enable bit is set, the 8051 core's INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

     HPRchg= 1   → No action.
           = 0   → Clears HSYNC presence change flag.
     VPRchg= 1   → No action.
           = 0   → Clears VSYNC presence change flag.
     HPLchg= 1   → No action.
           = 0   → Clears HSYNC polarity change flag.
     VPLchg= 1   → No action.
           = 0   → Clears VSYNC polarity change flag.
     HFchg = 1   → No action.
           = 0   → Clears HSYNC frequency change flag.
     VFchg = 1   → No action.
           = 0   → Clears VSYNC frequency change flag.

INTFLG (r) :   Interrupt flag.
     HPRchg= 1   → Indicates an HSYNC presence change.
     VPRchg= 1   → Indicates a VSYNC presence change.
     HPLchg= 1   → Indicates an HSYNC polarity change.
     VPLchg= 1   → Indicates a VSYNC polarity change.
     HFchg = 1   → Indicates an HSYNC frequency change or counter overflow.
     VFchg = 1   → Indicates a VSYNC frequency change or counter overflow.

INTEN (w) :   Interrupt enabler.
     EHPR = 1   → Enables HSYNC presence change interrupt.
     EVPR = 1   → Enables VSYNC presence change interrupt.
     EHPL = 1   → Enables HSYNC polarity change interrupt.
     EVPL = 1   → Enables VSYNC polarity change interrupt.
     EHF   = 1   → Enables HSYNC frequency change / counter overflow interrupt.
   EVF   = 1   → Enables VSYNC frequency change / counter overflow interrupt.

5. DDC & IIC Interface

5.1 DDC1 Mode

MTV012A enters DDC1 mode after reset. In this mode, VSYNC is used as a data clock when the HSCL pin remains at high. The data stream taken from an 8-bit FIFO in MTV012A is sent in a 9-bit packet that includes a null bit (=1) as packet separator. The software program should take care of the FIFO depth. The FIFO generates a FIFOI interrupt when there are fewer than N (N = 1, 2, 3 or 4 controlled by LS1, LS0) bytes to be output to the HSDA line. On the other hand, the FIFO sets the FIFOH flag when there are more than 7 bytes queuing for output. The FIFOI interrupt can be enabled or disabled by S/W. A simple way to control FIFO is to set {LS1,LS0}={1,0} and enable FIFOI, then load FIFO 4 bytes every time a FIFOI interrupt occurs. A special control bit "LDFIFO" can reduce S/W effort when EDID data is saved in EEPROM. If LDFIFO=1, FIFO will be automatically loaded when S/W reads MBUF XFR.

5.2 DDC2B Mode

MTV012A switches to DDC2B mode when it detects a high to low transition on the HSCL pin. Once MTV012A enters DDC2B mode, the host can access the EEPROM using IIC bus protocol as if the HSDA and HSCL are directly bypassed to ISDA and ISCL pins. MTV012A will return to DDC1 mode if HSCL is kept high for a 128-VSYNC clock period. However, it will permanently remain in DDC2B mode if a valid IIC access has been detected on the HSCL/HSDA bus. The DDC2 flag reflects the current DDC
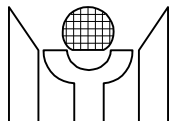
status; S/W may clear it by setting CLRDDC. The control bits M128/M256 are used to block the EEPROM write operation from the host if the address is over 128/256.

5.3 Master Mode IIC Function Block

The master mode IIC block is connected to the ISDA and ISCL pins. The software program can access the external EEPROM through this interface. Since the EDID/VDIF data and the display information share the common EEPROM, precaution must be taken to avoid bus conflict. In DDC1 mode, the IIC interface is controlled by MTV012A only. In DDC2B mode, the host may access the EEPROM directly. Software can test the HSCL condition by reading the BUSY flag, which is set in case of HSCL=0. A summary of master IIC access is illustrated as follows:

5.3.1. To Write EEPROM
1. Write to MBUF the EEPROM slave address (bit 0 = 0).
2. Set S bit to Start.
3. After MTV012A transmits this byte, a MI interrupt will be triggered.
4. The program can write MBUF to transfer the next byte, or set the P bit to stop.
* Please see the attachments about "Master IIC Transmission Timing".

5.3.2. To Read EEPROM
1. Write to MBUF the slave address (bit 0 = 1).
2. Set the S bit to Start.
3. After MTV012A transmits this byte, a MI interrupt will be triggered.
4. Set or reset the ACK flag according to the IIC protocol.
5. Read out to MBUF the useless byte in order to continue the data transfer.
6. After MTV012A receives a new byte, the MI interrupt is triggered again.
7. Reading MBUF also triggers the next receiving operation, but the P bit needs to be set before reading can terminate the operation.
* Please see the attachments about the "Master IIC Timing Receiving".

5.4 Slave Mode IIC Function Block

The slave mode IIC block can be connected to HSDA/HSCL pins or ISDA/ISCL pins, and selected by the SLVsel control bit. This block is receiving mode only. S/W may set the SLVADR register to determine the address range to which this block should respond. The block first detects an IIC slave address match condition, then issues a SLVMI interrupt. The data received from SDA is shifted onto the shift register and moved to the SLVBUF latch. The first byte loaded is the word address (the slave address is dropped). This block also generates a SLVBI each time the SLVBUF is loaded. If S/W can't read out the SLVBUF in time, the next byte will not be written to SLVBUF and the slave block returns NACK to the master. This feature guarantees the data integrity of communication. A WADR flag can tell S/W if the data in SLVBUF is a word address.
* Please see the attachments about "Slave IIC Block Timing".

6. Low Power Reset (LVR) & Watchdog Timer

When the voltage level of the power supply is below 4.0V for a specific time, the LVR will generate a chip reset signal. After the power supply is above 4.0V, LVR maintains the reset state for a 144 Xtal cycle to guarantee that the chip exit reset condition has a stable Xtal oscillation. The specific time of power supply in the low level is 3us and is adjustable by an external capacitor connected to the RST pin.

The watchdog timer automatically generates a device reset when it overflows. The interval of overflow is 0.25 sec x N, in which N is a number from 1 to 8, and can be programmed via register WDT(2:0). The timer function is disabled after power-on reset; the user can activate this function by setting WEN, and clear the timer by setting WCLR.

reg name	Addr	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MSTUS	00h (r)	X	SCLERR	DDC2	BERR	HFREQ	FIFOH	FIFOL	BUSY
MBUF	10h (r/w)	MBUF7	MBUF6	MBUF5	MBUF4	MBUF3	MBUF2	MBUF1	MBUF0
INTFLG	50h (r/w)	HPRchg	VPRchg	HPLchg	VPLchg	HFchg	VFchg	FIFOI	MI
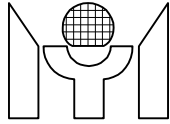
MCTR	00h (w)	LS1	LS0	LDFIFO	M256	M128	ACK	P	S
INTEN	60h (w)	EHPR	EVPR	EHPL	EVPL	EHF	EVF	EFIFO	EMI
FIFO	70h (w)	FIFO7	FIFO6	FIFO5	FIFO4	FIFO3	FIFO2	FIFO1	FIFO0
WDT	80h (w)	WEN	WCLR	CLRDDC	DIV253	LVSEL	WDT2	WDT1	WDT0
SLVCTR	90h (w)	ENSLV	SLVsel	ESLVBI	ESLVMI	X	X	X	X
SLVSTUS	91h (r)	WADR	SLVS	SLVBI	SLVMI	X	X	X	X
SLVINT	91h (w)	X	X	X	SLVMI	X	X	X	X
SLVBUF	92h (r)	SLVbuf7	SLVbuf6	SLVbuf5	SLVbuf4	SLVbuf3	SLVbuf2	SLVbuf1	SLVbuf0
SLVADR	93h (w)	SLVadr7	SLVadr6	SLVadr5	SLVadr4	SLVadr3	SLVadr2	SLVadr1	X

MCTR (w) :   Master IIC interface control register.

LS1, LS0   = 11 $\rightarrow$ FIFOL is the status which has a FIFO depth of < 5.

                 = 10 $\rightarrow$ FIFOL is the status which has a FIFO depth of < 4.

                 = 01 $\rightarrow$ FIFOL is the status which has a FIFO depth of < 3.

                 = 00 $\rightarrow$ FIFOL is the status which has a FIFO depth of < 2.

LDFIFO   = 1 $\rightarrow$ FIFO will be written while S/W reads MBUF.

M256   = 1 $\rightarrow$ Disables host writing EEPROM when address is over 256.

M128   = 1 $\rightarrow$ Disables host writing EEPROM when address is over 128.

ACK   = 1 $\rightarrow$ In receiving mode, there is no acknowledgment by MTV012A.

                 = 0 $\rightarrow$ In receiving mode, ACK is returned by MTV012A.

S, P   = $\uparrow$,0 $\rightarrow$ Start condition when Master IIC is not transferring.

                 = X,$\uparrow$ $\rightarrow$ Stop condition when Master IIC is not transferring.

                 = 1,X $\rightarrow$ Will resume transfer after a read/write MBUF operation.

                 = X,0 $\rightarrow$ Forces HSCL low and occupies the IIC bus.

 * MTV012A uses a 100KHz clock to sample the S/P bit; any pulse should sustain at least 20us.

 * A write/read MBUF operation can be recognized only after 10us of the MI flag's rising edge.

MSTUS (r) :   Master IIC interface status register.

SCLERR   = 1 $\rightarrow$ The ISCL pin is pulled-low by other devices during the
                                    transfer, and cleared when S=0.

DDC2   = 1 $\rightarrow$ DDC2B is active.

                 = 0 $\rightarrow$ MTV012A remains in DDC1 mode.

BERR   = 1 $\rightarrow$ IIC bus error, no ACK received from the slave, updated every time
                                    when slave sends ACK on the ISDA pin.

HFREQ   = 1 $\rightarrow$ MTV012A detects a higher than 200Hz clock on the VSYNC pin.

FIFOH   = 1 $\rightarrow$ FIFO high indicated.

FIFOL   = 1 $\rightarrow$ FIFO low indicated.

BUSY   = 1 $\rightarrow$ Host drives the HSCL pin to low.

 * While writing FIFO, the FIFOH/FIFOL flag will reflect the FIFO condition after 30us.

INTFLG (w) :   Interrupt flag. An interrupt event will set its individual flag and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

FIFOI   = 1 $\rightarrow$ No action.

         = 0 $\rightarrow$ Clears FIFOI flag.

MI   = 1 $\rightarrow$ No action.

         = 0 $\rightarrow$ Clears Master IIC bus interrupt flag (MI).

INTFLG (r) :   Interrupt flag.

FIFOI   = 1 $\rightarrow$ Indicates the FIFO low condition; when EFIFO is set, MTV012A will be
                           interrupted by INT1.

MI   = 1 $\rightarrow$ Indicates when a byte is sent/received to/from the IIC bus; when EEPI is
                           active, MTV012A will be interrupted by INT1.

INTEN (w) :   Interrupt enabler.

EFIFO   = 1 $\rightarrow$ Enables FIFO interrupt.
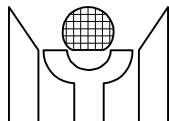
    EMI   = 1   → Enables master IIC bus interrupt.

MBUF (w) :   Master IIC data shift register write; after START and before STOP condition, this register will resume MTV012A's transmission to the IIC bus.

MBUF (r) :   Master IIC data shift register read; after START and before STOP condition, this register will resume MTV012A's receiving from the IIC bus.

WDT (w) :   Watchdog timer control register.

WEN	= 1	→ Enables the watchdog timer.
WCLR	= 1	→ Clears the watchdog timer.
CLRDDC	= 1	→ Clears the DDC2 flag.
LVSEL	= 1	→ Low voltage reset will occur when VDD < 4.1V.
	= 0	→ Low voltage reset will occur when VDD < 3.6V.
WDT2: WDT0	= 0	→ Overflow interval = 8 x 0.25 sec.
	= 1	→ Overflow interval = 1 x 0.25 sec.
	= 2	→ Overflow interval = 2 x 0.25 sec.
	= 3	→ Overflow interval = 3 x 0.25 sec.
	= 4	→ Overflow interval = 4 x 0.25 sec.
	= 5	→ Overflow interval = 5 x 0.25 sec.
	= 6	→ Overflow interval = 6 x 0.25 sec.
	= 7	→ Overflow interval = 7 x 0.25 sec.

FIFO (w) :   Writes FIFO contents.

SLVCTR (w) :   Slave IIC block control.

ENSLV	= 1	→ Enables slave IIC block.
	= 0	→ Disables slave IIC block.
SLVsel	= 1	→ Slave IIC connects to ISDA/ISCL.
	= 0	→ Slave IIC connects to HSDA/HSCL.
ESLVBI	= 1	→ Enables slave buffer interrupt.
ESLVMI	= 1	→ Enables slave address match interrupt.

**SLVSTUS** (r) :   Slave IIC block status.

WADR	= 1	→ The data in SLVBUF is a word address.
SLVS	= 1	→ The slave block has detected a START; will be cleared when STOP is detected.
SLVBI	= 1	→ SLVBUF has been loaded with a new data byte; reset by S/W reading SLVBUF.
SLVMI	= 1	→ Slave block has detected the slave address match condition; cleared by S/W writing 0 to SLVMI.

SLVINT (w) :   Slave block interrupt. The SLVBI/SLVMI interrupt will set its flag, and, if the corresponding interrupt enable bit is set, the 8051 INT1 source will be driven by a zero level. Software MUST clear this register while serving the interrupt routine.

SLVMI	= 1	→ No action.
	= 0	→ Clears SLVMI.

SLVBUF (r) :   Slave IIC data latch.

SLVADR (w) :   Slave IIC address to which the slave block should respond.
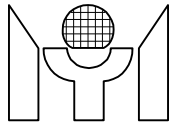
4.0 Test Mode Condition

In normal application, users should not allow MTV012 to enter its test/program mode, outlined as follows:

       Test Mode A: RESET=1 & DA9=0 & DA8=1 & DA7=1 & DA6=0

       Test Mode B: RESET'S falling edge & DA9=1 & DA8=0 & DA7=1 & DA6=0

5.0 ELECTRICAL PARAMETERS

5.1 Absolute Maximum Ratings

at: Ta= 0 to 70 ºC, VSS=0V

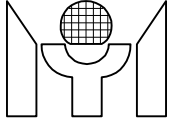| Name	Symbol	Range	Unit
Maximum Supply Voltage	VDD	-0.3 to +6.0	V
Maximum Input Voltage	Vin	-0.3 to VDD+0.3	V
Maximum Output Voltage	Vout	-0.3 to VDD+0.3	V
Maximum Operating Temperature	Topg	0 to +70	ºC
Maximum Storage Temperature	Tstg	-25 to +125	ºC

5.2 Allowable Operating Conditions

at: Ta= 0 to 70 ºC, VSS=0V

Name	Symbol	Min.	Max.	Unit
Supply Voltage	VDD	4.0	6.0	V
Input "H" Voltage	Vih1	0.7 x VDD	VDD +0.3	V
Input "L" Voltage	Vil1	-0.3	0.15 x VDD	V
Operating Freq.	Fopg	-	15	MHz

5.3 DC Characteristics

at: Ta=0 to 70 ºC, VDD=4.0V ~ 6.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Output "H" Voltage; except open-drain pins and pin #s 16, 17, 29	Voh1	Ioh=-50uA	4			V
Output "H" Voltage; pin #s16, 17, 29	Voh2	Ioh=-1mA	4			V
Output "L" Voltage	Vol	Iol=8mA			0.45	V
Power Supply Current	Idd	Active		18	24	mA
		Idle		1.3	4.0	mA
		Power-Down		50	80	uA
RST Pull-Down Resistor	Rrst	VDD=5V	50		150	Kohm
Pin Capacitance	Cio				15	pF

5.4 AC Characteristics

at: Ta=0 to 70 ºC, VDD=4.0V ~ 6.0V, VSS=0V

Name	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal Frequency	fXtal			8		MHz
PWM DAC Frequency	fDA	fXtal=8MHz	31.25		31.62	KHz
PWM DAC Frequency	fDA	fXtal=12MHz	46.875		47.43	KHz
HS Input Pulse Width	tHIPW	fXtal=8MHz	0.3		12	uS
VS Input Pulse Width	tVIPW	fXtal=8MHz	3			US
HS Input Pulse Width	tHIPW	fXtal=12MHz	0.2		8	US
VS Input Pulse Width	tVIPW	fXtal=12MHz	2			US
HSYNC to HBLANK Output Jitter	tHHBJ				5	NS
H+V to VBLANK Output Delay	tVVBD	fXtal=8MHz		16		uS
H+V to VBLANK Output Delay	tVVBD	fXtal=12MHz		10		uS
VS Pulse Width in H+V Signal	tVCPW	fXtal=8MHz	32			uS
VS Pulse Width in H+V Signal	tVCPW	fXtal=12MHz	20			uS

6.0 PACKAGE DIMENSION

40 PIN PDIP 600 mil

MTV012A Revision 1.1 12/23/1998