μPD2364E
8,192 x 8-BIT MASK-PROGRAMMABLE NMOS ROM

Revision 2

Description

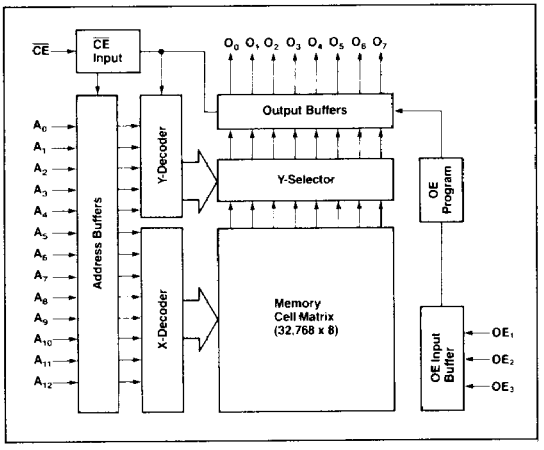
The μPD2364E is a 65,536-bit Read-only Memory utilizing NMOS silicon gate technology. The device is static in operation, organized as 8,192 words by 8 bits and operates from a single +5V power supply. The device has three-state outputs and all inputs and outputs are fully TTL-compatible. The chip select pins are mask-programmable and can be specified by selecting 1, 0, and Don't-care data. Pinout is compatible with 2764 EPROMs.

Features

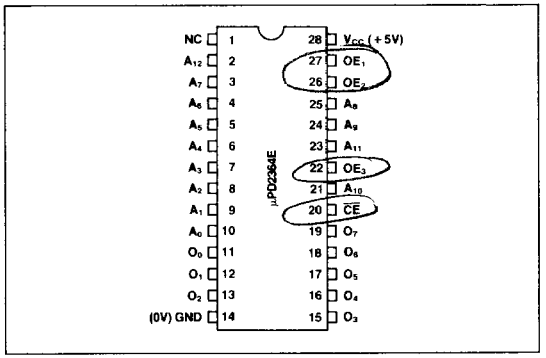
- ☐ All inputs and outputs are fully TTL-compatible
- ☐ Three-state outputs for direct bus compatibility
- ☐ Single +5V ± 5% power supply
- ☐ Three mask-programmable chip selects
- ☐ 2 performance ranges:

Device	Access Time	Power Supply	
		Active	Standby
μPD2364E	250ns	80mA	20mA
μPD2364E-1	200ns	80mA	20mA

Block Diagram



Pin Configuration



Pin Identification

Pin No.	Symbol	Function
1	NC	No Connection.
2–10, 21, 23–25	A_0–A_{12}	Address Inputs.
11–13, 15–19	O_0–O_7	Three-state Data Outputs.
14	GND	Ground.
20	$\overline{CE}$	Chip Enable.
22, 26–27	OE_1–OE_3	Mask-programmable Chip Selects.
28	V_{CC}	Single +5V Power Supply.

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Absolute Maximum Ratings*

Supply Voltage, V_{CC}	−0.5V to +7V
Input Voltage, V_I	−0.5V to +7V
Output Voltage, V_O	−0.5V to +7V
Operating Temperature, T_{OPR}	−10°C to +70°C
Storage Temperature, T_{STG}	−65°C to +150°C

*COMMENT: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = −10°C to +70°C

		Limits							
		μPD2364E			μPD2364E-1				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_I			10			10	pF	f = 1MHz
Output Capacitance	C_O			15			15	pF	f = 1MHz

DC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5V ± 5%

		Limits				
Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.1		V_{CC} + 1.0	V	
Input Low Voltage	V_{IL}	−0.5		+0.7	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −400μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	$V_O = V_{CC}$, chip deselected
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = 0V, chip deselected
Supply Voltage Current	I_{CC1}		45	80	mA	CE = V_{IL}
Supply Voltage Current	I_{CC2}		12	20	mA	CE = V_{IH}, standby mode

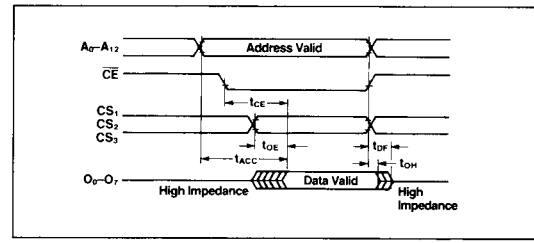
AC Characteristics

T_A = −10°C to +70°C; V_{CC} = +5 ± 5%

		Limits							
		μPD2364E			μPD2364E-1				
Parameter	Symbol	Min	Typ	Max	Min	Typ	Max	Unit	Test Conditions①
Access Time	t_{ACC}			250			200	ns	
Chip Enable Access Time	t_{CE}			250			200	ns	
$\overline{OE}_1$ to $\overline{OE}_3$ Output On Time	t_{OE}	10		110	10		100	ns	
Output Hold Time	t_{OH}	0			0			ns	
Output Disable Time	t_{DF}	0		100	0		90	ns	

Notes: ① Input rise and fall times (t_R, t_F): 20ns
Timing reference levels: Input and Output voltages = 0.8V and 2.0V
Load = 1 TTL + 100 pF

Timing Waveform



Definitions

Access Time, t_{ACC}

Access time is the maximum time between the application of a valid address and the corresponding valid data out.

Output Hold Delay, t_{OH}

Output hold delay is the minimum time after an address change that the previous data remains valid.

Chip Enable Access Time, t_{CE}

The maximum time between application of a valid chip enable input and the corresponding valid outputs.

Output Enable Time, t_{OE}

Output enable time is the maximum delay between chip selects becoming true and output data becoming valid.

Output Disable Time, t_{DF}

Output disable time is the delay between chip selects or chip enable becoming false and output stages going to the high impedance state. t_{DF} is specified as CE or OE, whichever comes first.

Custom Programming Instructions

Bit pattern submittal options

The customer's unique bit pattern can be submitted in several convenient methods that are easy for the ROM customer, and readily verifiable for accuracy. The bit pattern can be delivered to NEC contained within:

1. One programmed 2764 EPROM
2. Two programmed 2732 EPROMs

Bit pattern verification

For customer verification of the submitted bit pattern, several alternatives are also available. The following are those found to be most expeditious.

Customer Pattern Submitted Via	Verification Routine
1. One programmed 2764 EPROM	Customer sends NEC one additional erased 2764. NEC programs the spare 2764 with the data from the programmed 2764, and returns it to the customer for verification.
2. Two programmed 2732 EPROMs	Customer sends NEC two additional erased 2732s. NEC programs the spare 2732s with the data from the programmed EPROMs and returns them to the customer for verification.