AKM

AK2353B

Integrated Base Band LSI for Cordless Telephone Sets with Scrambler

Features

- ☐ Integrated voice band filters with MSK MODEM(2400bps), COMPANDOR and scrambler for cordless telephone sets
- ☐ Low voltage operation (1.9V~5.5V)
- ☐ Fully integrated COMPANDOR, only two external capacitors are required
- ☐ Buffer amplifier for direct drive of a ceramic receiver
- ☐ Switchable reception level (0/+6dB)
- ☐ Transmission and reception voice mute
- ☐ Adjustable limiter level
- ☐ Gain setting amplifiers for receiver and transmitter sections
- ☐ Power down mode
- ☐ 3.58MHz oscillator
- ☐ Frequency invertor scrambler, 2 inversion frequencies are selectable
- ☐ Scrambler bypass mode
- ☐ Frame detection
- ☐ Control register serial interface access
- ☐ Low power CMOS
- ☐ Minimal external components
- ☐ Package: 44 pin QFP / 64 pin SQFP

General Description

AK2353B is an integrated base band LSI for cordless telephone sets. Not only voice band filters but also a 2400bps MSK MODEM (for data communication) and a COMPANDOR (for noise reduction) are integrated into monolithic CMOS LSI.

The COMPANDOR circuit is fully integrated. Therefore, only an external capacitor is required for each compressor and expander. The fully integrated COMPANDOR is also free from aging problem.

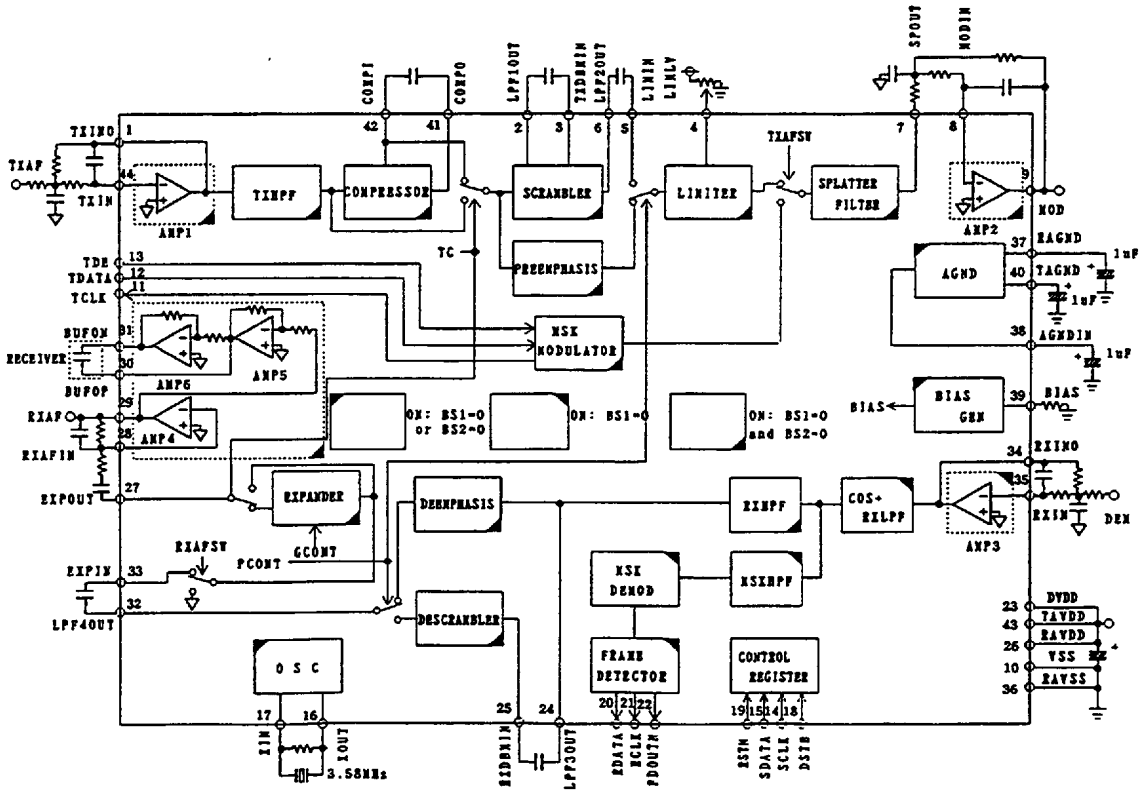
The 2400bps MSK MODEM assures reliable high speed data communication. A 3.58MHz oscillator circuit is integrated, which may also be used for DTMF tone generator clock. No special clock is required for the MSK MODEM.

Frequency invertor is integrated for scrambling. Two inversion frequencies are selectable.

High-pass filter, compressor, pre-emphasis, scrambler, limiter, MSK modulator, splatter filter, etc. are integrated for transmitter.

Band-pass filter, de-emphasis, descrambler, expander, buffer, MSK demodulator, frame detector, etc. are integrated for receiver.

Block Diagram



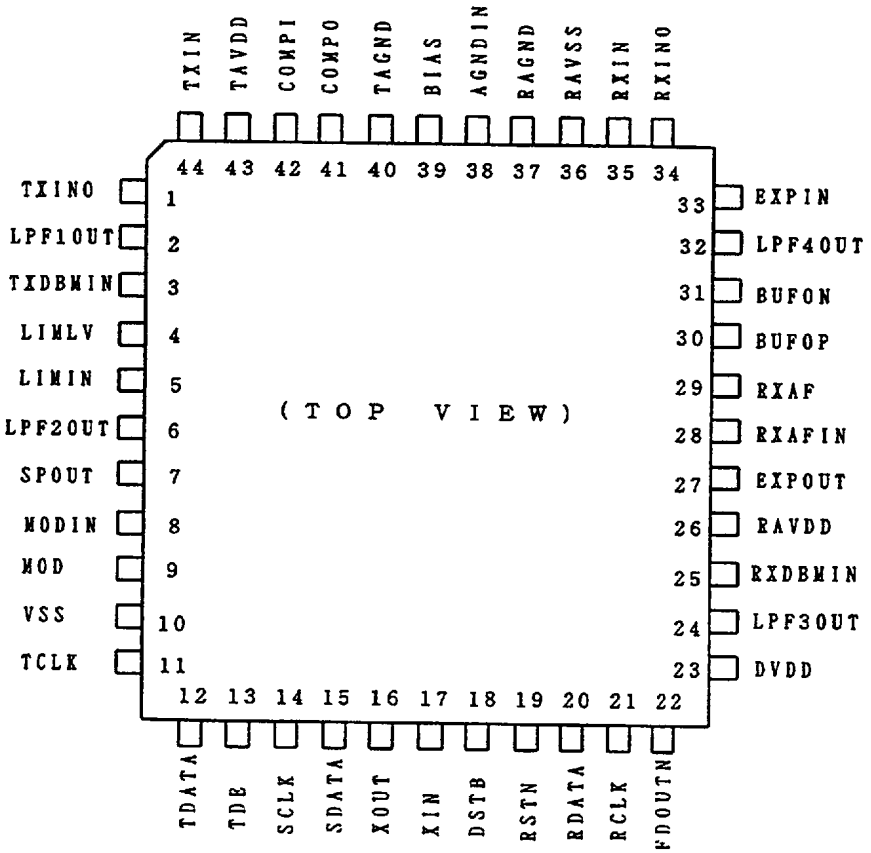
Note: The above pins refer to 44-pin QFP

Ordering Information

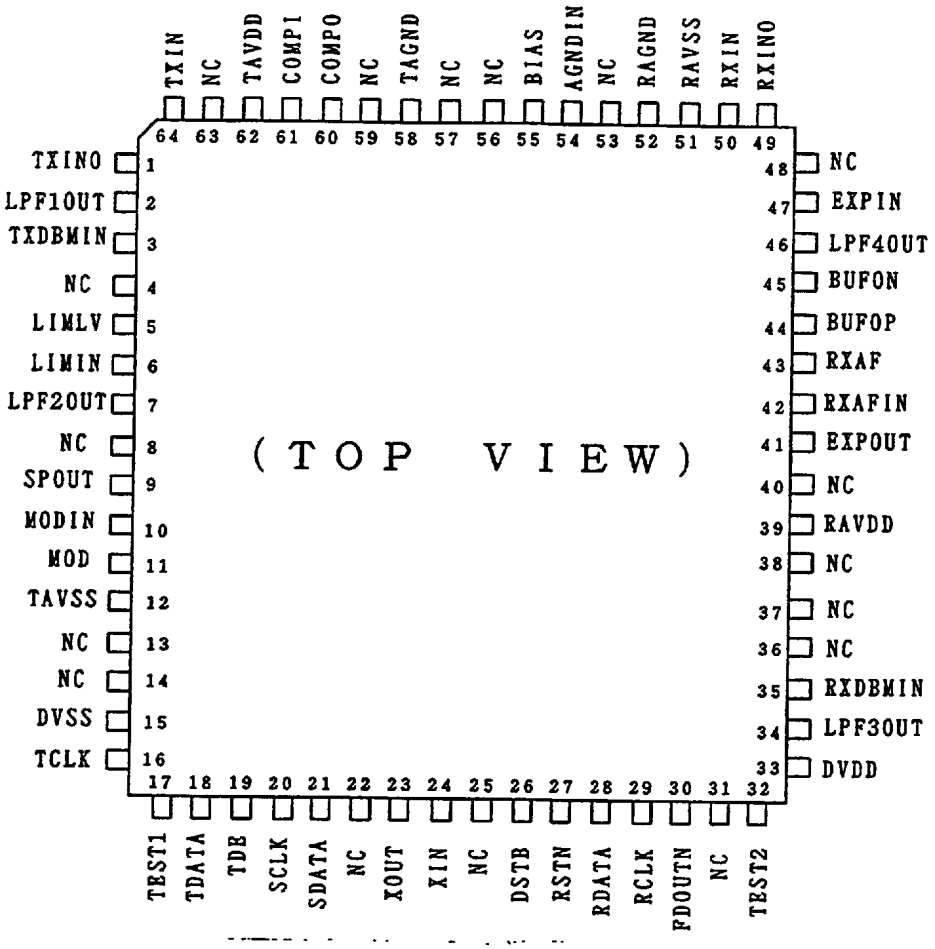
AK2353B	44 pin QFP
AK2353BV	64 pin SQFP

Pin Assignments

■ 44 pin QFP



■ 64 pin SQFP


TXIN 64
NC 63
TAVDD 62
COMPI 61
COMPO 60
NC 59
TAGND 58
NC 57
NC 56
BIAS 55
AGNDIN 54
NC 53
RAGND 52
RAVSS 51
RXIN 50
RXINO 49
TXINO 1
LPF1OUT 2
TXDBMIN 3
NC 4
LIMLV 5
LIMIN 6
LPF2OUT 7
NC 8
SPOUT 9
MODIN 10
MOD 11
TAVSS 12
NC 13
NC 14
DVSS 15
TCLK 16
NC 48
EXPIN 47
LPF4OUT 46
BUFON 45
BUFOP 44
RXAF 43
RXAFIN 42
EXPOUT 41
NC 40
RAVDD 39
NC 38
NC 37
NC 36
RXDBMIN 35
LPF3OUT 34
DVDD 33
TEST1 17
TDATA 18
TDB 19
SCLK 20
SDATA 21
NC 22
XOUT 23
XIN 24
NC 25
DSTB 26
RSTN 27
RDATA 28
RCLK 29
FDOUTN 30
NC 31
TEST2 32
(T O P V I E W)

Circuit Configuration

Functional Block	Functions
AMP1	An Op-Amp for transmit voice signal gain adjustment and anti-aliasing filtering for the succeeding switched capacitor filters (SCF). Adjust the gain to 30dB or less and the cut-off frequency to around 10kHz by properly selecting external capacitor and resistor values.
TxHPF	SCF high pass filter to eliminate 300Hz or lower components contained in the transmit voice signal.
Compress-or	Compress the amplitude of the transmit voice signal.
Pre-Emphasis	Emphasize the high frequency components in the transmit voice signal in order to improve the signal-to-noise performance of the modulated signal.
Scrambler	Frequency inversion method is used for scrambling. Two inversion frequencies are selectable by KEY. Scrambler or pre-emphasis circuit is selectable by PCONT.
Limiter	Amplitude limiting circuit to limit the maximum frequency deviation of the modulated signal. Limiter level is adjustable by varying DC level applying to "LIMLV" pin. The limiter level is set to a pre-fixed level if "LIMLV" pin is left open.
Splatter Filter	SC filter to reject 3kHz or higher components contained in the limiter output signal or MSK Modulator signal.
AMP2	An Op-Amp to form a smoothing filter for the transmit SCF output. Adjust the gain to 0dB and the cut-off frequency to around 10kHz by properly selecting external capacitor and resistor values.
MSK Modulator	Generate 2400bps MSK signal in accordance with digital input signal applied on TDATA pin. "H" : 1.2kHz "L" : 2.4kHz
AMP3	An Op-Amp for receive signal gain adjustment and anti-aliasing filtering for the succeeding SC filters. Adjust the gain to 30dB or less and the cut-off frequency to around 10kHz by properly selecting external capacitor and resistor values.
COS + RxLPF	SC filter to reject 3kHz or higher components contained in the receive signal.
RxHPF	SC filter to reject 300Hz or lower components contained in the receive voice signal.
De-Emphasis	Equalize the pre-emphasized voice signal to original.
De-Scrambler	Inverted signal will be inverted again to recover original signal. Descrambler or de-emphasis circuit is selectable by PCONT.

Functional Block	Function
Expander	Expand the signal amplitude, which was compressed by the compressor to original. GCONT pin sets the expander gain 0dB or 6dB.
AMP4	An Op-Amp to form a smoothing filter for the receiver SCF output. Adjust the gain to 0dB and set the cut-off frequency to around 20kHz by properly selecting external capacitor and resistor values.
MSK HPF	SC filter to reject 100Hz or lower components contained in the received MSK signal.
MSK Demodulator	To recover 2400bps receive data and clock from the MSK signal fed on RXIN pin. 1.2kHz : "H" 2.4kHz : "L"
Frame Detector	Detect received frame pattern. FRPT=1: 1100010011010110 (Base set) FRPT=0: 1001001100110110 (Hand set)
AMP5 AMP6	Inverting, non-inverting buffers to directly drive a ceramic receiver.
BIAS GEN	Bias generator circuit for internal Op Amps.
AGND	Ground reference voltage generator circuit for internal analog signal processing.
OSC Circuit	A 3.58MHz reference clock generator with an external quartz Crystal resonator and a resistor.
Battery Saving	Battery saving mode selection circuit. 1 of 4 modes is selectable by BS1 and BS2 registers.

Pin/Function Descriptions

Pin#	Name	I/O	Function
1 (1)	TXINO	O	AMP1 Output pin.
2 (2)	LPF1OUT	O	Scrambler filter output pin. Connect to TXDBMIN through an external capacitor.
3 (3)	TXDBMIN	I	Scrambler double balanced mixer input pin.
- (4)	NC	-	No connection.
4 (5)	LIMLV	I	Limiter level adjust pin. The limiter level may be adjusted by varying the DC level applied on this pin. If this pin is left open, a pre-determined level is set.
5 (6)	LIMIN	I	Limiter input pin.
6 (7)	LPF2OUT	O	Scrambler signal output pin. Connect to LIMIN through an external capacitor.
- (8)	NC	-	No connection.
7 (9)	SPOUT	O	Splatter filter output pin.
8 (10)	MODIN	I	Transmit signal input pin to be modulated (inverted input pin of AMP2). Form the smoothing filter by external capacitors and resistors.
9 (11)	MOD	O	Transmit signal output pin to be modulated. Can drive 10k ohm load or more.
10 (-)	VSS	-	Negative power supply pin.
- (12)	TAVSS	-	Negative analog power supply pin for transmitter section.
- (13)	NC	-	No connection.
- (14)	NC	-	No connection.
- (15)	DVSS	-	Negative power supply pin for digital circuit.
11 (16)	TCLK	O	Clock output pin for transmit MSK data. 2.4kHz clock is output when TDE pin is "LOW". It stays "HIGH" when TDE is "HIGH".
- (17)	TEST1	I	Test pin Left open or tie to VSS.
12 (18)	TDATA	I	Transmit MSK data input pin. Data is sampled on the rising edge of TCLK clock.
13 (19)	TDE	I	Transmit MSK signal control pin. "H" : MSK signal off (MUTE) "L" : MSK signal on
14 (20)	SCLK	I	Serial clock input pin.
15 (21)	SDATA	I	Serial data Input pin. Input 10 bits serial data to the control register (see section "Serial Interface).
- (22)	NC	-	No connection.
16 (23) 17 (24)	XOUT XIN	O I	Quartz crystal resonator pins. By connecting a 3.58MHz resonator between these pins, a reference clock is generated internally. For external clock operation, left XOUT pin open and an external clock source to XIN pin.

Pin#	Name	I/O	Function
- (25)	NC	-	No connection
18 (26)	DSTB	I	Serial data strobe input pin.
19 (27)	RSTN	I	Serial data reset input pin. The control register is initialized to the preset value when this pin is set to low level. As for the value, see section "Serial Interface".
20 (28)	RDATA	0	Receive MSK MODEM data output pin. Data is output at the falling edge of RCLK clock.
21 (29)	RCLK	0	Recovered clock output pin. A 2.4kHz clock is output which is recovered from the received MSK signal.
22 (30)	FDOUTN	0	Frame detection output pin This pin goes to low level, when detecting frame pattern.
- (31)	NC	-	No connection
- (32)	TEST2	I	Test pin Left open or tie to VSS.
23 (33)	DVDD	-	Positive power supply pin for digital section.
24 (34)	LPF3OUT	0	Descrambler low pass filter output pin. Connect to RXDBMIN through capacitor.
25 (35)	RXDBMIN	I	Receiver side double balanced mixer input.
- (36)	NC	-	No connection
- (37)	NC	-	No connection
- (38)	NC	-	No connection
26 (39)	RAVDD	-	Positive power supply pin for analog receiver section.
- (40)	NC	-	No connection
27 (41)	EXPOUT	0	Expander output pin.
28 (42)	RXAFIN	I	Received voice signal input pin. A smoothing filter is formed with external capacitors and resistors.
29 (43)	RXAF	0	Receiver voice signal output pin. Can drive 10k ohm load or more.
30 (44) 31 (45)	BUFOP BUFON	0 0	Receiver side high pass filter output pins. Connect a ceramic receiver to these pins.
32 (46)	LPF4OUT	0	De-emphasis/Descrambler output pin. Connect to EXPIN through an external capacitor.
33 (47)	EXPIN	I	Expander input pin.
- (48)	NC	-	No connection
34 (49)	RXINO	0	AMP3 output pin.
35 (50)	RXIN	I	Received de-modulated signal input pin (inverted input of AMP3). A pre-filter is formed with external capacitors and resistors.
36 (51)	RAVSS	-	Negative analog power supply for receiver section.
37 (52)	RAGND	0	Analog ground pin for receiver section. To stabilize the analog ground, connect to the ground through an external capacitor.

Pin#	Name	I/O	Function
- (53)	NC	-	No connection
38 (54)	AGNDIN	I	Analog ground input pin. To stabilize the analog ground, connect to the ground through an external capacitor.
39 (55)	BIAS	I	Bias resistor pin. A 47kΩ resistor is connected between VSS and this pin.
- (56)	NC	-	No connection
- (57)	NC	-	No connection
40 (58)	TAGND	O	Analog ground pin for transmitter section. To stabilize the analog ground, connect to the ground through an external capacitor.
- (59)	NC	-	No connection
41 (60)	COMPO	O	Compressor output pin.
42 (61)	COMPI	I	Compressor rectifier input pin. This pin should be connected to COMPO pin through an external capacitor.
43 (62)	TAVDD	-	Positive power supply pin for transmit section.
- (63)	NC	-	No connection
44 (64)	TXIN	I	Transmit voice signal input pin (inverted input pin of AMP1). A microphone amplifier is formed by external capacitors and resistors.

( ) indicate the pin# for 64 pin SQFP.

Absolute Maximum Ratings

TAVSS, RAVSS, DVSS, VSS = 0V ; (Note①)

Parameter	Symbol	Min	Max	Units
Power Supply Voltages : (TAVDD, RAVDD, DVDD)	VA+	-0.3	7	V
Input Current (Excluding power supply pins)	I_{IN}	-	±10	mA
Analog Input Voltage	V_{INA}	-0.3	(VA+)+0.3	V
Digital Input Voltage	V_{IND}	-0.3	(VA+)+0.3	V
Storage Temperature	Tstg	-55	130	℃

Notes ① : All voltages are referenced to VSS pin

Note : Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

Recommended Operating Conditions

TAVSS, RAVSS, DVSS, VSS = 0V ; (Note①)

Parameter		Symbol	Min	Typ	Max	Units
Ambient Operating Temperature		Ta	-10		70	℃
PowerSupply Voltage :R_{BIAS}= 47kΩ (TAVDD,RAVDD,DVDD)		VDD	1.9	2.0	5.5	V
Analog Ground Reference Voltage		AGND		1/2VDD		V
Power Supply Current	Mode0	Idd0		0.1	0.25	mA
	Mode1	Idd1		0.8	1.5	
	Mode2	Idd2		1.4	2.5	
	Mode3	Idd3		7.0	10	

Note① : All voltages are referenced to VSS pin.

Analog Characteristics

f=1kHz TC="1" PCONT="1" GCONT="1"

0dBm=0.775Vrms
0dBx=-5dBm @ 2V (note⑩)

1) TX Section

Parameter	min	typ	max	Units
Reference Input Signal Level @TXIN0		-10		dBx
Absolute Gain TXIN0→MOD 1kHz (Note①)	-1.5	0	1.5	dB
Limiter Level TXIN0→MOD 1kHz (Note①) without External R Adjustable Range with R	-9	-8	-7 -7	dBx
Compressor linearity TXIN0→MOD (Note①,②) TXIN0=-44dBx TXIN0=-50dBx	-20 -24	-17.0 -20.0	-14 -16	dB
Noise Level TXIN→MOD (Note①,③)			-40	dBm
Compressor distortion TXIN0→COMP0 TXIN0=0dBx			-35	dB
MSK Output Signal Level TDATA→MOD (Note①) 1.2kHz Output	-9	-8	-7	dBx
MSK Signal Distortion TDATA→MOD (Note①) 1.2kHz Output			-28	dB

2) RX Section

Parameter	min	typ	max	Units
Reference Input Signal Level @RXIN0		-10		dBx
Absolute Gain RXIN0→BUF0N,BUF0P (Note④)	-1.5	0	1.5	dB
Receive Gain RXIN0→BUF0N,BUF0P (Note⑤) GCONT="0"	5.5	6.0	6.5	dB
Expandor linearity RXIN0→BUF0N,BUF0P RXIN0=-25dBx (Note④,⑥) RXIN0=-30dBx	-33 -44	-30.0 -40.0	-27 -35	dB
Noise Level RXIN0→LPF30UT (Note③,④)			-70	dBm
Expandor distortion RXIN0→RXAF RXIN0=-5dBx			-35	dB
MSK Input Signal Level RXIN0→RDATA 1.2kHz Input	-14	-8	-2	dBx

3) General Characteristics

Parameter	min	typ	max	Units
Absolute gain TXIN0→BUF0N,BUF0P KEY="0" and "1" TXIN0=-10dBx (Note⑦,⑧)	-1.5	0	+1.5	dB
Distortion TXIN0→BUF0N,BUF0P KEY="0" and "1" TXIN0=-10dBx (Note③,⑦,⑧)		-50	-45	dB
Crosstalk @BUF0N,BUF0P (Note④,⑨) Transmit→Receive TXIN0=0dBx			-60	dBm
Crosstalk @MOD (Note④,⑨) Receive→Transmit RXIN0=0dBx			-60	dBm

4) Filter Characteristics

Parameter		min	typ	max	Units
Transmitter Over-All Response (Fig.1)	100Hz			-40	
TXIN0→MOD	300Hz	-12	-10.5	-9	
TC="0" PCONT="1"	2.5kHz	6.5	8	9.5	dB
Referenced to 0dB at 1kHz	3kHz	6.5	8	9.5	
	5kHz			-7	
Receiver Over-All Response (Fig.2)	100Hz			-4	
RXIN0→LPF40UT	250Hz		12	13.5	
PCONT="1"	300Hz	9	10.5		dB
Referenced to 0dB at 1kHz	3kHz	-10.5	-9	-7.5	
	5kHz			-15	

Note① : Including external parts, see "Application Circuit Examples".
Note② : 0dB is the Reference level at MOD.
Note③ : C-Message weighted.
Note④ : GCONT="1" Including external parts, see "Application Circuit Examples".
Note⑤ : Difference between the gain with GCONT="1" and GCONT="0".
Note⑥ : 0dB is the Reference level at BUFON and BUFOP.
Note⑦ : TC="1" PCONT="0" GCONT="1"
Note⑧ : Including external parts, see "Application Circuit Examples".
AMP3 gain is 0dB and MOD pin connected to DEM.
Note⑨ : TC="0" PCONT="0" GCONT="1"
Note⑩ : Definition of "dBx"

$$0dBx = -5 + 20\log(X/2)\ [dBm]$$

where, X: Power Supply Voltage [V]
Example: 0dBx = -5dBm @2V

☐ Filter Characteristics

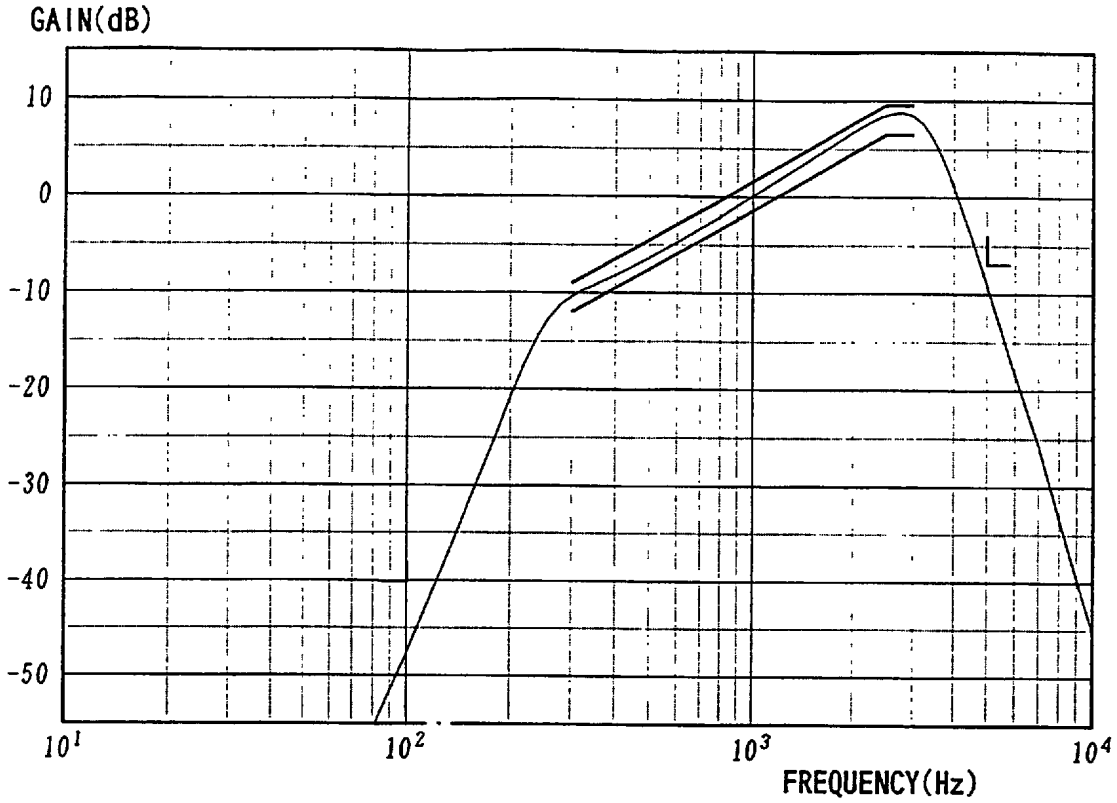


Fig.1 Total Frequency Response of Transmitter Section

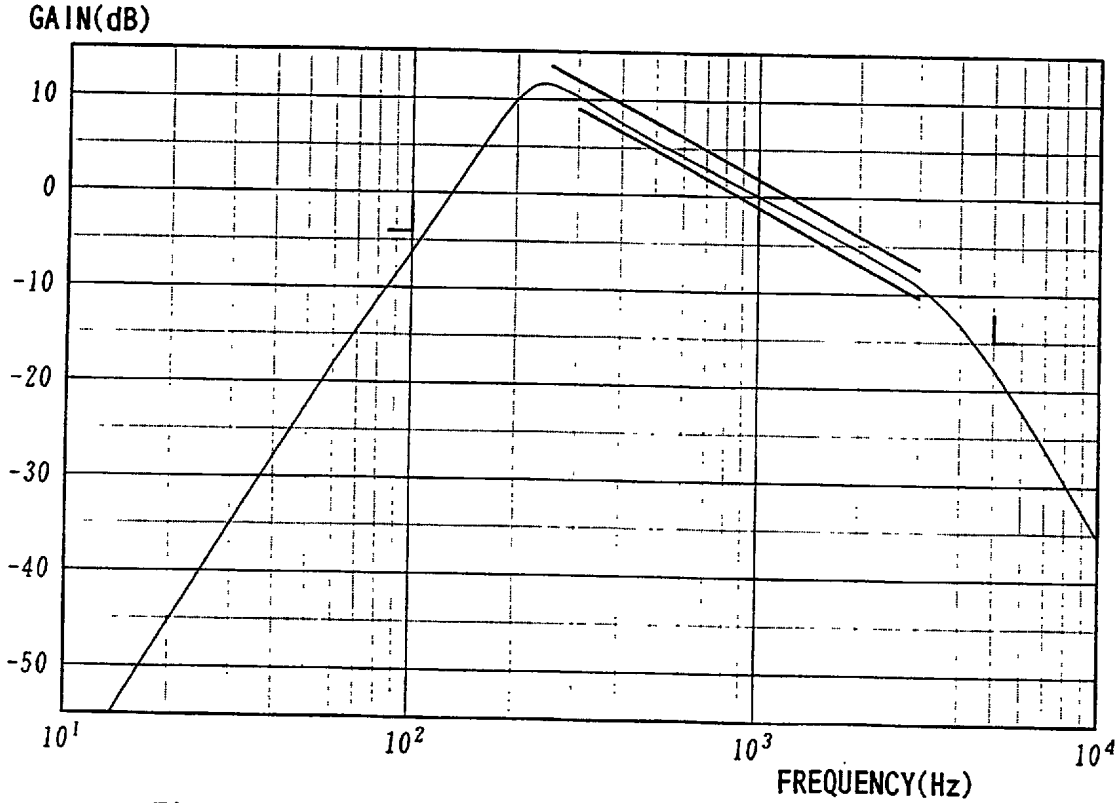
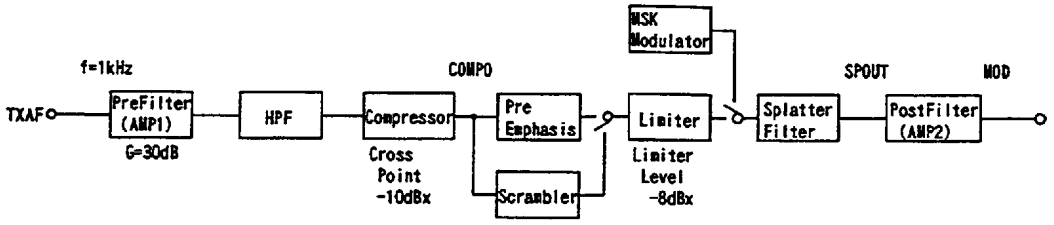
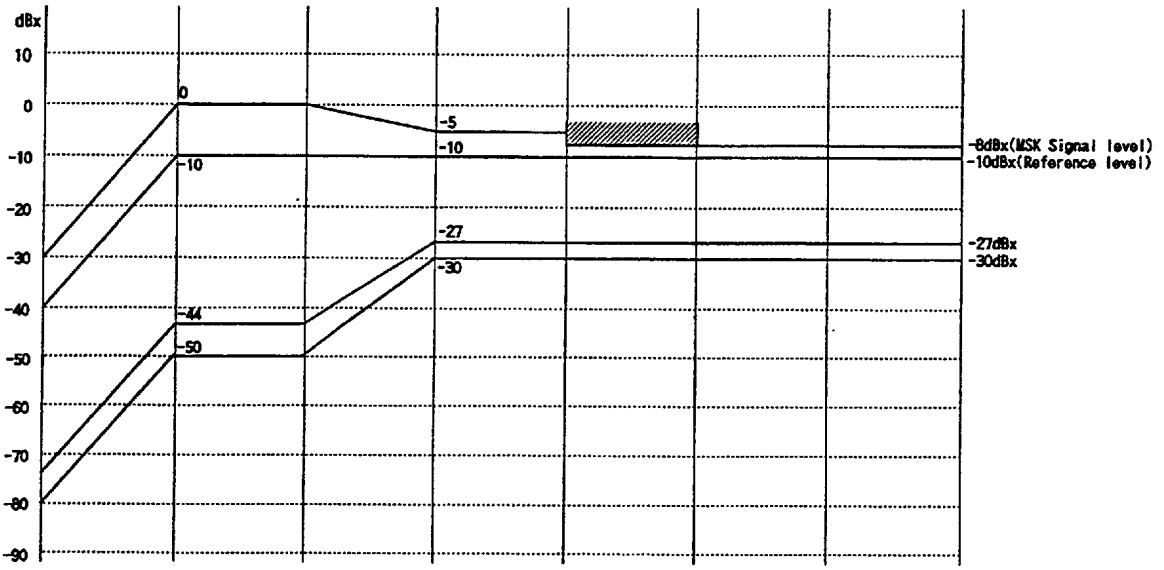


Fig.2 Total Frequency Response of Receiver Section

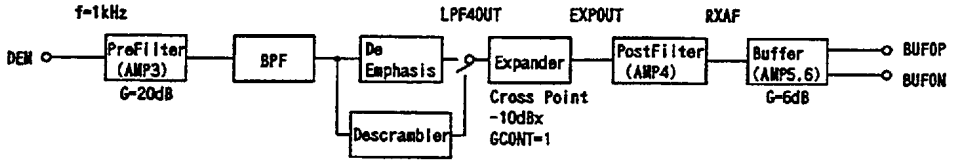
Level Diagram

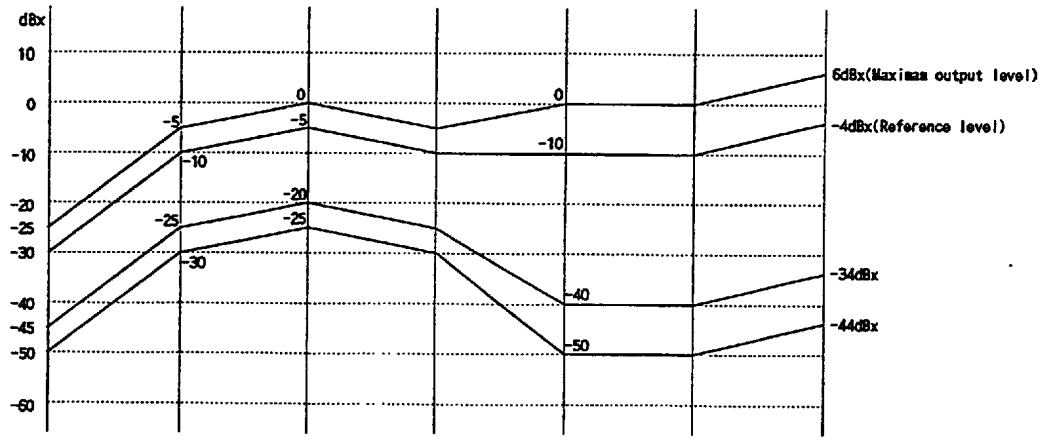
1) TX Section





2) RX Section





Note : Definition of "dBx"

0dBx = -5 + 20log(X/2) [dBm]

where, X: Power Supply Voltage [V]

Example: 0dBx = -5dBm @2V

Digital Characteristics

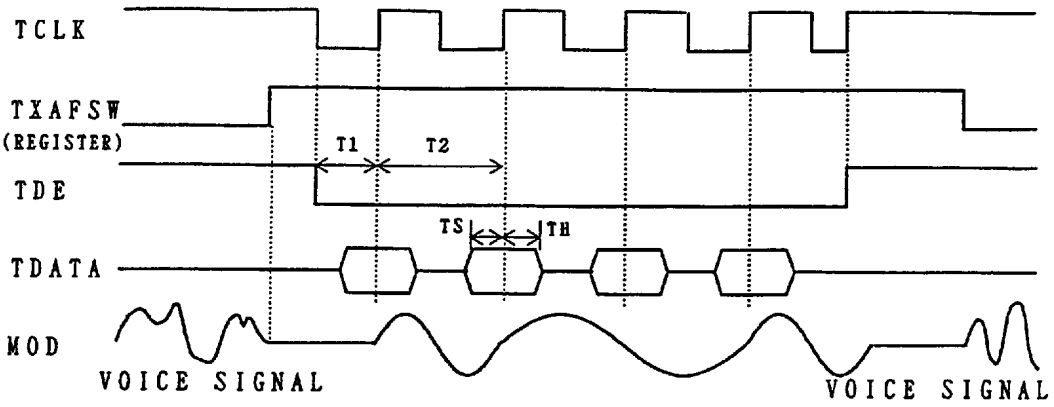
1. DC Characteristics

Parameter	Pin	Symbol	Min	Typ	Max	Units
High Level Input Voltage	(1)	V_{IH}	70%VDD			V
Low Level Input Voltage	(1)	V_{IL}			30%VDD	V
High Level Input Current V_{IH}=VDD	(1)	I_{IH}			10	μA
Low Level Input Current V_{IL}=0V	(1)	I_{IL}	-10			μA
High Level Output Voltage I_{OH}=-0.1mA	(2)	V_{OH}	90%VDD			V
Low Level Output Voltage I_{OL}=0.6mA	(2)	V_{OL}			0.3	V

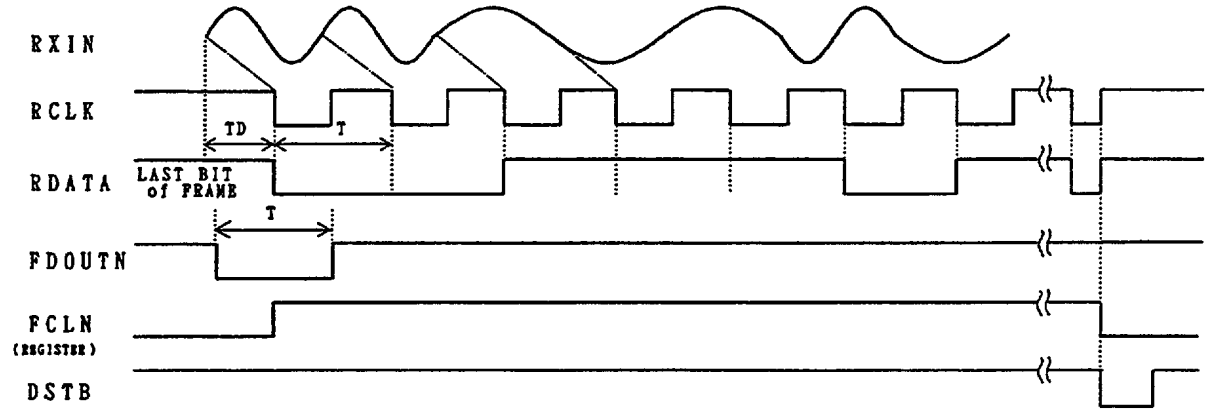
(1) TDE, TDATA, RSTN, DSTB, SDATA, SCLK
(2) TCLK, RDATA, RCLK, FDOUTN

2. Switching Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Master Clock Frequency	fclk		3.579545		MHz
MSK Modulator Timing					
TDE Falling to TCLK Rising	T1		208.3		μs
TCLK Period	T2		416.7		μs
TDATA Set Up Time	TS	1			μs
TDATA Hold Time	TH	1			μs
MSK Demodulator Timing					
RCLK Period & FDOUTN pulse width	T	402.2	416.7		μs
Analog Input to RDATA Edge	TD	400		900	μs
Serial Data Input Timing					
Clock Pulse Width 1	ta	500			ns
Clock Pulse Width 2	tb	500			ns
SDATA Set Up Time	tc	100			ns
SDATA Hold Time	td	100			ns
STROBE Set Up Time	te	100			ns
STROBE Pulse Width	tf	100			ns
STROBE Dehold Time	tg	100			ns
RESET Pulse Width	th	100			ns
RESET Cancel Time	ti	500			ns
Digital Input Rising Time	tj			100	ns
Digital Input Falling Time	tk			100	ns

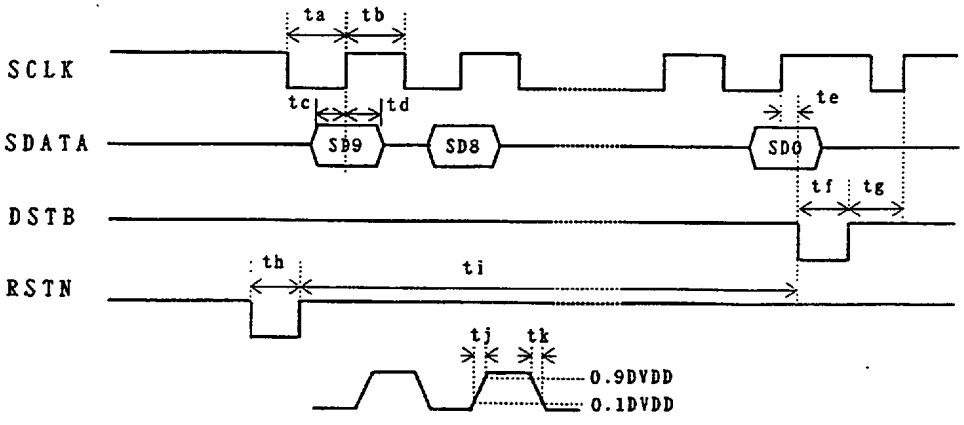


MSK Modulator



- RDATA and RCLK remain "H" untill the synchronous frame is detected.
- FDUTN remains "L" and FCLN "H" during "T" period after the synchronous frame is detected.
- RDATA and RCLK output normal data after the synchronous frame is detected.
- The synchronous frame detector halts when FCLN is set "H".
- When FCLN is set "L", RDATA and RCLK go "H" and wait for next synchronous frame.

MSK Demodulator



Serial Data Input

Serial Interface

AK2353B is controlled by setting the control register through serial interface. The function of control register is described below.

■ Control Register

	SD0	SD1	SD2	SD3	SD4
Functions	GCONT	RXAFSW	TC	PCONT	TXAFSW
After Reset	1	0	1	1	0

	SD5	SD6	SD7	SD8	SD9
Functions	BS1	BS2	KEY	FRPT	FCLN
After Reset	0	1	1	0	0

Note: Reset when RSTN = "L"
Data format to the serial interface is SD9 first

1) Expander Gain Setting

GCONT	Expander Gain
1	0 [dB]
0	6 [dB]

2) Mute

TXAFSW	TDE	RXAFSW	MOD	RXAF
0	1	-	Voice	-
1	1	-	Mute	-
1	0	-	MSK Signal	-
-	-	0	-	Voice
-	-	1	-	Mute

Note: TDE is an input pin instead of the register

3) Compressor ON/OFF

TC	Compressor
1	ON
0	OFF

4) Scrambler ON/OFF

PCONT	Scrambler/Emphasis
1	Pre-emphasis & De-emphasis
0	Scrambler

5) Power Down Mode

BS1	BS2	Mode	Voice Pass & Transmit MODEM	Receive MODEM	Oscillator
1	1	Mode0	OFF	OFF	OFF
1	0	Mode1	OFF	OFF	ON
0	1	Mode2	OFF	ON	ON
0	0	Mode3	ON	ON	ON

6) Scrambler Carrier Frequency

KEY	Carrier Frequency
1	3.107 [kHz]
0	3.290 [kHz]

7) Frame Pattern

FRPT	Pattern	Base/Hand
1	1100010011010110	Base Set
0	1001001100110110	Hand Set

8) RCLK & RDATA Output

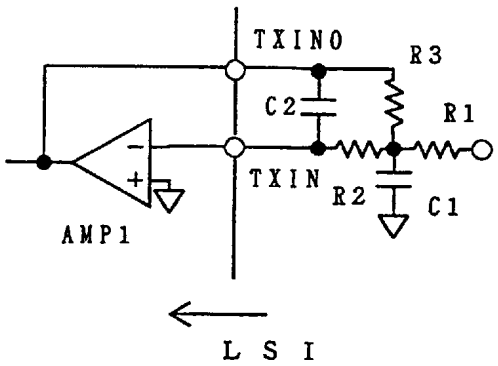
FCLK	RCLK & RDATA Output
1	Enable
0	Disable

Application Circuit Examples

External circuit examples

① AMP1

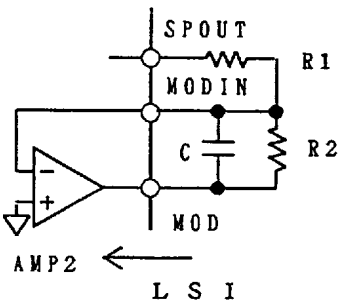
- AMP1 may be used as a transmit Mic Amp.
- Adjust the gain to 30dB or less.
- If 100kHz or higher frequency noise is expected on input signal, an anti-aliasing filter must be configured.
- A circuit configuration example below shows a 2nd order low pass filter with the cut-off frequency at 10kHz. The filter also has 30dB gain.



C1=2200pF
C2=33pF
R1=R2=10k Ω
R3=330k Ω

② AMP2

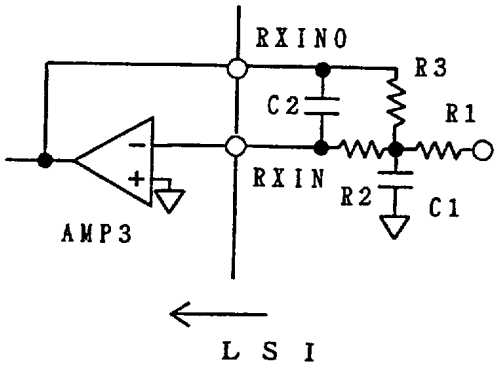
- AMP2 may be used as a smoothing filter and gain adjustment of the transmit signal.
- Smoothing filter is used to eliminate a 112kHz clock component contained in the splatter filter output.
- Another transmit signal may also be added using this OP-amp.
- The circuit example below shows a 1st order low pass filter with 13kHz cut-off frequency and 0dB gain.



C=220pF
R1=R2=56k Ω

③ AMP3

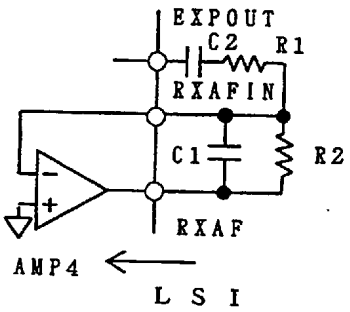
- AMP3 may be used as gain adjustment of receive signal and an anti-aliasing filter to eliminate 100kHz or higher noise.
- Adjust the gain to be 30dB or less.
- Following circuit shows a 2nd order low pass filter with 40kHz cut-off frequency and 20dB gain.



C1=560pF
C2=27pF
R1=10k Ω
R2=9.1k Ω
R3=100k Ω

④ AMP4

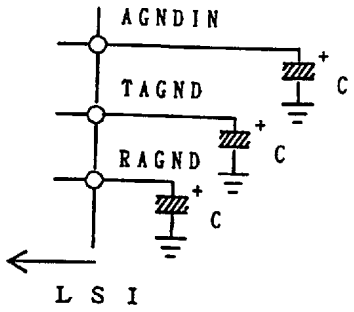
- AMP4 may configure a smoothing filter and a gain adjustment circuit for the receive signal.
- The smoothing filter is used to reject 448kHz clock component contained in the expander output (EXPOUT).
- Following circuit example shows a 1st order low pass filter with 19kHz cut-off frequency and 0dB gain.



C1=150pF
C2=0.022 μF
R1=R2=56k Ω

⑤ AGND stabilization capacitor

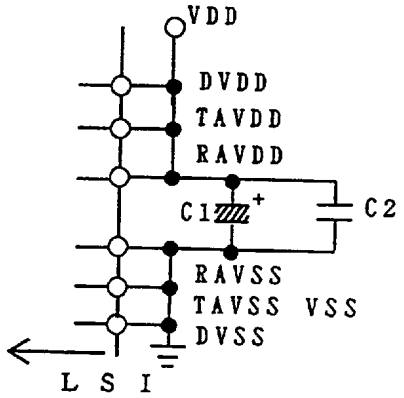
- 0.3 μF or larger capacitors should be connected between TAGND pin and AVSS, RAGND pin and AVSS respectively in order to stabilize analog ground.
- In order to minimize effect of ripple on power-supply, an appropriate capacitor is also recommended to place between AGNDIN pin and AVSS.
- Connection Example is shown below.



C=1 μF

⑥ Power supply stabilization capacitor

- To minimize the effect of power supply noise, a couple of capacitors should be placed between DVDD, TAVDD, RAVDD pins and DVSS, TAVSS, RAVSS pins.

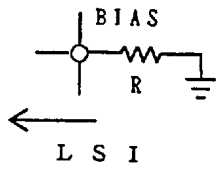


C1=22 μF(Electrolytic)

C2=0.1 μF(Ceramic)

⑦ Bias-current setting resistor

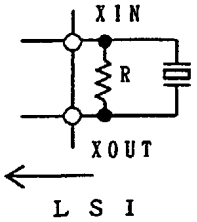
- Bias-current of Op Amp is set by connecting a 47kΩ resistor between Bias pin and VSS.



R= 47k Ω

⑧ Crystal Oscillator

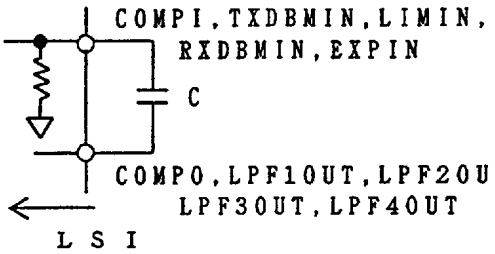
- Crystal resonator and a resistor should be connected as shown below for on-chip oscillator operation.
- For external clock operation, left XOUT open and tie an external clock to XIN.



Frequency: 3.58MHz
or 3.579545MHz
R=1M Ω

⑨ AC Coupling Capacitors

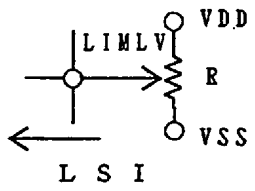
-In order to cut the DC off-set voltages generated in each function block, AC coupling capacitors are recommended for inter-block connections.



C=0.033 μF
(RXDBMIN-LPF3OUT C=0.068 μF
TXDBMIN-LPF4OUT)

⑩ Limiter Level Adjusting Resistor

- Limiter level may be adjusted by varying the DC level on LIMLV pin. The DC level applied on this pin must be above TAGND voltage.
- The limit level is as follows :
  TAGND ± a [V] (a= | LIMLV-TAGND |)
- If this pin is left open, a pre-determined level is set.



R=50k Ω

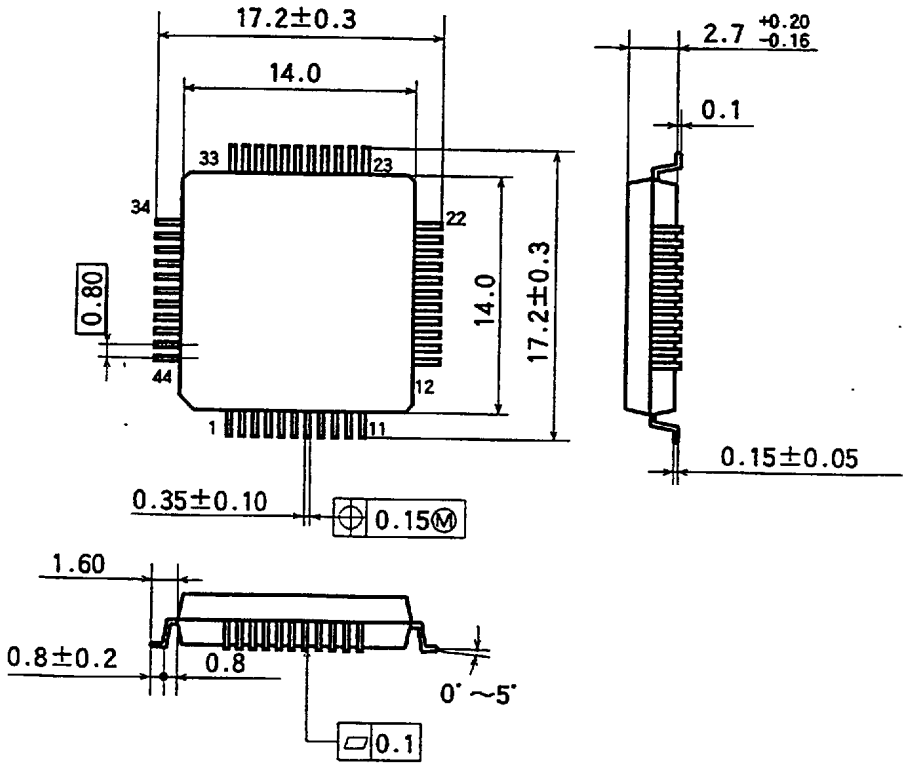
Package

☐ 44 pin QFP

■ Marking

(1) Pin # 1 indication
(2) Date Code : 7 Digits
(3) Marketing Code : AK2353B
(4) Country of Origin
(5) Asahi Kasei Logo

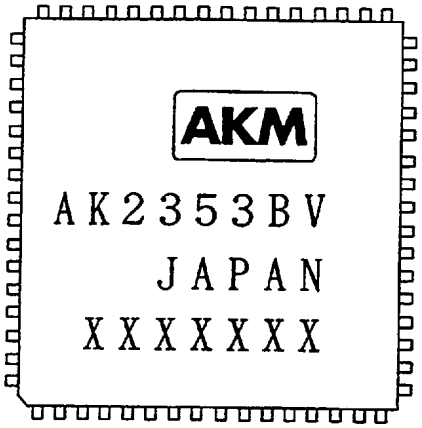
■ Outline Dimensions



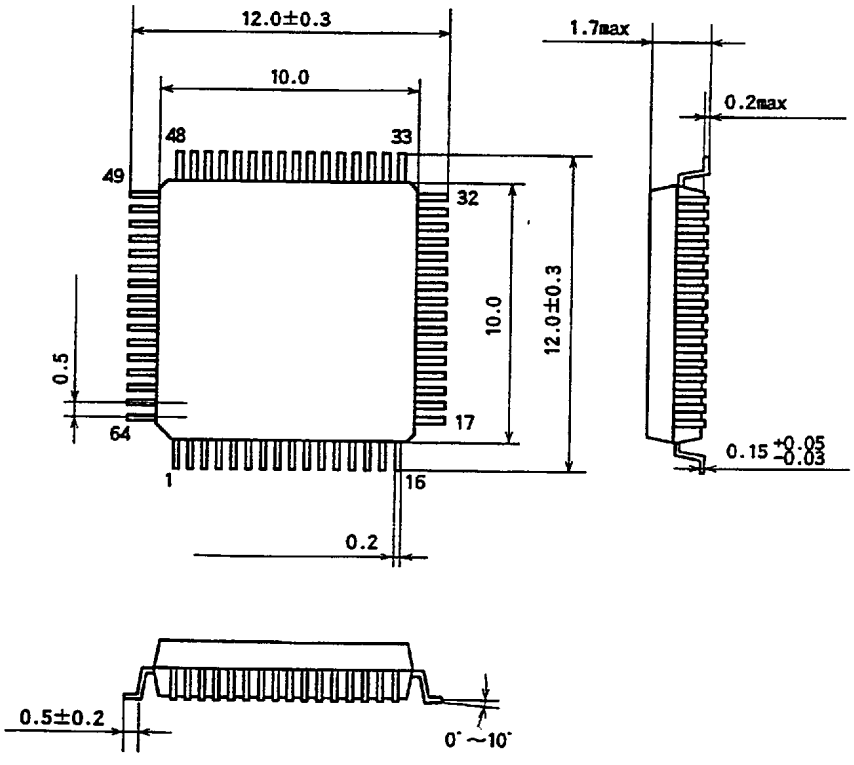
☐ 64 pin SQFP

■ Marking

(1) Pin # 1 indication
(2) Date Code : 7 Digits
(3) Marketing Code : AK2353BV
(4) Country of Origin
(5) Asahi Kasei Logo



■ Outline Dimensions



※ Specifications are subject to change without notice.
※ Operations beyond the specifications are not guaranteed.