



512Kx32 SRAM 3.3V MODULE

PRELIMINARY*

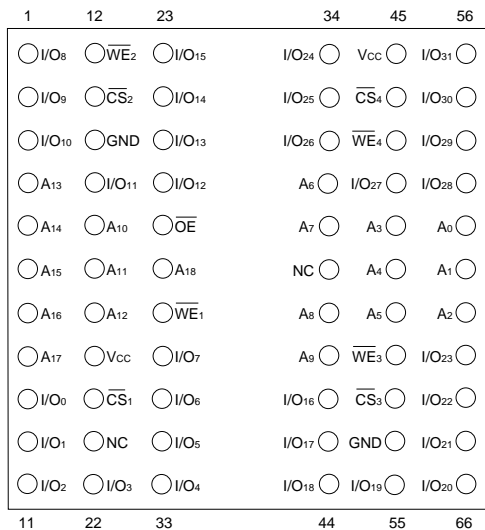
FEATURES

- Access Times of 15, 17, 20ns
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.075 inch square, Hermetic Ceramic HIP (Package 400)
 - 68 lead, 22.4mm (0.88") CQFP, 4.6mm (0.180") high, (Package 509)
 - 68 lead, 23.9mm (0.940" sq.) Low Profile CQFP (G1U), 3.56mm (0.140") high, (Package 519)
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Commercial, Industrial and Military Temperature Ranges
- Low Voltage Operation:
 - 3.3V ± 10% Power Supply
- Low Power CMOS
- TTL Compatible Inputs and Outputs
- Fully Static Operation:
 - No clock or refresh required.
- Three State Output.
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32V-XG2TX - 8 grams typical
 - WS512K32V-XG1UX - 5 grams typical
 - WS512K32NV-XH1X - 13 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

PIN CONFIGURATION FOR WS512K32NV-XH1X

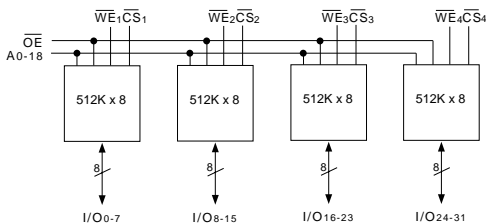
TOP VIEW



PIN DESCRIPTION

| | |
|---------------------|---------------------|
| I/O ₀₋₃₁ | Data Inputs/Outputs |
| A ₀₋₁₈ | Address Inputs |
| \overline{WE}_1-4 | Write Enables |
| \overline{CS}_1-4 | Chip Selects |
| \overline{OE} | Output Enable |
| V _{CC} | Power Supply |
| GND | Ground |
| NC | Not Connected |

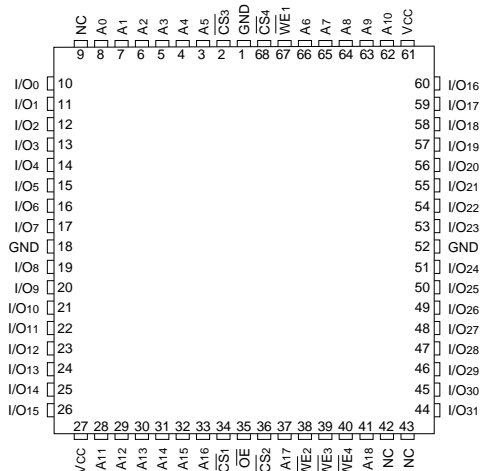
BLOCK DIAGRAM





PIN CONFIGURATION FOR WS512K32V-XG2TX AND WS512K32V-XG1UX

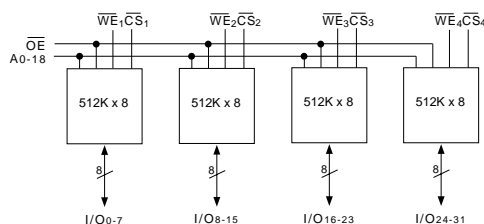
TOP VIEW



PIN DESCRIPTION

| | |
|--------------------|---------------------|
| I/O0-31 | Data Inputs/Outputs |
| A0-18 | Address Inputs |
| $\overline{WE}1-4$ | Write Enables |
| $\overline{CS}1-4$ | Chip Selects |
| \overline{OE} | Output Enable |
| Vcc | Power Supply |
| GND | Ground |
| NC | Not Connected |

BLOCK DIAGRAM





ABSOLUTE MAXIMUM RATINGS

| Parameter | Symbol | Min | Max | Unit |
|--------------------------------|------------------|------|------|------|
| Operating Temperature | T _A | -55 | +125 | °C |
| Storage Temperature | T _{STG} | -65 | +150 | °C |
| Signal Voltage Relative to GND | V _G | -0.5 | 4.6 | V |
| Junction Temperature | T _J | | 150 | °C |
| Supply Voltage | V _{CC} | -0.5 | 4.6 | V |

RECOMMENDED OPERATING CONDITIONS

| Parameter | Symbol | Min | Max | Unit |
|--------------------|-----------------|------|-----------------------|------|
| Supply Voltage | V _{CC} | 3.0 | 3.6 | V |
| Input High Voltage | V _{IH} | 2.2 | V _{CC} + 0.3 | V |
| Input Low Voltage | V _{IL} | -0.3 | +0.8 | V |

TRUTH TABLE

| \overline{CS} | \overline{OE} | \overline{WE} | Mode | Data I/O | Power |
|-----------------|-----------------|-----------------|-------------|----------|---------|
| H | X | X | Standby | High Z | Standby |
| L | L | H | Read | Data Out | Active |
| L | X | L | Write | Data In | Active |
| L | H | H | Out Disable | High Z | Active |

CAPACITANCE

(T_A = +25°C)

| Parameter | Symbol | Conditions | Max | Unit |
|--|------------------|-------------------------------------|-----|------|
| \overline{OE} capacitance | C _{OE} | V _{IN} = 0 V, f = 1.0 MHz | 50 | pF |
| \overline{WE}_{1-4} capacitance HIP (PGA) | C _{WE} | V _{IN} = 0 V, f = 1.0 MHz | 20 | pF |
| CQFP G2T/G1U | | | 20 | |
| \overline{CS}_{1-4} capacitance | C _{CS} | V _{IN} = 0 V, f = 1.0 MHz | 20 | pF |
| Data I/O capacitance | C _{I/O} | V _{I/O} = 0 V, f = 1.0 MHz | 20 | pF |
| Address input capacitance | C _{AD} | V _{IN} = 0 V, f = 1.0 MHz | 50 | pF |

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS

(V_{CC} = 3.3V ± 0.3V, T_A = -55°C to +125°C)

| Parameter | Sym | Conditions | | | Units |
|--------------------------------------|----------------------|---|-----|-----|-------|
| | | | Min | Max | |
| Input Leakage Current | I _{LI} | V _{IN} = GND to V _{CC} | | 10 | μA |
| Output Leakage Current | I _{LO} | \overline{CS} = V _{IH} , \overline{OE} = V _{IH} , V _{OUT} = GND to V _{CC} | | 10 | μA |
| Operating Supply Current (x 32 Mode) | I _{CC} x 32 | \overline{CS} = V _{IL} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 3.6V | | 400 | mA |
| Standby Current | I _{SB} | \overline{CS} = V _{IH} , \overline{OE} = V _{IH} , f = 5MHz, V _{CC} = 3.6V | | 200 | mA |
| Output Low Voltage | V _{OL} | I _{OL} = 4.0mA | | 0.4 | V |
| Output High Voltage | V _{OH} | I _{OH} = -4.0mA | 2.4 | | V |

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V.

NOTE: Contact factory for low power option.



AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = -55°C to +125°C)

| Parameter | Symbol | -15 | | -17 | | -20 | | Units |
|------------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Read Cycle | | | | | | | | |
| Read Cycle Time | t _{RC} | 15 | | 17 | | 20 | | ns |
| Address Access Time | t _{AA} | | 15 | | 17 | | 20 | ns |
| Output Hold from Address Change | t _{OH} | 0 | | 0 | | 0 | | ns |
| Chip Select Access Time | t _{ACS} | | 15 | | 17 | | 20 | ns |
| Output Enable to Output Valid | t _{OE} | | 8 | | 8 | | 10 | ns |
| Chip Select to Output in Low Z | t _{CLZ'} | 1 | | 1 | | 1 | | ns |
| Output Enable to Output in Low Z | t _{OLZ'} | 0 | | 0 | | 0 | | ns |
| Chip Disable to Output in High Z | t _{CHZ'} | | 8 | | 8 | | 10 | ns |
| Output Disable to Output in High Z | t _{OHZ'} | | 8 | | 8 | | 10 | ns |

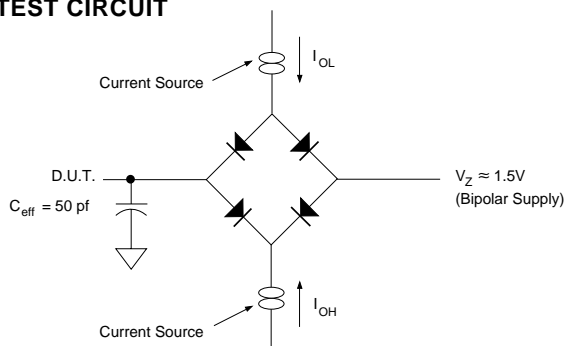
1. This parameter is guaranteed by design but not tested.

AC CHARACTERISTICS
(V_{CC} = 3.3V, T_A = -55°C to +125°C)

| Parameter | Symbol | -15 | | -17 | | -20 | | Units |
|----------------------------------|-------------------|-----|-----|-----|-----|-----|-----|-------|
| | | Min | Max | Min | Max | Min | Max | |
| Write Cycle | | | | | | | | |
| Write Cycle Time | t _{WC} | 15 | | 17 | | 20 | | ns |
| Chip Select to End of Write | t _{CW} | 12 | | 12 | | 14 | | ns |
| Address Valid to End of Write | t _{AW} | 12 | | 12 | | 14 | | ns |
| Data Valid to End of Write | t _{DW} | 9 | | 9 | | 10 | | ns |
| Write Pulse Width | t _{WP} | 12 | | 14 | | 14 | | ns |
| Address Setup Time | t _{AS} | 0 | | 0 | | 0 | | ns |
| Address Hold Time | t _{AH} | 0 | | 0 | | 0 | | ns |
| Output Active from End of Write | t _{OW'} | 2 | | 3 | | 3 | | ns |
| Write Enable to Output in High Z | t _{WHZ'} | | 8 | | 8 | | 9 | ns |
| Data Hold Time | t _{DH} | 0 | | 0 | | 0 | | ns |

1. This parameter is guaranteed by design but not tested.

AC TEST CIRCUIT



AC TEST CONDITIONS

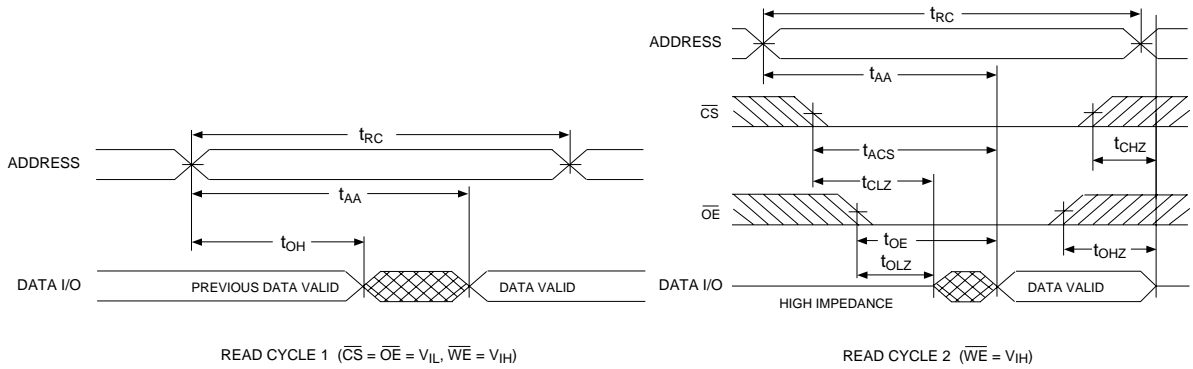
| Parameter | Typ | Unit |
|----------------------------------|--|------|
| Input Pulse Levels | V _{IL} = 0, V _{IH} = 2.5 | V |
| Input Rise and Fall | 5 | ns |
| Input and Output Reference Level | 1.5 | V |
| Output Timing Reference Level | 1.5 | V |

NOTES:

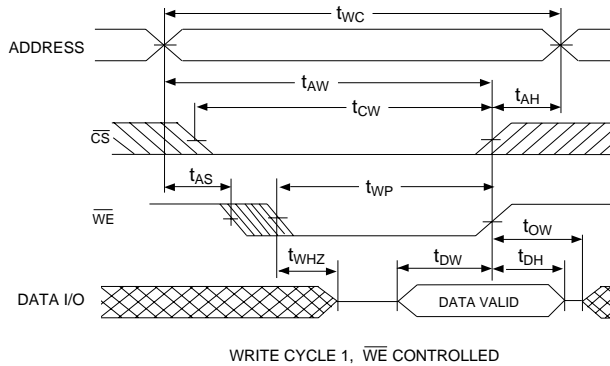
V_Z is programmable from -2V to +7V.
 I_{OL} & I_{OH} programmable from 0 to 16mA.
 Tester Impedance Z₀ = 75 Ω.
 V_Z is typically the midpoint of V_{OH} and V_{OL}.
 I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.
 ATE tester includes jig capacitance.



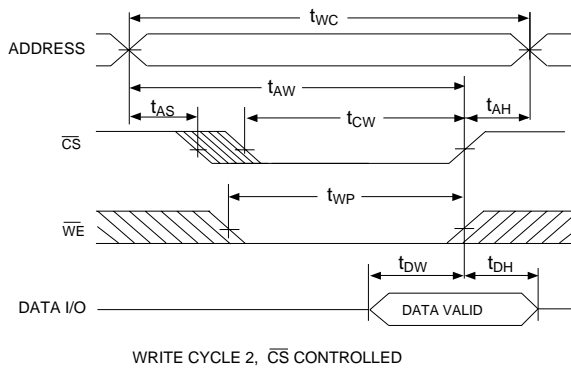
TIMING WAVEFORM - READ CYCLE



WRITE CYCLE - \overline{WE} CONTROLLED

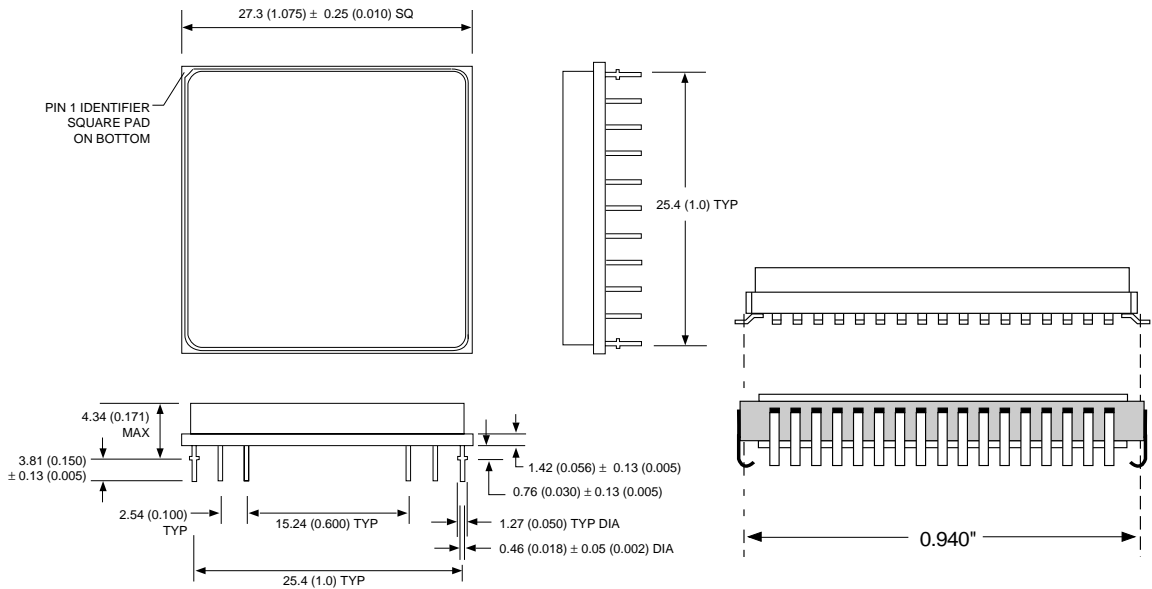


WRITE CYCLE - \overline{CS} CONTROLLED





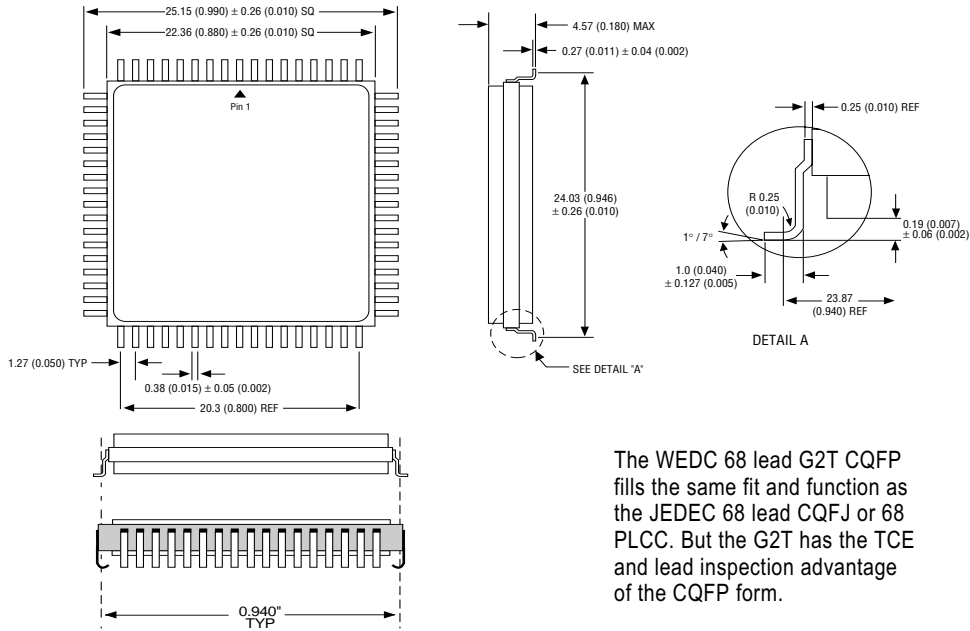
PACKAGE 400: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H1)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



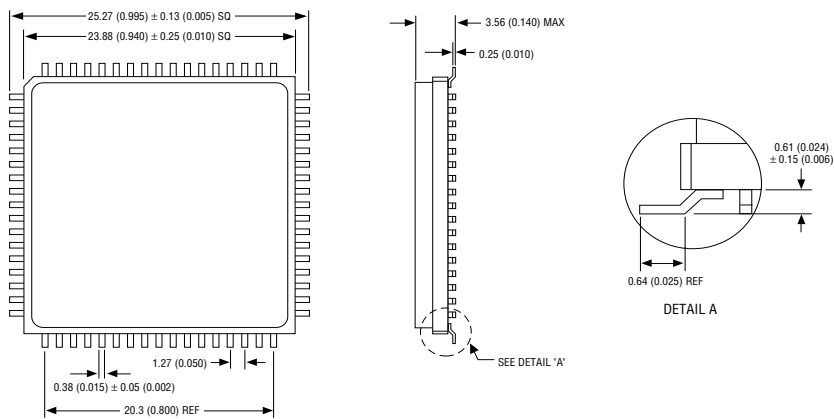
PACKAGE 509: 68 LEAD, LOW PROFILE CERAMIC QUAD FLAT PACK, CQFP (G2T)



The WEDC 68 lead G2T CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2T has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

PACKAGE 519: 68 LEAD, CERAMIC QUAD FLAT PACK, LOW PROFILE CQFP (G1U)



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES



ORDERING INFORMATION

W S 512K 32 X V - XXX X X X

LEAD FINISH:

Blank = Gold plated leads

A = Solder dip leads

DEVICE GRADE:

M = Military -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H1 = 1.075" sq. Ceramic Hex In Line Package, HIP (Package 400)

G2T = 22.4mm CQFP (Package 509)

G1U = 23.9mm Low Profile CQFP (Package 519)

ACCESS TIME (ns)

Low Voltage Supply 3.3V ± 10%

IMPROVEMENT MARK:

N = No Connect at pin 21 and 39 in HIP for Upgrades

ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

SRAM

WHITE ELECTRONIC DESIGNS CORP.