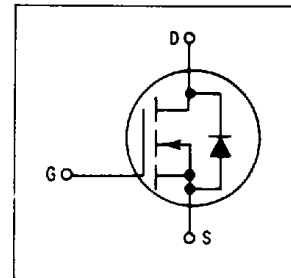


MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA
Designer's Data Sheet
Power Field Effect Transistor
N-Channel Enhancement
Mode Silicon Gate

This TMOS Power FET is designed for high voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS} , $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads


MTP10N25
TMOS POWER FET
10 AMPERES
 $R_{DS(on)} = 0.45 \text{ OHM}$
250 VOLTS


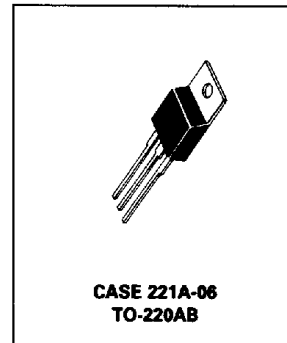
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MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	250	Vdc
Drain-Gate Voltage ($R_{GS} = 1 \text{ M}\Omega$)	V_{DGR}	250	Vdc
Gate-Source Voltage — Continuous	V_{GS}	± 20	Vdc
— Non-repetitive ($t_p \leq 50 \mu\text{s}$)	V_{GSM}	± 40	Vpk
Drain Current — Continuous	I_D	10	Adc
— Pulsed	I_{DM}	30	
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	P_D	100	Watts
Derate above 25°C		0.8	W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	-65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance			°C/W
Junction to Case	$R_{\theta JC}$	1.25	
Junction to Ambient	$R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering	T_L	260	°C
Purposes, 1/8" from case for 5 seconds			



Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
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OFF CHARACTERISTICS

Drain-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	$V_{(BR)DSS}$	250	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = \text{Rated } V_{DSS}, V_{GS} = 0$) ($V_{DS} = 0.8 \text{ Rated } V_{DSS}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	—	0.2 1	mAdc
Gate-Body Leakage Current, Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSR}	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 1 \text{ mA}$) $T_J = 100^\circ\text{C}$	$V_{GS(th)}$	2 1.5	4.5 4	Vdc
Static Drain-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 5 \text{ Adc}$)	$R_{DS(on)}$	—	0.45	Ohm
Drain-Source On-Voltage ($V_{GS} = 10 \text{ V}$) ($I_D = 10 \text{ Adc}$) ($I_D = 5 \text{ Adc}, T_J = 100^\circ\text{C}$)	$V_{DS(on)}$	—	5.6 4.5	Vdc
Forward Transconductance ($V_{DS} = 15 \text{ V}, I_D = 5 \text{ A}$)	g_{FS}	3.5	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	($V_{DS} = 25 \text{ V}, V_{GS} = 0,$ $f = 1 \text{ MHz}$) See Figure 11	C_{iss}	—	1500	pF
Output Capacitance		C_{oss}	—	400	
Reverse Transfer Capacitance		C_{rss}	—	100	

SWITCHING CHARACTERISTICS* ($T_J = 100^\circ\text{C}$)

Turn-On Delay Time	($V_{DD} = 25 \text{ V}, I_D = 0.5 \text{ Rated } I_D$ $R_{gen} = 50 \text{ ohms}$) See Figures 9, 13 and 14	$t_{d(on)}$	—	50	ns
Rise Time		t_r	—	250	
Turn-Off Delay Time		$t_{d(off)}$	—	100	
Fall Time		t_f	—	120	
Total Gate Charge	($V_{DS} = 0.8 \text{ Rated } V_{DSS},$ $I_D = \text{Rated } I_D, V_{GS} = 10 \text{ V}$) See Figure 12	Q_g	37 (Typ)	60	nC
Gate-Source Charge		Q_{gs}	21 (Typ)	—	
Gate-Drain Charge		Q_{gd}	16 (Typ)	—	

SOURCE DRAIN DIODE CHARACTERISTICS*

Forward On-Voltage	($I_S = \text{Rated } I_D$ $V_{GS} = 0$)	V_{SD}	1.6 (Typ)	2.5	Vdc
Forward Turn-On Time		t_{on}	Limited by stray inductance		
Reverse Recovery Time		t_{rr}	300 (Typ)	—	ns

INTERNAL PACKAGE INDUCTANCE (TO-220)

Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_d	3.5 (Typ) 4.5 (Typ)	—	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad.)	L_s	7.5 (Typ)	—	nH

*Pulse Test. Pulse Width $\leq 300 \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL ELECTRICAL CHARACTERISTICS

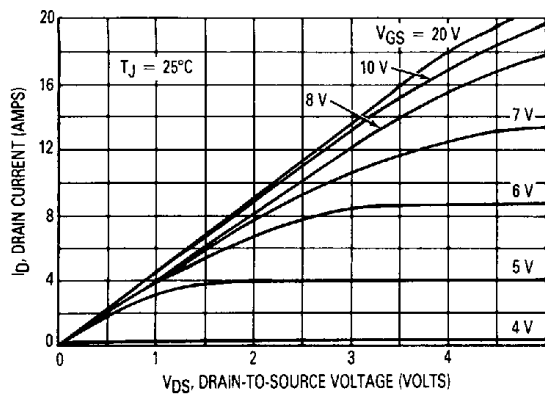


Figure 1. On-Region Characteristics

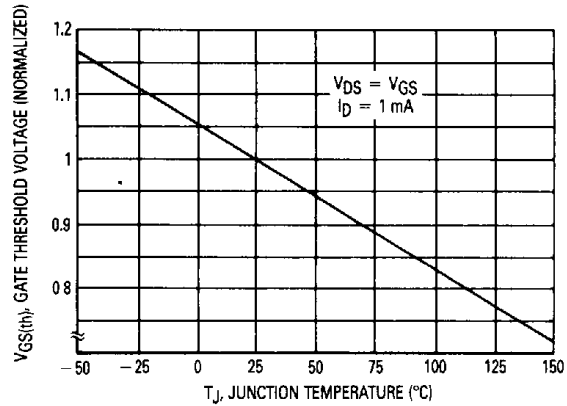


Figure 2. Gate-Threshold Voltage Variation With Temperature

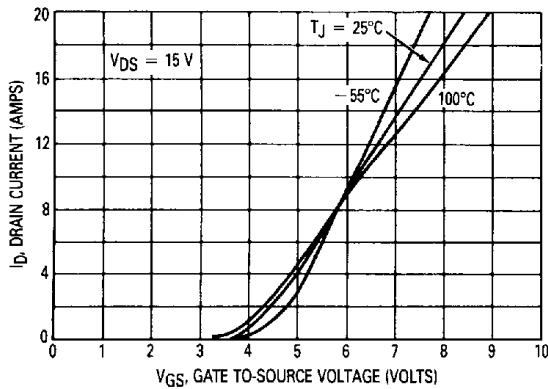


Figure 3. Transfer Characteristics

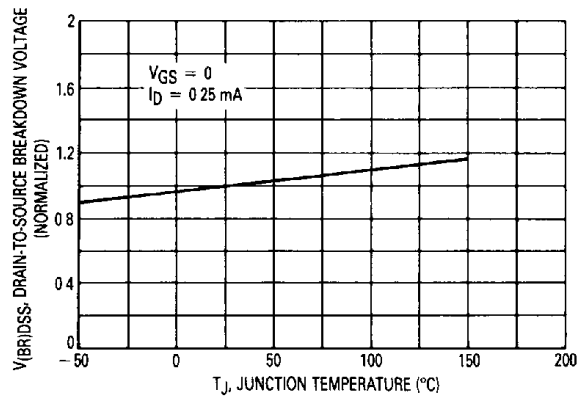


Figure 4. Breakdown Voltage Variation With Temperature

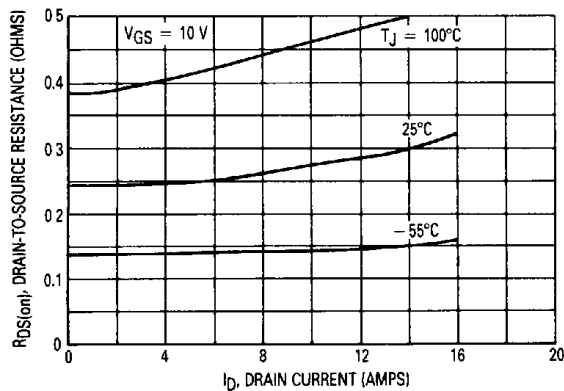


Figure 5. On-Resistance versus Drain Current

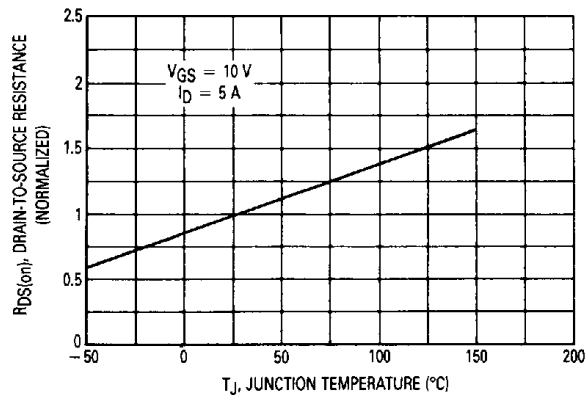


Figure 6. On-Resistance Variation With Temperature

SAFE OPERATING AREA INFORMATION

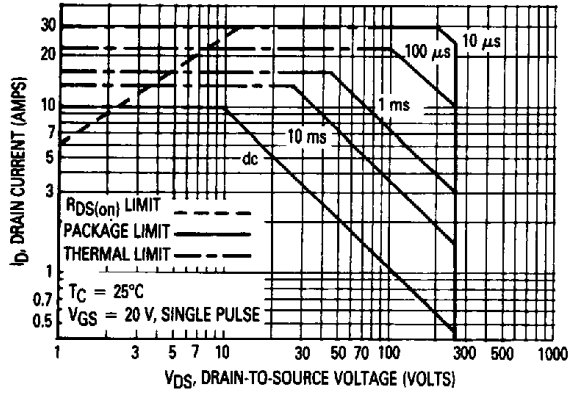


Figure 7. Maximum Rated Forward Biased Safe Operating Area

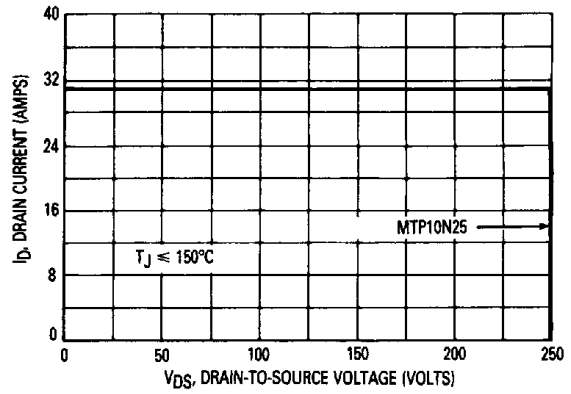


Figure 8. Maximum Rated Switching Safe Operating Area

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FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

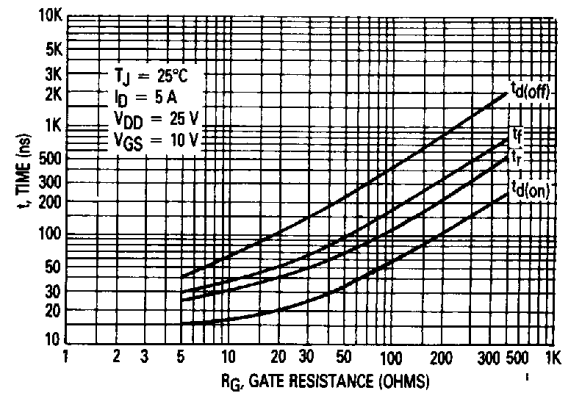


Figure 9. Resistive Switching Time versus Gate Resistance

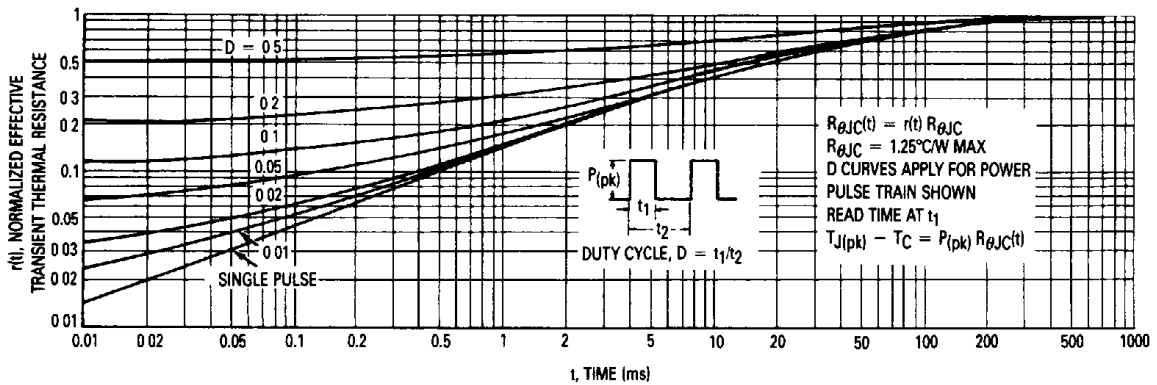


Figure 10. Thermal Response

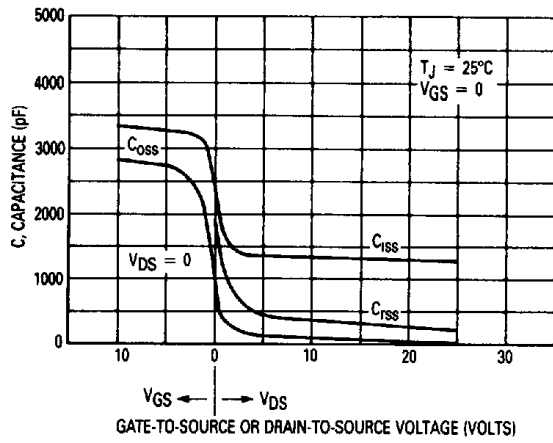


Figure 11. Capacitance Variation

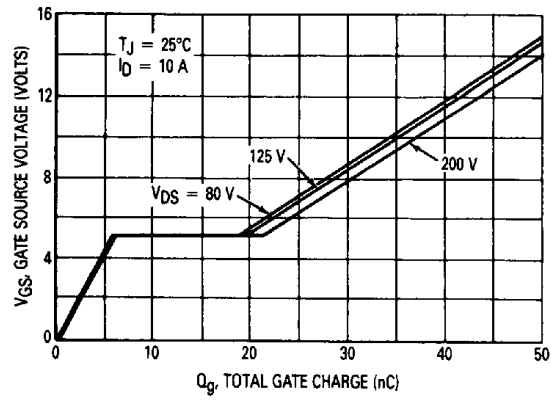


Figure 12. Gate Charge versus Gate-To-Source Voltage

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RESISTIVE SWITCHING

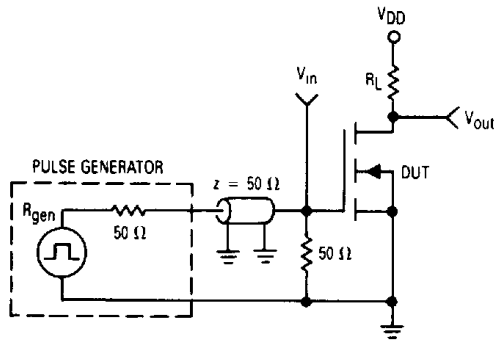


Figure 13. Switching Test Circuit

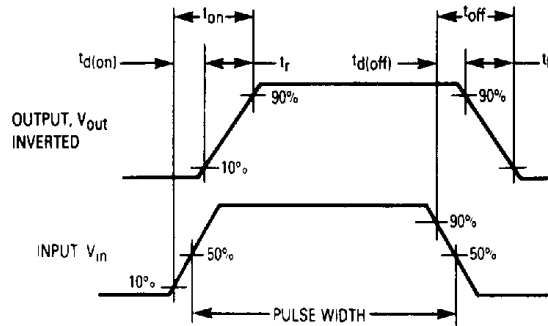


Figure 14. Switching Waveforms