

# CA555, CA555C, LM555, LM555C, NE555

Timers for Timing Delays and Oscillator Application in Commercial, Industrial and Military Equipment

May 1997

#### Features

- Accurate Timing From Microseconds Through Hours
- Astable and Monostable Operation
- · Adjustable Duty Cycle
- Output Capable of Sourcing or Sinking up to 200mA
- Output Capable of Driving TTL Devices
- Normally ON and OFF Outputs
- High Temperature Stability . . . . . . . . 0.005%/°C
- Directly Interchangeable with SE555, NE555, MC1555, and MC1455

## **Applications**

- Precision Timing
- Pulse Generation
- Sequential Timing
- Pulse Detector
- Time Delay Generation
- Pulse Width and Position Modulation

## Ordering Information

PART NUMBER (BRAND)	TEMP. RANGE ( <sup>O</sup> C)	PACKAGE	PKG. NO.
CA0555E	-55 to 125	8 Ld PDIP	E8.3
CA0555M (555)	-55 to 125	8 Ld SOIC	M8.15
CA0555M96 (555)	-55 to 125	8 Ld SOIC †	M8.15
CA0555T	-55 to 125	8 Pin Metal Can	T8.C
CA0555CE	0 to 70	8 Ld PDIP	E8.3
CA0555CM (555C)	0 to 70	8 Ld SOIC	M8.15
CA0555CM96 (555C)	0 to 70	8 Ld SOIC †	M8.15
CA0555CT	0 to 70	8 Pin Metal Can	T8.C
LM555N	-55 to 125	8 Ld PDIP	E8.3
LM555CN	0 to 70	8 Ld PDIP	E8.3
NE555N	0 to 70	8 Ld PDIP	E8.3

NOTE: † Denotes Tape and Reel

## Description

The CA555 and CA555C are highly stable timers for use in precision timing and oscillator applications. As timers, these monolithic integrated circuits are capable of producing accurate time delays for periods ranging from microseconds through hours. These devices are also useful for astable oscillator operation and can maintain an accurately controlled free running frequency and duty cycle with only two external resistors and one capacitor.

The circuits of the CA555 and CA555C may be triggered by the falling edge of the waveform signal, and the output of these circuits can source or sink up to a 200mA current or drive TTL circuits.

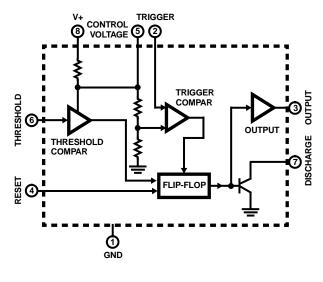
These types are direct replacements for industry types in packages with similar terminal arrangements e.g. SE555 and NE555, MC1555 and MC1455, respectively. The CA555 type circuits are intended for applications requiring premium electrical performance. The CA555C type circuits are intended for applications requiring less stringent electrical characteristics.

#### **Pinouts**

#### LM555, LM555C, NE555 (PDIP) TOP VIEW GND 1 8 V+ 7 DISCHARGE TRIGGER 2 OUTPUT 3 THRESHOLD CONTROL RESET 4 VOLTAGE CA555, CA555C (METAL CAN) TOP VIEW GND DISCHARGE TRIGGER (2 **THRESHOLD** OUTPUT CONTROL VOLTAGE RESET

CA555, CA555C (PDIP, SOIC)

## Functional Block Diagram



## CA555, CA555C, LM555, LM555C, NE555

#### **Absolute Maximum Ratings Thermal Information** $\theta_{JA}$ (°C/W) $\theta_{JC}$ (°C/W) Thermal Resistance (Typical, Note 1) 170 85 100 N/A **Operating Conditions** 160 N/A Temperature Range Maximum Junction Temperature (Hermetic Package) . . . . . . . . 175 $^{\rm o}$ C CA555, LM555 . . . . . -55°C to 125°C Maximum Junction Temperature (Plastic Package) . . . . . . . . 150°C Maximum Storage Temperature Range . . . . . -65°C to 150°C Maximum Lead Temperature (Soldering 10s).....300°C (SOIC - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

## **Electrical Specifications** $T_A = 25^{\circ}C$ , V+ = 5V to 15V Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	CA555, LM555			CA555C, LM555C, NE555			
			MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DC Supply Voltage	V+		4.5	-	18	4.5	-	16	V
DC Supply Current (Low State), (Note 2)	l+	V+ = 5V, R <sub>L</sub> = ∞	-	3	5	-	3	6	mA
		V+ = 15V, R <sub>L</sub> = ∞	-	10	12	-	10	15	mA
Threshold Voltage	$V_{TH}$		-	$(^{2}/_{3})V+$	-	-	$(^{2}/_{3})V+$	-	V
Trigger Voltage		V+ = 5V	1.45	1.67	1.9	-	1.67	-	V
		V+ = 15V	4.8	5	5.2	-	5	-	V
Trigger Current			-	0.5	-	-	0.5	-	μΑ
Threshold Current (Note 3)	I <sub>TH</sub>		-	0.1	0.25	-	0.1	0.25	μΑ
Reset Voltage			0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			-	0.1	-	-	0.1	-	mA
Control Voltage Level		V+ = 5V	2.9	3.33	3.8	2.6	3.33	4	V
		V+ = 15V	9.6	10	10.4	9	10	11	V
Output Voltage	V <sub>OL</sub>	V+ = 5V, I <sub>SINK</sub> = 5mA	-	-	-	-	0.25	0.35	V
Low State		I <sub>SINK</sub> = 8mA	-	0.1	0.25	-	-	-	V
		V+ = 15V, I <sub>SINK</sub> = 10mA	-	0.1	0.15	-	0.1	0.25	V
		I <sub>SINK</sub> = 50mA	-	0.4	0.5	-	0.4	0.75	V
		I <sub>SINK</sub> = 100mA	-	2.0	2.2	-	2.0	2.5	V
		I <sub>SINK</sub> = 200mA	-	2.5	-	-	2.5	-	V
Output Voltage	V <sub>OH</sub>	V+ = 5V, I <sub>SOURCE</sub> = 100mA	3.0	3.3	-	2.75	3.3	-	V
High State		V+ = 15V, I <sub>SOURCE</sub> = 100mA	13.0	13.3	-	12.75	13.3	-	V
		I <sub>SOURCE</sub> = 200mA	-	12.5	-	-	12.5	-	V
Timing Error (Monostable)		$R_1$ , $R_2 = 1$ kΩ to 100kΩ,	-	0.5	2	-	1	-	%
Frequency Drift with Temperature		C = 0.1μF Tested at V+ = 5V, V+ = 15V	-	30	100	-	50	-	ppm/ <sup>o</sup> C
Drift with Supply Voltage	1		-	0.05	0.2	-	0.1	-	%/V

<sup>1.</sup>  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

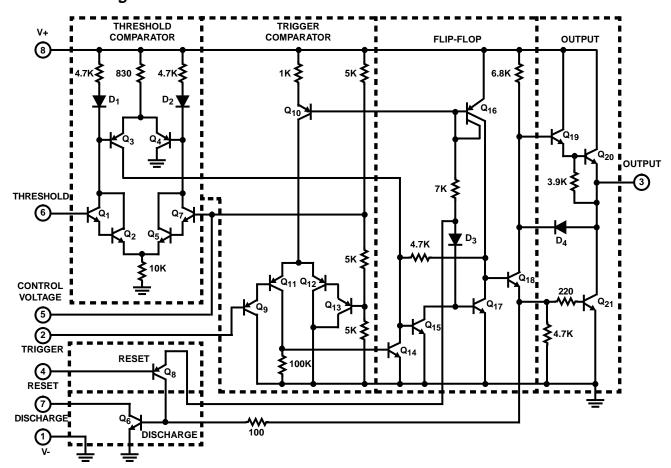
## **Electrical Specifications** $T_A = 25^{\circ}C$ , $V_{+} = 5V$ to 15V Unless Otherwise Specified (Continued)

			CA555, LM555			CA555C, LM555C, NE555			
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Output Rise Time	t <sub>R</sub>		-	100	1	-	100	-	ns
Output Fall Time	t <sub>F</sub>		-	100	ı	-	100	-	ns

#### NOTES:

- 2. When the output is in a high state, the DC supply current is typically 1mA less than the low state value.
- 3. The threshold current will determine the sum of the values of  $R_1$  and  $R_2$  to be used in Figure 4 (astable operation); the maximum total  $R_1 + R_2 = 20M\Omega$ .

## Schematic Diagram



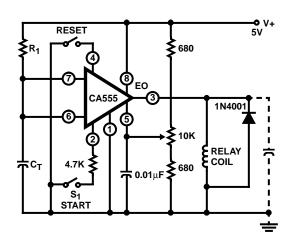
NOTE: Resistance values are in ohms.

## Typical Applications

#### **Reset Timer (Monostable Operation)**

Figure 1 shows the CA555 connected as a reset timer. In this mode of operation capacitor  $C_T$  is initially held discharged by a transistor on the integrated circuit. Upon closing the "start" switch, or applying a negative trigger pulse to terminal 2, the integral timer flip-flop is "set" and releases the short circuit across  $C_T$  which drives the output voltage "high" (relay ener-

gized). The action allows the voltage across the capacitor to increase exponentially with the constant  $t = R_1C_T$ . When the voltage across the capacitor equals 2/3 V+, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.



NOTE: All resistance values are in ohms.

#### FIGURE 1. RESET TIMER (MONOSTABLE OPERATION)

Since the charge rate and threshold level of the comparator are both directly proportional to V+, the timing interval is relatively independent of supply voltage variations. Typically, the timing varies only 0.05% for a 1V change in V+.

Applying a negative pulse simultaneously to the reset terminal (4) and the trigger terminal (2) during the timing cycle discharges  $C_T$  and causes the timing cycle to restart. Momentarily closing only the reset switch during the timing interval discharges  $C_T$ , but the timing cycle does not restart.

Figure 2 shows the typical waveforms generated during this mode of operation, and Figure 3 gives the family of time delay curves with variations in  $R_1$  and  $C_T$ .

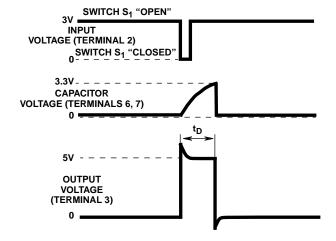


FIGURE 2. TYPICAL WAVEFORMS FOR RESET TIMER

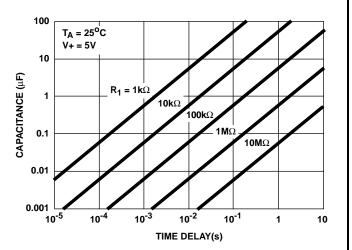


FIGURE 3. TIME DELAY vs RESISTANCE AND CAPACITANCE

#### Repeat Cycle Timer (Astable Operation)

Figure 4 shows the CA555 connected as a repeat cycle timer. In this mode of operation, the total period is a function of both  $R_1$  and  $R_2$ 

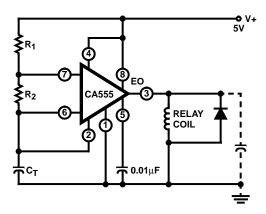


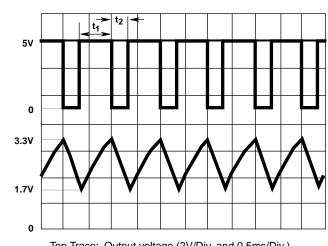
FIGURE 4. REPEAT CYCLE TIMER (ASTABLE OPERATION)

$$T = 0.693 \; (R_1 + 2R_2) \; C_T = t_1 + t_2$$
 where  $t_1 = 0.693 \; (R_1 + R_2) \; C_T$  and  $t_2 = 0.693 \; (R_2) \; C_T$ 

the duty cycle is:

$$\frac{t_1}{t_1 + t_2} = \frac{R_1 + R_2}{R_1 + 2R_2}$$

Typical waveforms generated during this mode of operation are shown in Figure 5. Figure 6 gives the family of curves of free running frequency with variations in the value of  $(R_1 + 2R_2)$  and  $C_T$ .



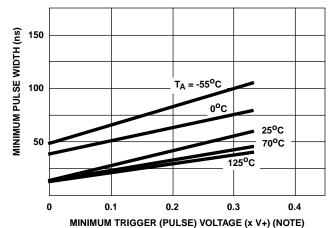
100  $T_A = 25^{\circ}C, V + = 5V$ 10 CAPACITANCE (µF)  $R_1 + 2R_2 = 1k\Omega$ 100 $k\Omega$ 0.1 0.01 0.001 10<sup>5</sup> 10<sup>-1</sup> 10<sup>2</sup> 10<sup>3</sup> 10<sup>4</sup> 10 FREQUENCY (Hz)

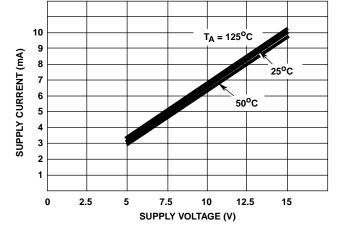
Top Trace: Output voltage (2V/Div. and 0.5ms/Div.) Bottom Trace: Capacitor voltage (1V/Div. and 0.5ms/Div.)

FIGURE 5. TYPICAL WAVEFORMS FOR REPEAT CYCLE TIMER

FIGURE 6. FREE RUNNING FREQUENCY OF REPEAT CYCLE
TIMER WITH VARIATION IN CAPACITANCE AND
RESISTANCE

## **Typical Performance Curves**





NOTE: Where x is the decimal multiplier of the supply voltage.

FIGURE 7. MINIMUM PULSE WIDTH vs MINIMUM TRIGGER VOLTAGE

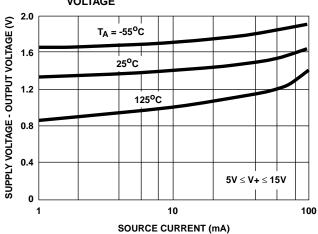


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

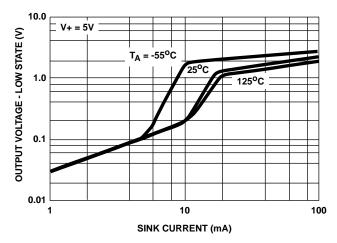


FIGURE 9. OUTPUT VOLTAGE DROP (HIGH STATE) vs SOURCE CURRENT

FIGURE 10. OUTPUT VOLTAGE LOW STATE vs SINK CURRENT

