

FEATURES

- 9-bit latch
- Extended 100E VEE range of -4.2V to -5.5V
- Parity detection/generation
- 800ps max. D to Output
- Reset
- Internal 75KΩ input pull-down resistors
- Fully compatible with Motorola MC10E/100E175
- Available in 28-pin PLCC package

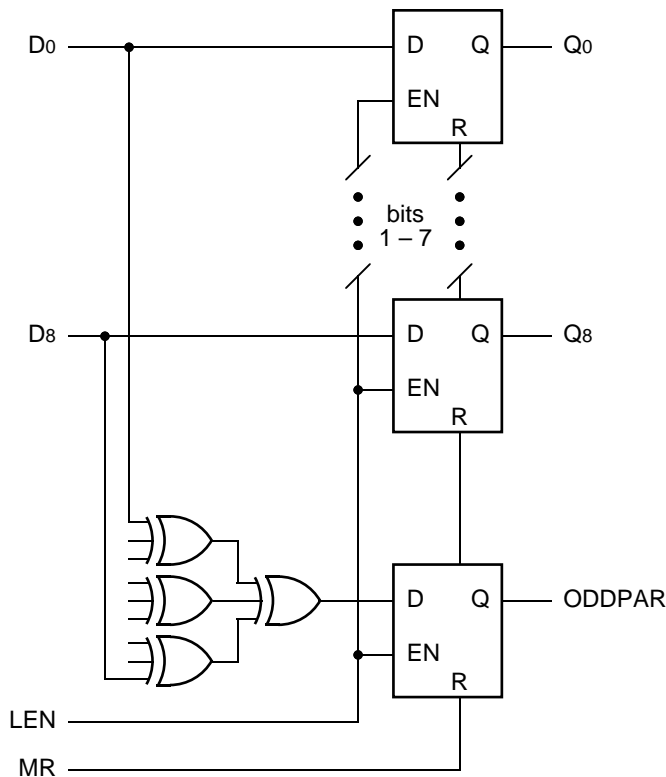
DESCRIPTION

The SY10/100E175 are 9-bit latches. They also feature a tenth latched output (ODDPAR) which is formed as the odd parity of the nine data inputs (ODDPAR is HIGH if an odd number of the inputs are HIGH).

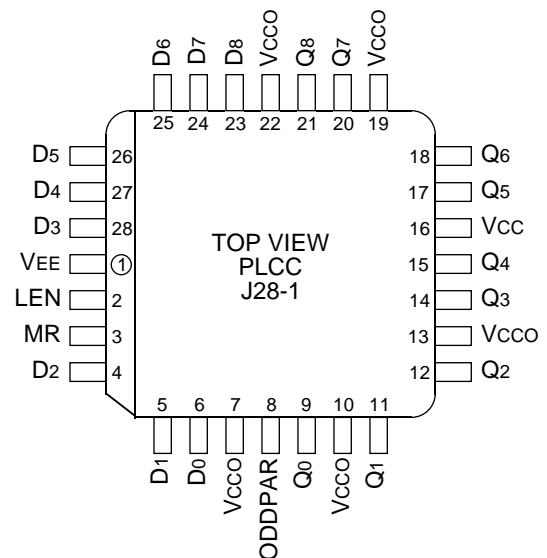
The E175 can also be used to generate byte parity by using D8 as the parity-type select (L = even parity, H = odd parity) and using ODDPAR as the byte parity output.

The LEN pin latches the data when asserted with a logical high and makes the latch transparent when placed at a logic low level.

BLOCK DIAGRAM



PIN CONFIGURATION



PIN NAMES

Pin	Function
D0 – D8	Data Inputs
LEN	Latch Enable
MR	Master Reset
Q0 – Q8	Data Outputs
ODDPAR	Parity Output
Vcco	Vcc to Output

TRUTH TABLE

D	LEN	MR	Q	ODDPAR
H	L	L	H	H if odd no. of D _n HIGH
L	L	L	L	H if odd no. of D _n HIGH
X	H	L	Q ₀	Q ₀
X	X	H	L	L

DC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—
I _{EE}	Power Supply Current	—	—	—	—	—	—	—	—	—	mA	—
		10E	110	132	110	132	110	132	110	132		
		100E	110	132	110	132	127	152	127	152		

AC ELECTRICAL CHARACTERISTICSV_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = V_{CC0} = GND

Symbol	Parameter	T _A = 0°C			T _A = +25°C			T _A = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output D to Q D to ODDPAR LEN to Q LEN to ODDPAR MR to Q (t _{PHL}) MR to ODDPAR (t _{PHL})	450 850 525 525 525 525	600 1150 700 700 700 700	800 1450 900 900 900 900	450 850 525 525 525 525	600 1150 700 700 700 700	800 1450 900 900 900 900	450 850 525 525 525 525	600 1150 700 700 700 700	800 1450 900 900 900 900	ps	—
t _s	Set-up Time D (Q) D (ODDPAR)	275 900	100 700	— —	275 900	— —	— —	275 900	— —	— —	ps	—
t _H	Hold Time D (Q) D (ODDPAR)	175 -300	-100 -700	— —	175 -300	— —	— —	175 -300	— —	— —	ps	—
t _{RR}	Reset Recovery Time	850	600	—	850	600	—	850	600	—	ps	—
t _{skew}	Within-Device Skew LEN, MR D to Q D to ODDPAR	— — —	75 75 200	— — —	— — —	75 75 200	— — —	— — —	75 75 200	— — —	ps	1
t _r t _f	Rise/Fall Times 20–80%	300	500	800	300	500	800	300	500	800	ps	—

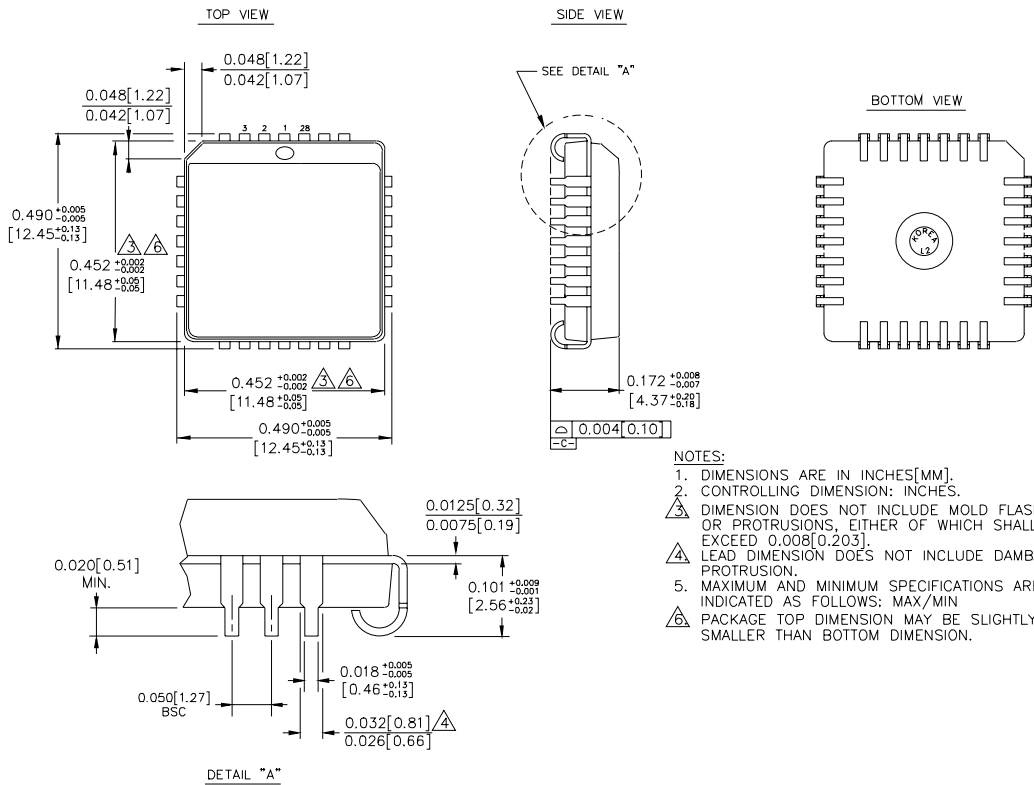
NOTE:

1. Within-device skew is defined as identical transitions on similar paths through a device.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E175JC	J28-1	Commercial
SY10E175JCTR	J28-1	Commercial
SY100E175JC	J28-1	Commercial
SY100E175JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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