

74F794 8-Bit Register with Readback

General Description

The 74F794 is an 8-bit register with readback capability designed to store data as well as read the register information back onto the data bus. The I/O bus (D bus) has 3-STATE outputs. Current sinking capability is 64 mA on both the D and Q busses.

Data is loaded into the registers on the LOW-to-HIGH transition of the clock (CP). The output enable (\overline{OE}) is used to enable data on D_0 - D_7 . When \overline{OE} is LOW, the output of the registers is enabled on D_0 - D_7 , enabling D as an output bus. When OE is HIGH, D_0 - D_7 are inputs to the registers configuring D as an input bus.

Features

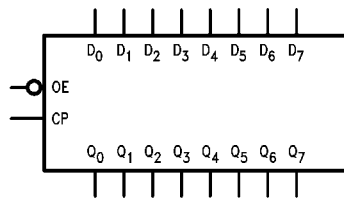
- 3-STATE outputs on the I/O port
- D and Q output sink capability of 64 mA
- Functionally and pin equivalent to the 74LS794

Ordering Code:

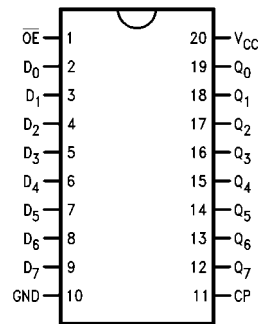
Order Number	Package Number	Package Description
74F794SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F794PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



Input Loading/Fan-Out

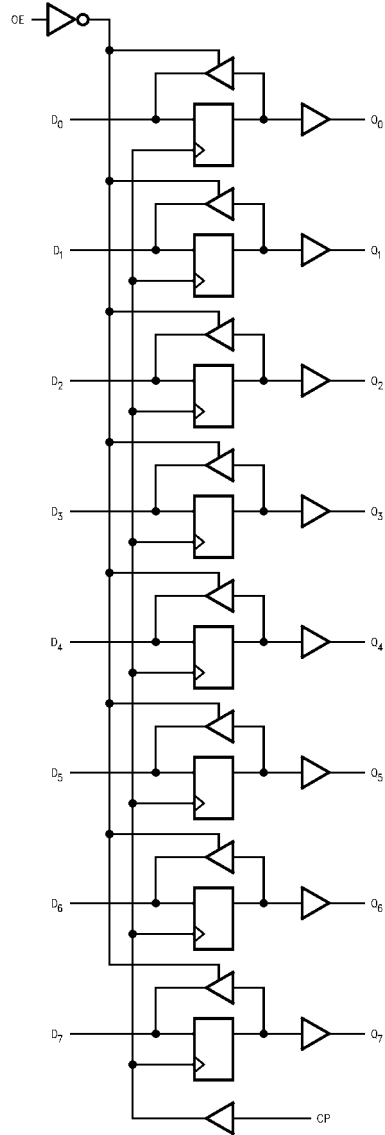
Pin Names	Description	HIGH/LOW	
		(U.L.)	Current
\overline{OE}	Output Enable Input	1.0/1.0	20 μ A/-0.6 mA
CP	Clock Pulse Inputs	1.0/1.0	20 μ A/-0.6 mA
D_0 - D_7	D Bus Inputs/ 3-STATE Outputs	3.5/1.083	70 μ A/-650 μ A
Q_0 - Q_7	Q Bus Outputs	750/106.6	-15 mA/64 mA

Truth Table

Inputs		Outputs	
CP	\overline{OE}	Q	D
L or H or \downarrow	L	Q_n	Output, Q
L or H or \downarrow	H	Q_n	Input
\uparrow	L	Q_n	Output, Q (Note 1)
\uparrow	H	D	Input

Note 1: In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_n .

Logic Diagram



Absolute Maximum Ratings ^(Note 2)		Recommended Operating Conditions	
Storage Temperature	-65°C to +150°C	Free Air Ambient Temperature	0°C to 70°C
Ambient Temperature under Bias	-55° to +125°C	Supply Voltage	+4.5V to +5.5V
Junction Temperature under Bias	-55°C to +150°C		
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V		
Input Voltage (Note 3)	-0.5V to +7.0V		
Input Current (Note 3)	-30 mA to +5.0 mA		
ESD Last Passing Voltage (Min)	4000V		
Voltage Applied to Output			
In HIGH State (with V _{CC} = 0V)			
Standard Output	-0.5V to V _{CC}		
3-STATE Output	-0.5V to +5.5V		
Current Applied to Output			
in LOW State (Max)	Twice the Rated I _{OL} (mA)		

Note 2: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 3: In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_n.

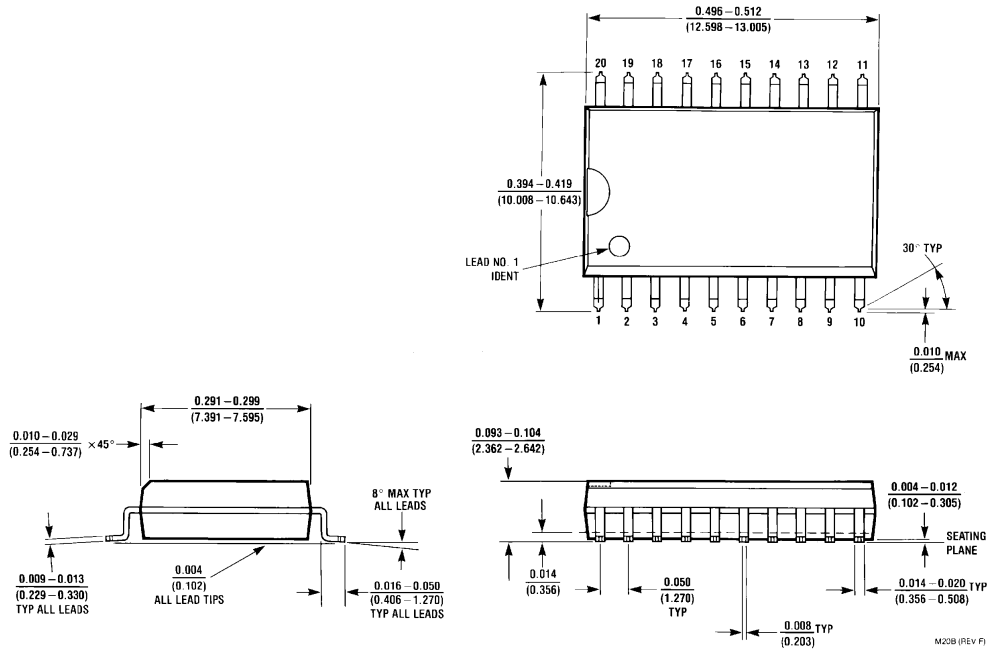
Note 4: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics over Operating Temperature Range unless otherwise specified

Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	2.4	2.8		V	Min	I _{OH} = -3 mA I _{OH} = -15 mA
V _{OL}	Output LOW Voltage		0.45	0.55	V	Min	I _{OL} = 64 mA
I _{IH}	Input HIGH Current			5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V (\overline{OE} , CP)
I _{BVIT}	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V _{IN} = 5.5V (D _n)
I _{CEx}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6	mA	Max	V _{IN} = 0.5V (\overline{OE} , CP)
I _{OS}	Output Short-Circuit Current	-100		-225	mA	Max	V _{OUT} = 0V
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (D _n)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (D _n)
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Circuit Leakage Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{ZZ}	Bus Drainage Test			100	μA	0.0	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current			65	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current			80	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current			80	mA	Max	V _O = HIGH Z

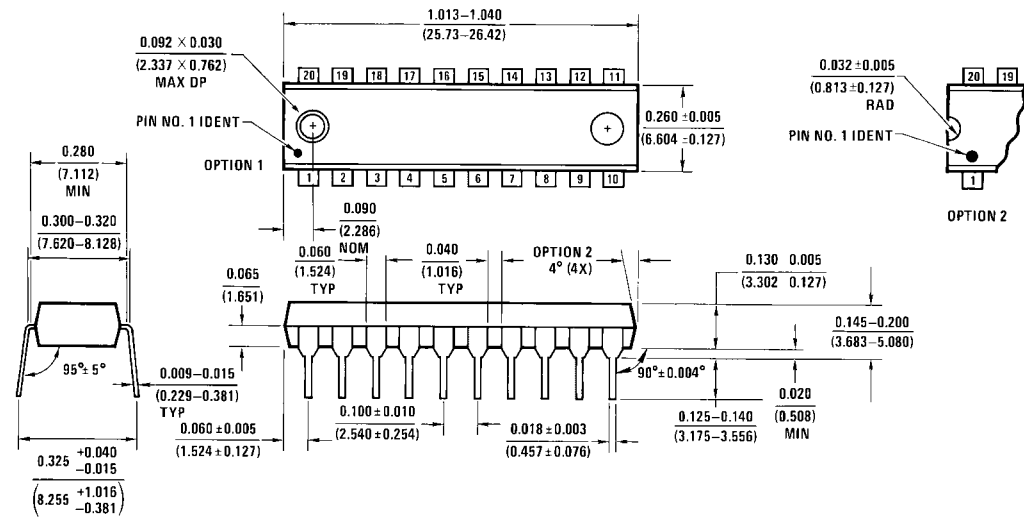
AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
f _{MAX}	Maximum Clock Frequency	90			90		MHz
t _{PLH}	Propagation Delay	2.5		7.0	2.5	8.0	ns
t _{PHL}	CP to Q _n	2.5		8.0	2.5	9.0	
t _{PZH}	Output Enable Time	2.3		8.5	2.0	9.0	ns
t _{PZL}		2.0		10.0	2.0	10.5	
t _{PHZ}	Output Disable Time	1.0		7.0	1.0	8.0	ns
t _{PLZ}		1.0		7.0	1.0	8.0	
t _S (H)	Setup Time, HIGH or LOW	4.0			4.0		ns
t _S (L)	Bus to Clock	4.0			4.0		
t _H (H)	Hold Time, HIGH or LOW	1.5			1.5		ns
t _H (L)	Bus to Clock	1.5			1.5		
t _W (H)	Clock Pulse Width	5.8			5.8		ns
	HIGH or LOW	5.8			5.8		

Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
Package Number M20B**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



N20A (REV G)

20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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