

Bluetooth Module

HBH1X1M

Data Book

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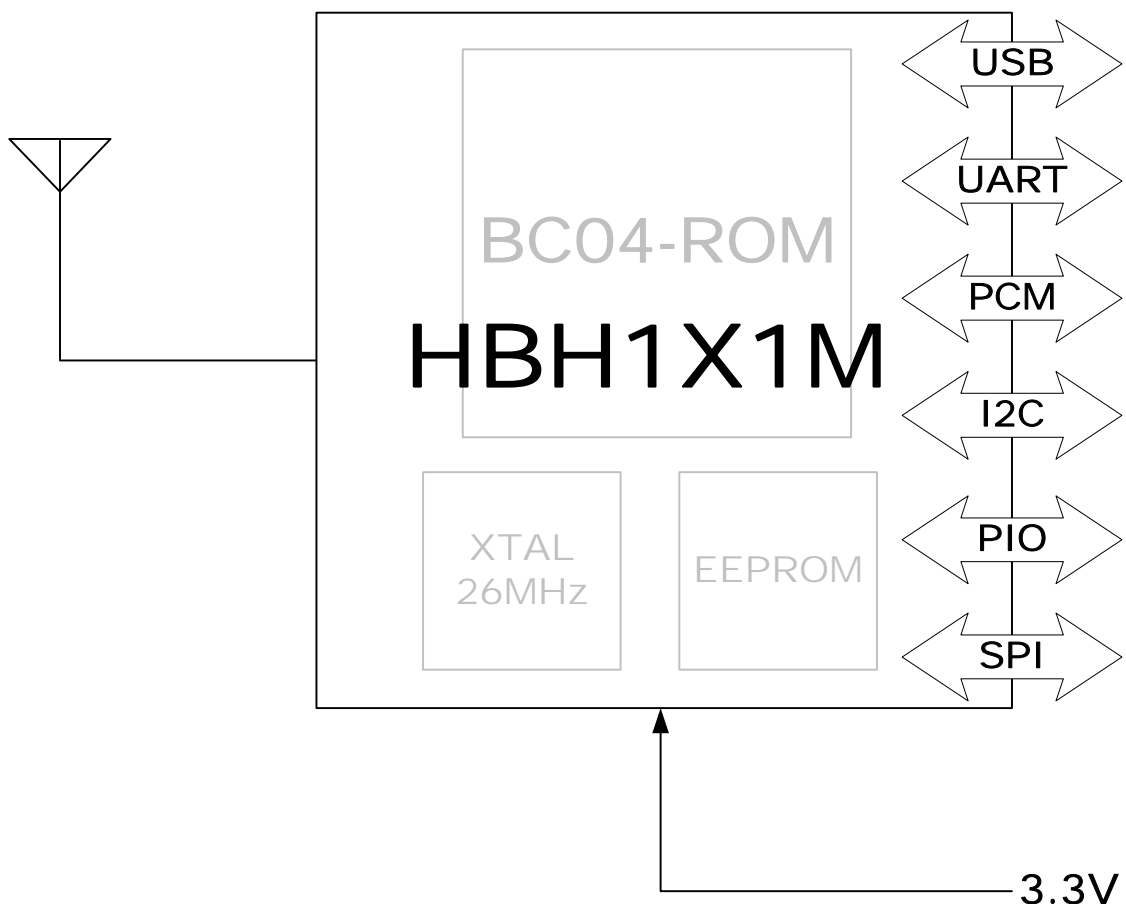
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1. General

1.1 Overview

This specification covers Bluetooth module (class-1) which complies with Bluetooth specification version 2.0 + EDR and integrates RF & Baseband controller in small package. This Module has deployed CSR's BC04-ROM CSP EDR chipset.

All detailed specification including pinouts and electrical specification may be changed without notice.



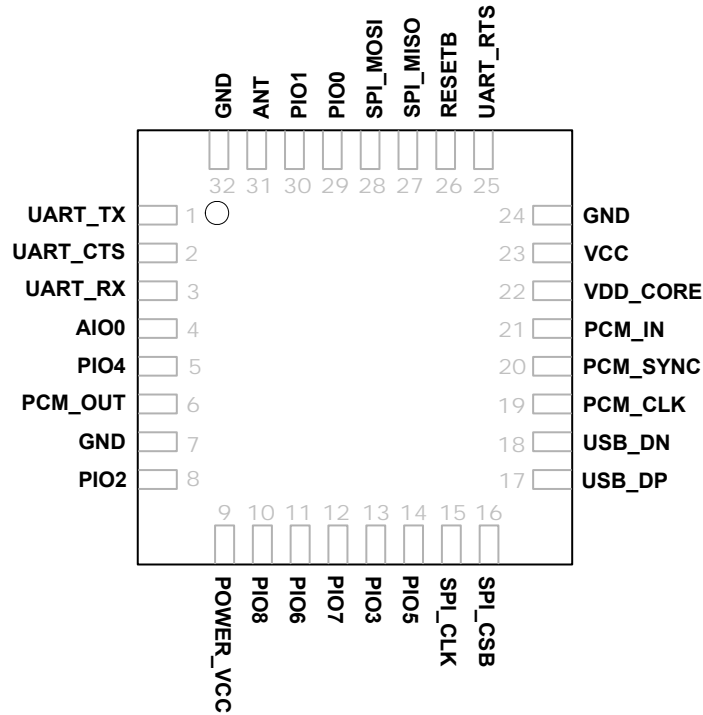
1.2 Features

- Fully Qualified Bluetooth v2.0 + EDR System
- Enhanced Data Rate (EDR) compliant with v2.0 of specification for both 2Mbps and 3Mbps modulation modes
- Full-speed Bluetooth Operation with Full Piconet Support
- Scatternet Support
- Ultra Low Power Consumption
- Excellent Compatibility with Cellular Telephones
- Support for 802.11 Co-existence
- RoHS Compliant
- Integrated transcoders for A-law, u-law and linear PCM
- UART interface with programmable baud rate up to 3Mbits/s with an optional bypass mode
- Full-speed USB v2.0 interface supports OHCI and UHCI host interface
- Standard HCI (UART and USB) support
- Integrated 4Mbit ROM & 48Kbyte RAM
- Integrated 26MHz Reference Clock
- Competitive Size (10.0mm x 10.0mm x 1.6mm : LGA 32Pin)

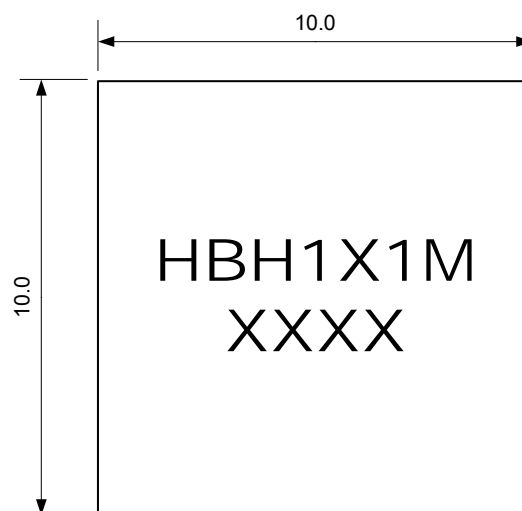
1.3 Application

- Cellular Handsets
- Personal Digital Assistants (PDA)
- Space critical application
- Digital Cameras and other high-volume consumer product
- USB Dongle

1.4 Pin Configuration & Outline



HBH1X1M Pin Configuration



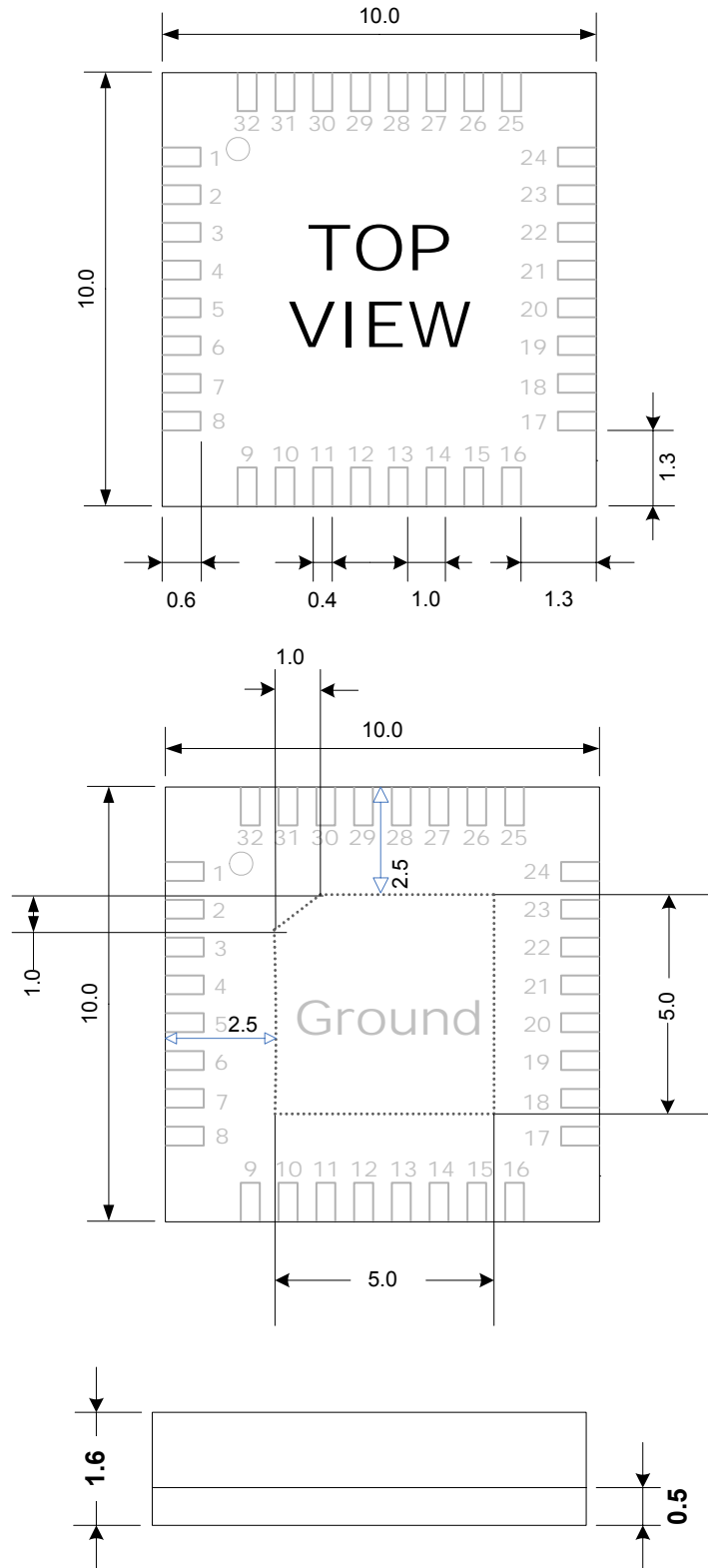
HBH1X1M Outline

1.5 Device Terminal Functions

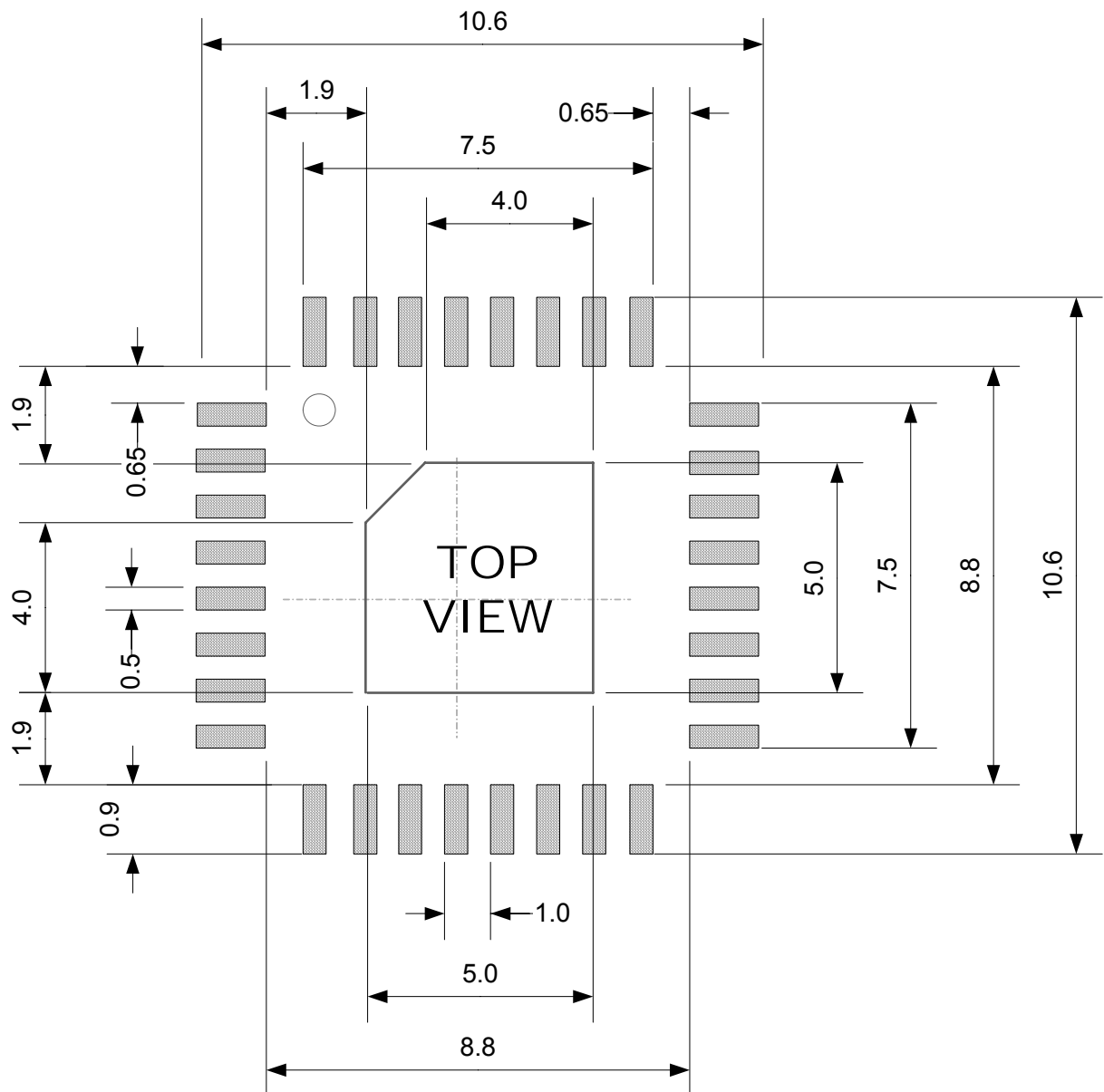
Function	Pin Name	Pin No.	Description
PCM Interface	PCM_OUT	6	Synchronous data output
	PCM_IN	21	Synchronous data input
	PCM_CLK	19	Synchronous data clock
	PCM_SYNC	20	Synchronous data sync
UART Interface	UART_TXD	1	UART data output
	UART_RXD	3	UART data input (idle status high)
	UART_RTS	25	UART request to send, active low
	UART_CTS	2	UART clear to send, active low
SPI Interface	CSB	16	Chip select for Synchronous Serial Interface Active low
	CLK	15	Serial Peripheral Interface clock
	MISO	27	Serial Peripheral Interface data output
	MOSI	28	Serial Peripheral Interface data input
USB Interface	USB_DN	18	USB data minus
	USB_DP	17	USB plus with selectable internal 1.5K pull-up resistor
PIO Interface	PIO0	29	Don't use this pin, this pin is used for switching external PA and LNA
	PIO1	30	Don't use this pin, this pin is used for switching external PA and LNA
	PIO2	8	Programmable input/output line
	PIO3	13	Programmable input/output line
	PIO4	5	UART Bypass(UART_TX)
	PIO5	14	UART Bypass(UART_RTS)
	PIO6	11	UART Bypass(UART_CTS) / E2PROM(SCL)
	PIO7	12	UART Bypass(UART_RX) / E2PROM(SDA)
Others	AIO0	4	General purpose analogue interface
	VDD_CORE	22	Positive supply for internal digital circuit
	RESETB	26	Reset if low. Input debounced so must be low For > 5ms to cause a reset

Others	ANT	31	RF connection to antenna
	VCC	23	D.C input voltage for operation (3.0 ~ 3.3)
	POWER_VCC	9	D.C input voltage for operation (3.0 ~ 3.3)
	GND	7, 24, 32	Ground

1.6 Package Dimensions



1.7 Land Pattern Recommendation



2 Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Minimum	Maximum
Storage temperature	-40℃	85℃
Supply voltage : VCC	-0.4V	3.7V
Other terminal voltages	VSS-0.4V	VCC+0.4V

Recommended Operating Conditions		
Operating Conditions	Minimum	Maximum
Operating temperature range	-20℃	80℃
Supply voltage range		
VCC	3.0V	3.3V
POWER_VCC	3.0V	3.3V

2.2 Power Consumption

Operation Mode	Connection Type	UART Rate (Kbits/s)	Average	Unit
Inquiring mode	--	115.2	46	mA
ACL data transfer no traffic	Master	115.2	4.7	mA
ACL data transfer with file transfer	Master	115.2	8.5	mA
SCO connection HV3	Master	38.4	46	mA
Standby Host connection	--	38.4	0.29	mA

Note :

Conditions : 25℃, 3.3V supply

2.3 RF Characteristics

Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output power	Normal	-11	17	18	dBm
Power density	Normal		15	16	dBm
Power control	Normal	2	4	8	dBm
Frequency range	Normal	2400.9		2481.5	MHz
20dB bandwidth for modulated carrier	Normal		850	1000	KHz
Adjacent channel power	±2MHz			-20	dBm
	±3MHz			-40	
	±4MHz			-40	
Modulation Characteristics	$\Delta f1_{avg}$	140	160	175	KHz
	$\Delta f2_{max}$	115	140		KHz
	$\Delta f2_{avg} / \Delta f1_{avg}$	80	90	99	%
Initial carrier frequency tolerance	Normal	-15		15	KHz
Carrier frequency Drift	One slot packet(DH1)	-20		20	kHz
	Three slot packet(DH3)	-25		25	
	Five slot packet(DH5)	-30		30	

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Out of band spurious emissions	30MHz ~ 1GHz			-36	dBm
	1GHz ~12.75GHz			-40	
	1.8GHz ~5.1GHz			-47	
	5.1GHz ~5.3GHz			-47	

Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	-70	-87		dBm
Sensitivity level (0.1% BER)	Multi slot packet	-70	-87		dBm
C/I performance	co - channel			11	dBm
	1MHz (Adjacent channel)			0	
	2MHz (2 nd Adjacent channel)			-30	
	≥3MHz (3 rd Adjacent channel)			-40	
Blocking performance	30MHz ~ 2000MHz	-10			MHz
	2000MHz ~ 2400MHz	-27			
	2500MHz ~ 3000MHz	-27			
	3000MHz ~ 12.75GHz	-10			
Intermodulation performance	n = 5	-39			KHz
Maximum input level		-20	-10		

3 Terminal Description

3.1 UART

Four signals are used to implement the UART function. **UART_TXD** and **UART_RXD** transfer data between the two devices. The remaining two signals, **UART_CTS** and **UART_RTS**, can be used to implement RS232 hardware flow control where both are active low indicators.

3.1.1 UART Setting

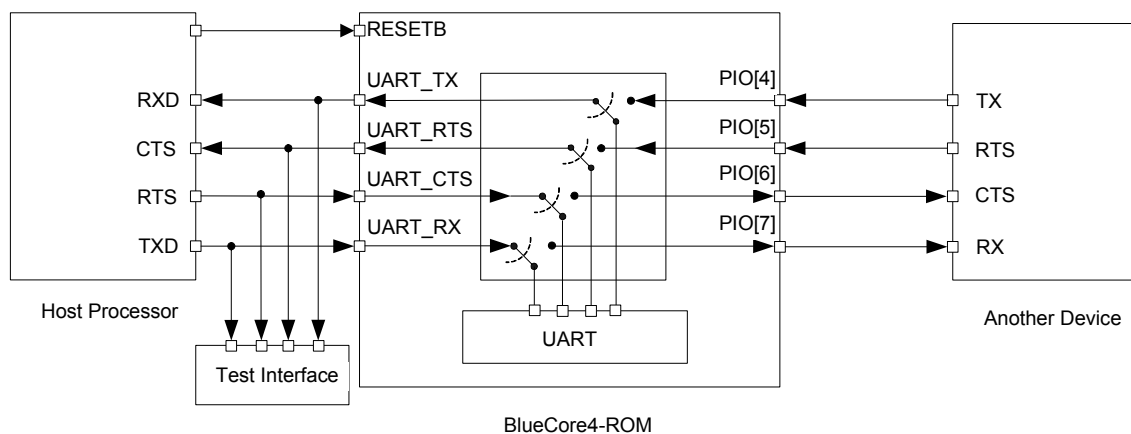
User can change data format the following selection using PSKEY. However, host shall communicate with default setting UART connection initiated at first time.

$$\text{Baud Rate} = (\text{PSKEY_UART_BAUD_RATE}) / 0.004096$$

Parameter	Possible value
Baud Rate	9600 ~ 3M Baud
Flow Control	RTS/CTS or None
Parity	None, Odd or Even
Number of Stop Bits	1 or 2
Bits per channel	8

3.1.2 UART Bypass Mode

Switch the bypass to PIO[7:4] as shown in figure. When the bypass mode has been invoked, module enters the deep sleep state indefinitely.



3.2 USB

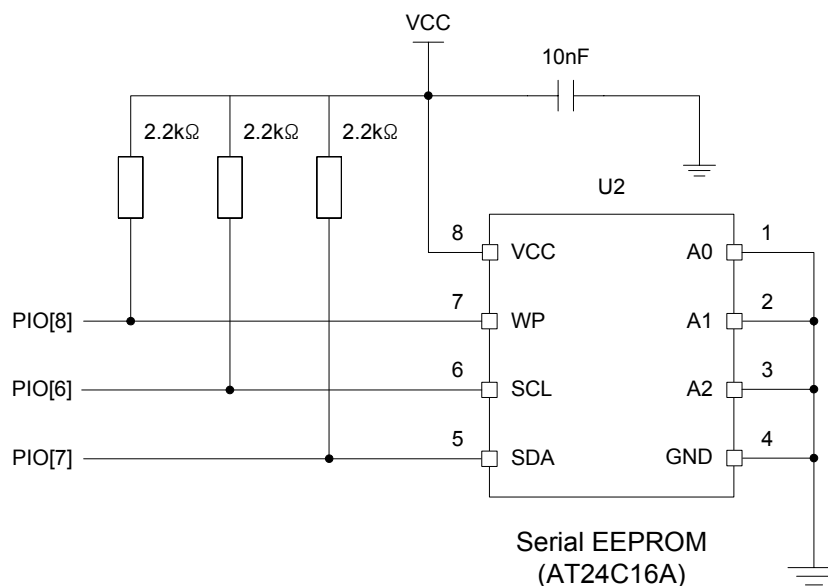
This Bluetooth module contains a full speed (12Mbit/s) USB interface that is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0 + EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as a set of USB speakers.

USB is a master/slave oriented system (in common with other USB peripherals). This Module only supports USB slave operation.

3.3 I²C

PIO[8:6] can be used to form an interface. The interface is driven by “bit banging” these PIO pins using software. Therefore it is suited only to relatively slow functions such as driving a dot matrix liquid crystal display (LCD).

Note. PIO[7:6] dual functions, UART bypass and EEPROM support, therefore devices using an EEPROM connect support UART bypass mode. PIO Lines need to be pulled-up through 2.2KΩ resistors.



3.4 PCM

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband layer of the on-chip firmware. It dose not pass through the HCI protocol layer.

Hardware allows the data to be sent to and received from a SCO connection

This module interfaces directly to PCM audio devices including the following :

- **Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices**
- **OKI MSM7705 for channel A-law and u-law CODEC**
- **Motorola MC145481 8-bit A-law and u-law CODEC**
- **Motorola MC145483 13-bit linear CODEC**
- **STW 5093 and 5094 14-bit linear CODECs**

3.4.1 PCM Configuration

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32 and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tristating of PCM_OUT.

Parameter	Possible value
Mode	Slave, Master
Clock Rate	Master Mode : 128, 256, 512KHz Slave Mode : up to 2048KHz
Sync Formats	Long frame sync, Short frame sync
Data Formats	13 or 16bit linear, 8 - bit A - law to u - law

4 Boot Interface Configures

The firmware configures itself when it boots by reading the value on a set PIO pins

Pin Values			Host Transport	Features	
PIO[0]	PIO[1]	PIO[4]		Auto System Clock	Auto Baud Rate
0	0	0	BCSP (Default)	Available	Available
0	0	1	BCSP with UART configured to use 2 stop bits and no parity	Available	Available
0	1	1	USB, 26 MHz Crystal	Not available	Not appropriate
1	0	0	Three-wire UART	Available	Available
1	0	1	H4DS	Available	Available
1	1	0	UART (H4)	Available	Available
1	1	1	Undefined	-	-

5 Application Schematic

