Ultra-Low-Noise, High PSRR, Low-Dropout, 300mA Linear Regulator

Features

- Wide Operating Voltage: 2.3V~6V
- Low Dropout Voltage: 290mV @ 3V/300mA
- Fixed Output Voltages: 1.5V~3.5V with step 100mV, 2.85V
- Guaranteed 300mA Output Current
- High PSRR: 74dB before 10KHz
- Low Output Noise: 36μV_{RMS} at 100Hz to 100KHz
- Current Limit Protection
- Controlled Short Circuit Current: 50mA
- Over Temperature Protection
- Stable with 1μF Capacitor for Any Load
- Excellent Load/Line Transient
- SOT23-5 and SC70-5 Packages
- Lead Free Available (RoHS Compliant)

Applications

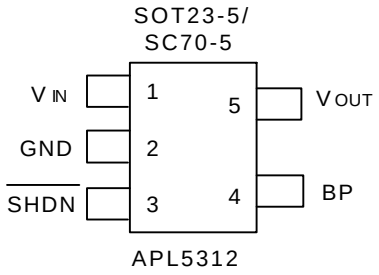
- Cellular Phones
- Portable and Battery-Powered Equipment
- Wireless LANs
- GPS

General Description

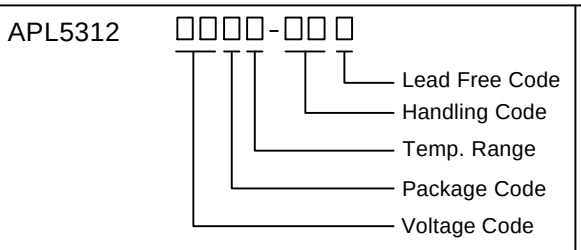
The APL5312 is a ultra low noise, low dropout linear regulator, which operate from 2.3V to 6V input voltage and deliver up to 300mA. Typical dropout voltage is only 290mV at 300mA loading. Designed for use in RF applications, the high PSRR 74dB and low noise 36μV_{RMS} makes it an ideal choice.

Design with an internal P-channel MOSET pass element, the APL5312 maintain a low supply current, independent of the load current and dropout voltage. Other features include thermal-shutdown protection and current limit protection to ensure specified output current and controlled short-circuit current. The APL5312 regulator come in a miniature SOT23-5 and SC70-5 package.

Pin Configuration



Ordering and Marking Information



Package Code
B : SOT23-5 S5 : SC70-5
Operating Ambient Temp. Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Voltage Code
15 : 1.5V 30 : 3.0V
Lead Free Code
L : Lead Free Device Blank : Original Device

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

SOT23-5 packages

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5312-15/B	339X	APL5312-16/B	33AX	APL5312-17/B	33BX	APL5312-18/B	33CX
APL5312-19/B	33DX	APL5312-20/B	33EX	APL5312-21/B	33FX	APL5312-22/B	33GX
APL5312-23/B	33HX	APL5312-24/B	33IX	APL5312-25/B	33JX	APL5312-26/B	33KX
APL5312-27/B	33LX	APL5312-28/B	33MX	APL5312-29/B	33NX	APL5312-30/B	33OX
APL5312-31/B	33PX	APL5312-32/B	33QX	APL5312-33/B	33RX	APL5312-34/B	33SX
APL5312-35/B	33TX	APL5312-285/B	33αX				

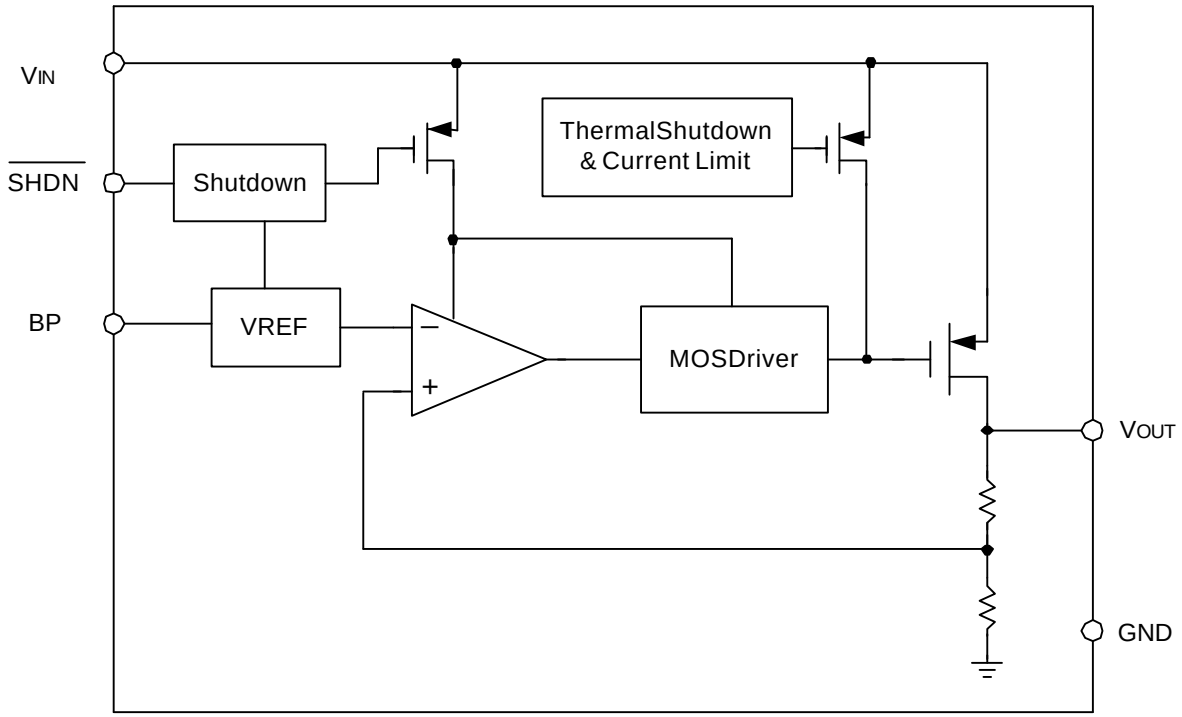
SC70-5 packages

Product Name	Marking	Product Name	Marking	Product Name	Marking	Product Name	Marking
APL5312-15/S5	339	APL5312-16/S5	33A	APL5312-17/S5	33B	APL5312-18/S5	33C
APL5312-19/S5	33D	APL5312-20/S5	33E	APL5312-21/S5	33F	APL5312-22/S5	33G
APL5312-23/S5	33H	APL5312-24/S5	33I	APL5312-25/S5	33J	APL5312-26/S5	33K
APL5312-27/S5	33L	APL5312-28/S5	33M	APL5312-29/S5	33N	APL5312-30/S5	33O
APL5312-31/S5	33P	APL5312-32/S5	33Q	APL5312-33/S5	33R	APL5312-34/S5	33S
APL5312-35/S5	33T	APL5312-285/S	33α				

Pin Description

PIN		I/O	Description
No.	Name		
1	V_{IN}	I	Voltage supply input pin
2	GND		GND pin
3	$\overline{SHDN}$	I	Shutdown control pin, low = off, high = normal
4	BP	I	Bypass signal pin in fixed output type device
5	V_{OUT}	O	Regulator output pin

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN}, V_{OUT}	Input Voltage or Out Voltage	6.5	V
$\overline{SHDN}$/BP	V_{OUT} Shutdown Control Pin/Bypass Signal Pin	6.5	V
$R_{TH,JA}$	Thermal Resistance-Junction to Ambient (Note) SOT23-5 SC70-5	 240 325	℃ /W
PD	Power Dissipation, T_A = 25 ℃ (Note) SOT23-5 SC70-5	 410 310	mW
T_J	Operating Junction Temperature	0 to 125	℃
T_{STG}	Storage Temperature Range	-65 to +150	℃
T_L	Lead Temperature (Soldering, 10 second)	260	℃

Note: When mounted on a (Copper foil area 50%, 45x45x1.6tmm) glass epoxy board.

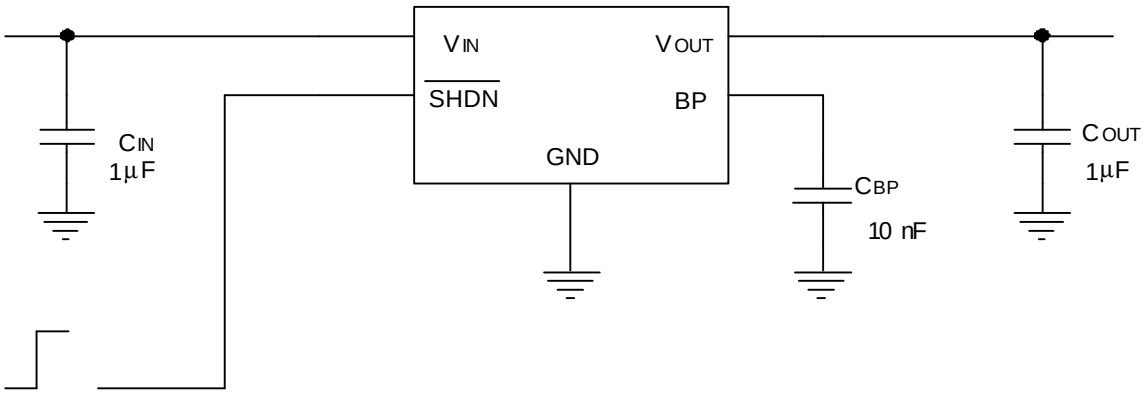
Electrical Characteristics

Unless otherwise noted these specifications apply over full temperature, V_{IN} = V_{OUT}+1V, C_{IN} = C_{OUT} = 1µ F, T_A = -40 to 85°C .Typical values refer to T_A = 25°C.

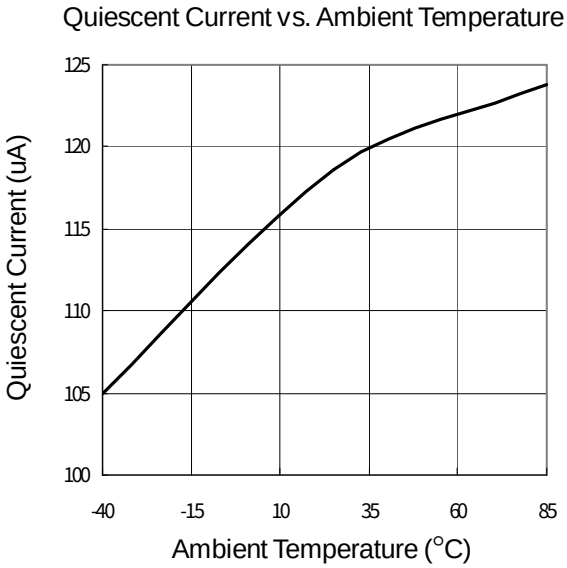
Symbol	Parameter	Test Condition	APL5312			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2.3		6	V
V_{OUT}	Output Voltage Accuracy	V_{IN} = 5V	-2		2	%
	Output Voltage Range		1.5		3.5	V
I_{LIMIT}	Circuit Current Limit		450	500	550	mA
I_Q	Quiescent Current	I_{OUT} = 0mA		120	160	µA
		I_{OUT} = 300mA		120	160	
I_{OUT}	Load Current			300		mA
REG_{LINE}	Line Regulation	V_{OUT}+0.5V<V_{IN}<6V, I_{OUT} = 10mA		0.1	0.3	%
REG_{LOAD}	Load Regulation	V_{IN} = V_{OUT}+1V, 0mA<I_{OUT}<300mA		0.8	1.5	%
V_{DROP}	Dropout Voltage (Note)	V_{OUT} =1.5V, I_{OUT} = 300mA		520	680	mV
		V_{OUT} = 2V, I_{OUT} = 300mA		430	560	
		V_{OUT} = 3V, I_{OUT} = 300mA		290	380	
PSRR	Ripple Rejection	f = 1kHz, C_{BP}=10nF, I_{OUT}=10mA		73		dB
		f = 10kHz, C_{BP}=10nF, I_{OUT} = 10mA		74		
		f = 100KHz, C_{BP} = 10nF, I_{OUT} = 10mA		55		
I_{SHORT}	Short Current	V_{OUT} = 0V		50		mA
e_n	Noise	f = 100Hz to 100kHz, C_{BP} = 10nF, I_{OUT} = 10mA		36		μV_{RMS}
V_{SHDN}	High Threshold Voltage		1.6		V_{IN}+0.3	V
	Low Threshold Voltage		-0.3		0.4	
I_{SHDN}	Shutdown Input Bias Current	V_{SHDN} = V_{IN}		0.1	1	µA
I_{QSHDN}	Shutdown Supply Current	SHDN = Low, V_{IN} = V_{OUT}+1V		0.1	1	µA
T_{EXIT}	Shutdown Exit Delay	V_{OUT} = 90%, R_{LOAD} = 50Ω		100		µS
OTS	Over Temperature Shutdown			160		℃
	Over Temperature Shutdown Hysteresis			20		℃
TC	Output Voltage Temperature Coefficient	T_J = -40~125 ℃		100		ppm/℃
C_{OUT}	Output Capacitor			1		µF
	ESR		0.025		1	Ω

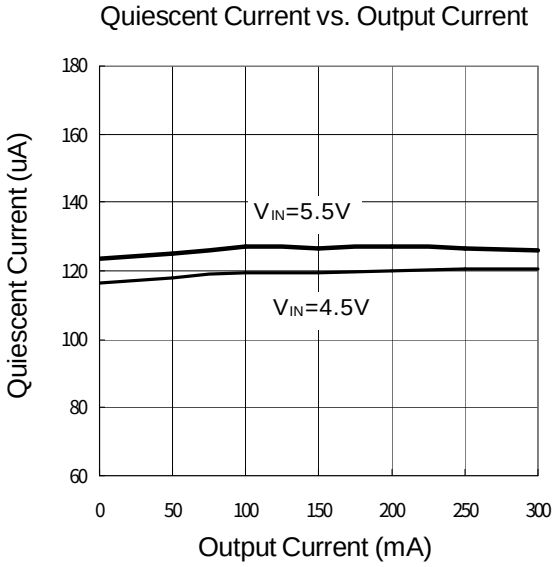
Note: Dropout voltage definition: V_{IN}-V_{OUT} when V_{OUT} is 2% below the value of V_{OUT} for V_{IN}= V_{OUT} +1V.

Typical Application Circuit



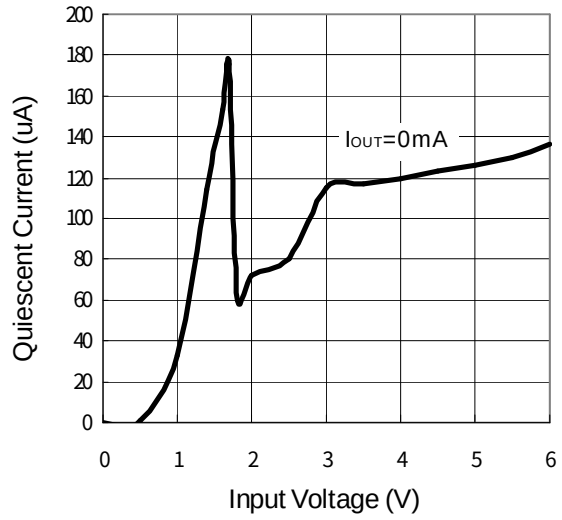
Typical Characteristics



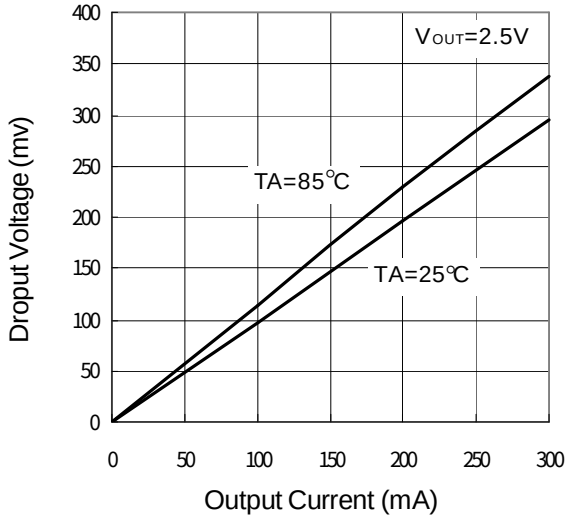


Typical Characteristics (Cont.)

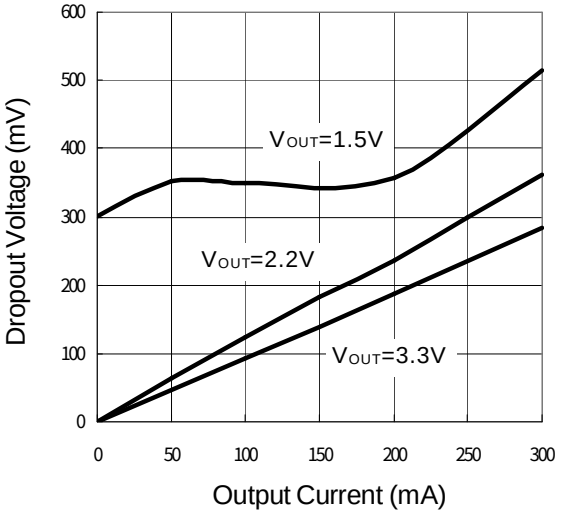
Quiescent Current vs. Input Voltage



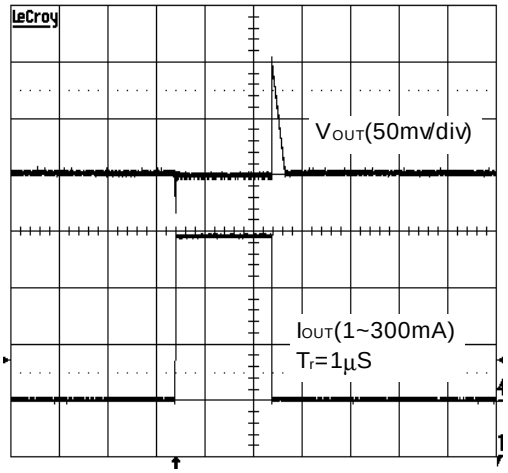
Dropout Voltage vs.Output Current



Dropout Voltage vs. Output Current

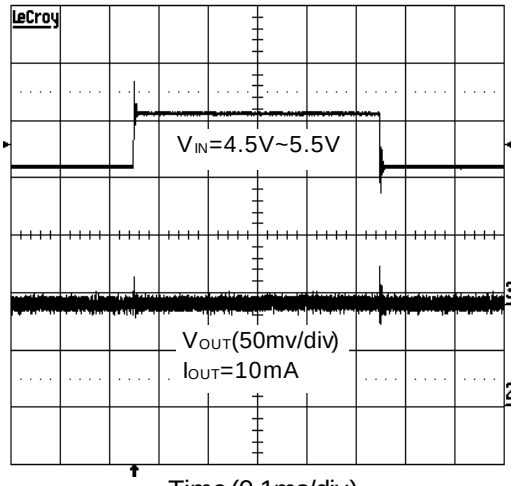


Load Transient

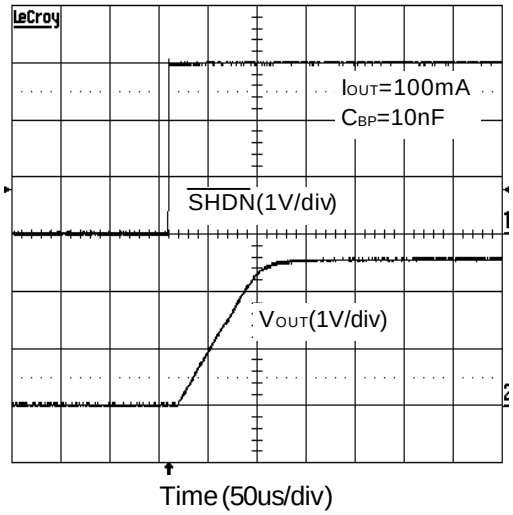


Typical Characteristics (Cont.)

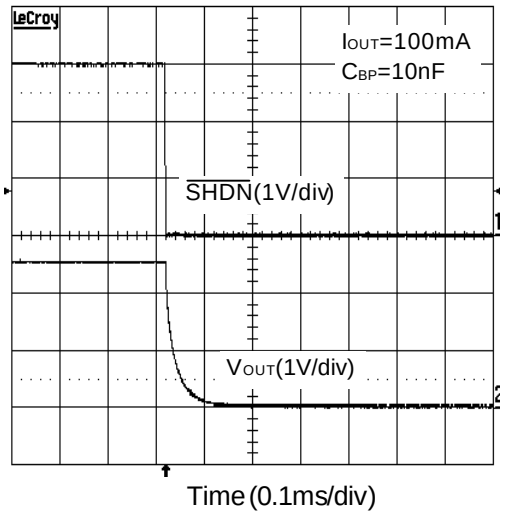
Line Transient



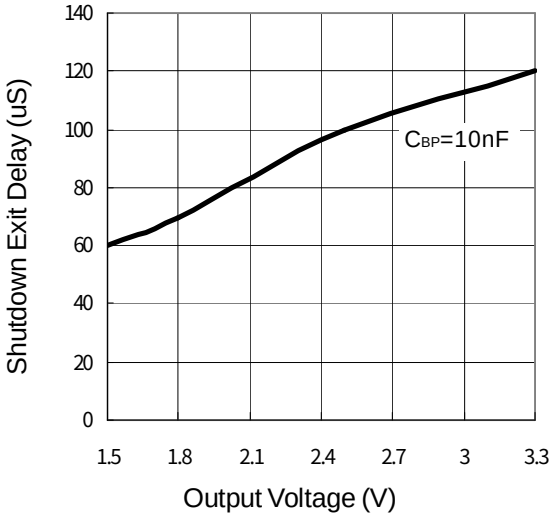
Exiting Shutdown Waveform



Entering Shutdown Delay

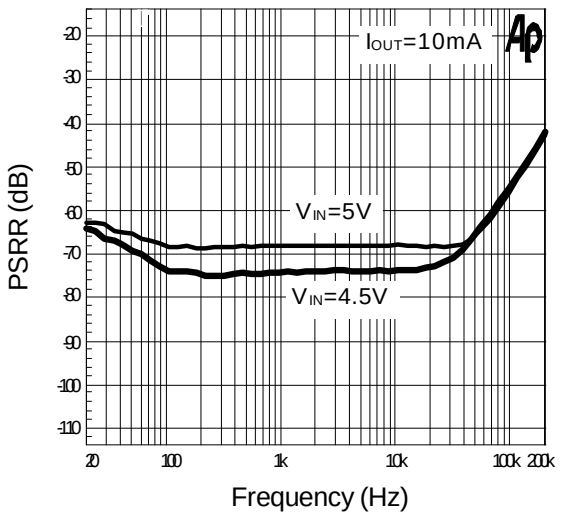


Shutdown Exit Delay

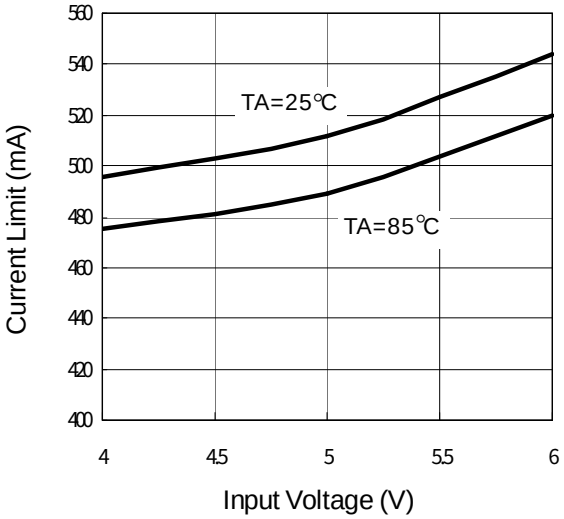


Typical Characteristics (Cont.)

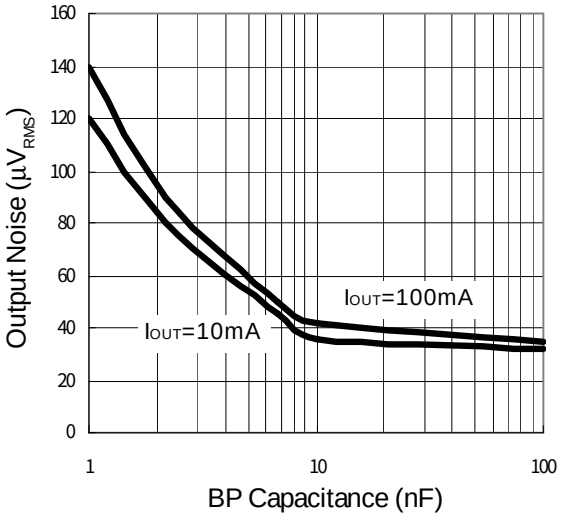
PSRR vs. Frequency



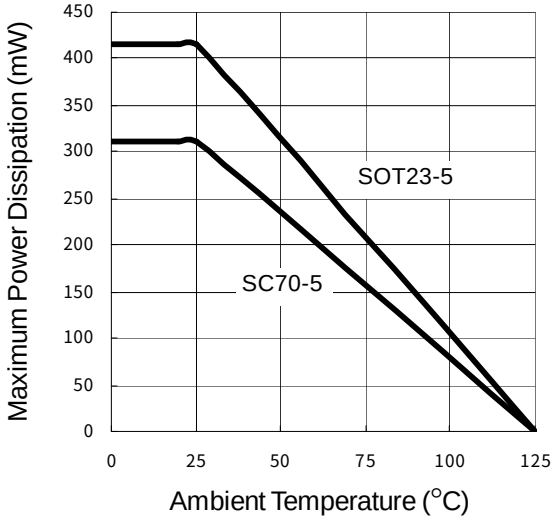
Current Limit vs. Input Volatge



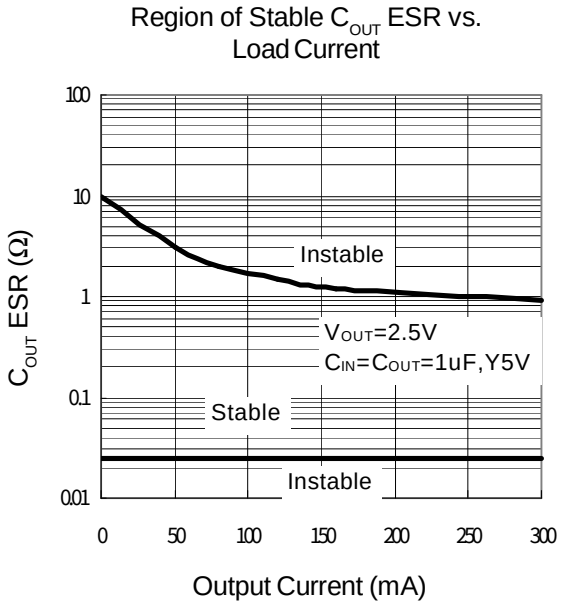
Output Noise vs. BP Capacitance



Maximun Power Dissipation vs. Ambient Temperature



Typical Characteristics (Cont.)



Application Information

Output Voltage Selection

The APL5312 are supplied with factory-set output voltages from 1.5V to 3.5V.

Capacitor Selection and Regulation Stability

The APL5312 uses at least a 1µF capacitor on the input. This capacitor can use Aluminum, Tantalum or Ceramic capacitors. Input capacitor with large value and low ESR provides better PSRR and line-transient response. The output capacitor also can use Aluminum, Tantalum or Ceramic capacitor, and its proper values is at least 1µF, ESR must be above 25mΩ. Large output capacitor values can reduce noise and improve load-transient response, stability, and PSRR. With X5R and Y5V dielectrics, 1µF is sufficient at all operating temperatures. The selection of output capacitor's is important because it with C_{OUT} form a zero to provide the sufficient phase margin (see the Figure C_{OUT} ESR vs. Load Current).

Bypass Capacitor

Use a 10nF bypass capacitor at BP for low-output voltage noise. The leakage current going into the BP pin should be less than 10nA. Increasing the capacitance slightly decreases the output noise. Value above 0.1µF and below 1nF are not recommended (see the Figure Output Noise vs. BP Capacitance).

Noise, PSRR, and Load-Transient Response

The APL5312 is designed to deliver ultra-low noise and high PSRR, as well as low dropout and low quiescent currents in battery–powered systems. When operating from sources other than batteries, improve PSRR and transient response can be achieved by increasing input and output capacitors, and bypass capacitor to from the passive filtering

Application Information (Cont.)

Noise, PSRR, and Load-Transient Response (Cont.)

techniques (see the Figure Output Noise vs. BP Capacitance).

Shutdown

The APL5312 has an active high enable function. Force $\overline{SHDN}$ high (>1.6V) enables the V_{OUT}, $\overline{SHDN}$ low (<0.4V) disables the V_{OUT}. Enter the shutdown mode, it also causes the output voltage to discharge through a 500Ω resistance to ground. In shutdown mode, the quiescent current can reduce to 0.1uA. The $\overline{SHDN}$ pin cannot be floating, a floating $\overline{SHDN}$ pin may cause an indeterminate state on the output. If it is no use, connect to V_{IN} for normal operation.

Input-Output (Dropout) Voltage

The minimum input-output voltage differential (dropout) determines the lowest usable supply voltage. The dropout voltage is a function of drain-to-source on resistance multiplied by the load current.

Current Limit

APL5312 includes a current-limit circuitry for linear regulator. The current limit protection, which sense the current flows the P-channel MOSFET, and controls the output voltage. The point where limiting occurs is I_{OUT} = 500mA . The output can be shorted to ground for an indefinite amount of time without damaging to the part.

Thermal Protection

Thermal protection limits total power dissipation in the APL5312. When the junction temperature exceeds T_J = +160°C, the thermal sensor generate a logic signal to turn off the pass element and let IC to cool. When the IC's junction temperature cools by 20°C, the thermal sensor will turn the pass element on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of fault conditions.

Operating Region and Power Dissipation

The thermal resistance of the case and circuit board, ambient and junction air temperature, and the rate of air flow all control the APL5312's maximum power dissipation. The power dissipation across the device is $P = I_{OUT} (V_{IN}-V_{OUT})$. The maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / (\theta_{JC} + \theta_{CA})$$

$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

where $T_J - T_A$ is the temperature difference between the junction and ambient air.

θ_{JC} is the thermal resistance of the package, θ_{CA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air, θ_{JA} = is the thermal resistance between Junction and ambient air. For continual operation, do not exceed the absolute maximum junction Temperature rating of T_J = 125°C.

For example:

The SOT23-5 package has maximum power dissipation 300mW at T_A = 55°C, relatively 225mW at SC70-5 package (see the Figure Maximum Power Dissipation vs. Ambient Temperature).

V_{IN} = 5V, I_{OUT} = 250mA, V_{OUT} = 3.3V,

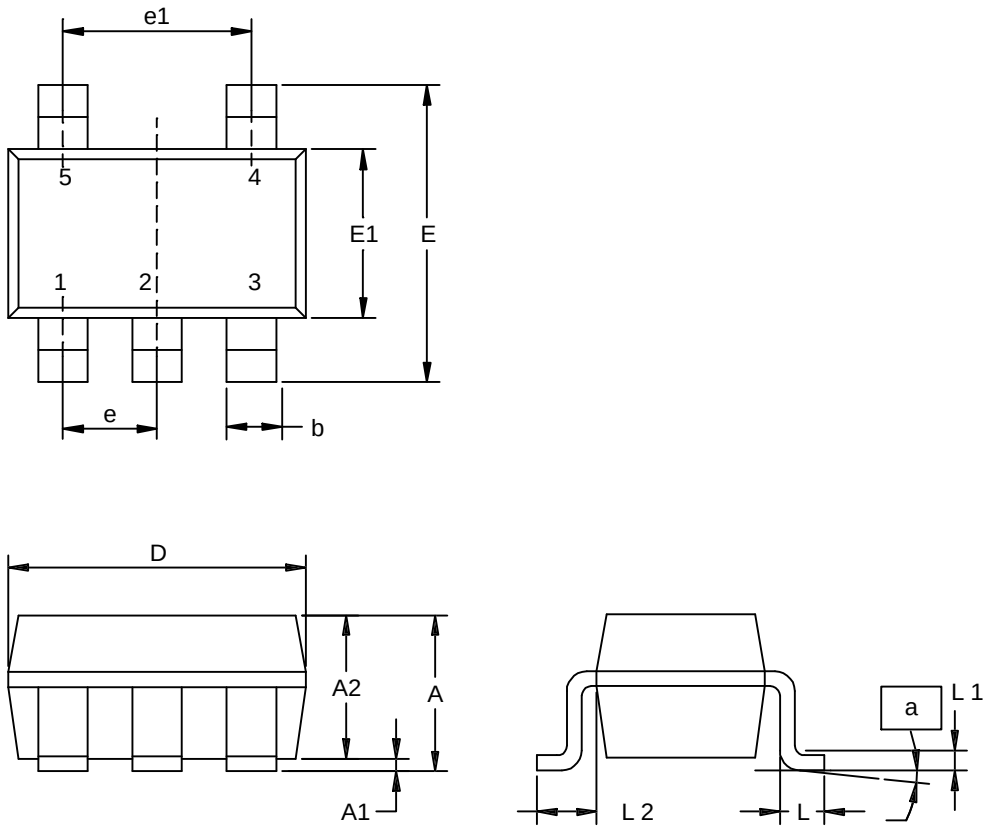
P_D = (5-3.3)V x 150mA = 255mW

According the power dissipation issue, we should adapt the SOT23-5 package. It could reduce the thermal resistance to maintain the IC longer life.

The GND pin provides an electrical connection to ground and channeling heat away. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into ambient air.

Packaging Information

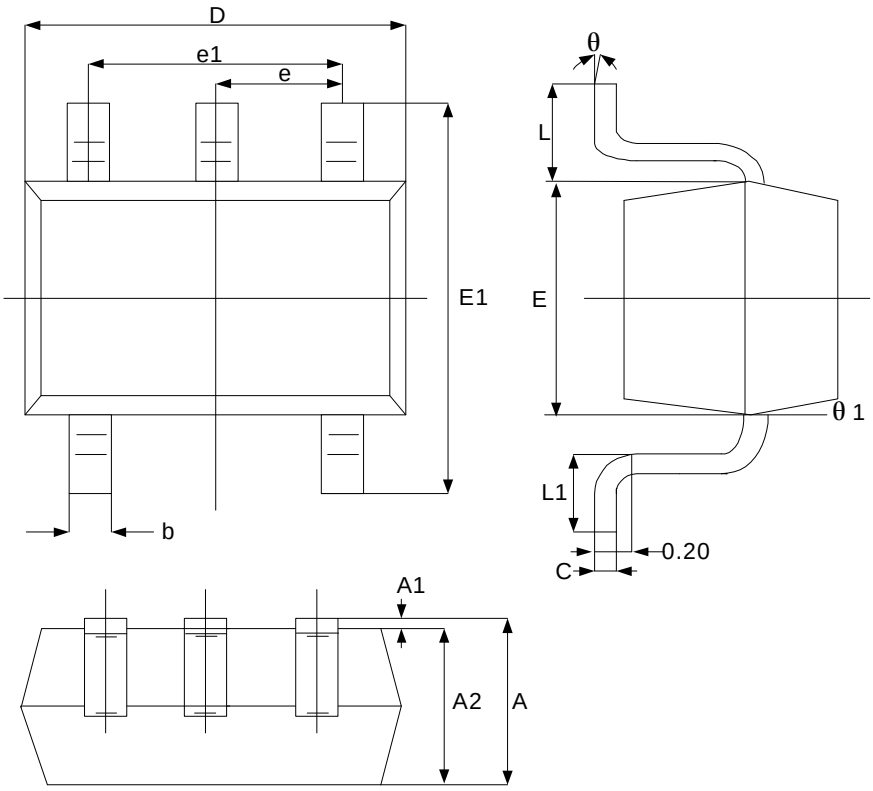
SOT-23-5



Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.95	1.45	0.037	0.057
A1	0.05	0.15	0.002	0.006
A2	0.90	1.30	0.035	0.051
b	0.35	0.55	0.0138	0.0217
D	2.8	3.00	0.110	0.118
E	2.6	3.00	0.102	0.118
E1	1.5	1.70	0.059	0.067
e	0.95		0.037	
e1	1.90		0.075	
L	0.35	0.55	0.014	0.022
L1	0.20 BSC		0.008 BSC	
L2	0.5	0.7	0.020	0.028
a	0°	10°	0°	10°

Packaging Information

SC70-5

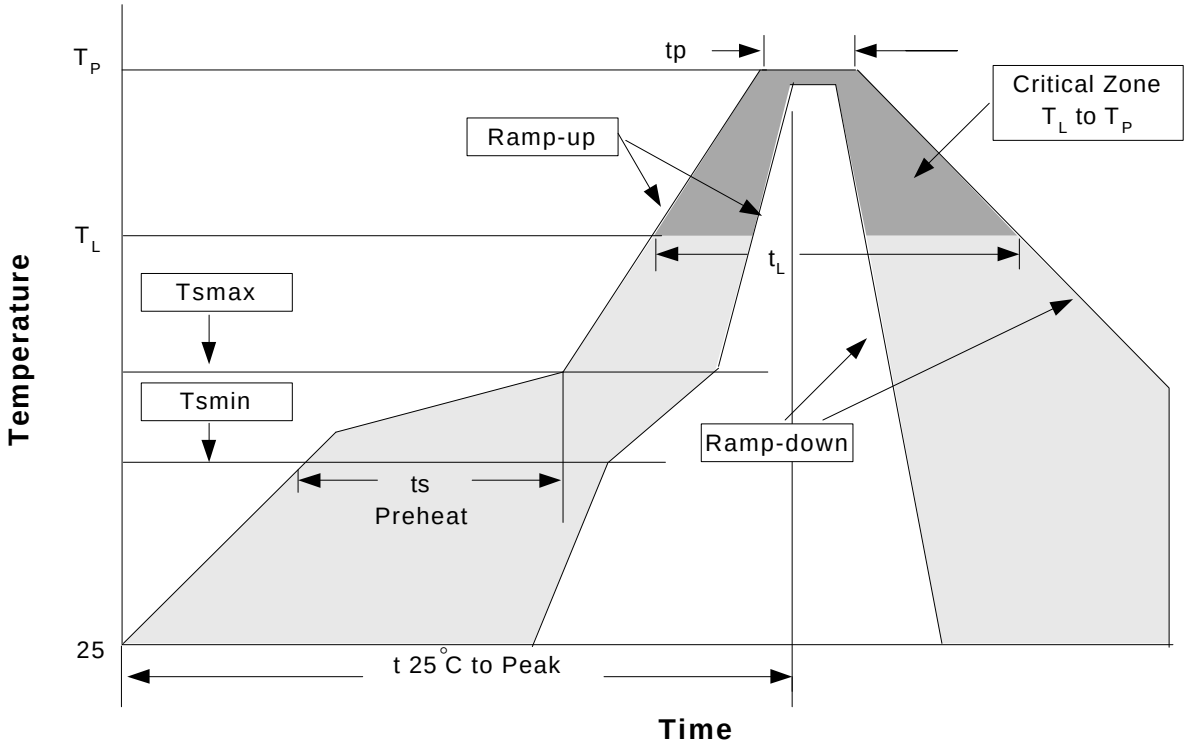


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.80	1.10	0.031	0.043
A1	0.00	0.10	0.000	0.004
A2	0.80	1.00	0.031	0.039
b	0.15	0.30	0.008	0.012
c	0.08	0.25	0.003	0.010
D	1.90	2.15	0.074	0.084
E	1.15	1.35	0.045	0.053
E1	2.00	2.20	0.078	0.086
e	0.65TYP		0.026TYP	
e1	1.20	1.40	0.047	0.055
L	0.53REF		0.021PEF	
L1	0.26	0.46	0.010	0.018
θ	0°	8°	0°	8°
θ1	4°	10°	4°	10°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles(Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

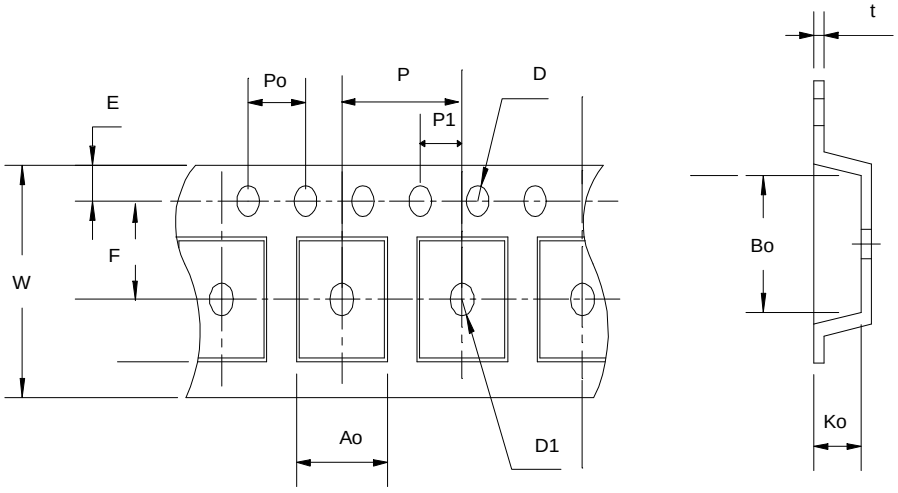
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

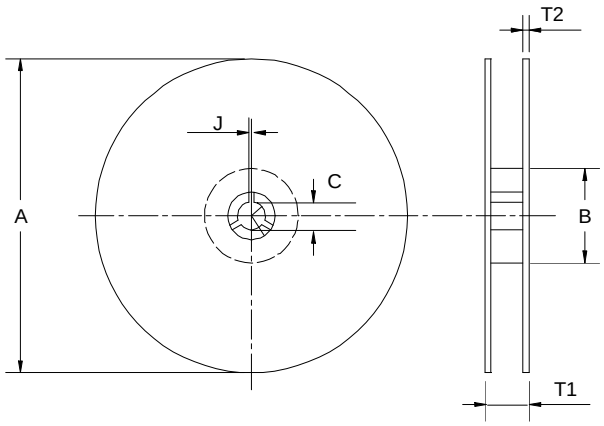
Reliability Test Program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C, 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @125°C
PCT	JESD-22-B,A102	168 Hrs, 100%RH, 121°C
TST	MIL-STD-883D-1011.9	-65°C~150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms, 1_{tr} > 100mA

Carrier Tape



Carrier Tape (Cont.)



Application	A	B	C	J	T1	T2	W	P	E
SOT23-5	178±1	72 ± 1.0	13.0 + 0.2	2.5 ± 0.15	8.4 ± 2	1.5± 0.3	8.0+ 0.3 - 0.3	4 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	3.5 ± 0.05	1.5 +0.1	1.5 +0.1	4.0 ± 0.1	2.0 ± 0.1	3.15 ± 0.1	3.2± 0.1	1.4± 0.1	0.2±0.03
Application	A	B	C	J	T1	T2	W	P	E
SC70-5	178±1	14.4 ± 0.4	13.0 + 0.2	1.15 ± 0.1	12. ±0.2	2.8± 0.2	8.0+ 0.3 - 0.1	4 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	3.5 ± 0.05	1.55± 0.05	1.00 +0.25	4.0 ± 0.1	2.0 ± 0.05	2.4 ± 0.1	2.4± 0.1	1.19± 0.1	0.25±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOT23-5	8	5.3	3000
SC70-5	8	5.3	3000

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