Low Power Microcontroller with 300kHz RC Oscillator

Features

- Low Power - typical 4.0µA active mode
  - typical 2.5µA standby mode
  - typical 0.3µA sleep mode
  @ 1.8V, 32kHz, 25 °C
- Low Voltage - 1.8 to 5.5V
- RC oscillator 30 - 300kHz
- buzzer - three tone
- ROM - 2k × 16 (Mask Programmed)
- RAM - 96 × 4 (User Read/Write)
- 2 clocks per instruction cycle
- RISC architecture
- 4 software configurable 4-bit ports
- Up to 16 inputs (4 ports)
- Up to 12 outputs (3 ports)
- Serial (Output) Write buffer - SWB
- Voltage level detection
- Analogue watchdog
- Timer watchdog
- 8 bit timer / event counter
- Internal interrupt sources (timer, event counter, prescaler)
- External interrupt sources (portA + portC)

Description

The EM6605 series is an advanced single chip low cost, mask programmed CMOS 4-bit microcontroller. It contains ROM, RAM, watchdog timer, oscillation detection circuit, combined timer / event counter, prescaler, voltage level detector and a number of clock functions. Its low voltage and low power operation make it the most suitable controller for battery, stand alone and mobile equipment. The EM66XX series is manufactured using EM Microelectronic's Advanced Low Power CMOS Process.

Typical Applications

- sensor interfaces
- domestic appliances
- security systems
- automotive controls
- TV & audio remote controls
- measurement equipment
- R/F and IR. control

Figure 1.Architecture

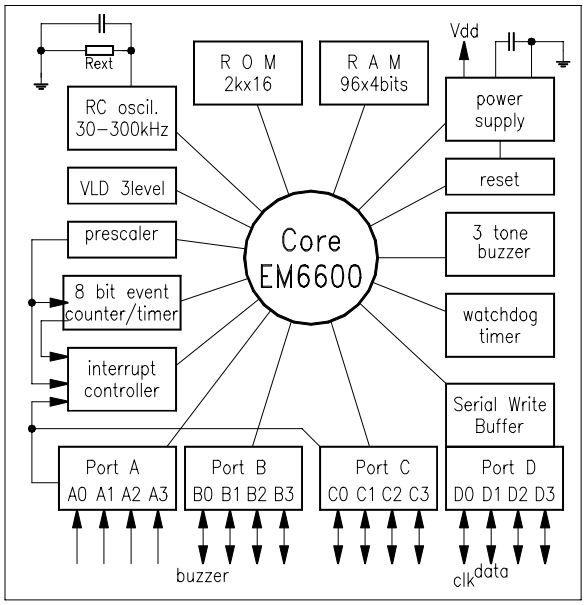
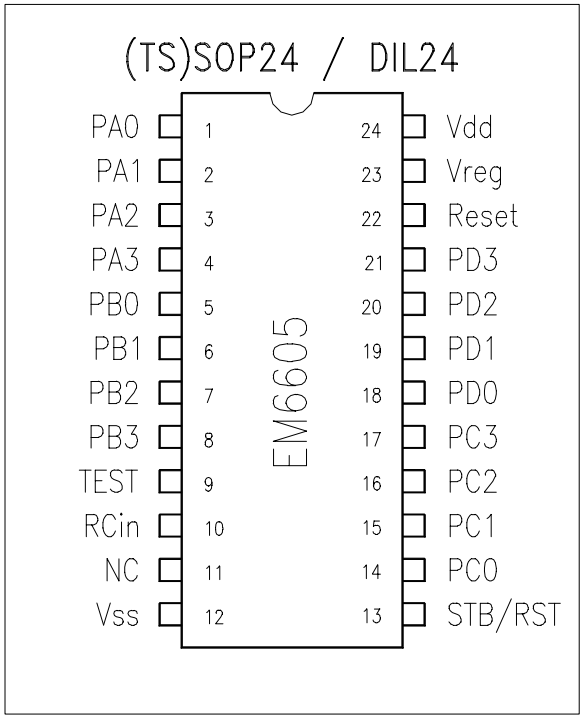


Figure 2.Pin Configuration



EM6605 at a glance

- **Power Supply**

- Low Voltage, low power architecture including internal voltage regulator
- 1.8V ... 5.5 V battery voltage
- 4.0□A in active mode
- 2.5□A in standby mode
- 0.3□A in sleep mode

@ 1.8V, 32kHz, 25 °C

- RC oscillator from 30-300kHz

- **RAM**

- 96 x 4 bit, direct addressable

- **ROM**

- 2048 x 16 bit metal mask programmable

- **CPU**

- 4 bit RISC architecture
- 2 clock cycles per instruction
- 72 basic instructions

- **Main Operating Modes and Resets**

- Active mode (CPU is running)
- Standby mode (CPU in Halt)
- Sleep mode (No clock, Reset State)
- Initial reset on Power-On (POR)
- External reset pin
- Watchdog timer (time-out) reset
- Oscillation detection watchdog reset
- Reset with input combination on PortA (metal option)

- **Supply Voltage Level Detector**

- 3 software selectable levels defined by user between 1.9V and 4.5V)
- Busy flag during measure
- Active only on request during measurement to reduce power consumption

- **4-Bit Input PortA**

- Direct input read
- Debounced or direct input selectable (reg.)
- Interrupt request on input's rising or falling edge, selectable by register.
- Pull-down or none, selectable by met. mask
- Software test variables for conditional jumps
- PA3 input for the event counter
- Reset with input combination on PortA (metal option)

- **4-Bit Input/Output PortB**

- separate input or output selection by register
- Pull-up, Pull-down or none, selectable by metal mask if used as Input
- Buzzer output on PB0

- **4-Bit Input/Output PortC**

- Input or Output port as a whole port
- Debounced or direct input selectable (reg.)
- Interrupt request on input's rising or falling edge, selectable by register.
- Pull-up, pull-down or none, selectable by metal mask if used as input
- CMOS or N-channel open drain mode

- **4-Bit Input/Output PortD**

- Input or Output port as a whole port
- Pull-up, Pull-down or none, selectable by metal mask if used as Input
- CMOS or N-channel open drain mode
- Serial Write Buffer clock and data output

- **Serial (output) Write Buffer**

- max. 256 bits long clocked with ck[15]/ck[14]/ck[12]/ck[11] = 16/8/2/1kHz
- automatic send mode
- interactive send mode : interrupt request when buffer is empty

- **RCoscillator**

- RC oscillator with an external resistor for frequency adjustment in range from 30kHz to 300kHz
- Production tolerance ±20%
- Temperature toll. ±5%, -20°C<T<70°C

- **Buzzer Output**

- if used output on PB0
- 3 tone buzzer - 1kHz, 2kHz, 2.66kHz @32kHz

- **Prescaler**

- 15 stage system clock divider down to 1 Hz
- 3 interrupt requests : 1Hz/8Hz/32Hz
- Prescaler reset ck[14]-ck[1] (from 8kHz-1Hz)

- **8-bit Timer / Event Counter**

- 8-bit auto-reload count-down timer
- 6 different clocks from prescaler
- or event counter from the PA3 input
- parallel load
- interrupt request when comes to 00 hex.

- **Interrupt Controller**

- 4 external interrupt sources from PortA
- 3 internal interrupt sources, prescaler, timer and Serial Write Buffer
- each interrupt request is individually maskable
- interrupt request flag is cleared automatically on register read

NOTE: All frequencies on this page are related to 32.7kHz typical system clock

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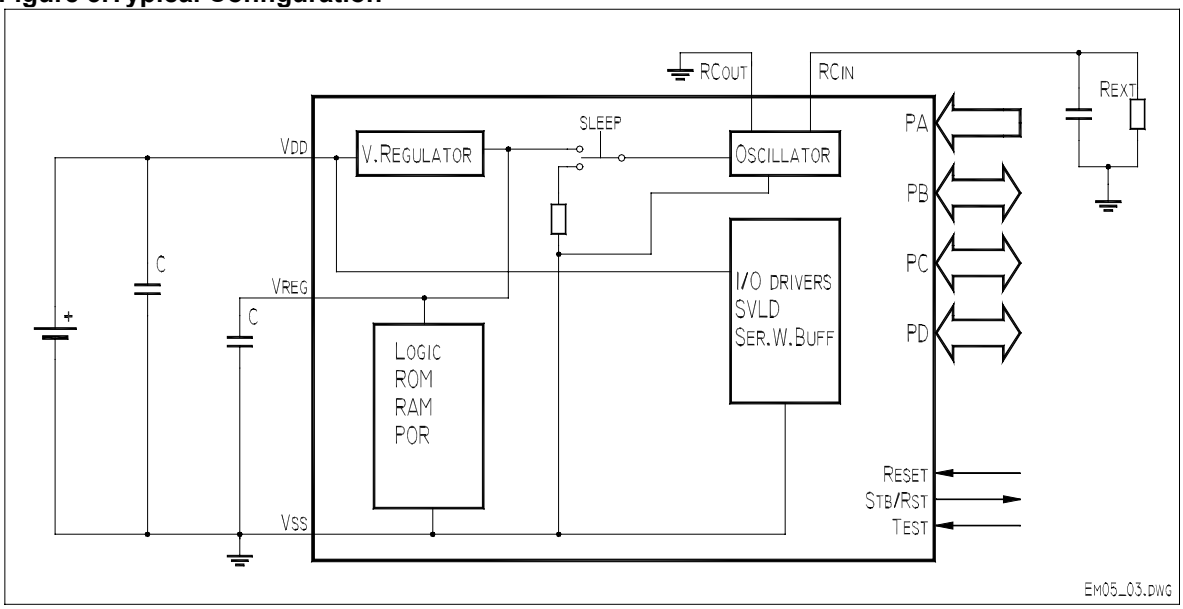
Table 1. Pin Description

Pin Number	Pin Name	Function	Remarks
1	port A, 0	input 0 port A	interrupt request; tvar 1
2	port A, 1	input 1 port A	interrupt request; tvar 2
3	port A, 2	input 2 port A	interrupt request; tvar 3
4	port A, 3	input 3 port A	interrupt request; event counter input
5	port B, 0	input / output 0 port B	buzzer output
6	port B, 1	input / output 1 port B	
7	port B, 2	input / output 2 port B	
8	port B, 3	input / output 3 port B	
9	test	test input terminal	for EM test purpose only
10*	RCin	RC external resistor	typically 120kOhm - 330kOhm
11	RCout/NC	RC output frequency	connect it at Vss - Ground
12	Vss	negative power supply terminal	
13	STB/RST	strobe / reset status	µC reset state + port B, C, D, write
14	port C, 0	input / output 0 port C	interrupt request
15	port C, 1	input / output 1 port C	interrupt request
16	port C, 2	input / output 2 port C	interrupt request
17	port C, 3	input / output 3 port C	interrupt request
18	port D, 0	input / output 0 port D	SWB Serial Clock Output
19	port D, 1	input / output 1 port D	SWB Serial Data Output
20	port D, 2	input / output 2 port D	
21	port D, 3	input / output 3 port D	
22	reset	reset terminal	Active high (internal pull-down)
23	Vreg	internal voltage regulator	Needs typ. 100nF capacitor tw. Vss
24	Vdd	positive power supply terminal	

Figure 3.Typical Configuration



- **RCin node is hi impedance node and the connection towards Rext to fix the frequency should be as short as possible. Treat this node as Quartz node.**

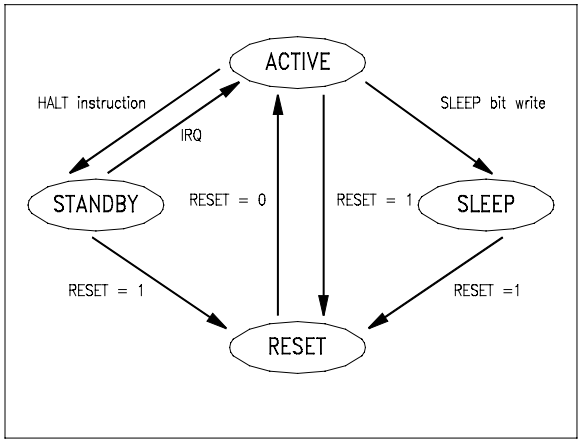
For Vdd less then 2.0V it is recommended that Vdd is connected directly to Vreg

For Vdd>2.2V then the configuration shown in Fig.3 should be used.

1.Operating modes

The EM6605 has two low power dissipation modes: STANDBY and SLEEP. Figure 4 is a transition diagram for these modes.

Figure 4.Mode Transition diagram



1.1.STANDBY Mode

Executing a HALT instruction puts the EM6605 into STANDBY mode. The voltage regulator, oscillator, Watchdog timer, interrupts and timer/event counter are operating. However, the CPU stops since the clock related to instruction execution stops. Registers, RAM, and I/O pins retain their states prior to STANDBY mode. STANDBY is cancelled by a RESET or an Interrupt request if enabled.

Table 2 **:** shows the state of the EM6605 functions in STANDBY and SLEEP modes.

Table 2.StandBy and Sleep Activities

FUNCTION	STANDBY	SLEEP
Oscillator	Active	Stopped
Instruction Execution	Stopped	Stopped
Registers and Flags	Retained	Reset
Interrupt Functions	Active	Stopped
RAM	Retained	Retained
Timer/Counter	Active	Stopped
Watchdog	Active	Stopped
I/O pins	Active	High-Z or Retained
Supply VLD	Stopped	Stopped
Reset pin	Active	Active

1.2.SLEEP Mode

Writing to the **SLEEP** bit in the **IntRq** register puts the EM6605 in SLEEP mode. The oscillator stops and most functions of the EM6605 are inactive. To be able to write the **SLEEP** bit, the **SLmask** bit must first be set to 1. In SLEEP mode only the voltage regulator and RESET input are active. The RAM data integrity is maintained. SLEEP mode may be cancelled only by a RESET at the terminal pin of the EM6605. The RESET must be high for at least 2µsec.

Due to the cold start characteristics of the oscillator, waking up from SLEEP mode may take some time to guarantee that the oscillator has started correctly. During this time the circuit is in RESET and the strobe output STB/RST is high. Waking up from SLEEP mode clears the **SLEEP** flag but not the **SLmask** bit. By reading **SLmask** one can therefore determine if the EM6605 was powered up (**SLmask** = 0), or woken from SLEEP mode (**SLmask** = 1).

2.Power Supply

The EM6605 is supplied by a single external power supply between Vdd and Vss, the circuit reference being at Vss (ground). A built-in voltage regulator generates Vreg providing regulated voltage for the oscillator and internal logic. Output drivers are supplied directly from the external supply Vdd. A typical connection configuration is shown in Figure 3.

For Vdd less then 2.0V it is recommended that Vdd is connected directly to Vreg

For Vdd>2.2V then the configuration shown in Fig.3 should be used.

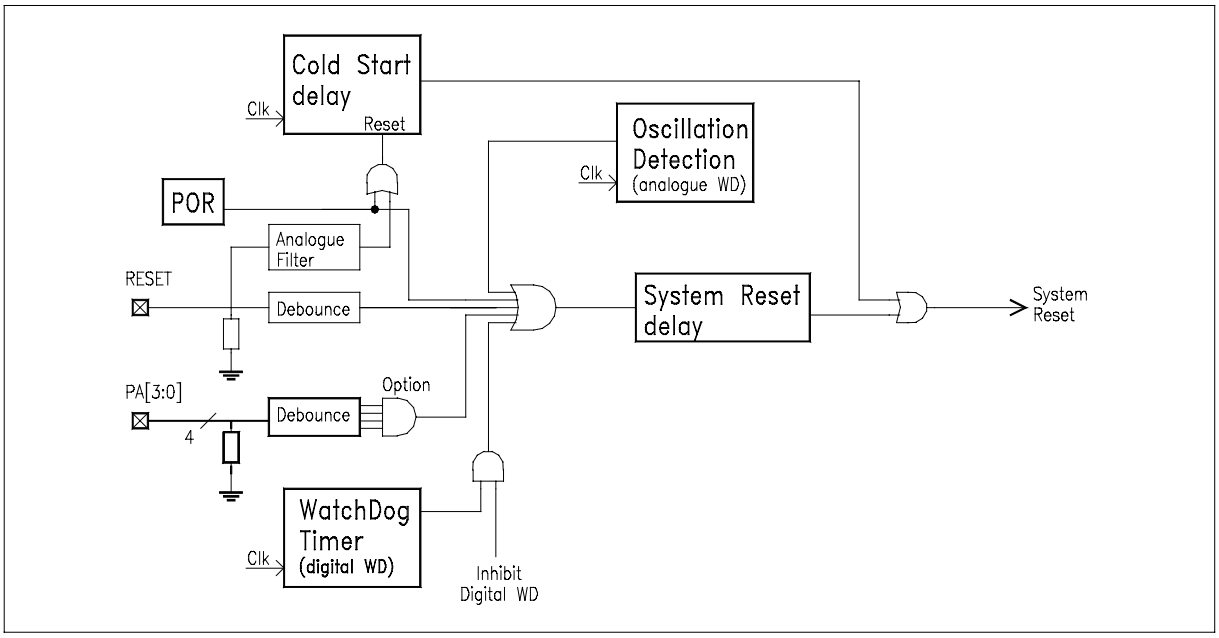
3. Reset

To initialise the EM6605, a system RESET must be executed. There are four methods of doing this:

(1) Initial RESET from the oscillation detection circuit.
(2) External RESET from the RESET PIN.
(3) External RESET by simultaneous high input to terminals PA0..PA3.
(Combinations defined by metal option)
(4) Watchdog RESET (software option).

During any of these RESET's the STB/RST output pin is high.

Figure 5.System reset generation



3.1.Oscillation detection circuit

At power on, the built-in voltage regulator starts to follow the supply voltage until Vdd becomes higher than Vreg. Since it is Vreg which supplies the oscillator and this needs time to stabilise, Power-On-Reset with the oscillation detection circuit therefore counts the first 64 or 128 oscillator clocks after power-on and holds the system in RESET. The system will consequently remain in RESET during Cold Start time - tCoSt (see table 6) for at least 2msec or 4msec second after power up from the 32kHz clock ***(*f1)*** - see Table 6 for frequencies.

After power up the Analogue Watchdog circuit monitors the oscillator. If it stops for any reason other then SLEEP mode, then a RESET is generated and the STB/RES pin is driven high.

3.2.Reset Pin

During active or STANDBY mode the RESET terminal has a debouncer to reject noise and therefore must be active high for at least 2ms = tdebS / 16ms = tdebL ***(*f1)*** (CLK = 32kHz) - software selectable by **DebCK** in **CIRQD** register. (see / Table 32)

At power on, or when cancelling SLEEP mode, the debouncer is not active and so RESET must satisfy the filter time constant (typ. 1µsec) such that the RESET must be active high for at least 2µsec.

3.3.Input port (PA0..PA3) RESET

With a mask option it is possible to choose from four PortA reset combinations. The selected ports must be simultaneously high for at least 2ms = tdebS / 16ms = tdebL **(*f1)** (CLK = 32kHz) due to the presence of debouncers. Note also, that RESET with port A is not possible during SLEEP mode.

Below are the combinations of Port A (PA0..PA3) inputs which can be used to generate a RESET. They can be selected by metal « **PortA RESET** » mask option described in chapter 14.

Table 3.PortA Inputs RESET options

	Function	**Opt. Code**
Option A	no inputs RESET	RA0
Option B	RESET = PA0 * PA1	RA1
Option C	RESET = PA0 * PA1 * PA2	RA2
Option D	RESET = PA0 * PA1 * PA2 * PA3	RA3

3.4. Watchdog Timer RESET

The Watchdog Timer RESET is a software option and if used it will generate a RESET if it is not cleared. See section 5. Watchdog timer for details.

Table 4.Watchdog-Timer Option

Watchdog Function	**NoWD** bit in **Option** register
Without Watchdog Time-out reset	1
With Watchdog Time-out reset	0

3.5.CPU State after RESET

RESET initialises the CPU as shown in the Table below.

Table 5.Initial Value After RESET

name	**bits**	**symbol**	**initial value**
Program counter 0	12	PC0	$000 (as a result of Jump 0)
Program counter 1	12	PC1	undefined
Program counter 2	12	PC2	undefined
stack pointer	2	SP	SP(0) selected
index register	7	IX	undefined
Carry flag	1	CY	undefined
Zero flag	1	Z	undefined
HALT	1	HALT	0
Instruction register	16	IR	Jump 0
periphery registers	4		see peripheral memory map

4.Oscillator

A built-in RC oscillator circuit generates the system operating clock ***ck[16]*** for the CPU and peripheral circuits with the help of an externally connected resistor (between RCin and Vss) which determins the frequency and a capacitor for better frequency stability (refer also to chapter 16.2). The oscillator circuit is supplied by the regulated voltage, Vreg. In SLEEP mode the oscillator is stopped.

NOTE: Because the frequency can be selected by the user with an external resistor in a range from 30kHz - 130kHz (LF range) or 100kHz - 330kHz (HF range) (LF or HF range selected by metal option, refer to chapter 14) there is a table of corresponding frequencies for 3 different system clock frequencies. From now on besides each freq. name ***ck[x]*** there will be also an example for 32 768 Hz system clock marked by **(*f1)** to indicate first - lowest frequency.

Table 6. Prescaler clock name definitions and frequency examples

function	Name	frequency 1 (*f1)	frequency 2 (*f2)	frequency 3 (*f3)
system clock	ck[16]	32 768 Hz	131 072 Hz	327 680 Hz
sys. clock / 2	ck[15]	16 348 Hz	65 536 Hz	163 480 Hz
sys. clock / 4	ck[14]	8 192 Hz	32 768 Hz	81 920 Hz
sys. clock / 8	ck[13]	4 096 Hz	16 348 Hz	40 960 Hz
sys. clock / 16	ck[12]	2 048 Hz	8 192 Hz	20 480 Hz
sys. clock / 32	ck[11]	1 024 Hz	4 096 Hz	10 240 Hz
sys. clock / 64	ck[10]	512 Hz	2 048 Hz	5 120 Hz
sys. clock / 128	ck[9]	256 Hz	1 024 Hz	2 560 Hz
sys. clock / 256	ck[8]	128 Hz	512 Hz	1 280 Hz
sys. clock / 512	ck[7]	64 Hz	256 Hz	640 Hz
sys. clock / 1024	ck[6]	32 Hz	128 Hz	320 Hz
sys. clock / 2048	ck[5]	16 Hz	64 Hz	160 Hz
sys. clock / 4096	ck[4]	8 Hz	32 Hz	80 Hz
sys. clock / 8192	ck[3]	4 Hz	16 Hz	40 Hz
sys. clock / 16384	ck[2]	2 Hz	8 Hz	20 Hz
sys. clock / 32768	ck[1]	1 Hz	4 Hz	10 Hz
debouncer - long	tdebL	16 msec	4 msec	1.6 msec
debouncer - short	tdebS	2 msec	0.5 msec	0.2 msec
cold start delay	tCoSt	~ 2 msec	~ 1 msec	~ 0.7 msec
1st buzzer freq.	ck[buz1]	1 024 Hz	4 096 / *512 Hz	10 240/ *1 280 Hz
2nd buzzer freq.	ck[buz2]	2 048 Hz	8 192 / *1 024 Hz	20 480/ *2 560 Hz
3rd buzzer freq.	ck[buz3]	2 667 Hz	10 667 Hz	26 667 Hz

buzzer frequencies for Hi frequency system clock have metal option

4.1.Prescaler

The input to the prescaler is the system clock signal. The prescaler consists of a fifteen element divider chain which delivers clock signals for the peripheral circuits such as the timer/counter, buzzer, I/O debouncers and edge detectors, as well as generating prescaler interrupts.

Table 7.Prescaler interrupt source

Interrupt frequency	PSF1	PSF0
mask(no interrupt)	0	0
ck[1] (1Hz ***f1**)	0	1
ck[4] (8Hz ***f1**)	1	0
ck[6] (32Hz ***f1**)	1	1

The frequency of prescaler interrupts is software selectable, as shown in Table 7

Table 8.Prescaler control register - PRESC

Bit	Name	Reset	R/W	Description
3	**MTim**	0	R/W	Timer/Counter Interrupt Mask
2	**PRST**	-	R/W	Prescaler reset
1	**PSF1**	0	R/W	Prescaler Interrupt select 1
0	**PSF0**	0	R/W	Prescaler Interrupt select 0

5. Watchdog timer

If for any reason the CPU crashes, then the watchdog timer can detect this situation and output a system reset signal. This function can be used to detect program overrun. For normal operation the watchdog timer must be reset periodically by software at least once every three seconds **(*f1)** (CLK = 32kHz) or a system reset signal is generated to CPU and periphery. The watchdog is active during STANDBY. The watchdog reset function can be deactivated by setting the **NoWD** bit to 1 in the **Option** register.

In worst case because of prescaler reset function WD time-out can come down to 2 seconds.

The watchdog timer is reset by writing 1 to the **WDRST** bit. Writing 0 to **WDRST** has no effect.

The watchdog timer also operates in STANDBY mode. It is therefore necessary to reset it if this mode continues for more than three seconds **(*f1)**. One method of doing this is to reset it with the prescaler ck[1] interrupt (1Hz ***f1** such, that the watchdog is reset every second).

Table 9.Watchdog register - WD

Bit	Name	Reset	R/W	Description
3	**WDRST**	-	R/W	Watchdog timer reset
2	**Slmask**	-	R/W	SLEEP mask bit
1	**WD1**	0	R	WD Timer data ck[1]/4 (1/4Hz ***f1**)
0	**WD0**	0	R	WD Timer data ck[1]/2 (1/2 Hz ***f1**)

6.INPUT and OUTPUT ports

The EM6605 has four independent 4-bit ports, as shown in Table 9.

Table 10.Input / Output Ports Overview

Port	Mode	Mask Options	Function(s)
PA(0:3)	Input	Pull-Up/Down (*) Debouncer (*) + or - IRQ edge RESET combination	Input Interrupt Software Test Variable PA3 input for event counter RESET input(s)
PB(0:3)	Individual input or output	Nch open drain output Pull-Up/Down on input	Input or Output PB0 for buzzer output
PC(0:3)	Port input or output	Pull-Up/Down (*) + or - IRQ edge (*) Debouncer Nch open drain output	Input or Output Port Interrupt
PD(0:3)	Port input or Output	Pull-Up/Down on Input Nch open drain output	Input or Output Port PD0 -SWB serial clock output PD1 -SWB serial data output

(*) Some options can be set also by **Option** Register .

Table 11.Option register - Option

Bit	Name	Reset	R/W	Description
3	**IRQedgeR**	0	R/W	Rising edge interrupt for portA&C
2	**debPCN**	0	R/W	PortC without/with debouncer
1	**debPAN**	0	R/W	PortA without/with debouncer
0	**NoWD**	0	R/W	WatchDog timer Off

IRQedgeR - Valid for both PortA and PortC input interrupt edge. At RESET it is cleared to 0 selecting the falling edge at the input as the interrupt source. When set to 1 the rising edge is active. (Option 2 on Fig.6 and Fig.8)

debPAN - by default after reset it is 0 enabling the debouncers on whole portA. Writing it to 1 removes the debouncers from the PortA. (Option 2 on Fig.6)

debPCN - by default after reset it is 0 enabling the debouncers on whole portC. Writing it to 1 removes the debouncers from the PortC. (Option 2 on Fig.8)

NoWD - by default after reset it is 0 = Watchdog timer is On. Writing it to 1 removes the WatchDog timer.

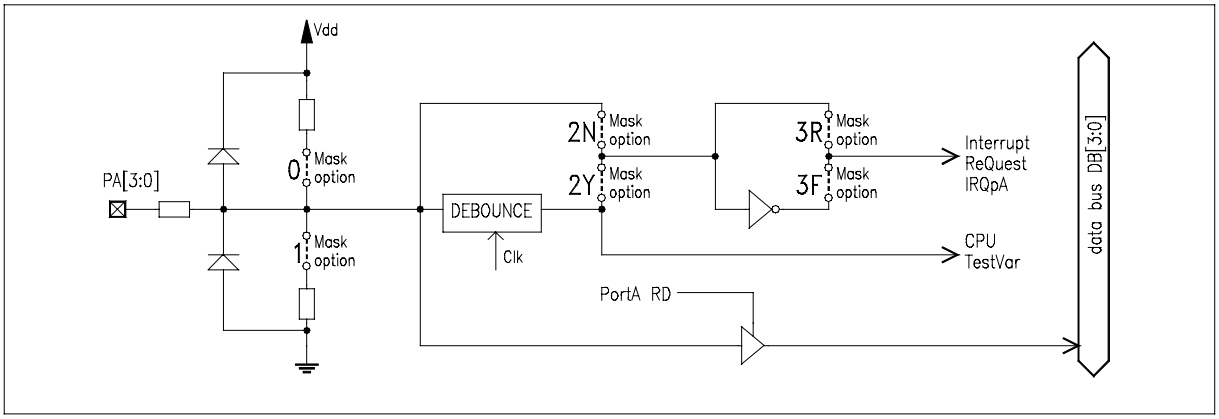
6.1.PortA

The EM6605 has one four bit general purpose input port. Each of the input port terminals PA3..PA0 has an internal Pull-Up/Down resistor which can be selected with mask options. Port information is read directly from the pin into a register.

On inputs PA0, PA1, PA2 and PA3 debouncers for noise rejection are added by default. For interrupt generation, one can choose between either direct input or debounced input. With the **debPAN** bit at 0 in the Option register all the PortA inputs are debounced and with the **debPAN** bit at 1 none of the PortA inputs are debounced. With the debouncer selected the input must be stable during two rising edges of ck[11] or ck[8] clocks (1024Hz or 128Hz **(*f1)** at 32kHz). This corresponds to a worst case of ***t**debS* or ***t**debL* shown in table 6. PortA terminals PA0, PA1 and PA2 are also used as input conditions for conditional software branches as shown on the next page:

Debounced **PA0** is connected to CPU **TestVar1**
Debounced **PA1** is connected to CPU **TestVar2**
Debounced **PA2** is connected to CPU **TestVar3**

Figure 6.Port A



Additionally, PA3 can also be used as the input terminal for the event counter (see section 8).

The input port PA(0:3) also has individually selectable interrupts. Each port has its own interrupt mask bit in the **MPortA** register. When an interrupt occurs inspection of the **IRQpA** and the **IntRq** registers allows the source of the interrupt to be identified. The **IRQpA** register is automatically cleared by a RESET, by reading the register. Reading **IRQpA** register also clears the **INTPA** flag in **IntRq** register. At initial RESET the **MPortA** is set to 0, thus disabling any input interrupts.

See also section 9 for further details about the interrupt controller.

6.2.PortA registers

Table 12.PortA input status register - PortA

Bit	Name	Reset	R/W	Description
3	**PA3**	-	R	PA3 input status
2	**PA2**	-	R	PA2 input status
1	**PA1**	-	R	PA1 input status
0	**PA0**	-	R	PA0 input status

Table 13.PortA Interrupt request register - IRQpA

Bit	Name	Reset	R/W	Description
3	**IRQpa3**	0	R	input PA3 interrupt request flag
2	**IRQpa2**	0	R	input PA2 interrupt request flag
1	**IRQpa1**	0	R	input PA1 interrupt request flag
0	**IRQpa0**	0	R	input PA0 interrupt request flag

Table 14.PortA interrupt mask register - MportA

Bit	Name	Reset	R/W	Description
3	**MPA3**	0	R/W	interrupt mask for input PA3
2	**MPA2**	0	R/W	interrupt mask for input PA2
1	**MPA1**	0	R/W	interrupt mask for input PA1
0	**MPA0**	0	R/W	interrupt mask for input PA0

6.3.PortB

The EM6605 has one four bit general purpose I/O port. Each bit PB(0:3) can be separately configured by software to be either input or output by writing to the corresponding bit of the **CIOPortB** control register. The **PortB** register is used to read data when in input mode and to write data when in output mode. On each terminal Pull-Up/Down resistor can be selected by metal option when input.

Input mode is set by writing 0 to the corresponding bit in the **CIOPortB** register. This results in a high impedance state with the status of the pin being read from register **PortB.** Output mode is set by writing 1 to the corresponding bit in the **CIOPortB** register. Consequently the output terminal follows the status of the bits in the **PortB** register. At initial RESET the **CIOPortB** register is set to 0, thus setting the port to an input. Additionally, PB0 can also be used as a three tone buzzer output. For details see section 7.

6.4.PortB registers

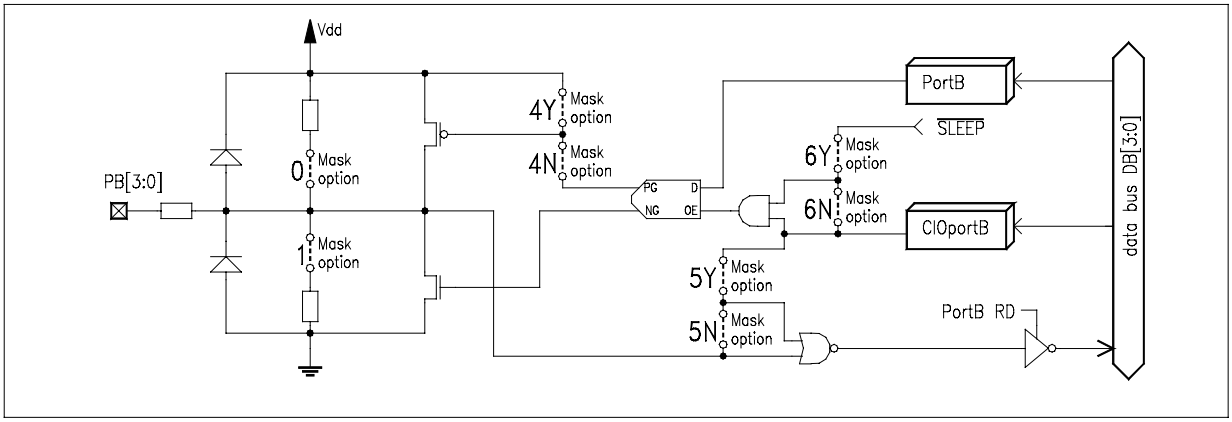
Table 15.PortB input status register - PortB

Bit	Name	Reset	R/W	Description
3	**PB3**	-	R/W	PB3 I/O data
2	**PB2**	-	R /W	PB2 I/O data
1	**PB1**	-	R/W	PB1 I/O data
0	**PB0**	-	R /W	PB0 I/O data

Table 16.PortB Input/Output control register - CIOportB

Bit	Name	Reset	R/W	Description
3	**CIOPB3**	0	R/W	PB3 Input/Output select
2	**CIOPB2**	0	R/W	PB2 Input/Output select
1	**CIOPB1**	0	R/W	PB1 Input/Output select
0	**CIOPB 0**	0	R/W	PB0 Input/Output select

Figure 7.Port B



If metal mask option ***5Y*** (Input blocked when Output) is used and the port is declared as the Output (**CIOPortB** = 1111b) the real port information cannot be read directly. In this case no direct logic operations (like AND **PortB**) on Output ports are possible. This logic operation can be made if an image of the Port saved in the RAM which we store after on the output port. This is valid for PortB, PortC and PortD when declared as output and the metal Option ***5Y*** is used. In the case of metal option **5N** selected direct logic operations on output ports are possible.
If metal mask option ***6Y*** (Output Hi-Z in SLEEP mode) the active Output will go Tristate when the circuit goes into SLEEP mode. In the case of ***6N*** output stay active also in the SLEEP mode.

6.5.PortC

This port can be configured as either input or output (not bitwise selectable). When in input mode it implements the identical interrupt functions as PortA. The **PortC** register is used to read data when input mode and to write data when in output mode. Input mode is set by writing 0 to the I/O control bit **CIOPC** in register **CPIOB** and the input becomes high impedance. On each terminal Pull-Up/Down resistor can be selected by metal option which are active only when selected as input. The output mode is selected by writing 1 to **CIOPC** bit, and the terminal follows the bits in the **PortC** register.

When PortC is used as an input, interrupt functions as described for **PortA** can be enabled. Input to the interrupt logic can be direct or via a debounced input. With the **debPCN** bit at 0 in the Option register all the PortC inputs are debounced and with the **debPCN** bit at 1 none of the PortC inputs are debounced. **MPortC** is the interrupt mask register for this port and **IRQpC** is the portC interrupt request register. See also section 9.

By writing the **PA&C** bit in the **CPIOB** data register it is possible to combine PortA and PortC interrupt requests (logic AND) as shown in Table 16.

At initial reset, the **CPIOC** control register is set to 0, and the port is in input mode. The **MPortC** register is also set to 0, therefore disabling interrupts.

Table 17.Ports A&C Interrupt Request

IRQPA	IRQPC	PA&C	Request to CPU
0	0	X	No
0	1	0	Yes
1	0	0	Yes
1	1	0	Yes
0	1	1	No
1	0	1	No
1	1	1	Yes

6.6.PortC registers

Table 18.PortC input/output register - PortC

Bit	Name	Reset	R/W	Description
3	**PC3**	-	R/W	PC3 I/O data
2	**PC2**	-	R /W	PC2 I/O data
1	**PC1**	-	R/W	PC1 I/O data
0	**PC0**	-	R /W	PC0 I/O data

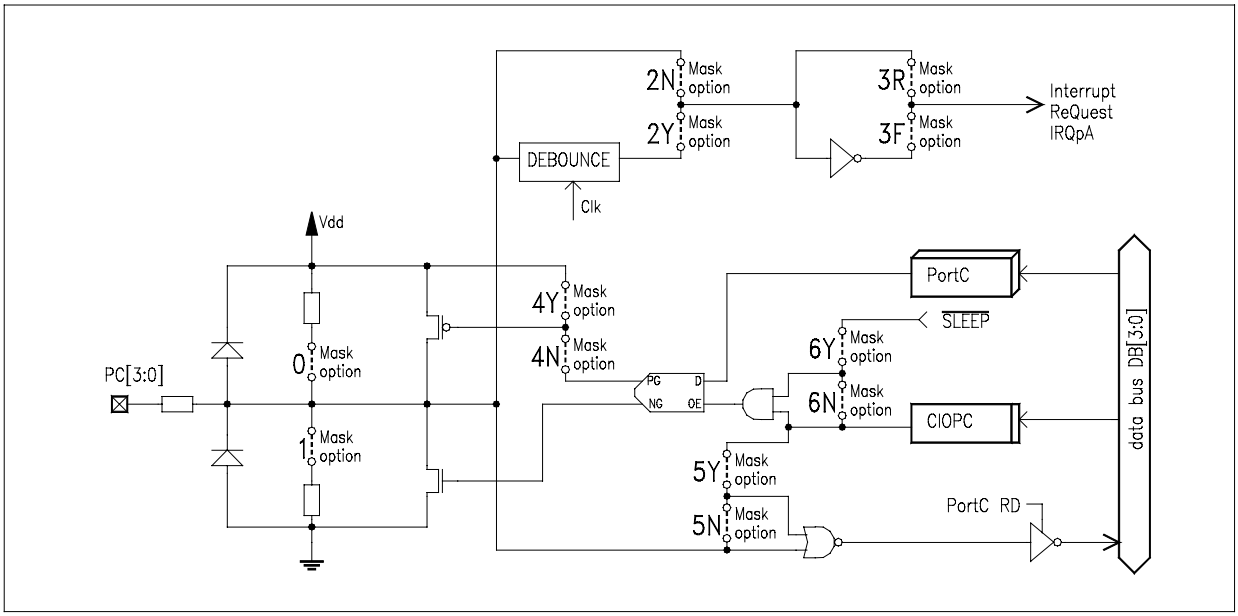
Table 19.PortC Interrupt request register - IRQpC

Bit	Name	Reset	R/W	Description
3	**IRQpc3**	0	R	input PC3 interrupt request flag
2	**IRQpc2**	0	R	input PC2 interrupt request flag
1	**IRQpc1**	0	R	input PC1 interrupt request flag
0	**IRQpc0**	0	R	input PC0 interrupt request flag

Table 20.PortC interrupt mask register - MportC

Bit	Name	Reset	R/W	Description
3	**MPC3**	0	R/W	interrupt mask for input PC3
2	**MPC2**	0	R/W	interrupt mask for input PC2
1	**MPC1**	0	R/W	interrupt mask for input PC1
0	**MPC0**	0	R/W	interrupt mask for input PC0

Figure 8.Port C



For PortC and PortD metal options ***5Y/N*** and ***6Y/N*** are Port-wise (for the whole port).

For PortB these options are bit-wise (every terminal can have individual mask set-up for the options ***5Y/N*** and ***6Y/N***).

6.7.PortD

The EM6605 has one all purpose I/O port similar to PortC but without interrupt capability. The **PortD** register is used to read input data when an input and to write output data for output. The input line can be pulled down (metal option) when the port is used as input. Input mode is set by writing 0 to the I/O control bit **CIOPD** in register **CPIOB**, and the terminal becomes high impedance. On each terminal Pull-Up/Down resistor can be selected by metal option which are active only when selected as input.

Output mode is set by writing 1 to the control bit **CIOPD.** Consequently, the terminal follows the status of the bits in the **PortD** register. If Serial Write Buffer function is enabled PD0 and PD1 terminals of PortD output serial clock and serial data respectively. For details see **11.0 Serial Write Buffer**.

6.8.PortD registers

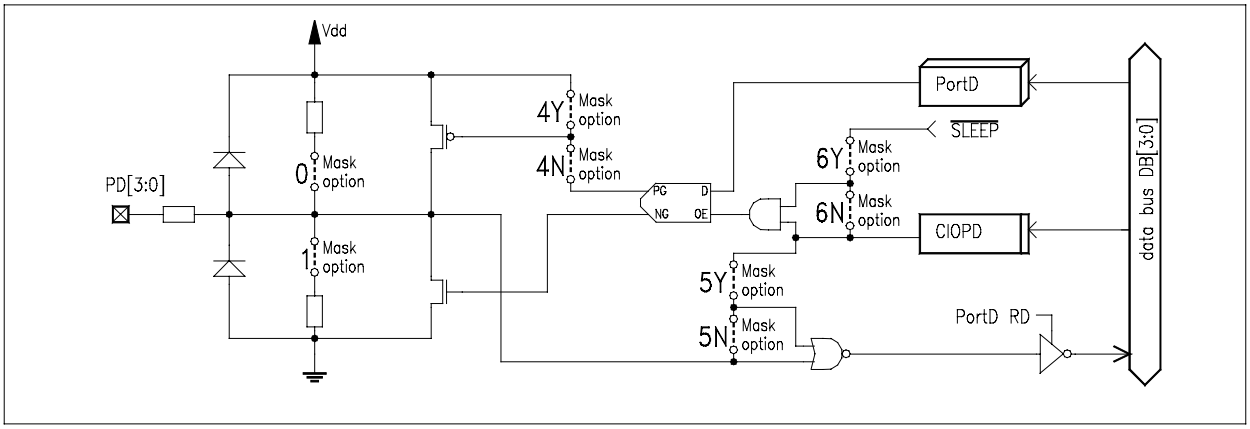
Table 21.PortD Input/Output register - PortD

Bit	Name	Reset	R/W	Description
3	**PD3**	0	R/W	PD3 I/O data
2	**PD2**	0	R/W	PD2 I/O data
1	**PD1**	0	R/W	PD1 I/O data
0	**PD0**	0	R/W	PD0 I/O data

Table 22.Ports control register - CPIOB

Bit	Name	Reset	R/W	Description
3	-	-	R/W	not used
2	**CIOPD**	0	R/W	I/O PortD select
1	**CIOPC**	0	R/W	I/O PortC select
0	**PA&C**	0	R/W	Logical AND of IRQ's from PortA & PortC

Figure 9.Port D



7.BUZZER

The EM6605 has one 50% duty cycle output with three different frequencies which can be used to drive a buzzer. I/O terminal PB0 is used for this function when the buzzer is enabled by setting the **BUen** bit to 1 . Table 23 below shows how to select the frequency by writing to the **BCF1** and **BCF0** control flags in the **BEEP** register.

After writing to the buzzer control register **BEEP,** the chosen frequency (or silence) is selected immediately. With the **BUen** bit set to 1, the selected frequency is output at PB0. When the **BUen** is set to 0 PB0 is used as a normal I/O terminal of PortB. The **BUen** bit has a higher priority over the I/O control bit **CIOPB0** in the **CIOPortB** register.

Table 23.Buzzer frequency selection

Tone frequency	BCF1	BCF0
silence	0	0
ck[buz1] = ck[11] or ck[8] by metal option (1024 Hz ***f1**)	0	1
ck[buz2] = ck[12] or ck[10] by metal option (2048 Hz ***f1**)	1	0
ck[buz3] (2667 Hz ***f1**)	1	1

7.1.Buzzer Register

Table 24.Buzzer control register - BEEP

Bit	Name	Reset	R/W	Description
3	**TimEn**	0	R/W	Timer/counter enable
2	**BUen**	0	R/W	Buzzer enable
1	**BCF1**	0	R/W	Buzzer Frequency control
0	**BCF0**	0	R/W	Buzzer Frequency control

8.Timer/Event Counter

The EM6605 has a built-in 8 bit auto-reload Timer/Event counter that takes an input from either the prescaler or Port PA3. If the Timer/Event counter counts down to $00 the interrupt request flag **INTTE** is set to 1. If the Timer/Event counter interrupt is enabled by setting the mask flag **MTimC** set to 1, then an interrupt request is generated to the CPU. See also section 9. If used as an event counter, pulses from the PA3 terminal are input to the event counter. See figure 10 and tables 29 and 30 on the next page for PA3 source selection (debounced or not, Rising/Falling edge). By default rising and debounced PA3 input is selected.

The timer control register **TimCtr** selects the auto-reload function and input clock source. At initial RESET this bit is cleared to 0 selecting no auto-reload. To enable auto-reload **TimAuto** must be set to 1. The timer/counter can be enabled or disabled by writing to the **TIMen** control bit in the **BEEP** register. At initial RESET it is cleared to 0. When used as timer, it is initialised according to the data written into the timer load/status registers **LTimLS** (low 4 bits) and **HTimLS** (high four bits). The timer starts to count down as soon as the **LTimLS** value is written. When loading the timer/event counter registers the correct order must be respected: First, write either the control register **TimCtr** or the high data nibble **HTimLS.** The last register written should be the low data nibble **LTimLS**. During count down, the timer can always be reloaded with a new value, but the high four bits will only be accepted during the write of the low four bits.

In the case of the auto-reload function, the timer is initialised with the value of the load registers **LTimLS** and **HTimLS**. Counting with the auto-reload function is only enabled during the write to the low four bits, (writing **TEauto** to 1 does not start the timer counting down with the last value in the timer load registers but it waits until a new **LTimLS** load). The timer counting to $00 generates a timer interrupt event and reloads the registers before starting to count down again. To stop the timer at any time, a write of $00 can be made to the timer load registers, this sets the **TimAuto** flag to 0. If the timer is stopped by writing the **TimEn** bit to 0, the timer status can be read. The current timer status can be always obtained by reading the timer registers **LTimLS** and **HTimLS**. For proper operation read ordering should be respected such that the first read should be of the **LTimLS** register followed by the **HTimLS** register. Example: To have continuos 1sec timer IRQ with 128Hz one has to write 128dec (80hex) in Timer registers with auto-reload.

Using the timer/counter as the event counter allows several possibilities:

1.) Firstly, load the number of PA3 input edges expected into the load registers and then generate an interrupt request when counter reaches $00.

2.) The second is to write timer/counter to $FF, then select the event counter mode, and lastly enable the event counter by setting the **TIMen** bit to 1, which starts the count.

Because the counter counts down, a binary complement has to be done in order to get the number of events at the PA3 input.

3) Another option is to use the timer/counter in conjunction with the prescaler interrupt, such that it is possible to count the number of the events during two consecutive ck[6], ck[4], ck[1], (32Hz, 8Hz or 1Hz ***f1**) prescaler interrupts.

Figure 10.Timer / Event Counter

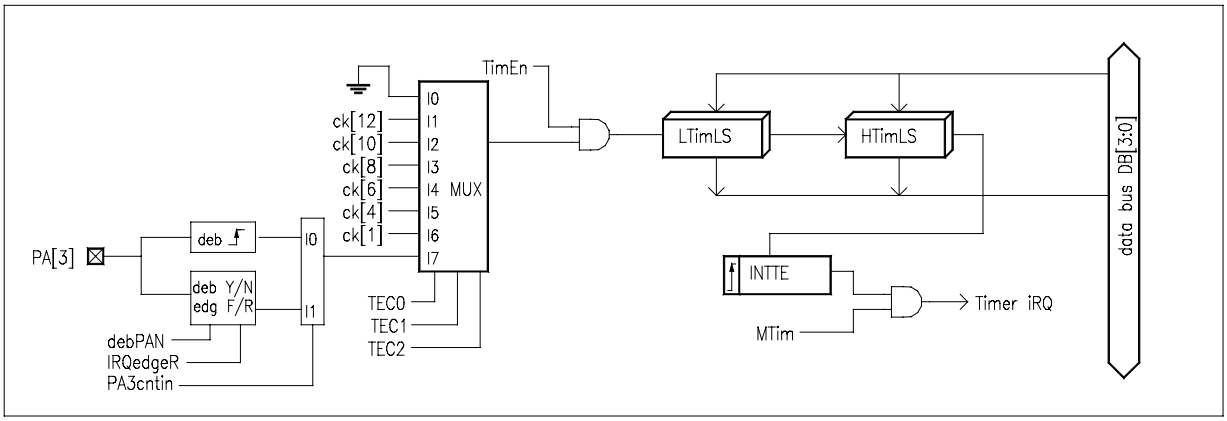


Table 25 shows the selection of inputs to the Timer/Event counter

Table 25.Timer Clock Selection

TEC2	TEC1	TEC0	Timer/Counter clock source
0	0	0	not active
0	0	1	ck[12] from prescaler; (2048 Hz ***f1**)
0	1	0	ck[10] from prescaler; (512 Hz ***f1**)
0	1	1	ck[8] from prescaler; (128 Hz ***f1**)
1	0	0	ck[6] from prescaler; (32 Hz ***f1**)
1	0	1	ck[4] from prescaler; (8 Hz ***f1**)
1	1	0	ck[1] from prescaler; (1 Hz ***f1**)
1	1	1	PA3 input terminal (see tables 29 and 30)

8.1.Timer/Counter registers

Table 26.Timer control register - TimCtr

Bit	Name	Reset	R/W	Description
3	**TimAuto**	0	R/W	Timer/Counter AUTO reload
2	**TEC2**	0	R/W	Timer/Counter mode 2
1	**TEC1**	0	R/W	Timer/Counter mode 1
0	**TEC0**	0	R/W	Timer/Counter mode 0

Table 27.LOW Timer Load/Status register - LTimLS (4 low bits)

Bit	Name	Reset	R/W	Description
3	**TL3/TS3**	0	R/W	Timer load/status bit 3
2	**TL2/TS2**	0	R/W	Timer load/status bit 2
1	**TL1/TS1**	0	R/W	Timer load/status bit 1
0	**TL0/TS0**	0	R/W	Timer load/status bit 0

Table 28.HIGH Timer Load/Status register - HTimLS (4 high bits)

Bit	Name	Reset	R/W	Description
3	**TL7/TS7**	0	R/W	Timer load/status bit 7
2	**TL6/TS6**	0	R/W	Timer load/status bit 6
1	**TL5/TS5**	0	R/W	Timer load/status bit 5
0	**TL4/TS4**	0	R/W	Timer load/status bit 4

Table 29.PA3 counter input selection register - PA3cnt

bit	Name	Reset	R/W	Description
3	-	-	-	empty
2	-	-	-	empty
1	-	-	-	empty
0	**PA3cntin**	0	R/W	PA0 input status

Table 30.PA3 counter input selection

PA3cntin	debPAN	IRQedgeR	Counter source
0	X	X	PA3 debounced rising edge
1	0	0	PA3 debounced falling edge
1	0	1	PA3 debounced rising edge
1	1	0	PA3 not debounced falling edge
1	1	1	PA3 not debounced rising edge

X (Don't care)

9.Interrupt Controller

The EM6605 has six different interrupt sources, each of which is maskable. These are:

External (3)	- PortA PA3..PA0 inputs
	- PortC PC3..PC0 inputs
	- combined AND of PortA * PortC
Internal (3)	- Prescaler ck[6] / ck[4] / ck[1] (32Hz / 8Hz / 1Hz ***f1**)
	- Timer/Event counter
	- SWB in interactive mode

For an interrupt to the CPU to be generated, the interrupt request flag must be set (**INT**xx), and the corresponding mask register bit must be set to 1 (**M**xx), the general interrupt enable flag (**INTEN**) must also be set to 1. The interrupt request can be masked by the corresponding interrupt mask registers **MPortx** for each input interrupt and by PSF0 ,PSF1 and **MTim** for internal interrupts. At initial reset the interrupt mask bits are set to 0. **INTEN** bit is set automatically to 1 by Halt Instruction except when starting the Automatic SWB transfer (see Serial Write Buffer (**SWB**) chapter 11)

The CPU is interrupted when one of the interrupt request flags is set to 1 in register **IntRq** and the **INTEN** bit is enabled in the control register CIRQD. **INTTE** and **INTPR** flags are cleared automatically after a read of the **IntRq** register. The other two interrupt flags **INTPA** (IRQ from PortA) and **INTPC** (IRQ from PortC) in **IntRq** register are cleared only after reading the corresponding Port interrupt request registers I**RQpA** and **IRQpC**. At the Power on reset and in SLEEP mode the **INTEN** bit is also set to 0 therefore not allowing any interrupt requests to the CPU until it is set to 1 by software.

Since the CPU has only one interrupt subroutine and because the **IntRq** register is cleared after reading, the CPU does not miss any of the interrupt requests which come during the interrupt service routine. If any occur during this time a new interrupt will be generated as soon as the CPU comes out of the current interrupt subroutine. Interrupt priority can be controlled through software by deciding which flag in the **IntRq** register should be serviced first.

For SWB interactive mode interrupt see section 11.0 Serial Write Buffer.

9.1.Interrupt control registers

Table 31.Main Interrupt request register - IntRq (Read Only)*

Bit	Name	Reset	R/W	Description
3	**INTPR**	0	R	Prescaler interrupt request
2	**INTTE**	0	R	Timer/counter interrupt request
1	**INTPC**	0	R	PortC Interrupt request
0	**INTPA**	0	R	PortA Interrupt request
2	**SLEEP**	0	W*	SLEEP mode flag

* Write bit 2 only if **SImask**=1

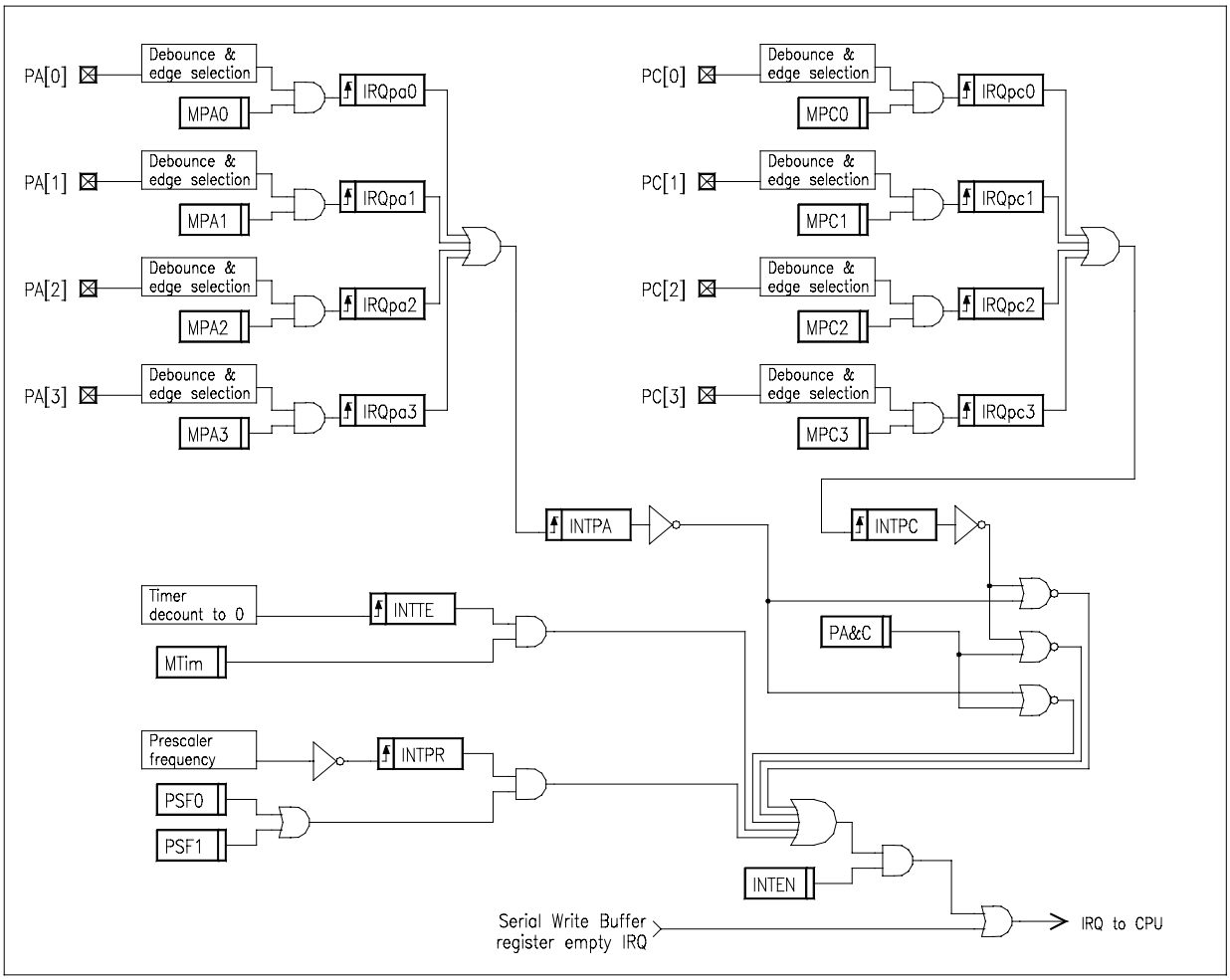
If the **SLEEP** flag is written with 1 then the EM6603 goes immediately into SLEEP mode (**SLmask** was at 1).

Table 32.register - CIRQD

Bit	Name	Reset	R/W	Description
3	RESERVED	-	-	-
2	RESERVED	-	-	-
1	**DebCK**	0	R/W	Debouncer clock select (0=tdebS : 1=tdebL) *
0	**INTEN**	0	R/W	Enable interrupt to CPU (1=enabled)

* see table 6

Figure 11.Interrupt Request generation



MTim — IRQ mask bit which can be written to 0 or 1 (1 to enable an interrupt)

INTTE — interrupt request flag which is set on the input rising edge

Timer IRQ flag **INTTE** and prescaler IRQ flag **INTPR** arrive independent of their mask bits not to loose any timing information. But the processor will be interrupted only with mask set to 1.

10.Supply Voltage Level Detector (SVLD)

The EM6605 has a software configurable built-in supply voltage level detector. Three levels can be defined between VDDmin + 100mV and VDDmax - 1000mV in steps of 100mV. During SLEEP mode this function is disabled.

The required voltage compare level is selected by writing the bits **VLC1** and **VLC2** in the **SVLD** control register which also activates the compare measurement. Since the measurement is not immediate the busy flag remains high during the measurement and is automatically cleared low when the measurement is finished. The result is indicated by inspection of the VLDR flag. If the result is 0 then the voltage level is higher than the selected compare level. And if 1 is lower than the compare level.

The result **VLDR** of the last measurement remains until the new one is started. The start of a new measurement resets the **VLDR** (SVLD result bit) to 0.

During the SVLD operation power consumption increases by approximately 3□A during one period of ck[9] (~3.9msec with ***f1**). The measurement internally starts with the rising ck[9] edge following the SVLD test command. The additional SVLD consumption stops after the falling edge of the ck[9] internal clock.

Table 33 lists the possible voltage levels

Table 33.SVLD level selection

Evaluation voltage	VLC1	VLC0
not active	0	0
VL1 (low level)	0	1
VL2	1	0
VL3 (high level)	1	1

10.1.SVLD register

Table 34.SVLD control register - SVLD

Bit	Name	Reset	R/W	Description
3	**VLDR**	0	R	SVLD result (0=higher 1=lower)
2	**busy**	0	R	measurement in progress
1	**VLC1**	0	R/W	SVLD level control 1
0	**VLC0**	0	R/W	SVLD level control 0

11.Serial (Output) Write Buffer - SWB

The EM6605 has simple Serial Write Buffer (**SWB**) which outputs serial data and serial clock.

The SWB is enabled by setting the bit **V03** in the **CLKSWB** register as well as setting port D to output mode. The combination of the possible PortD mode is shown in Table 357. In SWB mode the serial clock is output on port D0 and the serial data is output on port D1.

The signal TestVar[3], which is used by the processor to make conditional jumps, indicates "Transmission finished" in automatic send mode or "SWBbuffer empty" in interactive send mode. In interactive mode, TestVar[3] is equivalent to the interrupt request flags stored in **IntRq** register : it permits to recognize the interrupt source. (See also the interrupt handling section 9.Interrupt Controller for further information). To serve the "SWBbuffer empty " interrupt request, one only has to make a conditional jump on TestVar[3].

The Serial Write Buffer output clock frequency is selected by bits **ClkSWB0** and **ClkSWB1** in the **ClkSWB** register. The possible values are 1kHz (default), 2kHz, 8kHz or 16kHz and are shown in Table 35.

Table 36.SWB clock selection

SWB clock output	CkSWB1	CkSWB0
ck[11]; (= 1 024 Hz ***f1**)	0	0
ck[12]; (= 2 048 Hz ***f1**)	0	1
ck[14]; (= 8 192 Hz ***f1**)	1	0
ck[15]; (= 16 348 Hz ***f1**)	1	1

Table 376.SWB clock selection register - ClkSWB

Bit	Name	Reset	R/W	Description
3	**V03**	0	R/W	Serial Write buffer selection
2	-	0	R	RESERVED - read 0
1	**CkSWB1**	0	R/W	SWB clock selector 1
0	**CkSWB0**	0	R/W	SWB clock selector 0

Table 387.PortD status

PortD status	CIOPD	V03	PD0	PD1	PD2	PD3
« NORMAL »	0	0	input	input	input	input
« NORMAL »	0	1	input	input	input	input
« NORMAL »	1	0	output PD0	output PD1	output PD2	output PD3
« SWB »	1	1	serial clock Out	SWB serial data	output PD2	output PD3

When the SWB is enabled by setting the bit **V03** TestVar[3], which is used to make conditional jumps, is reassigned to the SWB and indicates either "SWBbuffer empty " interrupt or "Transmission finished" . After Power-on-RESET **V03** is cleared at "0" and TestVar[3] is consequently assigned to PA2 input terminal.

The SWB data is output on the rising edge of the clock. Consequently, on the receiver side the serial data can be evaluated on falling edge of the serial clock edge.

Figure 12.Serial write buffer

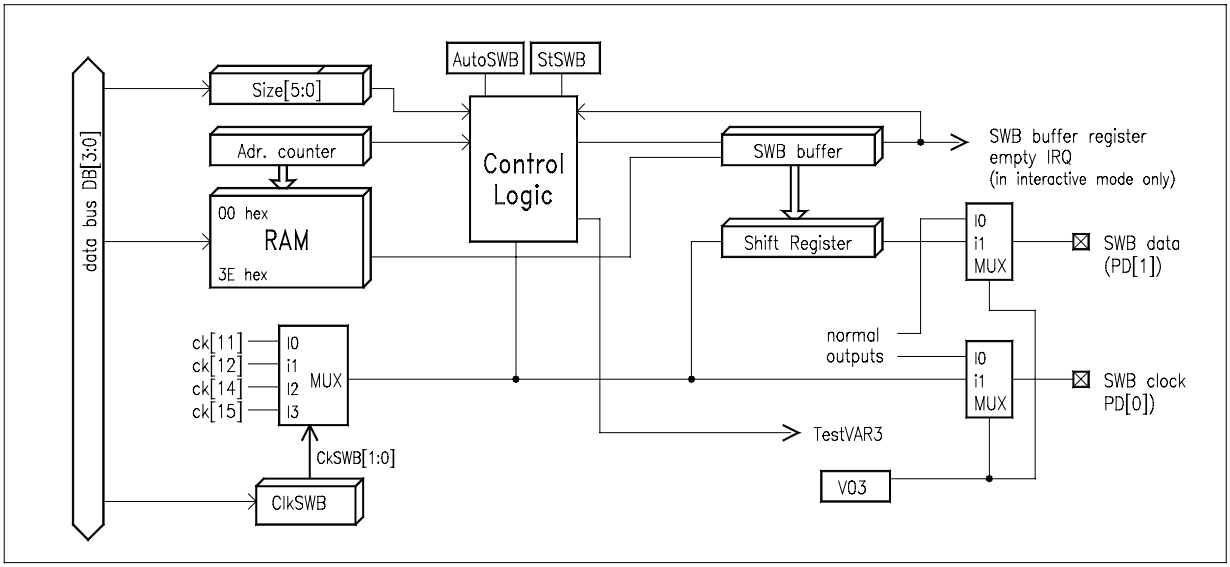


Table 39.SWB buffer register - SWbuff

Bit	Name	Reset	R/W	Description
3	**Buff3**	1	R/W	SWB buffer D3
2	**Buff2**	1	R/W	SWB buffer D2
1	**Buff1**	1	R/W	SWB buffer D1
0	**Buff0**	1	R/W	SWB buffer D0

Table 40.SWB Low size register - LowSWB

Bit	Name	Reset	R/W	Description
3	**Size[3]**	0	R/W	Auto mode buffer size bit3
2	**Size[2]**	0	R/W	Auto mode buffer size bit2
1	**Size[1]**	0	R/W	Auto mode buffer size bit1
0	**Size[0]**	0	R/W	Auto mode buffer size bit0

Table 41.SWB High size register - HighSWB

Bit	Name	Reset	R/W	Description
3	**AutoSWB**	0	R/W	SWB Automatic mode select
2	**StSWB**	0	R/W	SWB start interactive mode
1	**Size[5]**	0	R/W	Auto mode buffer size bit5
0	**Size[4]**	0	R/W	Auto mode buffer size bit4

The SWB has two operational modes, automatic mode and interactive mode.

11.1.SWB Automatic send mode

Automatic mode enables a buffer on a predefined length to be sent at high transmission speeds up to ck[15] (16khz ***f1**). In this mode user prepares all the data to be sent (minimum 8 bits, maximum 256 bits) in the RAM. The user then selects the clock speed, sets the number of data nibbles to be sent, selects automatic transmission mode (**AutoSWB** bit set to 1) and enters STANDBY mode by executing a HALT instruction. Once the HALT instruction is activated the SWB peripheral module sends the data in register **SWBuff** followed by the data in the RAM starting at address 00 up to the address specified by the bits **size[5:0**] located in the **LowSWB**, **HighSWB** registers.

During automatic transmission the general INTEN bit is disabled automatically to prevent other Interrupts to reset the standby mode. At the end of automatic transmission EM6603 leaves standby mode *(**INTEN** is automatically Enabled)* and sets TestVar[3] high. TestVar[3] = 1 is signaling SWB transmission is terminated.

As soon as **SWBAuto** is high, the general IntEn flag is disabled until the **SWBAuto** goes back low.

After automatic SWB transmission **INTEN** *bit becomes active high. Although set to 1 via the Halt instruction the bit* **INTEN** *is disabled throughout the whole SWB automatic transmission. It resumes to 1 at the end of transmission*.

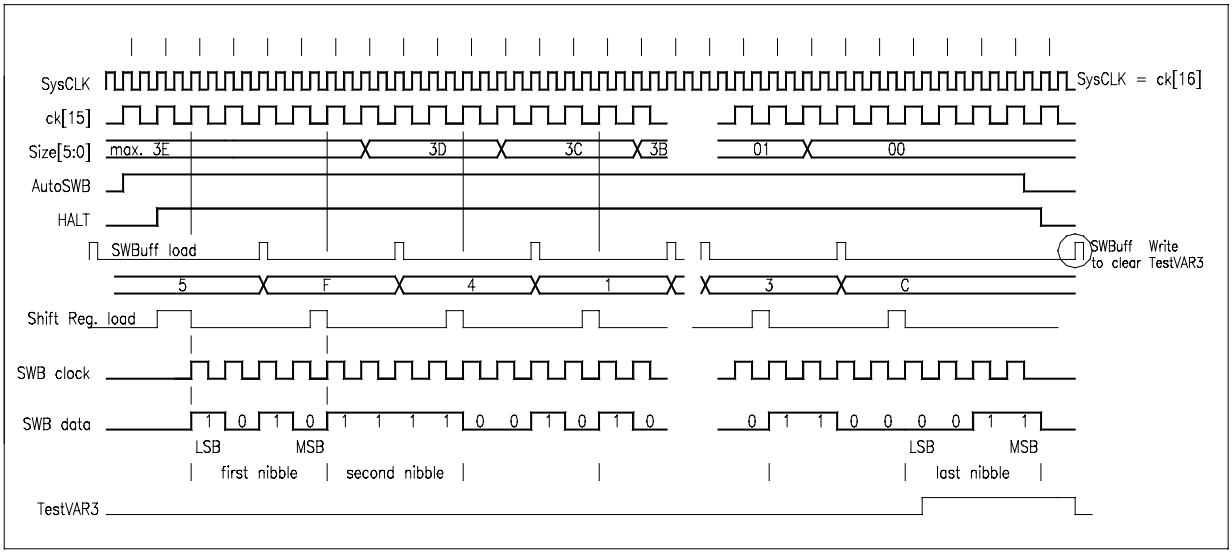
The data to be sent must be prepared in the following order:

First nibble to be sent must be written in the **SWBuff** register . The other nibbles must be loaded in the RAM from address 0 (second nibble at adr.0, third at adr.1,...) up to the address with last nibble of data to be send = "size" address. Max. address space for SWB is 3E ("size" 3E hex) what gives with **SWBuff** up to 64 nibbles (256 bits) of possible data to be sent. The minimum possible data length we can send in Automatic SWB mode is 8 bits when the last RAM address to be sent is 00 ("size" = 00)

Once data are ready in the RAM and in the **SWBuff**, user has to load the "size" (adr. of the last nibble to be send - bits **size[5:0]**) into the **LowSWB** and **HighSWB** register together with **AutoSWB** bit = 1.

Now everything is ready for serial transmission. To start the transmission one has to put the EM6603 in standby mode with the HALT instruction. With this serial transmission starts. When transmission is finished the TESTvar[3] (can be used for conditional jumps) becomes active High, the **AutoSWB** bit is cleared, the processor is leaving the Standby mode and **INTEN** is switched on.

Figure 13.Automatic Serial Write Buffer transmission



The processor now starts to execute the first instruction placed after the HALT instruction (for instance write of **SWBuff** register to clear TESTvar[3]), except if there was a IRQ during the serial transmission. In this case the CPU will go directly in the interrupt routine to serve other interrupt sources.

TestVar[3] stays high until **SWBuff** is rewritten. Before starting a second SWB action this bit must be cleared by performing a dummy write on **SWBuff** address.

Because the data in the RAM are still present one can start transmitting the same data once again only by recharging the **SWBuff** , **LowSWB** and **HighSWB** register together with **AutoSWB** bit and putting the EM6603 in HALT mode will start new transmission.

11.2.SWB Interactive send mode

In interactive SWB mode the reloading of the data transmission register **SWBbuff** is performed by the application program. This means that it is possible to have an unlimited length transmission data stream. However, since the application program is responsible for reloading the data a continuous data stream can only be achieved at ck[11] or ck[12] (1kHz or 2kHz ***1**) transmission speeds. For the higher transmission speeds a series of writes must be programmed and the serial output clock will not be continuous.

Serial transmission using the interactive mode is detailed in Figure 14. Programming of the SWB in interactive is achieved in the following manner:

Select the transmission clock speed using the bits **ClkSW0** and **ClkSW1** in the **ClkSWB** register.

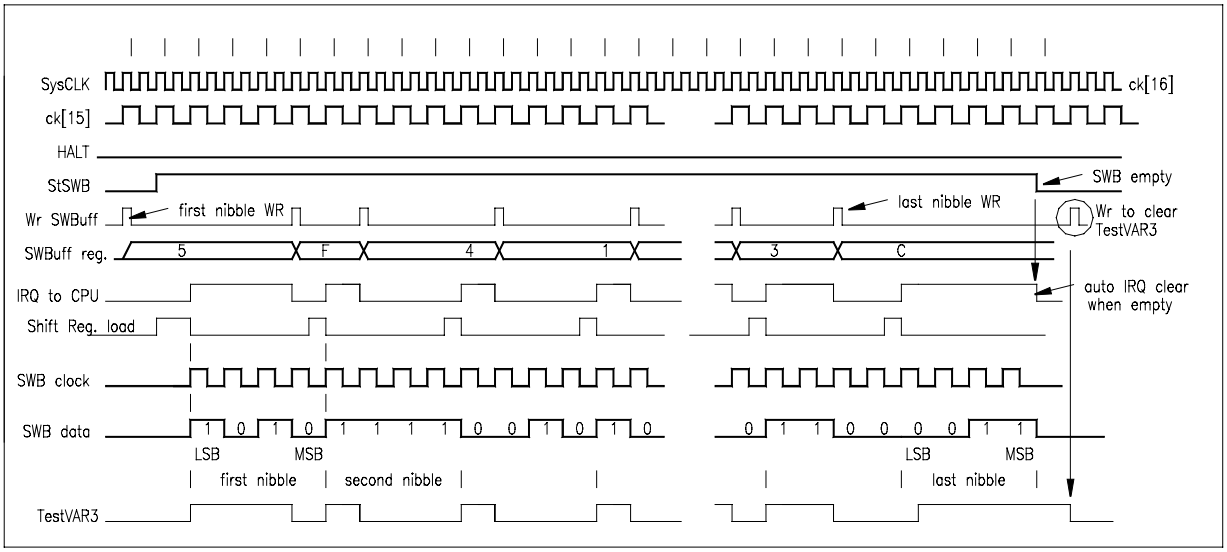
Load the first nibble of data into the SWB data register **SWBbuff**

Start serial transmission by selecting the bit **StSWB** in the register **HighSWB** register.

Once the data has been transferred into the serial transmission register a non maskable interrupt (SWBEmpty) is generated and TESTvar[3] goes high. The CPU goes in the interrupt routine, with the JPV3 as first instruction in the routine one can immediately jump to the SWB update routine to load the next nibble to be transmitted into the **SWBuff** register. If this reload is performed before all the serial data is shifted out then the next nibble is automatically transmitted. This is only possible at the transmission speeds of ck[11] or ck[12] (1kHz or 2kHz ***1**) due to the number of instructions required to reload the register. At the higher transmission speeds of ck[14] or ck[15] (8khz and 16khz ***1**) the application must restart the serial transmission by writing the **StSWB** in the High **SWBHigh** register after writing the next nibble to the **SWBbuff** register.

Each time the **SWBuff** register is written the "SWBbuffer empty interrupt" and TestVar[3] are cleared to "0". For proper operation the **SWBuff** register must be written before the serial clock drops to low during sending the last bit (MSB) of the previous data.

Figure 14.Interactive Serial Write Buffer transmission



After loading the last nibble in the **SWBbuff** register a new interrupt is generated when this data is transferred to an intermediate Shift Register. Precaution must be made in this case because the SWB will give repetitive interrupts until the last data is sent out completely and the **STSWB** bit goes low automatically. One possibility to overcome this is to check in the Interrupt subroutine that the **STSWB** bit went low before exiting interrupt. Be careful because if **STSWB** bit is cleared by software transmission is stopped immediately.

At the end of transmission a dummy write of **SWBuff** must be done to clear TESTvar[3] and "SWBbuffer empty interrupt" or the next transmission will not work.

12.STroBe / RESet Output

The STB/RST output pin is used to indicate the EM6605 RESET condition as well as write operations to ports B, C and D. For a PortB, PortC and PortD write operation the STROBE signal goes high for half of the system clock period. Write is effected on falling edge of the strobe signal and it can this be used to indicate when data changes at the output port pins. In addition, any EM6605 internal RESET condition is indicated by a continuous high level on STB/RES for the period of the RESET.

13.Test at EM - Active Supply Current test

For this purpose, five instructions at the end of the ROM will be added.

```
Testloop:  STI      00H, 0AH
           LDR      1BH
           NXORX
           JPZ      Testloop
           JMP      00H
```

To stay in the testloop, these values must be written in the corresponding addresses before jumping in the loop:

```
1BH:    0101b
32H:    1010b
6EH:    0010b
6FH:    0011b
```

Free space after last instruction: JMP 00H (0000)

Remark: empty space within the program are filled with NOP (FOFF).

14.Metal Mask Options

The following options can be selected at the time of programming the metal mask ROM.

Table 42 buzzer frequecies

	description	basic **(hi)**	reduced **(lo)**
ck[buz1]	1st buzzer frequency		
ck[buz2]	2nd buzzer frequency		

Put one cross in each line

Table 43 Input/Output Ports

		Pull-Up Yes / No	Pull-Down Yes / No	Nch-open drain Yes / No	Input blocked when Output Yes / No	Output Hi-Z in SLEEP mode Yes / No
		0	**1**	**4**	**5** *1	**6** *2
A0	**PA0 input**					
A1	**PA1 input**					
A2	**PA2 input**					
A3	**PA3 input**					
B0	**PB0 In/Out**					
B1	**PB1 In/Out**					
B2	**PB2 In/Out**					
B3	**PB3 In/Out**					
C0	**PC0 In/Out**					
C1	**PC1 In/Out**					
C2	**PC2 In/Out**					
C3	**PC3 In/Out**					
D0	**PD0 In/Out**					
D1	**PD1 In/Out**					
D2	**PD2 In/Out**					
D3	**PD3 In/Out**					

Put one letter (Y, N, R, F)in each BOX from proposed for the column.
***1** Port wise for PortC and PortD (one possibility for the whole port); PortB bit-wise
***2** Port-wise for PortC and PortD (one possibility for the whole port); PortB bit-wise

Table 44 PortA RESET option - One Option must be selected

		NO PortA reset combination	PA0 & PA1 logic AND input reset	PA0 & PA1 & PA2 logic AND input reset	PA0 & PA1 & PA2 & PA3 logic AND input reset
		0	**1**	**2**	**3**
RA	**PortA RESET**				

Table 45 SVLD levels – See 16.6 DC characteristics –SV Detector Levels – Write typ. value of used levels

		typ. **VL1** level [V]	typ. **VL2** level [V]	typ. **VL3** level [V]
VL	**SVLD level in Volts**			

Table 46 Frequency range – See Chapter 4 oscillator frequency range section

		LF range	**HF range**
RC	**Oscillator range**		

Software name is : _____.bin, dated _____

The customer should specify the required options at the time of ordering.
A copy of this sheet, as well as the « Software ROM characteristic file » generated by the assembler (*.STA) should be attached to the order.

15.Peripheral memory map

The following table shows the peripheral memory map of the EM6605. The address space is between $00 and $7F (Hex). Any addresses not shown can be considered to be reserved.

Register name	add hex	add dec	power up value	write_bits	read_bits	Remarks
			b'3210	Read/Write_bits		
RAM	00- 5f	0-95	xxxx	0: D0 1: D1 2: D2 3: D3		direct addressing
LTimLS	60	96	0000	0: TL0 1: TL1 2: TL2 3: TL3	0: TS0 1: TS1 2: TS2 3: TS3	low nibble of 8bit timer load and status register
HTimLS	61	97	0000	0: TL4 1: TL5 2: TL6 3: TL7	0: TS4 1: TS5 2: TS6 3: TS7	high nibble of 8bit timer load and status register
TimCtr	62	98	0000	0: TEC0 1: TEC1 2: TEC2 3:TimAUTO		timer control register with frequency selector
Option	63	99	0000	0: NoWD 1: debPAN 2: debPCN 3:IRQedgeR		option register
PA3cnt	65	101	xxx0	0: PA3cntin 1: - 2: - 3: -		PA3 counter input
ClkSWB	68	104	0000	0: CkSWB0 1: CkSWB1 2: - 3: V03		Clock selector for SWB
SWBuff	69	105	1111	0: Buff0 1: Buff1 2: Buff2 3: Buff3		SWB intermediate buffer
LowSWB	6A	106	0000	0: size[0] 1: size[1] 2: size[2] 3: size[3]		low nibble to define the size of data to be send in Automatic mode
HighSWB	6B	107	0000	0: size[4] 1: size[5] 2: StSWB 3:AutoSWB		the size of the data to be sent & SWB control
SVLD	6C	108	0000	0: VLC0 1: VLC1 2: - 3: -	0: VLC0 1: VLC1 2: busy 3: VLDR	voltage level detector control
CIRQD	6D	109	xx00	0: INTEN 1: DebCK 2: - 3: -		global interrupt enable debouncer clock
Index LOW	6E	110	xxxx			internally used for INDEX register
Index HIGH	6F	111	xxxx			internally used for INDEX register

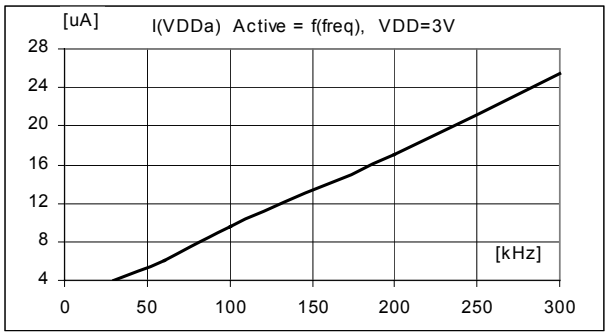
Register name	add hex	add dec	power up value	write_bits	read_bits	Remarks
			b'3210	Read/Write_bits		
IntRq	70	112	0000	0: - 1: - 2: SLEEP 3: -	0: INTPA 1: INTPC 2: INTTE 3: INTPR	interrupt requests sleep mode
WD	71	113	0000	0: - 1: - 2: SLmask 3: WDrst	0: WD0 1: WD1 2: SLmask 3: 0	WatchDog timer control and SLEEP mask
PortA	72	114	xxxx		0: PA0 1: PA1 2: PA2 3: PA3	Port A status
IRQpA	73	115	0000		0: IRQpa0 1: IRQpa1 2: IRQpa2 3: IRQpa3	Port A interrupt request
MPortA	74	116	0000	0: MPA0 1: MPA1 2: MPA2 3: MPA3		Port A mask
PortB	75	117	xxxx	0: PB0 1: PB1 2: PB2 3: PB3		Port B Input/Output
CIOportB	76	118	0000	0: CIOPB0 1: CIOPB1 2: CIOPB2 3: CIOPB3		Port B Input/Output individual control
PortC	77	119	xxxx	0: PC0 1: PC1 2: PC2 3: PC3		Port C Input/Output
IRQpC	78	120	0000		0: IRQpc0 1: IRQpc1 2: IRQpc2 3: IRQpc3	Port C interrupt request
MPortC	79	121	0000	0: MPC0 1: MPC1 2: MPC2 3: MPC3		Port C mask
PortD	7A	122	xxxx	0: PD0 1: PD1 2: PD2 3: PD3		Port D Input/Output
CPIOB	7C	124	x000	0: PA&C 1: CIOPC 2: CIOPD 3: -		PortAirq AND PortCirq PortC In/Out PortD In/Out
PRESC	7D	125	0000	0: PSF0 1: PSF1 2: PRST 3: MTim	0: PSF0 1: PSF1 2: 0 3: MTim	Prescaler control timer mask
BEEP	7E	126	0000	0: BCF0 1: BCF1 2: BUen 3: TimEn		Buzzer control Timer Enable
RegTestEM	*7F*	*127*	----	----	----	*reserved*

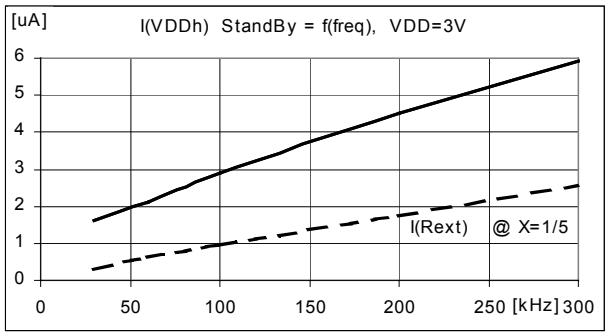
16.Measured Electrical Behaviors

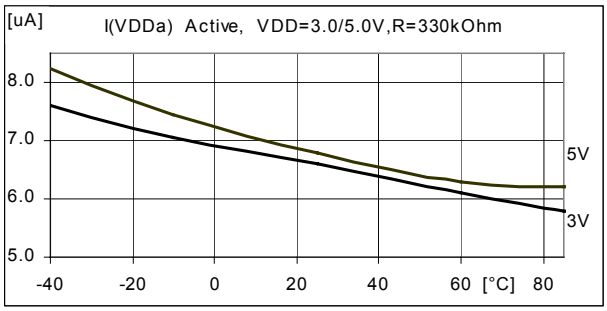
16.1. IDD Current

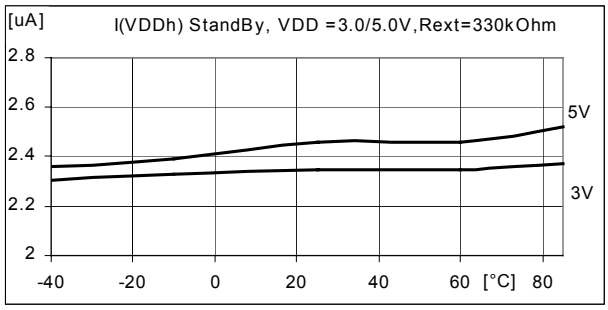
Specially the Stand-By current (IVDDh) depends on the current mirror ratio between the current which goes through an external resistor (IRext) and the current which is used in the internal RC oscillator capacitor (IRCint). Like that we can reduce the power consumption in StandBy mode. This current is approximately equal to:

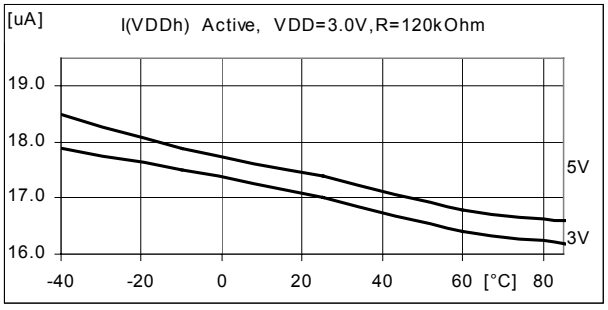
IR*ext* ~ 0.2V / Rext The internal Oscillator capacitor is charged with 1/5,1/4,1/3, or 1/2 of this current. All data here are with ratio IRCint / IRext = 1/5. IVDDa[µA] ~ IVDDh + f[kHz]*0.067

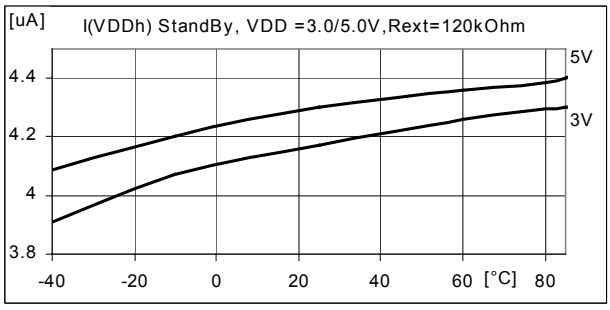


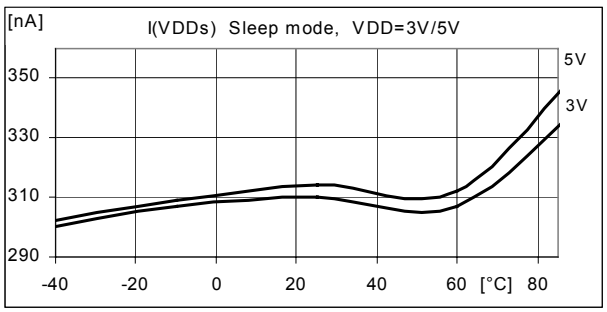










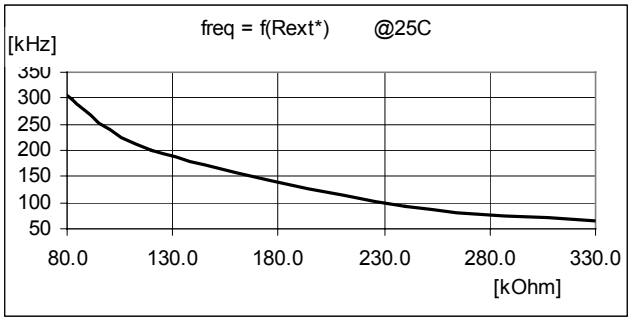


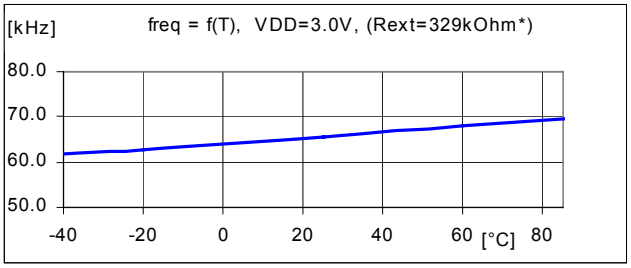
Current ratio I(RCint) / I(Rext)	frequency
X = 1/5	**f = f0**
X = 1/4	**f = f0 * 1.25**
X = 1/3	**f = f0 * 1.67**
X = 1/2	**f = f0 * 2.50**

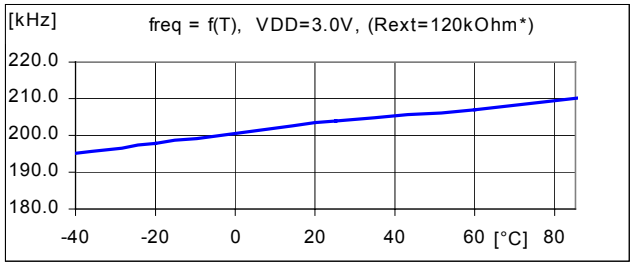
16.2.Frequency

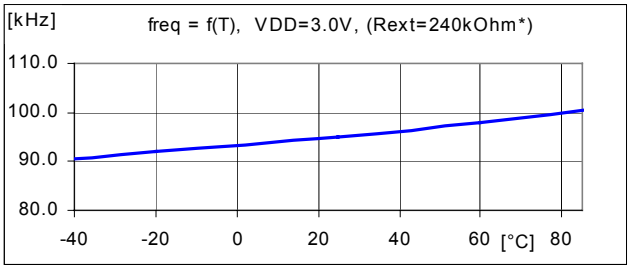
Last table on previous page shows already that we can adjust the frequency tw. needed resistor also with different current mirror **I**RCint / **I**Rext. Please contact EM Marin directly when ordering EM6605 if you would like to profit this possibility.

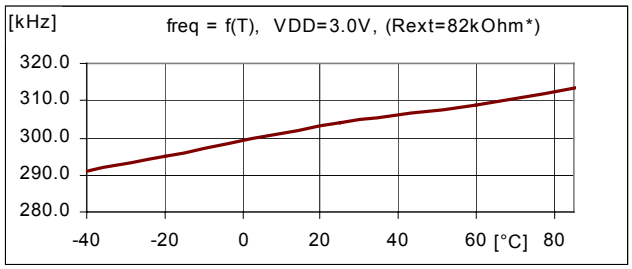
Next figures show the frequency dependence on Rext when **I**RCint / **I**Rext = 1/5



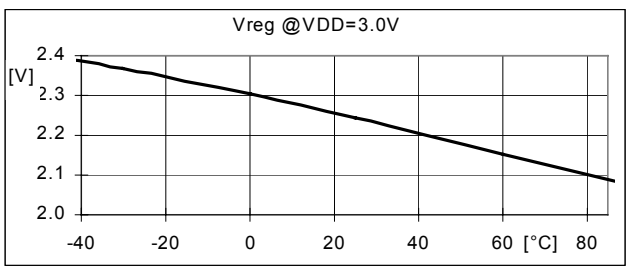


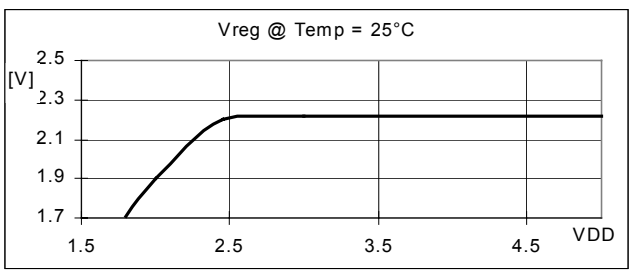




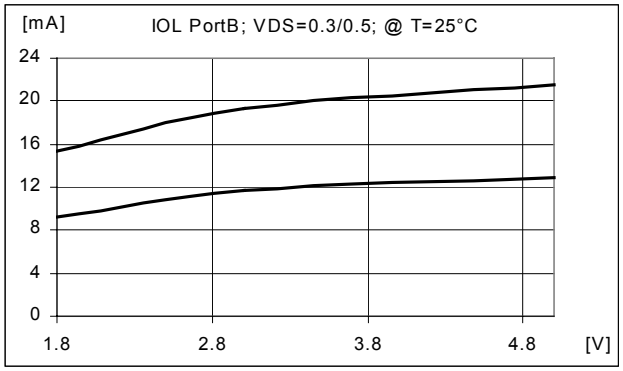


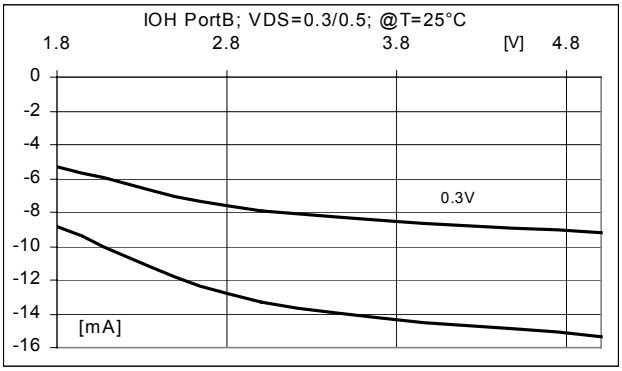
16.3.Regulated Voltage

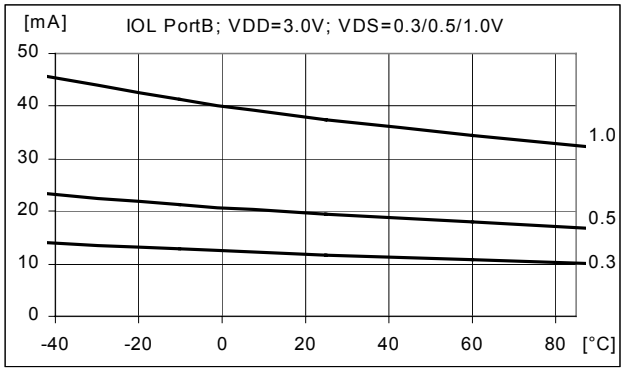


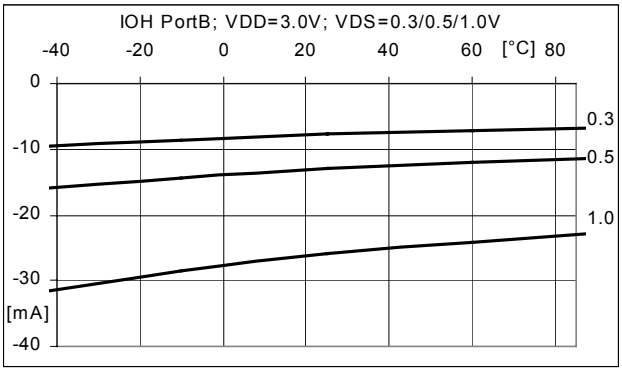


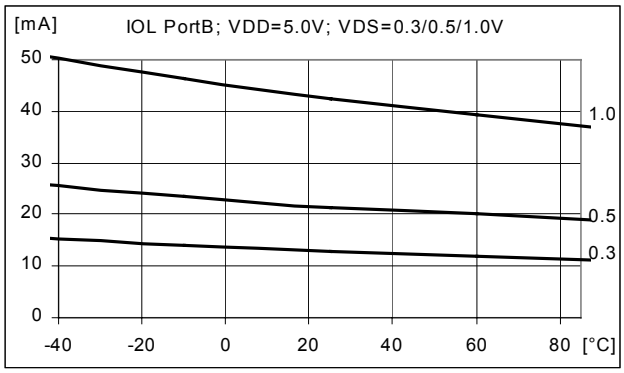
16.4. Output currents

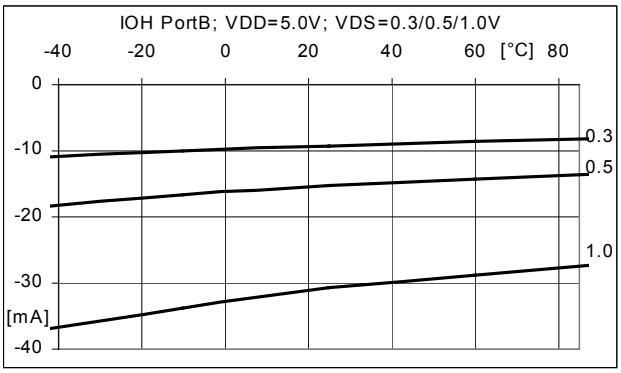


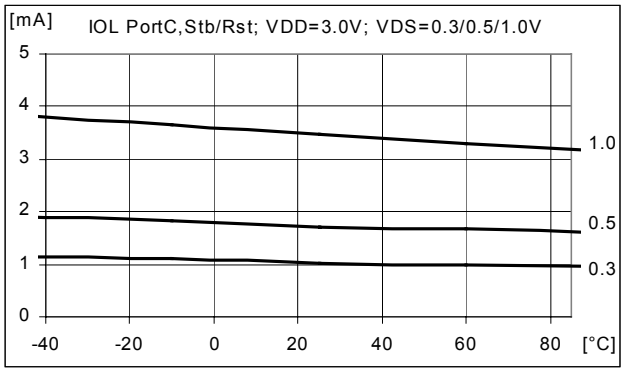


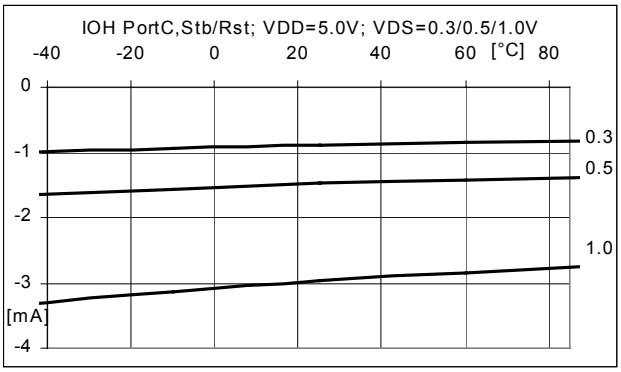




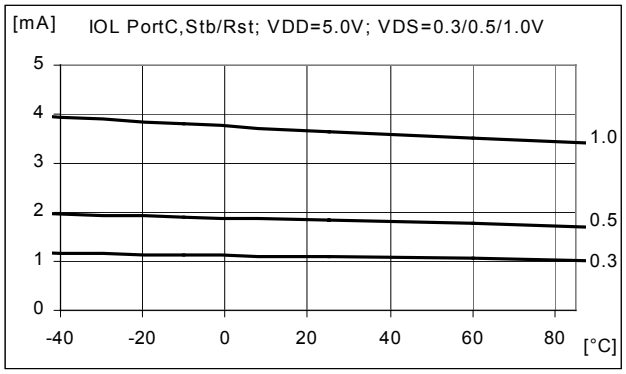


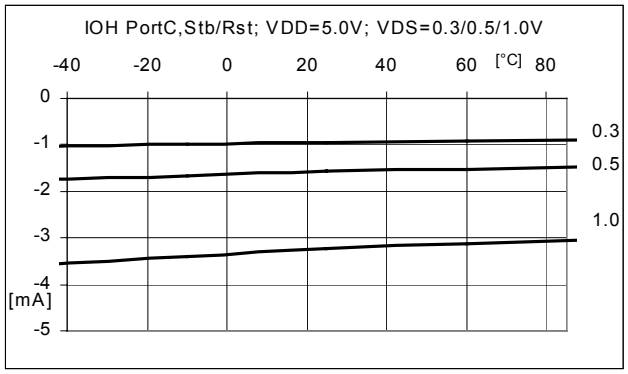


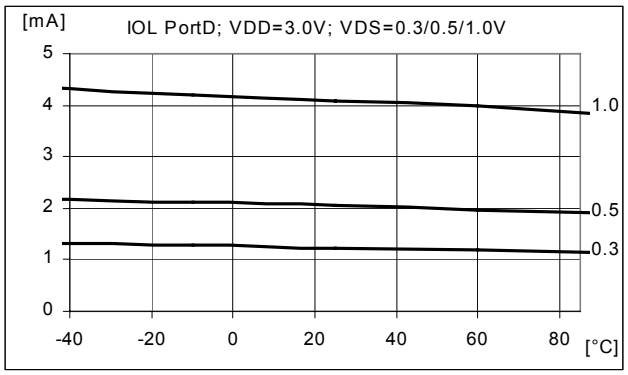


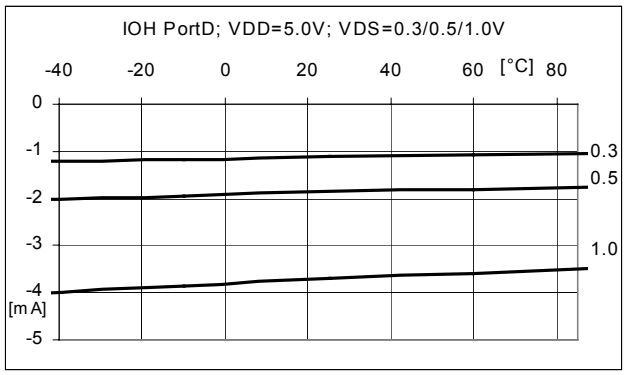


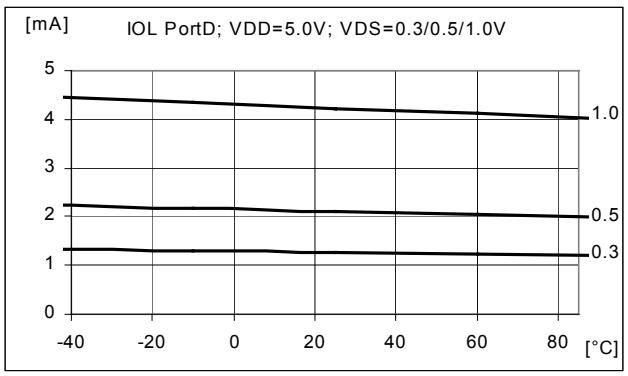
Output Currents – continued

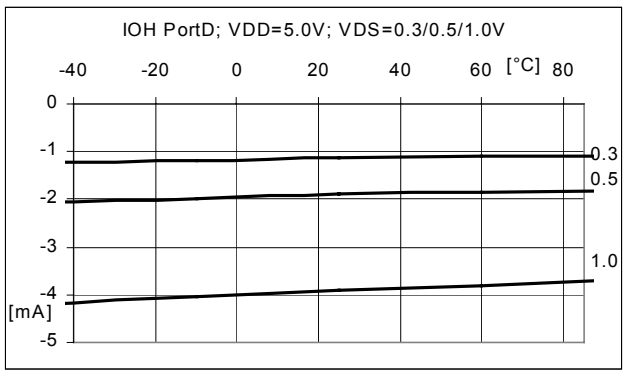




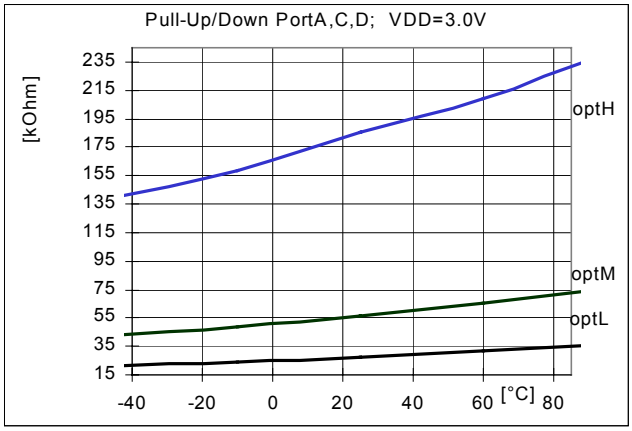


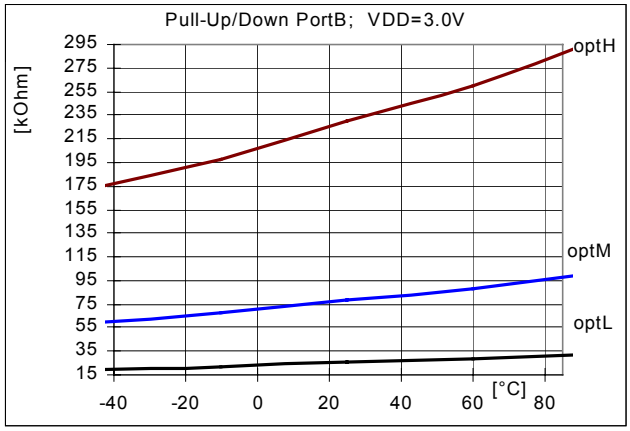


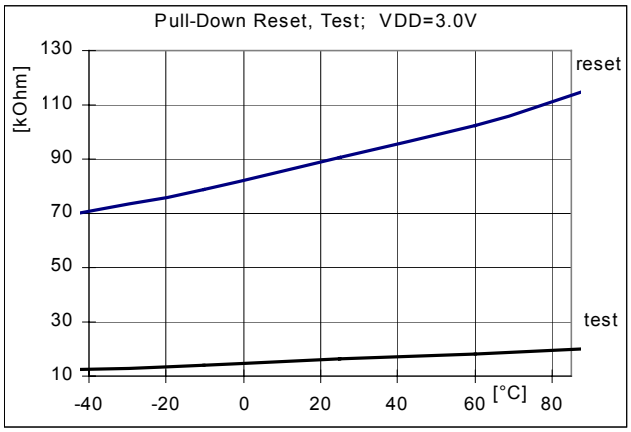




16.5.Pull Up / Down Resistors







17. Electrical specifications

17.1.Absolute maximum ratings

	min.	max.	unit
Supply voltage VDD-VSS	- 0.2	+ 6.0	V
Input voltage	VSS - 0.2	VDD+0.2	V
Storage temperature	- 50	+ 125	°C

Stresses above these maximum ratings may cause permanent damage to the device. Exposure beyond specified electrical characteristics may affect device reliability or cause malfunction.

17.2.Standard Operating Conditions

Parameter	value	Description
Temperature	-40°C...+85°C	
VDD (fmax. = 200kHz)	+1.8 ...+5.5V	With internal voltage regulator
VDD (fmax. = 300kHz)	+2.4 ...+5.5V	With internal voltage regulator
VSS	0 V (reference)	
CVreg	min. 100nF	regulated voltage capacitor tow. Vss
Rext (typical)	120kΩ - 330kΩ	external resistor to set frequency

17.3.Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions should be taken as for any other CMOS component.
Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range.

17.4.DC characteristics - Power Supply

Vdd=3.0V, T=25°C, Rext ≈ 120kΩ (note4) (unless otherwise specified), f ≈ 200kHz, IRCint / IRext = 1/5

Parameter	Conditions	Symb.	Min.	Typ. (note1)	Max.	Unit
ACTIVE Supply Current	(note2)	IVDDa		17.0	22.0	µA
ACTIVE Supply Current (in active mode)	(note2) (note3) -40°C...+85°C	IVDDa			25.0	µA
STANDBY Supply Current		IVDDh		4.1	6.0	µA
STANDBY Supply Current (in Halt mode)	(note3) -40°C...+85°C	IVDDh			8.0	µA
SLEEP Supply Current		IVDDs		0.3	0.5	µA
SLEEP Supply Current (SLEEP =1)	(note3) -40°C...+85°C	IVDDs			2.0	µA
POR voltage		VPOR		0.9	1.4	V
RAM data retention		Vrd	1.5			V
Regulated Voltage	Vreg not at Vdd	Vreg	1.8	2.2	2.6	V

Note: Pieces are tested with fixed resistors between 330kΩ and 120kΩ at the frequency used by the customer.

Note1: For current measurement the corresponding resistor for targeted frequency ±20% is selected; All I/O pins without internal Pull Up/Down are pulled to Vdd externally.
Note2: Test loop with successive writing and reading of two different addresses with an inverted values (five instructions should be reserved for this measurement),
Note3: NOT tested if delivered in chip form.
Note4: Test conditions for ACTIVE and STANDBY Supply current mode are: external resistor between the RCin and Vss pins.

17.5.DC characteristics - In/Out Pins

-40°C <T<85°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Input Low voltage						
I/O ports A,B,C,D	Pin at hi-impedance	**V**IL	Vss		0.3VDD	V
TEST			Vss		0.3VDD	V
Reset			Vss		0.3VDD	V
Qin (Note5)			Vss		0.3Vreg	V
Input High voltage						
I/O ports A,B,C,D	Pin at hi-impedance	**V**IH	0.7VDD		VDD	V
TEST			0.7VDD		VDD	V
Reset			0.7VDD		VDD	V
Qin (Note5)			0.9Vreg		Vreg	V
Output Low Current	VOL = 0.3V, VDD = 1.8V	**I**OL				
Port B				8.5		mA
Port C, STRB/RST				0.90		mA
Port D				1.10		mA
Output Low Current	VOL = 0.4V, VDD = 3.0V	**I**OL				
Port B			10.0	15.0		mA
Port C,D, STRB/RST			1.0	1.20		mA
Port D			1.0	1.60		
Output Low Current	VOL = 0.5V, VDD = 5.0V	**I**OL				
Port B				20.0		mA
Port C, STRB/RST				1.80		mA
Port D				2.00		mA
Output High Current	VOH = 1.5V, VDD = 1.8V	**I**OH				
Port B				5.40		mA
Port C, STRB/RST				0.70		mA
Port D				0.95		mA
Output High Current	VOH = 2.5V, VDD = 3.0V	**I**OH				
Port B			8.0	13.0		mA
Port C, STRB/RST			1.0	1.50		mA
Port D			1.0	1.80		mA
Output High Current	VOH = 4.5V, VDD = 5.0V	**I**OH				
Port B				15.0		mA
Port C, STRB/RST				1.70		mA
Port D				1.90		mA

-40°C <T<85°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Input pull-down (note5)	Pin at VDD = 1.8V	**Rin**				
I/O ports A,B,C,D (optionL)				25		kΩ
I/O ports A,B,C,D (optionM)				55		kΩ
I/O ports A,B,C,D (optionH)				170		kΩ
Reset				90		kΩ
Test				15		kΩ
Input pull-down (note5)	Pin at VDD = 3.0V	**Rin**				
I/O ports A,B,C,D (optionL)			10	25	50	kΩ
I/O ports A,B,C,D (optionM)			30	55	100	kΩ
I/O ports A,B,C,D (optionH)			80	170	330	kΩ
Reset			50	90	150	kΩ
Test			8	15	30	kΩ
Input pull-up (note5)	Pin at Vss / VDD = 1.8V	**Rin**				
I/O ports A,B,C,D (optionL)				25		kΩ
I/O ports A,B,C,D (optionM)				55		kΩ
I/O ports A,B,C,D (optionH)				170		kΩ
Input pull-up (note5)	Pin at Vss / VDD = 3.0V	**Rin**				
I/O ports A,B,C,D (optionL)			10	25	50	kΩ
I/O ports A,B,C,D (optionM)			30	55	100	kΩ
I/O ports A,B,C,D (optionH)			80	170	330	kΩ

Note5 : there are three options for the value of Pull-Up / Pull-Down resistors.
Option L (low value), Option M (med. value), Option H (high value)
All Resistors have a temperature coefficient of about +0.45%/°C

17.6.DC characteristics - S V D Levels

SVD = Supply Voltage Detector T= +25°C (unless otherwise specified)

1.9V < V_{L1} < V_{L2} < V_{L3} < 4.5V (V_{L1} > 1.3V, V_{L2} > 1.8V, V_{L3} > 2.0V) , @ 50 kHz < f < 250 kHz

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Supply Voltage Detector	T = +25°C					
SVLD lev3		V_{L3}	0.92 x V_{L3}	V_{L3}	1.08 x V_{L3}	V
SVLD lev2		V_{L2}	0.92 x V_{L2}	V_{L2}	1.08 x V_{L2}	V
SVLD lev1		V_{L1}	0.92 x V_{L1}	V_{L1}	1.08 x V_{L1}	V
Supply Voltage Detector	0°C...+65°C					
SVLD lev3		V_{L3}	0.90 x V_{L3}	V_{L3}	1.10 x V_{L3}	V
SVLD lev2		V_{L2}	0.90 x V_{L2}	V_{L2}	1.10 x V_{L2}	V
SVLD lev1		V_{L1}	0.90 x V_{L1}	V_{L1}	1.10 x V_{L1}	V
SVLD current consumption when activated	1.5V<VDD<3V	I_{SVLD}		3.0		µA

SVLD typical level values must be selected with a precision of 100 mV

17.7.RC Oscillator

T= +25°C (unless otherwise specified)

Parameter	Conditions	Symb.	Min.	Typ.	Max.	Unit
Fabrication process stability	(note1)	Df / f *	-20	±10 *	+20	%
Voltage stability (note2)	2.4 - 5.0 V	Df /f * DU	-2%	± 0.3	+2%	1/V
Temperature Stability (note2)	-40°C- +85°C	Df /f * DT	0.02%	+0.06%	0.1%	1/°C
Adjustable frequency range permitted (note 6)		freq	30	128	300	kHz
External resistor for frequency (note4) (note5)	Vdd>1.8V	Rext	80*	120-330	600*	kΩ
Ext. capacitor (parallel to Rext) (note4)		Cext		150	390	pF
Oscillator start time (note3)	Vdd>1.8V	tdosc		0.1	1	ms
System start time (note3) (oscillator+cold start reset)	Vdd>1.8V	tdsys		3	4	ms
Oscillation detector frequency	Vdd>1.8V & Vdd<5.0V	fOD		4.0	15	kHz

Note1: Typical value of ±10% for "Fabrication process stability" gives a range where about 93-98% of all pieces are situated relative to their mean frequency **f ***.

Note2: Oscillator stability in voltage and temperature is for frequency range from 30kHz - 300 kHz

Note3: Oscillator start time is for the worst case - 32 kHz frequency (low frequency)

Note4: External capacitor parallel to Rext which set the system frequency – The capacitor must be as close as possible to RCin pin. The connection tw. Resistor and Capacitor on this pin must be really as short as possible otherwise the RC oscillator has bigger jitter. (capacitor is not obligatory but can improve voltage dependance and reduce jitter.

Note5: External resistor Rext which can set the frequency can have bigger range but this should be discussed by EM for special cases only. Tests were made only during qualification of the product.

Note6: see also table 17.2.

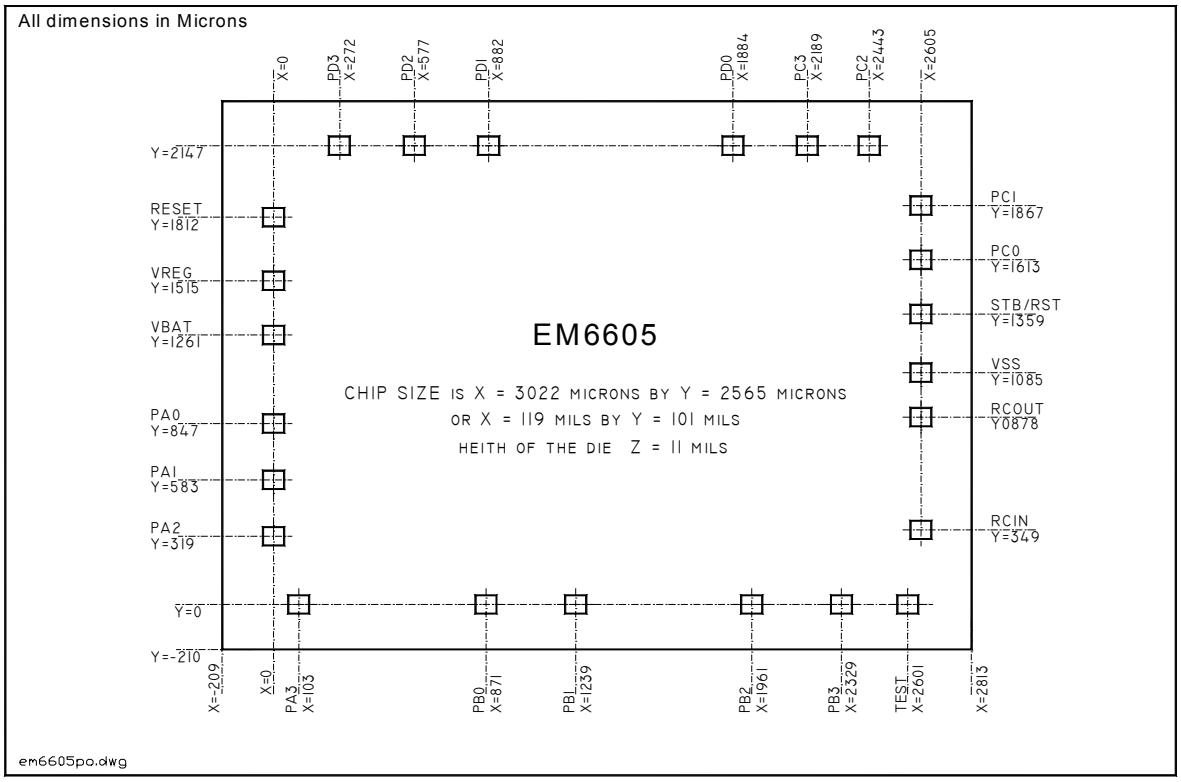
17.8.Input Timing characteristics

1.8V<Vdd<5.0V, -20°C <T<85°C (unless otherwise specified) at f=32kHz

Parameter	Conditions	Symb.	Min.	Unit
RESET pulse length to exit SLEEP mode	RESET from SLEEP	tRESsl	2	µs
RESET pulse length (debounced) PortA , C pulse length (debounced)	DebCK = 0 DebCK = 0	tdeb0 tdeb0	2 2	ms ms
RESET pulse length (debounced) PortA , C pulse length (debounced)	DebCK = 1 DebCK = 1	tdeb1 tdeb1	16 16	ms ms

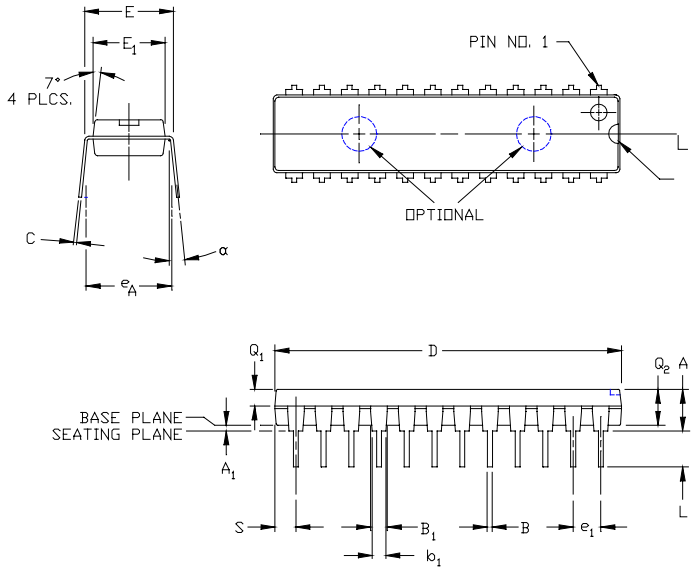
18. Pad Location Diagram

Figure 15. EM6605 PAD Location Diagram



19.Packages & Ordering informations

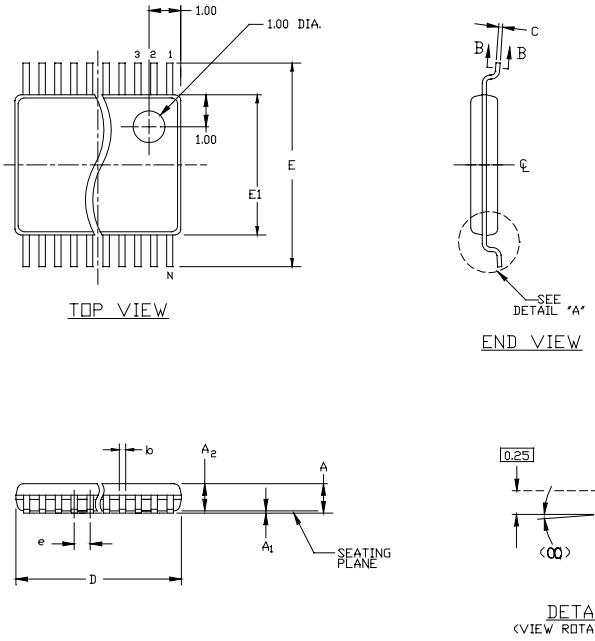
Figure 16. Dimensions of PDIP24 Package



SYMBOL	INCHES			MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A			.170			4.32
A_1	.015			0.38		
B	.015	.018	.022	0.38	0.46	0.56
B_1	.055	.060	.065	1.40	1.52	1.65
b_1	.045	.050	.055	1.14	1.27	1.40
C	.008	.010	.012	0.20	0.25	0.30
D	1.245	1.250	1.255	31.62	31.75	31.88
E	.300		.325	7.62		8.26
E_1	.250	.260	.270	6.35	6.60	6.86
e_1	.100 BSC			2.54 BSC		
e_A	.300 BSC			7.62 BSC		
L	.125		.135	3.18		3.43
α	0°		15°	0°		15°
N	24			24		
Q_1	.055	.060	.065	.140	1.52	1.65
Q_2		.130			3.30	
S	.070	.075	.080	1.78	1.91	2.03

P-DIP24 .300 INCH body width

Figure 17. Dimensions of TSSOP24 Package

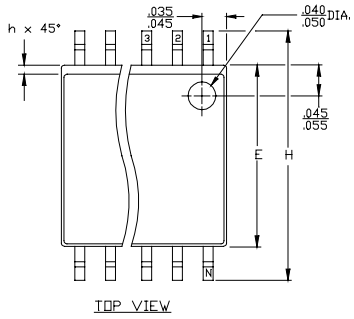


SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
D	7.80 BSC		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
θ	0°	——	8°

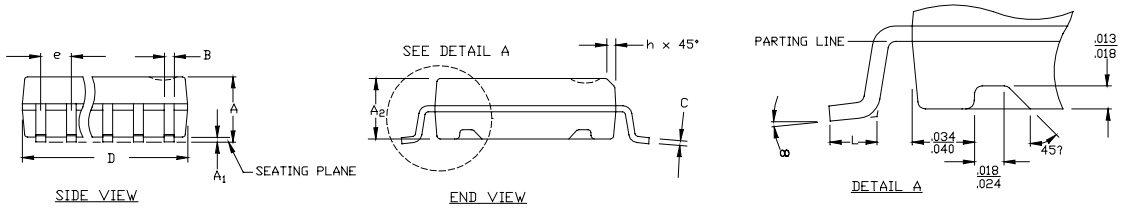
tssop-24.dwg

TSSOP24 (0.65mm pitch, 4.4mm body width)

Figure 18.Dimensions of SOIC24 Package



SYMBOL	DIMENSIONS in INCHES			DIMENSIONS in MILLIMETERS		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	.097	.101	.104	2.46	2.56	2.64
A_1	.0050	.009	.0115	0.127	0.22	0.29
A_2	.090	.092	.094	2.29	2.34	2.39
B	.014	.016	.019	0.35	0.41	0.48
C	.0091	.010	.0125	0.23	0.25	0.32
D	.602	.607	.612	15.29	15.42	15.54
E	.292	.296	.299	7.42	7.52	7.59
e	.050 BSC			1.27 BSC		
H	.400	.406	.410	10.16	10.31	10.41
h	.010	.013	.016	0.25	0.33	0.41
L	.024	.032	.040	0.61	0.81	1.02
N	24			24		
α	0°	5°	8°	0°	5°	8°



Sop-24.dwg

SOP-24(1.27mm pitch, 300mils body width)

19.1.Ordering Information

Packaged Device:

EM6605 %%% SO24 B

Customer Version:
customer-specific number
given by EM Microelectronic

Package:
SO24 = 24 pin SOIC
TP24 = 24 pin TSSOP
DL24 = 24 pin DIP (note 1)

Delivery Form:
A = Stick
B = Tape&Reel (for SO24 and TP24 only)

Device in DIE Form:

EM6605 %%% WS 11

Customer Version:
customer-specific number
given by EM Microelectronic

Die form:
WW = Wafer
WS = Sawn Wafer/Frame
WP = Waffle Pack

Thickness:
11 = 11 mils (280um), by default
27 = 27 mils (686um), not backlapped
(for other thickness, contact EM)

Note 1: Please contact EM Microelectronic-Marin S.A. for availability of DIP package.

Ordering Part Number (selected examples)

Part Number	Package/Die Form	Delivery Form/Thickness
EM6605%%%SO24A	24 pin SOIC	Stick
EM6605%%%SO24B	24 pin SOIC	Tape&Reel
EM6605%%%DL24A	24 pin DIP	Stick
EM6605%%%TP24B	24 pin TSSOP	Tape&Reel
EM6605%%%WS11	Sawn wafer	11 mils
EM6605%%%WP11	Die in waffle pack	11 mils

Please make sure to give the complete Part Number when ordering, including the 3-digit version. The version is made of 3 digits %%%: the first one is a letter and the last two are numbers, e.g. P01 , P12, etc.

19.2.Package Marking

DIP and SOIC marking:

First line:	E	M	6	6	0	5		0	%	%	Y
Second line:	P	P	P	P	P	P	P	P	P	P	P
Third line:	C	C	C	C	C	C	C	C	C	C	C

TSSOP marking:

E	M	6	6	0	5	%	%
P	P	P	P	P	P	P	P
		C	C	C	C	Y	P

Where: %% = last two-digits of the customer-specific number given by EM (e.g. 05, 12, etc.)
Y = Year of assembly
PP…P = Production identification (date & lot number) of EM Microelectronic
CC…C = Customer specific package marking on third line, selected by customer

19.3.Customer Marking

There are **11** digits available for customer marking on **DIP24** and **SO24**.
There are **4** digits available for customer marking on **TSSOP24**.

Please specify below the desired customer marking.

Updates since Rev A/152 (november 98)

Date of Update Name	Chapter concerned	New Version	Changes
01.11.01 PERT	All	11/01 B/400	Change Header & footer, Add URL mention
11.02.02 PERT	Pages 8, 29, 40	02/02 C/400	Add metal option RC osc table, frequency working range.
22.03.02 PERT	Page 40, 43	03.02 D/441	Change pad location diagram and ordering information