



512MB – 2x32Mx64 DDR SDRAM, UNBUFFERED, w/PLL, FBGA

FEATURES

- Fast data transfer rate: PC-2100 and PC-2700
- Clock speeds of 133 MHz and 166 MHz
- Two data transfers per clock cycle
- Supports ECC error detection and correction
- Bi-directional data strobes (DQS)
- Differential clock inputs (CK & CK#)
- Programmable Read Latency 2 and 2.5 (clock)
- Programmable Burst Length (2, 4 or 8)
- Programmable Burst type (sequential & interleave)
- Edge aligned data output, center aligned data input
- Auto and self refresh
- Serial presence detect (SPD) with EEPROM
- Dual Rank
- Power supply: $V_{cc} = V_{ccq} = +2.5V \pm 0.2V$ (133 and 166MHz)
- Gold edge contacts
- 200 pin, small-outline, SO-DIMM package
 - PCB height option:
31.75 mm (1.25")

DESCRIPTION

The WV3EG232M64EFSU is a 2x32Mx64 Double Data Rate SDRAM memory module based on 256Mb DDR SDRAM components. The module consists of sixteen 32Mx8 4 banks DDR SDRAMs in FBGA packages mounted on a 200 pin FR4 substrate.

Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges and Burst Lengths allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

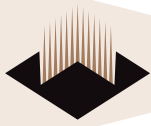
* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:

- RoHS compliant products
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	DDR333@CL=2.5	DDR266@CL=2	DDR266@CL=2.5
Clock Speed	166MHz	133MHz	133MHz
CL-trcd-trp	2.5-3-3	2-2-2	2.5-3-3



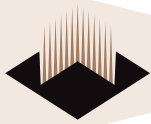
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	VREF	51	Vss	101	A9	151	DQ42
2	VREF	52	Vss	102	A8	152	DQ46
3	Vss	53	DQ19	103	Vss	153	DQ43
4	Vss	54	DQ23	104	Vss	154	DQ47
5	DQ0	55	DQ24	105	A7	155	Vcc
6	DQ4	56	DQ28	106	A6	156	Vcc
7	DQ1	57	Vcc	107	A5	157	Vcc
8	DQ5	58	Vcc	108	A4	158	*CK1#
9	Vcc	59	DQ25	109	A3	159	Vss
10	Vcc	60	DQ29	110	A2	160	*CK1
11	DQS0	61	DQS3	111	A1	161	Vss
12	DM0	62	DM3	112	A0	162	Vss
13	DQ2	63	Vss	113	Vcc	163	DQ48
14	DQ6	64	Vss	114	Vcc	164	DQ52
15	Vss	65	DQ26	115	A10/AP	165	DQ49
16	Vss	66	DQ30	116	BA1	166	DQ53
17	DQ3	67	DQ27	117	BA0	167	Vcc
18	DQ7	68	DQ31	118	RAS#	168	Vcc
19	DQ8	69	Vcc	119	WE#	169	DQS6
20	DQ12	70	Vcc	120	CAS#	170	DM6
21	Vcc	71	NC	121	CS0#	171	DQ50
22	Vcc	72	NC	122	CS1#	172	DQ54
23	DQ9	73	NC	123	NC	173	Vss
24	DQ13	74	NC	124	NC	174	Vss
25	DQS1	75	Vss	125	Vss	175	DQ51
26	DM1	76	Vss	126	Vss	176	DQ55
27	Vss	77	DNU	127	DQ32	177	DQ56
28	Vss	78	DNU	128	DQ36	178	DQ60
29	DQ10	79	NC	129	DQ33	179	Vcc
30	DQ14	80	NC	130	DQ37	180	Vcc
31	DQ11	81	Vcc	131	Vcc	181	DQ57
32	DQ15	82	Vcc	132	Vcc	182	DQ61
33	Vcc	83	NC	133	DQS4	183	DQS7
34	Vcc	84	NC	134	DM4	184	DM7
35	CK0	85	NC	135	DQ34	185	Vss
36	Vcc	86	NC	136	DQ38	186	Vss
37	CK0#	87	Vss	137	Vss	187	DQ58
38	Vss	88	Vss	138	Vss	188	DQ62
39	Vss	89	CK2*	139	DQ35	189	DQ59
40	Vss	90	Vss	140	DQ39	190	DQ63
41	DQ16	91	CK2#*	141	DQ40	191	Vcc
42	DQ20	92	Vcc*	142	DQ44	192	Vcc
43	DQ17	93	Vcc	143	Vcc	193	SDA
44	DQ21	94	Vcc	144	Vcc	194	SA0
45	Vcc	95	CKE1	145	DQ41	195	SCL
46	Vcc	96	CKE0	146	DQ45	196	SA1
47	DQS2	97	NC	147	DQS5	197	VCCSPD
48	DM2	98	NC	148	DM5	198	SA2
49	DQ18	99	A12	149	Vss	199	NC
50	DQ22	100	A11	150	Vss	200	NC

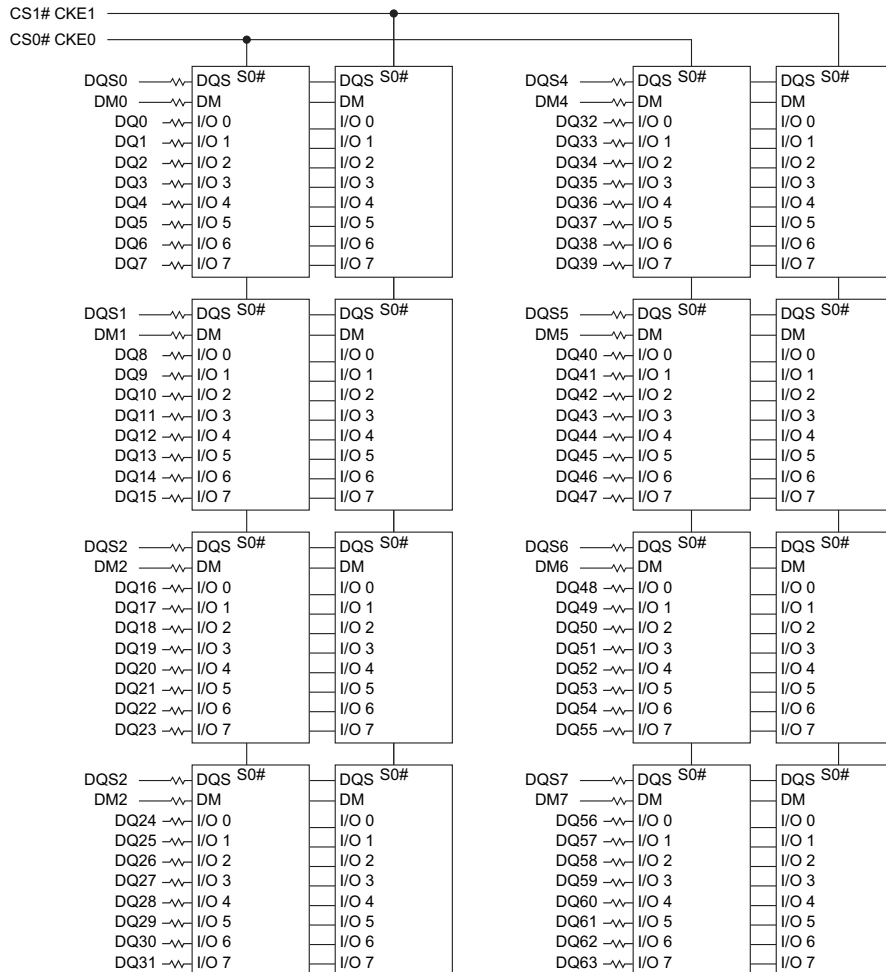
PIN NAMES

Symbol	Description
A0-A12	Address input
BA0, BA1	Bank Address
DQ0-DQ63	Input/Output: Data I/Os, Data bus
CK0, CK0#	Clock Input
CKE0-CKE1	Clock Enable Input
CS0#-CS1#	Chip Select Input
WE#, CAS#, RAS#	Command Input
DQS0-DQS7	Data Strobe
DM0-DM7	Data Write Mask
Vcc	Supply: Power Supply: +2.5V ±0.2V
Vccq	Power Supply for DQS
VccSPD	Supply: Serial EEPROM Positive Power Supply
VREF	Supply: SSTL_2 reference voltage
Vss	Supply: Ground
SCL	Serial Clock
SA0-SA2	Presence Detect Address Input
VccID	Vcc Identification Flag
SDA	Input/Output: Serial Presence-Detect Data
NC	No Connect
DNU	Do Not Use
RESET#	Reset Enable

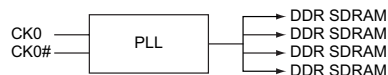
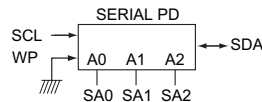
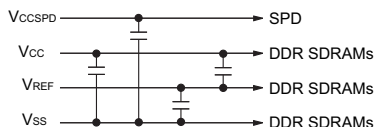
* These pins are not used in this module.



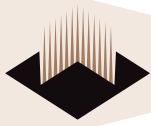
FUNCTIONAL BLOCK DIAGRAM



BA0, BA1 → BA0, BA1: DDR SDRAMs
 A0-A12 → A0-A12: DDR SDRAMs
 RAS# → RAS#: DDR SDRAMs
 CAS# → CAS#: DDR SDRAMs
 WE# → WE#: DDR SDRAMs



NOTE: 1.All resistor values are 22 Ω unless otherwise specified.



ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-0.5 ~ 3.6	V
Voltage on Vcc supply relative to Vss	V _{CC}	-1.0 ~ 3.6	V
Voltage on Vccq supply relative to Vss	V _{CCQ}	-0.5 ~ 3.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
 Functional operation should be restricted to recommended operating condition.
 Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS

T_A = 0°C to 70°C

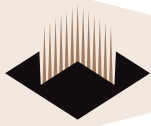
Parameter	Symbol	Min	Max	Unit	Note
Supply voltage(for device with a nominal V _{CC} of 2.5V)	V _{CC}	2.3	2.7	v	
I/O Supply voltage	V _{CCQ}	2.3	2.7	V	
I/O Reference voltage	V _{REF}	V _{CCQ} /2-50mV	V _{CCQ} /2+50mV	V	1
I/O Termination voltage(system)	V _{TT}	V _{REF} -0.04	V _{REF} +0.04	V	2
Input logic high voltage	V _{IH} (DC)	V _{REF} +0.15	V _{CCQ} +0.3	V	4
Input logic low voltage	V _{IL} (DC)	-0.3	V _{REF} -0.15	V	4
Input Voltage Level, CK and CK# inputs	V _{IN} (DC)	-0.3	V _{CCQ} +0.3	V	
Input Differential Voltage, CK and CK# inputs	V _{ID} (DC)	0.3	V _{CCQ} +0.6	V	3
Input crossing point voltage, CK and CK# inputs	V _{IX} (DC)	1.15	1.35	V	5
Input leakage current	I _I	-2	2	uA	
Output leakage current	I _{OZ}	-5	5	uA	
Output High Current(Normal strength driver); V _{OUT} = V _{TT} + 0.84V	I _{OH}	-16.8		mA	
Output High Current(Normal strength driver); V _{OUT} = V _{TT} - 0.84V	I _{OL}	16.8		mA	
Output High Current(Half strength driver); V _{OUT} = V _{TT} + 0.45V	I _{OH}	-9		mA	
Output High Current(Half strength driver); V _{OUT} = V _{TT} - 0.45V	I _{OL}	9		mA	

- Notes:
- Includes ± 25mV margin for DC offset on V_{REF}, and a combined total of ± 50mV margin for all AC noise and DC offset on V_{REF}, bandwidth limited to 20MHz. The DRAM must accommodate DRAM current spikes on V_{REF} and internal DRAM noise coupled TO V_{REF}, both of which may result in V_{REF} noise. V_{REF} should be de-coupled with an inductance of ≤ 3nH.
 - V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal to V_{REF}, and must track variations in the DC level of V_{REF}.
 - V_{ID} is the magnitude of the difference between the input level on CK and the input level on CK#.
 - These parameters should be tested at the pin on actual components and may be checked at either the pin or the pad in simulation. The AC and DC input specifications are relative to a V_{REF} envelop that has been bandwidth limited to 200MHZ.
 - The value of V_{IX} is expected to equal 0.5*V_{CCQ} of the transmitting device and must track variations in the dc level of the same.

CAPACITANCE

V_{CC} = 2.5, V_{CCQ} = 2.5V, T_A = 25 C, f = 1MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1,RAS#, CAS#, WE#)	C _{IN1}	38	47	pF
Input capacitance (CKE0,CKE1)	C _{IN2}	38	47	pF
Input capacitance (CS0#, CS1#)	C _{IN3}	36	44	pF
Input capacitance (CK0, CK0#)	C _{IN4}	36	40	pF
Input capacitance (DM0~DM7)	C _{IN5}	12	14	pF
Data & DQS input/output capacitance (DQ0~DQ63)	C _{OUT1}	12	14	pF



I_{DD} SPECIFICATIONS AND CONDITIONS

0°C ≤ T_A ≤ +70°C; V_{CC}, V_{CCQ} = +2.5V ±0.2V

PARAMETER/CONDITION	SYMBOL	MAX			UNITS
		DDR333 @CL=2.5	DDR266 @CL=2	DDR266 @CL=2.5	
Operating current – One bank Active-Precharge; t _{RC} = t _{RC} (min); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; DQ, DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	I _{DD0}	1160	1000	1000	mA
Operating current – One bank operation ; One bank open, BL=4, Reads — Refer to the following page for detailed test condition	I _{DD1}	1360	1200	1200	mA
Precharge power-down standby current; All banks idle; power-down mode; CKE ≤ V _{IL} (max); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; V _{IN} = V _{REF} for DQ, DQS and DM	I _{DD2P}	48	48	48	mA
Precharge Floating standby current; CS# ≥ V _{IH} (min); All banks idle; CKE ≥ V _{IH} (min); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs changing once per clock cycle; V _{IN} = V _{REF} for DQ, DQS and DM	I _{DD2F}	400	320	320	mA
Precharge Quiet standby current; CS# ≥ V _{IH} (min); All banks idle; CKE ≥ V _{IH} (min); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; Address and other control inputs stable with keeping ≥ V _{IH} (min) or ≤ V _{IL} (max); V _{IN} = V _{REF} for DQ, DQS and DM	I _{DD2Q}	320	290	290	mA
Active power - down standby current ; one bank active; power-down mode; CKE ≤ V _{IL} (max); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; V _{IN} = V _{REF} for DQ, DQS and DM	I _{DD3P}	560	480	480	mA
Active standby current; CS# ≥ V _{IH} (min); CKE ≥ V _{IH} (min); one bank active; active - precharge; t _{RC} = t _{RAS} (max); t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B; DQ, DQS and DM inputs changing twice per clock cycle; address and other control inputs changing once per clock cycle	I _{DD3N}	880	720	720	mA
Operating current - burst read; Burst length = 2; reads; contiguous burst; One bank active; address and control inputs changing once per clock cycle; CL = 2 at t _{CK} = 100Mhz for DDR200, CL = 2 at t _{CK} = 133Mhz for DDR266A, CL = 2.5 at t _{CK} = 133Mhz for DDR266B ; 50% of data changing at every burst; I _{OUT} = 0mA	I _{DD4R}	1720	1480	1480	mA
Operating current - burst write; Burst length = 2; writes; continuous burst; One bank active address and control inputs changing once per clock cycle; CL = 2 at t _{CK} = 100Mhz for DDR200, CL = 2 at t _{CK} = 133Mhz for DDR266A, CL = 2.5 at t _{CK} = 133Mhz for DDR266B; DQ, DM and DQS inputs changing twice per clock cycle, 50% of input data changing at every burst	I _{DD4W}	1720	1440	1440	mA
Auto refresh current; t _{RC} = t _{RFC} (min) - 8*t _{CK} for DDR200 at 100Mhz, 10*t _{CK} for DDR266A & DDR266B at 133Mhz; distributed refresh	I _{DD5}	1800	1640	1640	mA
Self refresh current; CKE ≤ 0.2V; External clock should be on; t _{CK} = 100Mhz for DDR200, 133Mhz for DDR266A & DDR266B	I _{DD6}	48	48	48	mA
Operating current - Four bank operation ; Four bank interleaving with BL=4 — Refer to the following page for detailed test condition	I _{DD7A}	2680	2360	2360	mA

Note: I_{DD} specification is based on Samsung components. Other DRAM Manufacturers specification may be different.

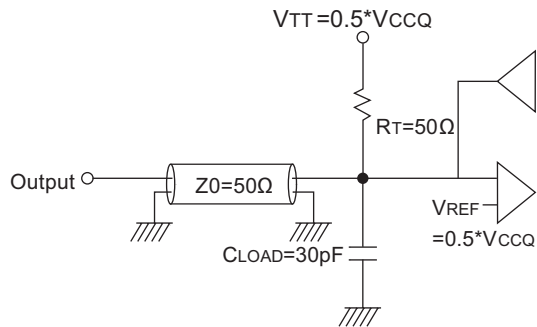


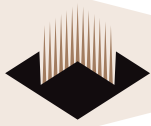
AC OPERATING TEST CONDITIONS

$V_{CC} = 2.5V, V_{CCQ} = 2.5V, 0^{\circ}C \leq T_A \leq +70^{\circ}C$

Parameter	Value	Unit
Input reference voltage for Clock	$0.5 * V_{CCQ}$	V
Input signal maximum peak swing	1.5	V
Input Levels(V_{IH}/V_{IL})	$V_{REF} + 0.31/V_{REF} - 0.31$	V
Input timing measurement reference level	V_{REF}	V
Output timing measurement reference level	V_{TT}	V
Output load condition	See Load Circuit	

OUTPUT LOAD CIRCUIT)



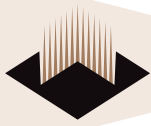


DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

0°C ≤ T_A ≤ +70°C; V_{CC} = V_{CCQ} = +2.5V ±0.2V
AC Operating Test Conditions

Parameter	Symbol	335		262		265		Unit	Note
		Min	Max	Min	Max	Min	Max		
Row cycle time	t _{RC}	60		65		65		ns	
Refresh row cycle time	t _{RFC}	72		75		75		ns	
Row active time	t _{RAS}	42	70K	45	120K	45	120K	ns	
RAS to CAS delay	t _{RCD}	18		20		20		ns	
Row precharge time	t _{RP}	18		20		20		ns	
Row active to Row active delay	t _{RRD}	12		15		15		ns	
Write recovery time	t _{WR}	15		15		15		ns	
Last data in to Read command	t _{WTR}	1		1		1		t _{CK}	
Col. address to Col. address delay	t _{CCD}	1		1		1		t _{CK}	
Clock cycle time	CL=2.0	7.5	12	7.5	12	10	12	ns	5
	CL=2.5	6	12	7.5	12	7.5	12	ns	5
Clock high level width	t _{CH}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
Clock low level width	t _{CL}	0.45	0.55	0.45	0.55	0.45	0.55	t _{CK}	
DQS-out access time from CK/CK#	t _{DQSK}	-0.6	+0.6	-0.75	+0.75	-0.75	+0.75	ns	
Output data access time from CK/CK#	t _{AC}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to output data edge	t _{DQSQ}	-	0.45	-	0.5	-	0.5	ns	5
Read Preamble	t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
Read Postamble	t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	
CK to valid DQS-in	t _{DQSS}	0.75	1.25	0.75	1.25	0.75	1.25	t _{CK}	
DQS-in setup time	t _{WPRES}	0		0		0		ns	2
DQS-in hold time	t _{WPRE}	0.25		0.25		0.25		t _{CK}	
DQS falling edge to CK rising-setup time	t _{DSS}	0.2		0.2		0.2		t _{CK}	
DQS falling edge from CK rising-hold time	t _{DSH}	0.2		0.2		0.2		t _{CK}	
DQS-in high level width	t _{DQSH}	0.35		0.35		0.35		t _{CK}	
DQS-in low level width	t _{DQSL}	0.35		0.35		0.35		t _{CK}	
DQS-in cycle time	t _{DSC}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}	
Address and Control Input setup time(fast)	t _{IS}	0.75		0.9		0.9		ns	6
Address and Control Input hold time(fast)	t _{IH}	0.75		0.9		0.9		ns	6
Address and Control Input setup time(slow)	t _{IS}	0.8		1.0		1.0		ns	6
Address and Control Input hold time(slow)	t _{IH}	0.8		1.0		1.0		ns	6
Data-out high impedance time from CK/CK#	t _{HZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data-out low impedance time from CK/CK#	t _{LZ}	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Input Slew Rate(for input only pins)	t _{SL(I)}	0.5		0.5		0.5		V/ns	6
Input Slew Rate(for I/O pins)	t _{SL(IO)}	0.5		0.5		0.5		V/ns	7
Output Slew Rate(x4,x8)	t _{SL(O)}	1.0	4.5	1.0	4.5	1.0	4.5	V/ns	
Output Slew Rate Matching Ratio(rise to fall)	t _{SLMR}	0.67	1.5	0.67	1.5	0.67	1.5		

AC Timing Parameters are based on Samsung components. Other DRAM Manufacturers parameters may be different.



DDR SDRAM COMPONENT ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (Continued)

0°C ≤ T_A ≤ 70°C, V_{CC} = +2.5V ±0.2V, V_{CCQ} = +2.5V ±0.2V

Parameter	Symbol	335		262		265		Unit	Note
		Min	Max	Min	Max	Min	Max		
Mode register set cycle time	t _{MRD}	12		15		15		ns	
DQ & DM setup time to DQS	t _{DS}	0.45		0.5		0.5		ns	7
DQ & DM hold time to DQS	t _{DH}	0.45		0.5		0.5		ns	7
Control & Address input pulse width	t _{IPW}	2.2		2.2		2.2		ns	
DQ & DM input pulse width	t _{DIPW}	1.75		1.75		1.75		ns	
Power down exit time	t _{PDEX}	6		7.5		7.5		ns	
Exit self refresh to non-Read command	t _{XSNR}	75		75		75		ns	4
Exit self refresh to read command	t _{XSRD}	200		200		200		t _{CK}	
Refresh interval time	t _{REFI}	7.8		7.8		7.8		us	1
Output DQS valid window	t _{QH}	t _{HP} -t _{QHS}	—	t _{HP} -t _{QHS}	—	t _{HP} -t _{QHS}	—	ns	5
Clock half period	t _{HP}	t _{CLmin} or t _{CHmin}	—	t _{CLmin} or t _{CHmin}	—	t _{CLmin} or t _{CHmin}	—	ns	
Data hold skew factor	t _{QHS}		0.55		0.75		0.75	ns	
DQS write postamble time	t _{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}	3
Active to Read with Auto precharge command	t _{RAP}	18		20		20			
Autoprecharge write recovery + Precharge time	t _{DAL}	(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		(t _{WR} /t _{CK}) + (t _{RP} /t _{CK})		t _{CK}	

- Maximum burst refresh cycle : 8
- The specific requirement is that DQS be valid (High or Low) on or before this CK edge. The case shown (DQS going from High_Z to logic Low) applies when no writes were previously in progress on the bus. If a previous write was in progress, DQS could be High at this time, depending on t_{DOSS}.
- The maximum limit for this parameter is not a device limit. The device will operate with a great value for this parameter, but system performance (bus turnaround) will degrade accordingly.
- A write command can be applied with t_{RCD} satisfied after this command.
- For registered DIMMs, t_{CL} and t_{CH} are ≥ 45% of the period including both the half period jitter (t_{JIT(HP)}) of the PLL and the half period jitter due to crosstalk (t_{JIT(crosstalk)}) on the DIMM.
- Input Setup/Hold Slew Rate Derating

Input Setup/Hold Slew Rate	Δt _{IS}	Δt _{IH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+50	+50
0.3	+100	+100

This derating table is used to increase t_{IS}/t_{IH} in the case where the input slew rate is below 0.5V/ns. Input setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

7. I/O Setup/Hold Slew Rate Derating

I/O Setup/Hold Slew Rate	Δt _{BS}	Δt _{BH}
(V/ns)	(ps)	(ps)
0.5	0	0
0.4	+75	+75
0.3	+150	+150

This derating table is used to increase t_{BS}/t_{BH} in the case where the I/O slew rate is below 0.5V/ns. I/O setup/hold slew rate based on the lesser of AC-AC slew rate and DC-DC slew rate.

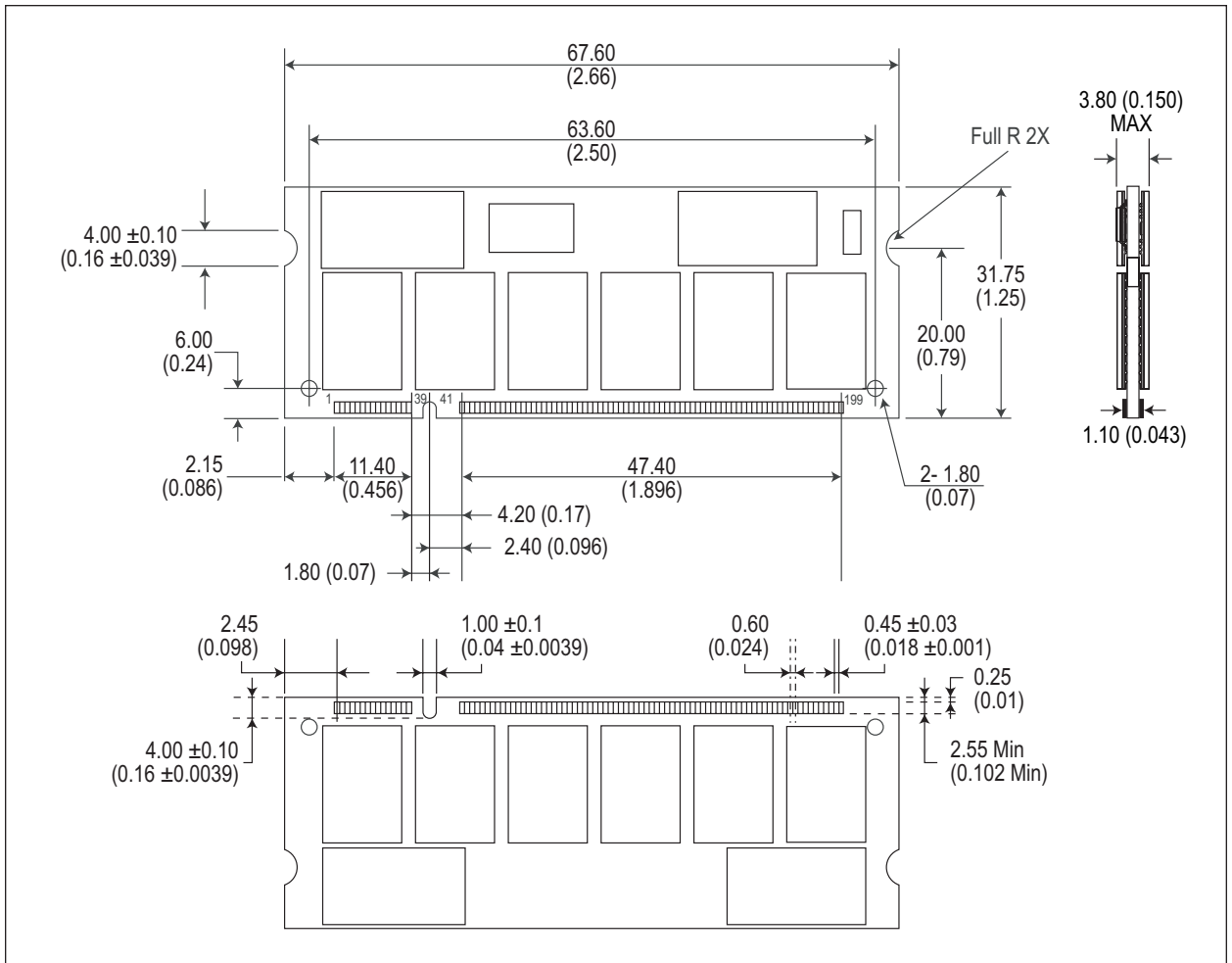


ORDERING INFORMATION FOR D4

Part Number	Speed	CAS Latency	t _{RC} D	t _{RP}	Height*
WV3EG232M64EFSU335D4xG	166MHz/333Mbps	2.5	3	3	31.75 (1.25") MAX
WV3EG232M64EFSU262D4xG	133MHz/266Mbps	2	2	2	31.75 (1.25") MAX
WV3EG232M64EFSU265D4xG	133MHz/266Mbps	2.5	3	3	31.75 (1.25") MAX

- NOTES:
- Consult Factory for availability of RoHS compliant products. (G = RoHS Compliant)
 - Vendor specific part numbers are used to provide memory components source control. The place holder for this is shown as lower case "x" in the part numbers above and is to be replaced with the respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
 - Consult factory for availability of industrial temperature (-40°C to 85°C) option

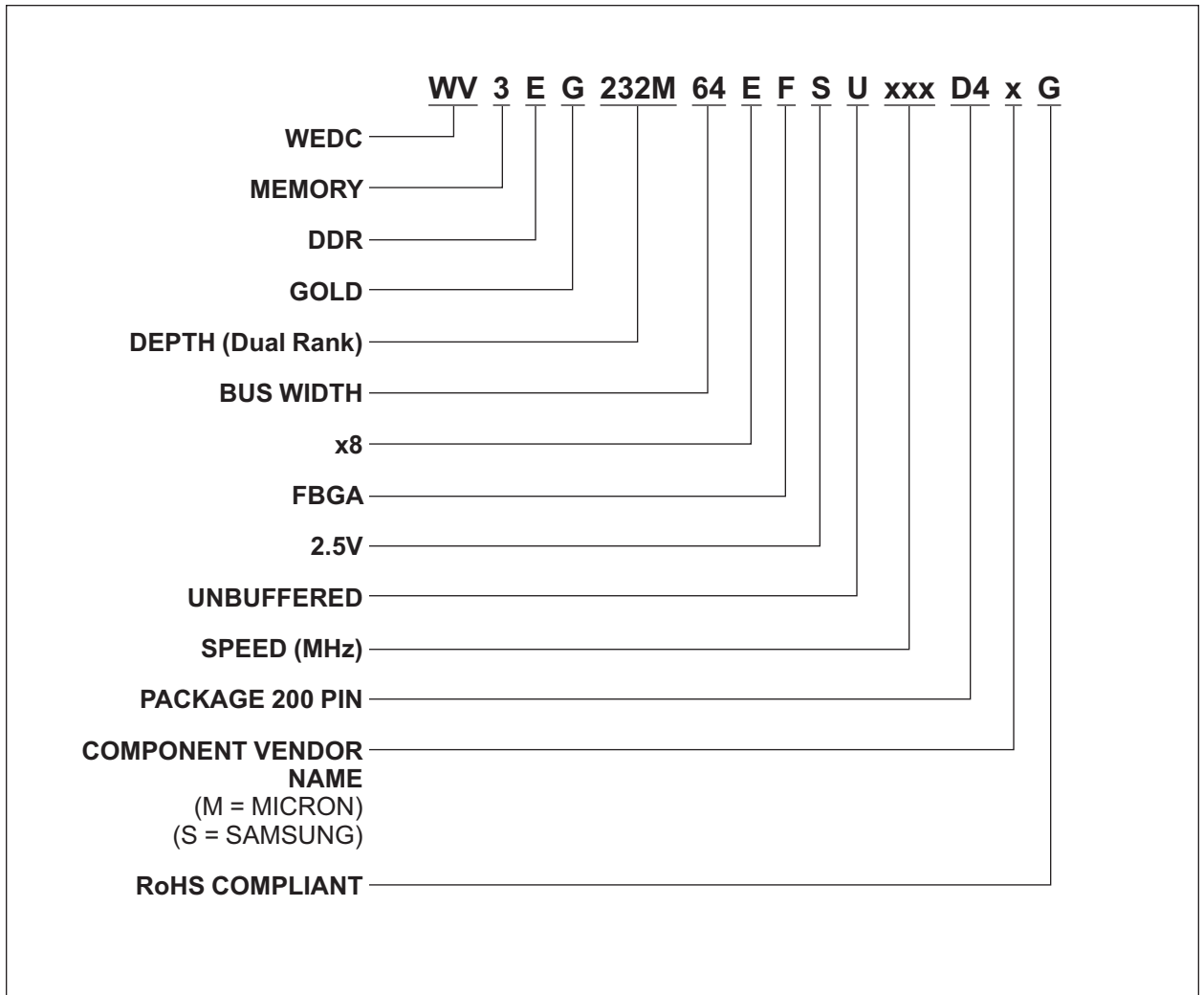
200-PIN DDR2 SODIMM DIMENSIONS



* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





Document Title

512MB – 2x32Mx64 DDR SDRAM, UNBUFFERED, w/PLL, FBGA

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	4-05	Advanced