

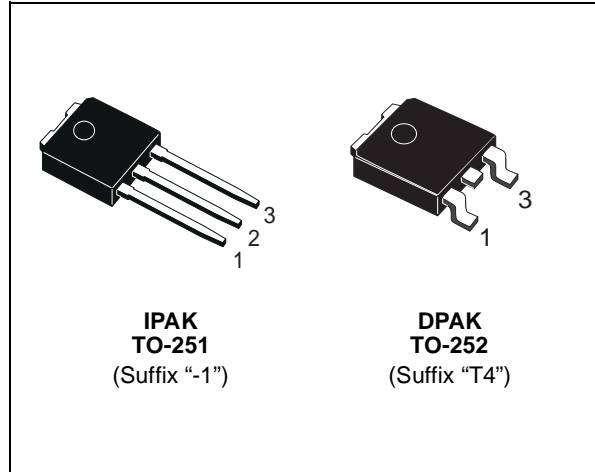


STD50NH02L

N-CHANNEL 24V - 0.0085 Ω - 50A DPAK/IPAK STripFET™ III POWER MOSFET

TYPE	V _{DSS}	R _{DS(on)}	I _D
STD50NH02L	24 V	< 0.0105 Ω	50 A

- TYPICAL R_{DS(on)} = 0.0085 Ω @ 10 V
- TYPICAL R_{DS(on)} = 0.012 Ω @ 5 V
- R_{DS(ON)} * Q_g INDUSTRY'S BENCHMARK
- CONDUCTION LOSSES REDUCED
- SWITCHING LOSSES REDUCED
- LOW THRESHOLD DEVICE
- THROUGH-HOLE IPAK (TO-251) POWER PACKAGE IN TUBE (SUFFIX "-1")
- SURFACE-MOUNTING DPAK (TO-252) POWER PACKAGE IN TAPE & REEL (SUFFIX "T4")



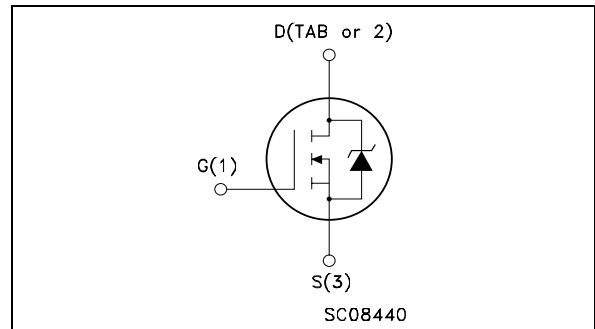
DESCRIPTION

The STD50NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This is suitable for the most demanding DC-DC converter application where high efficiency is to be achieved.

APPLICATIONS

- SPECIFICALLY DESIGNED AND OPTIMISED FOR HIGH EFFICIENCY DC/DC CONVERTERS

INTERNAL SCHEMATIC DIAGRAM



Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD50NH02LT4	D50NH02L	TO-252	TAPE & REEL
STD50NH02L-1	D50NH02L	TO-251	TUBE

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{spike(1)}	Drain-source Voltage Rating	30	V
V _{DS}	Drain-source Voltage (V _{GS} = 0)	24	V
V _{DGR}	Drain-gate Voltage (R _{GS} = 20 kΩ)	24	V
V _{GS}	Gate- source Voltage	± 20	V
I _D	Drain Current (continuous) at T _C = 25°C	50	A
I _D	Drain Current (continuous) at T _C = 100°C	36	A
I _{DM(2)}	Drain Current (pulsed)	200	A
P _{tot}	Total Dissipation at T _C = 25°C	60	W
	Derating Factor	0.4	W/°C
E _{AS (3)}	Single Pulse Avalanche Energy	280	mJ
T _{stg}	Storage Temperature	-55 to 175	°C
T _j	Max. Operating Junction Temperature		

STD50NH02L

THERMAL DATA

Rthj-case	Thermal Resistance Junction-case	Max	2.5	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	100	°C/W
T _I	Maximum Lead Temperature For Soldering Purpose		275	°C

ELECTRICAL CHARACTERISTICS (T_{CASE} = 25 °C UNLESS OTHERWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source Breakdown Voltage	I _D = 25 mA, V _{GS} = 0	24			V
I _{DSS}	Zero Gate Voltage Drain Current (V _{GS} = 0)	V _{DS} = 20 V V _{DS} = 20 V T _C = 125°C			1 10	μA μA
I _{GSS}	Gate-body Leakage Current (V _{DS} = 0)	V _{GS} = ± 20V			±100	nA

ON (4)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} I _D = 250 μA	1	1.8		V
R _{DS(on)}	Static Drain-source On Resistance	V _{GS} = 10 V I _D = 25 A V _{GS} = 5 V I _D = 12.5 A		0.0085 0.012	0.0105 0.020	Ω Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g _{fs} (4)	Forward Transconductance	V _{DS} = 15 V I _D = 25 A		27		S
C _{iss} C _{oss} C _{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V _{DS} = 16V f = 1 MHz V _{GS} = 0		1400 400 55		pF pF pF
R _G	Gate Input Resistance	f = 1 MHz Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		1		Ω

STD50NH02L

ELECTRICAL CHARACTERISTICS (continued)

SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	$V_{DD} = 10\text{ V}$ $I_D = 25\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		10 130		ns ns
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 10\text{ V}$ $I_D = 50\text{ A}$ $V_{GS} = 10\text{ V}$		24 5 3.4	32	nC nC nC
$Q_{oss}^{(5)}$	Output Charge	$V_{DS} = 16\text{ V}$ $V_{GS} = 0\text{ V}$		9.4		nC

SWITCHING OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	$V_{DD} = 10\text{ V}$ $I_D = 25\text{ A}$ $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		27 16	21.6	ns ns

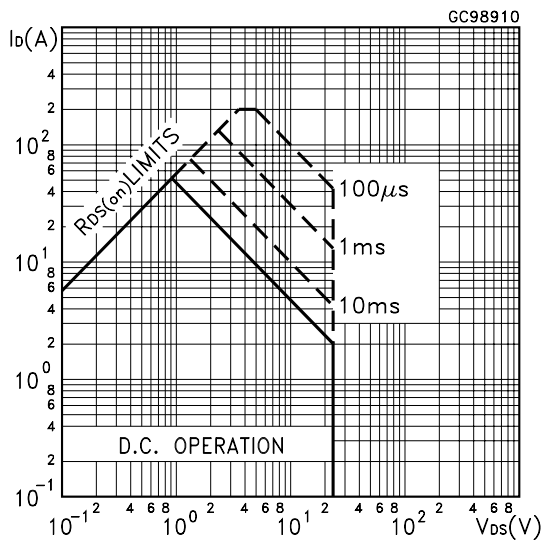
SOURCE DRAIN DIODE

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}	Source-drain Current Source-drain Current (pulsed)				50 200	A A
$V_{SD}^{(4)}$	Forward On Voltage	$I_{SD} = 25\text{ A}$ $V_{GS} = 0$			1.3	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 50\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 20\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		36 36 2		ns nC A

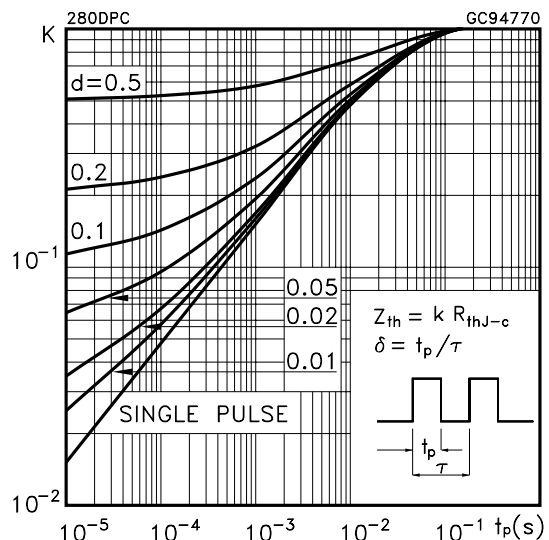
(1) Guaranteed when external $R_g=4.7\ \Omega$ and $t_f < t_{fmax}$.
 (2) Pulse width limited by safe operating area
 (3) Starting $T_j = 25\ ^\circ\text{C}$, $I_D = 25\text{ A}$, $V_{DD} = 15\text{ V}$

(4) Pulsed: Pulse duration = 300 μs , duty cycle 1.5 %.
 (5) $Q_{oss} = C_{oss} \cdot \Delta V_{in}$, $C_{oss} = C_{gd} + C_{ds}$. See Appendix A

Safe Operating Area

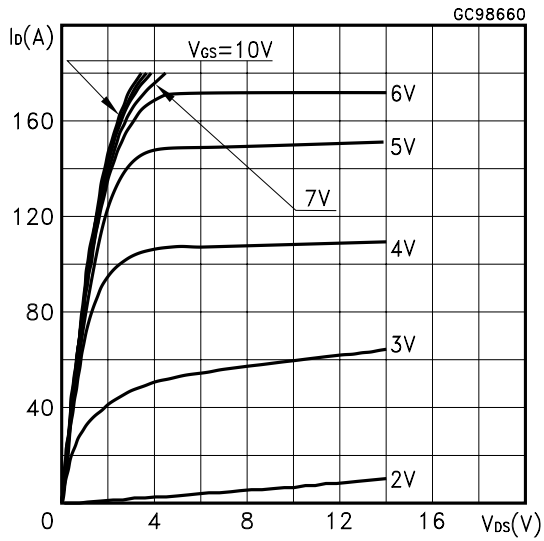


Thermal Impedance

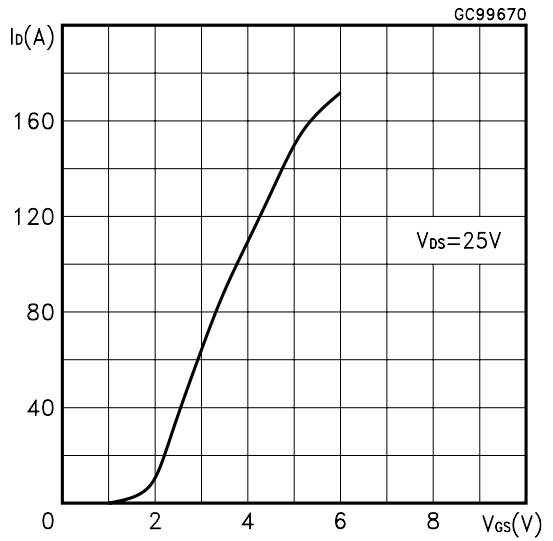


STD50NH02L

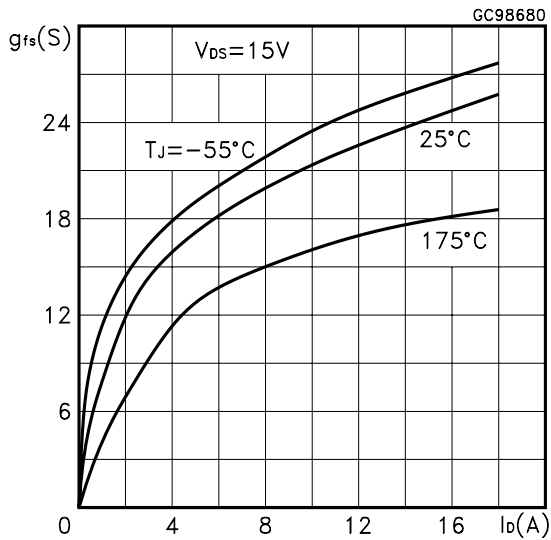
Output Characteristics



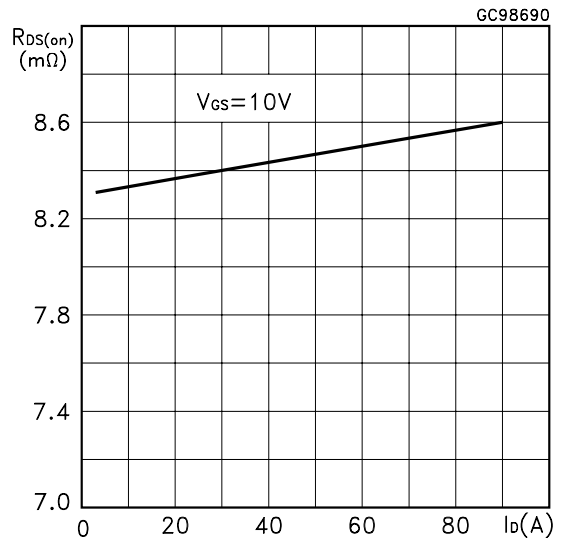
Transfer Characteristics



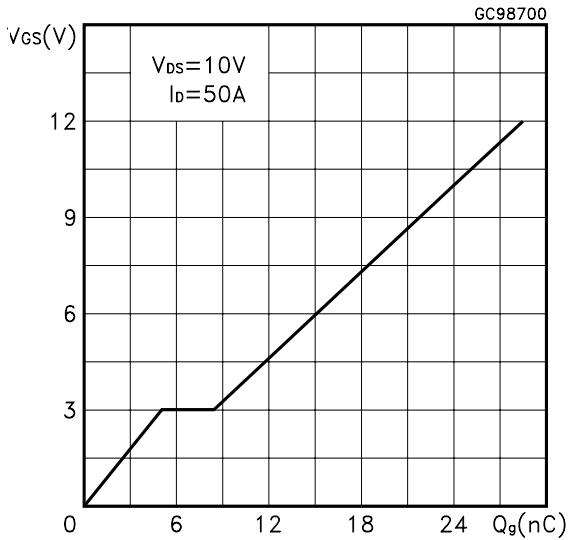
Transconductance



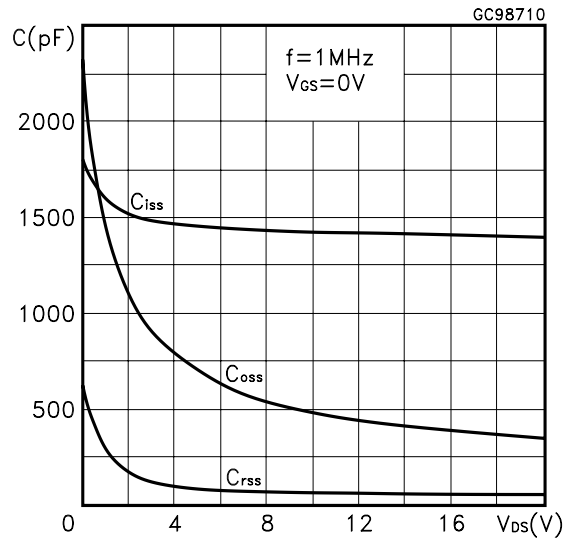
Static Drain-source On Resistance



Gate Charge vs Gate-source Voltage

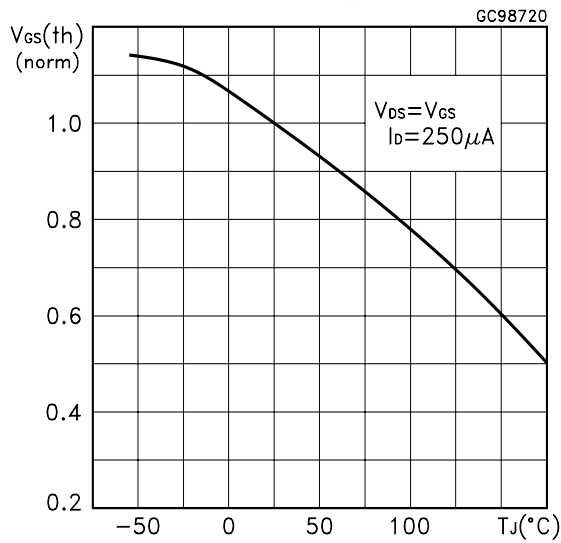


Capacitance Variations

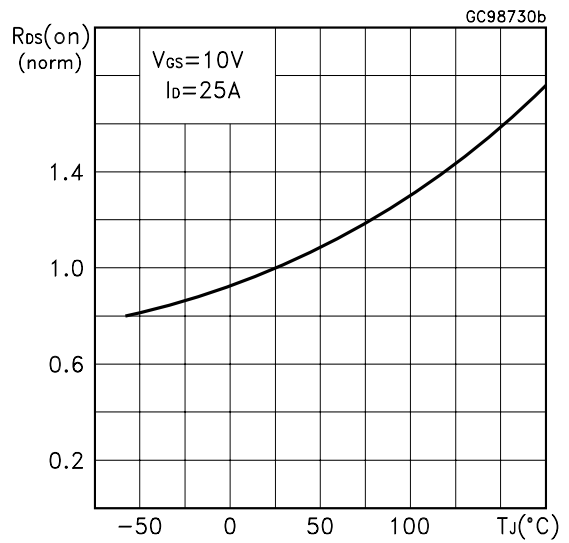


STD50NH02L

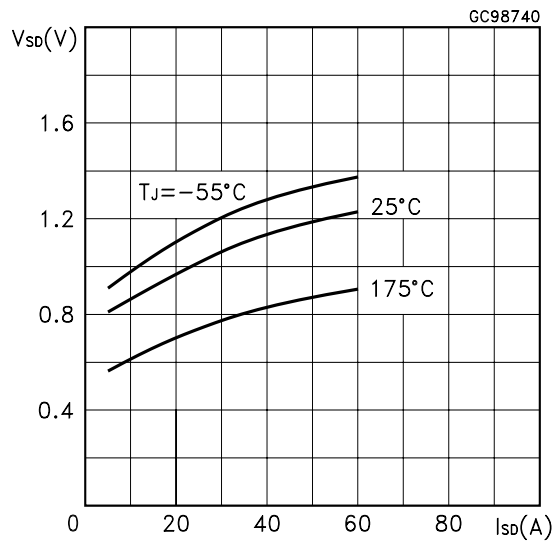
Normalized Gate Threshold Voltage vs Temperature



Normalized on Resistance vs Temperature



Source-drain Diode Forward Characteristics



Normalized Breakdown Voltage vs Temperature

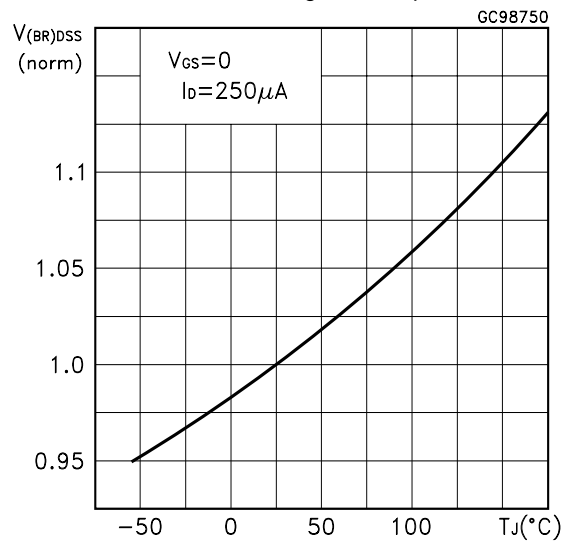


Fig. 1: Unclamped Inductive Load Test Circuit



Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuits For Resistive Load

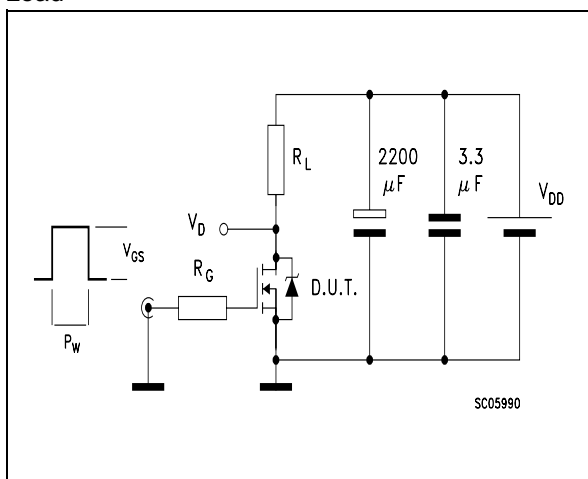


Fig. 4: Gate Charge test Circuit

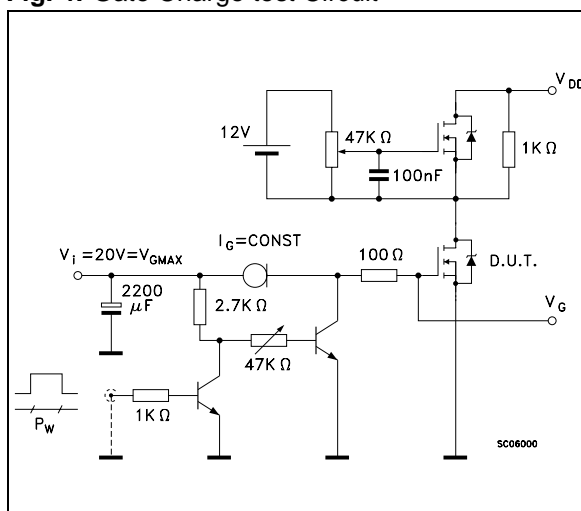
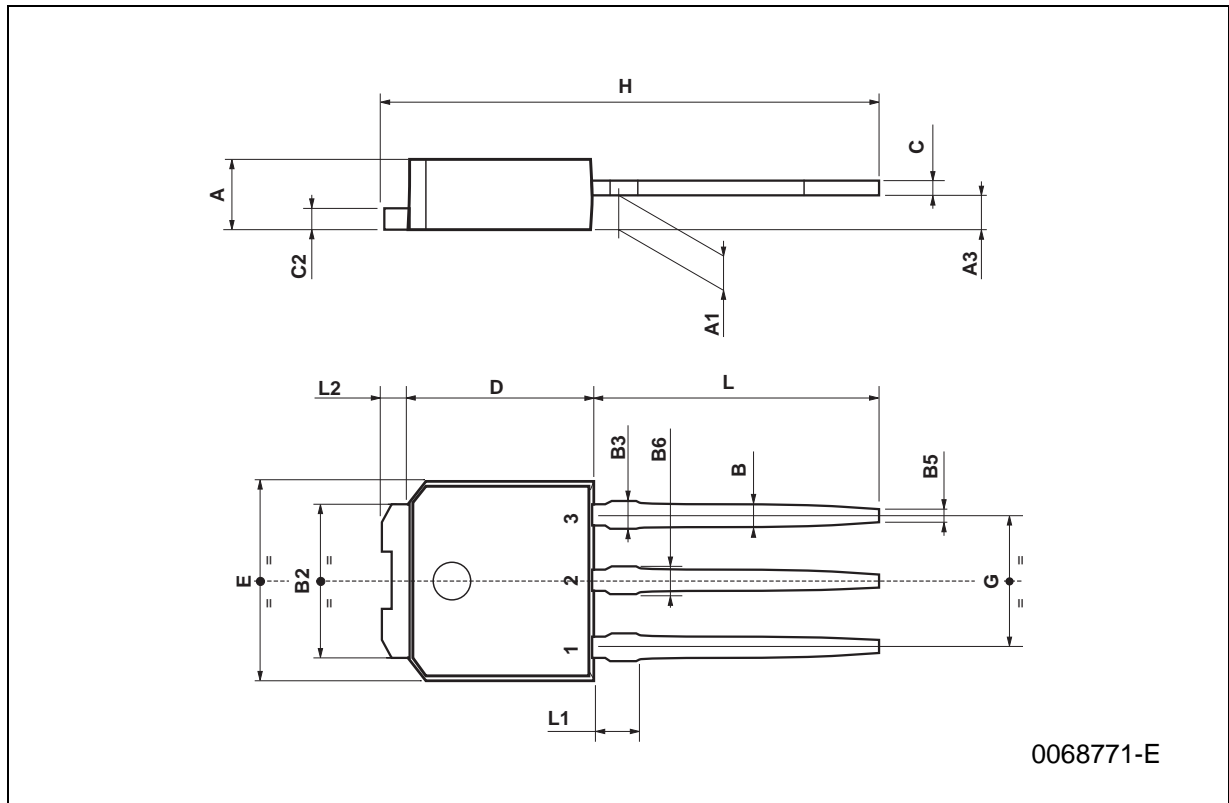


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



TO-251 (IPAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039

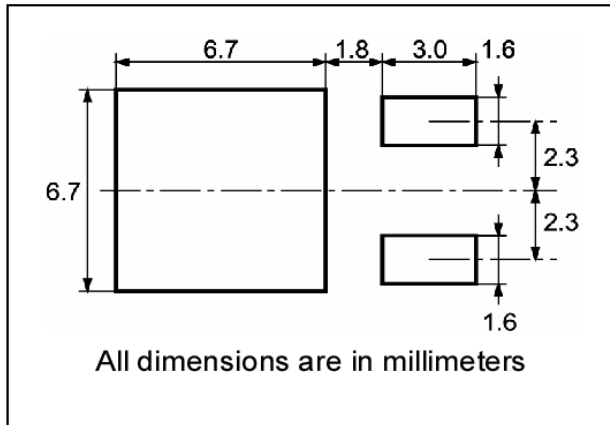


TO-252 (DPAK) MECHANICAL DATA

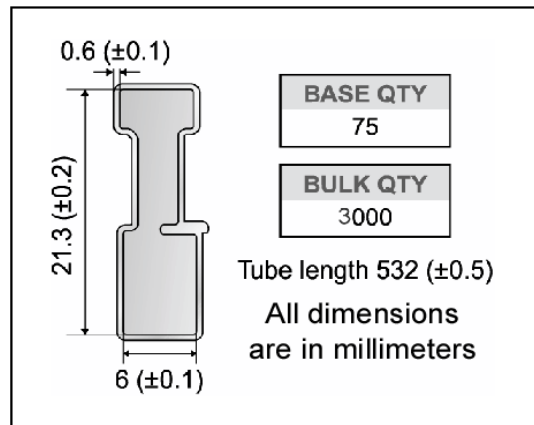
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.9	0.025		0.035
B2	5.2		5.4	0.204		0.212
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	9.35		10.1	0.368		0.397
L2		0.8			0.031	
L4	0.6		1	0.023		0.039



DPAK FOOTPRINT



TUBE SHIPMENT (no suffix)*



TAPE AND REEL SHIPMENT (suffix "T4")*

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

REEL MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
1000	1000

TAPE MECHANICAL DATA

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

Center line of cavity

TRL

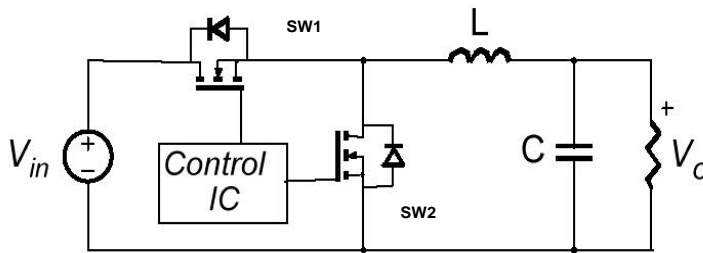
FEED DIRECTION

Bending radius R min.

For machine ref. only including draft and radii concentric around B0

APPENDIX A

Buck Converter: Power Losses Estimation



The power losses associated with the FETs in a Synchronous Buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

The low side (SW2) device requires:

- Very low $R_{DS(on)}$ to reduce conduction losses
- Small Q_{gls} to reduce the gate charge losses
- Small C_{oss} to reduce losses due to output capacitance
- Small Q_{rr} to reduce losses on SW₁ during its turn-on
- The C_{gd}/C_{gs} ratio lower than V_{th}/V_{gg} ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;

The high side (SW1) device requires:

- Small R_g and L_s to allow higher gate current peak and to limit the voltage feedback on the gate
- Small Q_g to have a faster commutation and to reduce gate charge losses
- Low $R_{DS(on)}$ to reduce the conduction losses.

STD50NH02L

		High Side Switch (SW1)	Low Side Switch (SW2)
$P_{\text{conduction}}$		$R_{\text{DS(on)SW1}} * I_L^2 * d$	$R_{\text{DS(on)SW2}} * I_L^2 * (1-d)$
$P_{\text{switching}}$		$V_{\text{in}} * (Q_{\text{gsth(SW1)}} + Q_{\text{gd(SW1)}}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
P_{diode}	Recovery	Not Applicable	$^1 V_{\text{in}} * Q_{\text{rr(SW2)}} * f$
	Conduction	Not Applicable	$V_{\text{f(SW2)}} * I_L * t_{\text{deadtime}} * f$
$P_{\text{gate(Q}_G)}$		$Q_{\text{g(SW1)}} * V_{\text{gg}} * f$	$Q_{\text{gls(SW2)}} * V_{\text{gg}} * f$
P_{Qoss}		$\frac{V_{\text{in}} * Q_{\text{oss(SW1)}} * f}{2}$	$\frac{V_{\text{in}} * Q_{\text{oss(SW2)}} * f}{2}$

Parameter	Meaning
d	Duty-cycle
Q_{gsth}	Post threshold gate charge
Q_{gls}	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
PQoss	Output capacitance losses

¹ Dissipated by SW1 during turn-on

Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

The ST logo is registered trademark of STMicroelectronics
© 2003 STMicroelectronics - All Rights Reserved

All other names are the property of their respective owners.

STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco -
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

<http://www.st.com>