Features

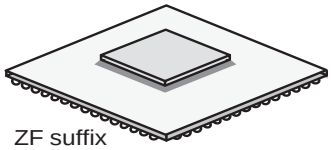
- **18.1SPECint95, Estimates 12.3 SPECfp95 at 400 MHz (PC755)**
- **15.7SPECint95, 9SPECfp95 at 350 MHz (PC745)**
- **733 MIPS at 400 MHz (PC755) at 641 MIPS at 350 MHz (PC745)**
- **Selectable Bus Clock (12 CPU Bus Dividers up to 10x)**
- **P_D Typical 6.4W at 400 MHz, Full Operating Conditions**
- **Nap, Doze and Sleep Modes for Power Savings**
- **Superscalar (3 Instructions per Clock Cycle) Two Instruction + Branch**
- **4 Beta Byte Virtual Memory, 4-GByte of Physical Memory**
- **64-bit Data and 32-bit Address Bus Interface**
- **32-KB Instruction and Data Cache**
- **Six Independent Execution Units**
- **Write-back and Write-through Operations**
- **f_{INT} max = 400 MHz (TBC)**
- **f_{BUS} max = 100 MHz**
- **Voltage I/O 2.5V/3.3V; Voltage Int 2.0V**

Description

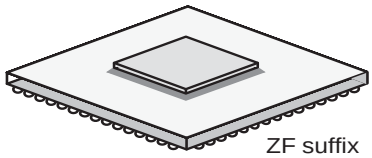
The PC755 and PC745 PowerPC® microprocessors are high-performance, low-power, 32-bit implementations of the PowerPC Reduced Instruction Set Computer (RISC) architecture, especially enhanced for embedded applications.

The PC755 and PC745 microprocessors differ only in that the PC755 features an enhanced, dedicated L2 cache interface with on-chip L2 tags. The PC755 is a drop-in replacement for the award winning PowerPC 750™ microprocessor and is footprint and user software code compatible with the MPC7400 microprocessor with AltiVec™ technology. The PC745 is a drop-in replacement for the PowerPC 740™ microprocessor and is also footprint and user software code compatible with the PowerPC 603e™ microprocessor. PC755/745 microprocessors provide on-chip debug support and are fully JTAG-compliant.

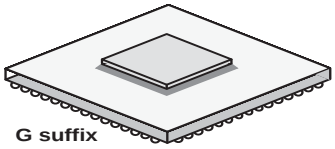
The PC745 microprocessor is pin compatible with the TSPC603e family.



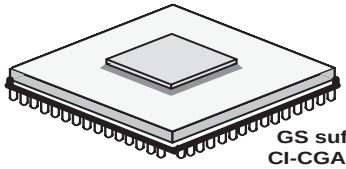
ZF suffix
PBGA255
Flip-Chip Plastic Ball Grid Array



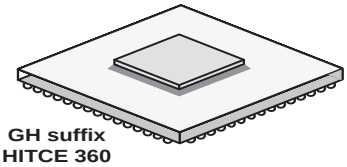
ZF suffix
PBGA360
Flip-Chip Plastic Ball Grid Array



G suffix
CBGA360
Ceramic Ball Grid Array



GS suffix
CI-CGA360
Ceramic Ball Grid Array with
Solder Column Interposer (SCI)



GH suffix
HITCE 360
Ceramic Ball Grid Array

PowerPC 755/745 RISC Microprocessor

PC755/745 Preliminary β-site

Rev. 2138D–HIREL–06/03

Screening

This product is manufactured in full compliance with:

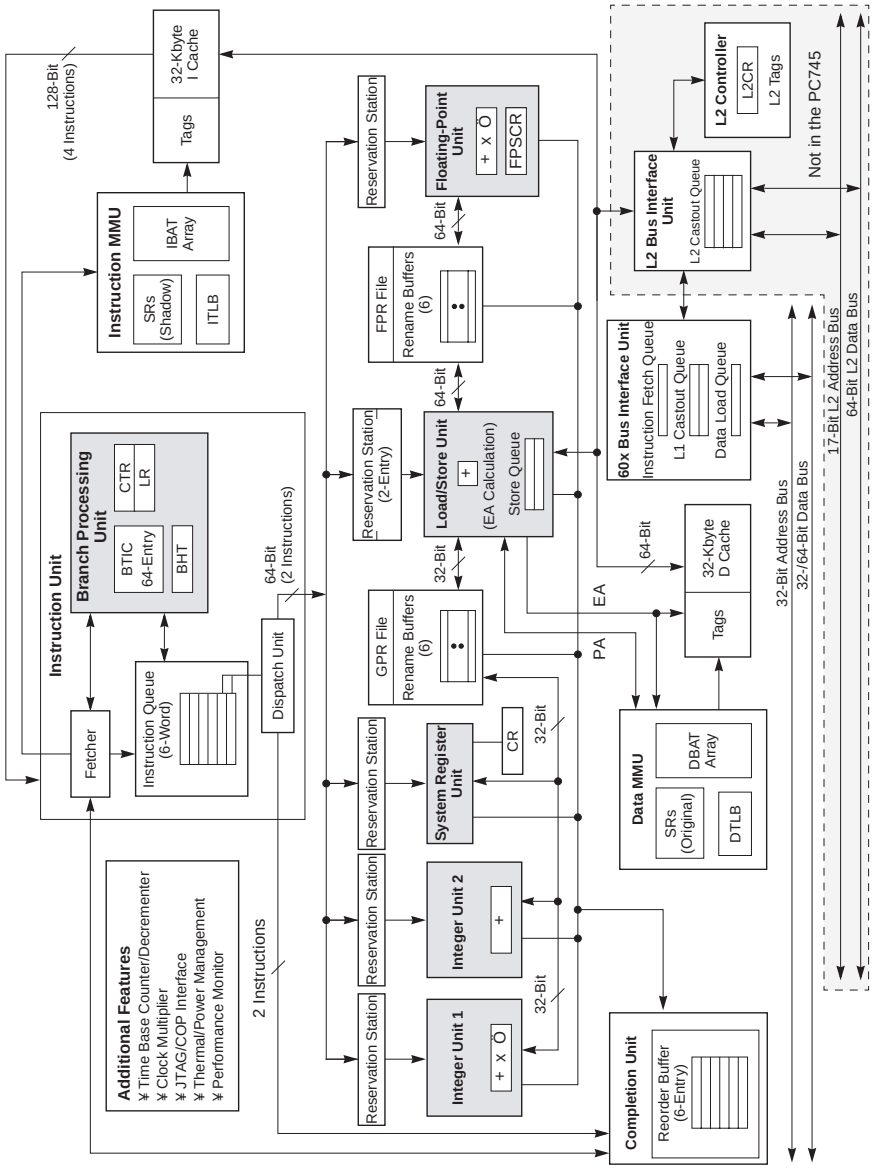
- CBGA + CI-CGA + FC-PBGA up screenings based upon Atmel standards
- HiTCE
- Full military temperature range (Tj = -55°C,+125°C)
  industrial temperature range (Tj = -40°C,+110°C)

General Description

Simplified Block Diagram

The PC755 is targeted for low power systems and supports power management features such as doze, nap, sleep, and dynamic power management. The PC755 consists of a processor core and an internal L2 Tag combined with a dedicated L2 cache interface and a 60x bus.

Figure 1. PC755 Block Diagram



General Parameters

The following list provides a summary of the general parameters of the PC755:

Technology	0.22 µm CMOS, six-layer metal
Die size	6.61 mm x 7.73 mm (51 mm^2)
Transistor count	6.75 million
Logic design	Fully-static Packages
PC745	Surface mount 255 Plastic Ball Grid Array (PBGA)
PC755	Surface mount 360 Plastic Ball Grid Array (PBGA) Surface mount 360 Ceramic Ball Grid Array (CI-CGA, CBGA, HiTCE)
Core power supply	2V ± 100 mV DC (nominal; some parts support core voltages down to 1.8V; see Table 5 for recommended operating conditions)
I/O power supply	2.5V ± 100 mV DC or 3.3V ± 165 mV DC (input thresholds are configuration pin selectable)

Features

This section summarizes features of the PC755's implementation of the PowerPC architecture. Major features of the PC755 are as follows:

- Branch Processing Unit
  - Four instructions fetched per clock
  - One branch processed per cycle (plus resolving 2 speculations)
  - Up to 1 speculative stream in execution, 1 additional speculative stream in fetch
  - 512-entry branch history table (BHT) for dynamic prediction
  - 64-entry, 4-way set associative Branch Target Instruction Cache (BTIC) for eliminating branch delay slots
- Dispatch Unit
  - Full hardware detection of dependencies (resolved in the execution units)
  - Dispatch two instructions to six independent units (system, branch, load/store, fixed-point unit 1, fixed-point unit 2, floating-point)
  - Serialization control (predispatch, postdispatch, execution serialization)
- Decode
  - Register file access
  - Forwarding control
  - Partial instruction decode
- Completion
  - 6 entry completion buffer
  - Instruction tracking and peak completion of two instructions per cycle
  - Completion of instructions in program order while supporting out-of-order instruction execution, completion serialization and all instruction flow changes
- Fixed Point Units (FXUs) that share 32 GPRs for Integer Operands
  - Fixed Point Unit 1 (FXU1)-multiply, divide, shift, rotate, arithmetic, logical
  - Fixed Point Unit 2 (FXU2)-shift, rotate, arithmetic, logical

  - Single-cycle arithmetic, shifts, rotates, logical
  - Multiply and divide support (multi-cycle)
  - Early out multiply
- Floating-point Unit and a 32-entry FPR File
  - Support for IEEE-754 standard single and double precision floating point arithmetic
  - Hardware support for divide
  - Hardware support for denormalized numbers
  - Single-entry reservation station
  - Supports non-IEEE mode for time-critical operations
- System Unit
  - Executes CR logical instructions and miscellaneous system instructions
  - Special register transfer instructions
- Load/Store Unit
  - One cycle load or store cache access (byte, half-word, word, double-word)
  - Effective address generation
  - Hits under misses (one outstanding miss)
  - Single-cycle unaligned access within double word boundary
  - Alignment, zero padding, sign extend for integer register file
  - Floating point internal format conversion (alignment, normalization)
  - Sequencing for load/store multiples and string operations
  - Store gathering
  - Cache and TLB instructions
  - Big and Little-endian byte addressing supported
  - Misaligned Little-endian supported
  - Level 1 Cache structure
  - 32K, 32 bytes line, 8-way set associative instruction cache (iL1)
  - 32K, 32 bytes line, 8-way set associative data cache (dL1)
  - Cache locking for both instruction and data caches, selectable by group of ways
  - Single-cycle cache access
  - Pseudo least-recently used (PLRU) replacement
  - Copy-back or Write Through data cache (on a page per page basis)
  - Supports all PowerPC memory coherency modes
  - Non-Blocking instruction and data cache (one outstanding miss under hits)
  - No snooping of instruction cache
- Level 2 (L2) Cache Interface (not implemented on PC745)
  - Internal L2 cache controller and tags; external data SRAMs
  - 256K, 512K, and 1-Mbyte 2-way set associative L2 cache support
  - Copyback or write-through data cache (on a page basis, or for all L2)
  - Instruction-only mode and data-only mode.
  - 64 bytes (256K/512K) or 128 bytes (1M) sectored line size

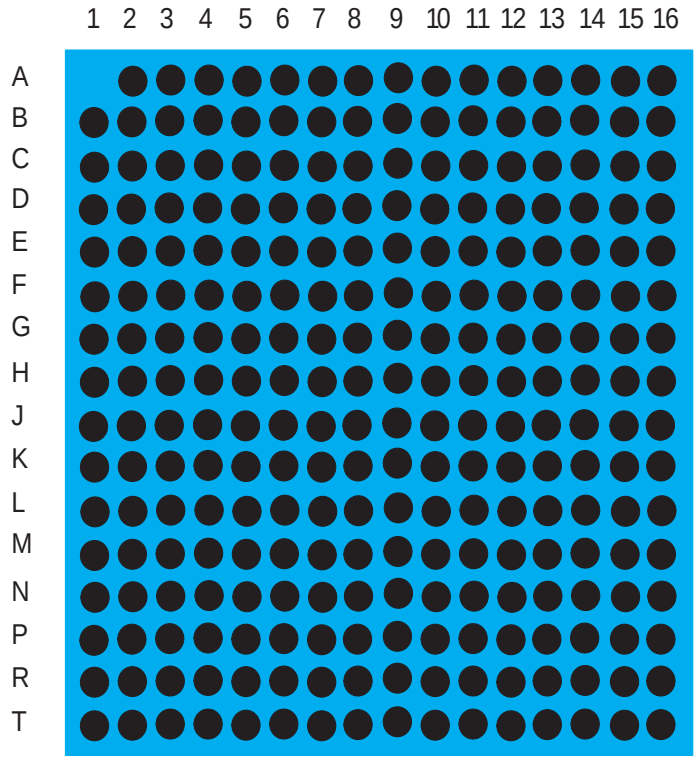
  - Supports flow through (register-buffer) synchronous burst SRAMs, pipelined (register-register) synchronous burst SRAMs (3-1-1-1 or strobeless 4-1-1-1) and pipelined (register-register) late-write synchronous burst SRAMs
  - L2 configurable to direct mapped SRAM interface or split cache/direct mapped or private memory
  - Core-to-L2 frequency divisors of 1, 1.5, 2, 2.5, and 3 supported
  - 64-bit data bus
  - Selectable interface voltages of 2.5V and 3.3V
  - Parity checking on both L2 address and data
- Memory Management Unit
  - 128 entry, 2-way set associative instruction TLB
  - 128 entry, 2-way set associative data TLB
  - Hardware reload for TLBs
  - Hardware or optional software tablewalk support
  - 8 instruction BATs and 8 data BATs
  - 8 SPRGs, for assistance with software tablewalks
  - Virtual memory support for up to 4 hexabytes (2^{52}) of virtual memory
  - Real memory support for up to 4 gigabytes (2^{32}) of physical memory
- Bus Interface
  - Compatible with 60X processor interface
  - 32-bit address bus
  - 64-bit data bus, 32-bit mode selectable
  - Bus-to-core frequency multipliers of 2x, 3x, 3.5x, 4x, 4.5x, 5x, 5.5x, 6x, 6.5x, 7x, 7.5x, 8x, 10x supported
  - Selectable interface voltages of 2.5V and 3.3V.
  - Parity checking on both address and data busses
- Power Management
  - Low-power design with thermal requirements very similar to PC740/750.
  - Selectable interface voltage of 1.8V/2.0V can reduce power in output buffers (compared to 3.3V)
  - Three static power saving modes: doze, nap, and sleep
  - Dynamic power management
- Testability
  - LSSD scan design
  - IEEE 1149.1 JTAG interface
- Integrated Thermal Management Assist Unit
  - One-ship thermal sensor and control logic
  - Thermal Management Interrupt for software regulation of junction temperature

Pin Assignments

Figure 2 (in part A) shows the pinout of the PC745, 255PBGA package as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

Figure 2. Pinout of the PC745, 255 PBGA Package as Viewed from the Top Surface

Part A



Not to Scale

Part B

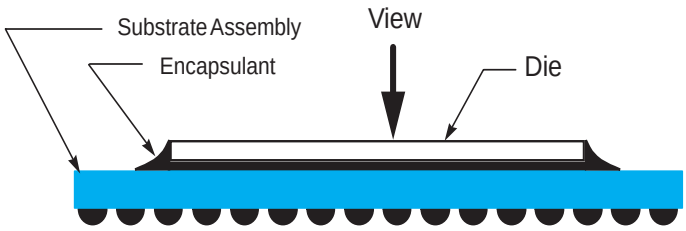
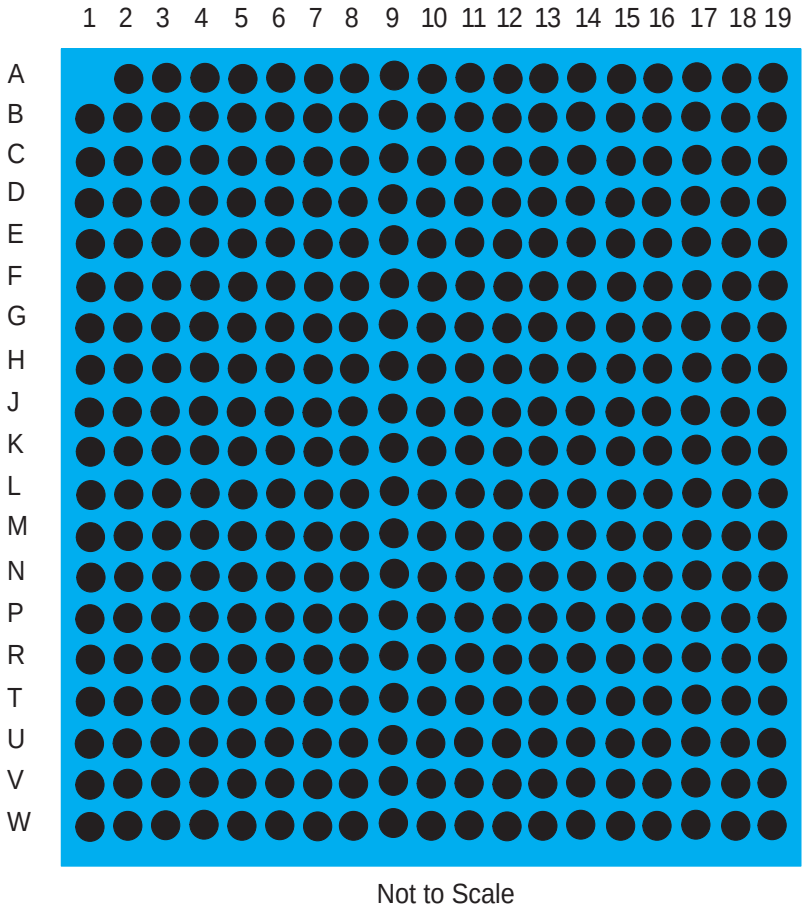


Figure 3 (in part A) shows the pinout of the PC755, 360 PBGA packages as viewed from the top surface. Part B shows the side profile of the PBGA package to indicate the direction of the top surface view.

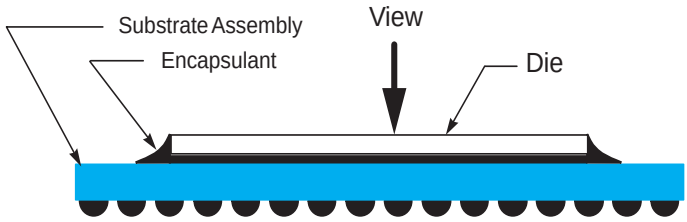
Figure 3. Pinout of the PC755, 360 PBGA, CBGA and CI-CGA Packages as Viewed from the Top Surface

Part A



Not to Scale

Part B



Pinout Listings Table 1 provides the pinout listing for the PC745, 255 PBGA package.

Table 1. Pinout Listing for the PC745, 255 PBGA Package

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported(1)	
				1.8V/2.0V	3.3V
A[0-31]	C16, E4, D13, F2, D14, G1, D15, E2, D16, D4, E13, G2, E15, H1, E16, H2, F13, J1, F14, J2, F15, H3, F16, F4, G13, K1, G15, K2, H16, M1, J15, P1	High	I/O	–	–
AACK	L2	Low	Input	–	–
ABB	K4	Low	I/O	–	–
AP[0-3]	C1, B4, B3, B2	High	I/O	–	–
ARTRY	J4	Low	I/O	–	–
AVDD	A10	–	–	2V	2V
BG	L1	Low	Input	–	–
BR	B6	Low	Output	–	–
BVSEL(3)(4)(5)	B1	High	Input	GND	3.3V
CI	E1	Low	Output	–	–
CKSTP_IN	D8	Low	Input	–	–
CKSTP_OUT	A6	Low	Output	–	–
CLK_OUT	D7	–	Output	–	–
DBB	J14	Low	I/O	–	–
DBG	N1	Low	Input	–	–
DBDIS	H15	Low	Input	–	–
DBWO	G4	Low	Input	–	–
DH[0-31]	P14, T16, R15, T15, R13, R12, P11, N11, R11, T12, T11, R10, P9, N9, T10, R9, T9, P8, N8, R8, T8, N7, R7, T7, P6, N6, R6, T6, R5, N5, T5, T4	High	I/O	–	–
DL[0-31]	K13, K15, K16, L16, L15, L13, L14, M16, M15, M13, N16, N15, N13, N14, P16, P15, R16, R14, T14, N10, P13, N12, T13, P3, N3, N4, R3, T1, T2, P4, T3, R4	High	I/O	–	–
DP[0-7]	M2, L3, N2, L4, R1, P2, M4, R2	High	I/O	–	–
DRTRY	G16	Low	Input	–	–
GBL	F1	Low	I/O	–	–
GND	C5, C12, E3, E6, E8, E9, E11, E14, F5, F7, F10, F12, G6, G8, G9, G11, H5, H7, H10, H12, J5, J7, J10, J12, K6, K8, K9, K11, L5, L7, L10, L12, M3, M6, M8, M9, M11, M14, P5, P12				
$\overline{\text{HRESET}}$	A7	Low	Input	–	–
INT	B15	Low	Input	–	–
L1_TSTCLK(2)	D11	High	Input	–	–
L2_TSTCLK(2)	D12	High	Input	–	–
LSSD_MODE(2)	B10	Low	Input	–	-–

Table 1. Pinout Listing for the PC745, 255 PBGA Package (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported(1)	
				1.8V/2.0V	3.3V
MCP	C13	Low	Input	–	–
NC (No-Connect)	B7, B8, C3, C6, C8, D5, D6, H4, J16, A4, A5, A2, A3, B5	–	–	–	–
OVDD	C7, E5, E7, E10, E12, G3, G5, G12, G14, K3, K5, K12, K14, M5, M7, M10, M12, P7, P10	–	–	1.8V/2.0V	3.3V
PLL_CFG[0-3]	A8, B9, A9, D9	High	Input	–	–
$\overline{\text{QACK}}$	D3	Low	Input	–	–
QREQ	J3	Low	Output	–	–
RSRV	D1	Low	Output	–	–
SMI	A16	Low	Input	–	–
SRESET	B14	Low	Input	–	–
SYSCLK	C9	–	Input	–	–
TA	H14	Low	Input	–	–
TBEN	C2	High	Input	–	–
TBST	A14	Low	I/O	–	–
TCK	C11	High	Input	–	–
TDI(5)	A11	High	Input	–	–
TDO	A12	High	Output	–	–
TEA	H13	Low	Input	–	–
TLBISYNC	C4	Low	Input	–	–
TMS(5)	B11	High	Input	–	–
$\overline{\text{TRST}}$(5)	C10	Low	Input	–	–
TS	J13	Low	I/O	–	–
TSIZ[0-2]	A13, D10, B12	High	Output	–	–
TT[0-4]	B13, A15, B16, C14, C15	High	I/O	–	–
WT	D2	Low	Output	–	–
V_{DD} 2	F6, F8, F9, F11, G7, G10, H6, H8, H9, H11, J6, J8, J9, J11, K7, K10, L6, L8, L9, L11	–	–	2V	2V
VOLTDET(6)	F3	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals and V_{DD} supplies power to the processor core and the PLL (after filtering to become AVDD). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL pin configuration of Table 4 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see Table 3.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. Uses one of 15 existing no-connects in PC745's 255-BGA package.
5. Internal pull up on die.
6. Internally tied to GND in the PC745 255-BGA package to indicate to the power supply that a low-voltage processor is present. This signal is not a power supply input.

Table 2 provides the pinout listing for the PC755, 360 PBGA, CBGA and CI-CGA + HiTCE

Table 2. Pinout Listing for the PC755, 360 PBGA, CBGA and CI-CGA Packages + HiTCE[8]

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
A[0-31]	A13, D2, H11, C1, B13, F2, C13, E5, D13, G7, F12, G3, G6, H2, E2, L3, G5, L4, G4, J4, H7, E1, G2, F3, J7, M3, H3, J2, J6, K3, K2, L2	High	I/O	–	–
$\overline{\text{AACK}}$	N3	Low	Input	–	–
$\overline{\text{ABB}}$	L7	Low	I/O	–	–
AP[0-3]	C4, C5, C6, C7	High	I/O	–	–
$\overline{\text{ARTRY}}$	L6	Low	I/O	–	–
AVDD	A8	-	-	2V	2V
$\overline{\text{BG}}$	H1	Low	Input	–	–
$\overline{\text{BR}}$	E7	Low	Output	–	–
BVSEL[3][5][6]	W1	High	Input	GND	3.3V
$\overline{\text{CI}}$	C2	Low	Output	–	–
CKSTP_IN	B8	Low	Input	–	–
CKSTP_OUT	D7	Low	Output	–	–
CLK_OUT	E3	–	Output	–	–
$\overline{\text{DBB}}$	K5	Low	I/O	–	–
$\overline{\text{DBDIS}}$	G1	Low	Input	–	–
$\overline{\text{DBG}}$	K1	Low	Input	–	–
$\overline{\text{DBWO}}$	D1	Low	Input	–	–
DH[0-31]	W12, W11, V11, T9, W10, U9, U10, M11, M9, P8, W7, P9, W9, R10, W6, V7, V6, U8, V9, T7, U7, R7, U6, W5, U5, W4, P7, V5, V4, W3, U4, R5	High	I/O	–	–
DL[0-31]	M6, P3, N4, N5, R3, M7, T2, N6, U2, N7, P11, V13, U12, P12, T13, W13, U13, V10, W8, T11, U11, V12, V8, T1, P1, V1, U1, N1, R2, V3, U3, W2	High	I/O	–	–
DP[0-7]	L1, P2, M2, V2, M1, N2, T3, R1	High	I/O	–	–
$\overline{\text{DRTRY}}$	H6	Low	Input	–	–
$\overline{\text{GBL}}$	B1	Low	I/O	–	–
GND	D10, D14, D16, D4, D6, E12, E8, F4, F6, F10, F14, F16, G9, G11, H5, H8, H10, H12, H15, J9, J11, K4, K6, K8, K10, K12, K14, K16, L9, L11, M5, M8, M10, M12, M15, N9, N11, P4, P6, P10, P14, P16, R8, R12, T4, T6, T10, T14, T16	–	–	GND	GND
$\overline{\text{HRESET}}$	B6	Low	Input	–	–
$\overline{\text{INT}}$	C11	Low	Input	–	–
L1_TSTCLK[2]	F8	High	Input	–	–
L2ADDR[0-16]	L17, L18, L19, M19, K18, K17, K15, J19, J18, J17, J16, H18, H17, J14, J13, H19, G18	High	Output	–	–

Table 2. Pinout Listing for the PC755, 360 PBGA, CBGA and CI-CGA Packages + HiTCE[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
L2AVDD	L13	–	–	2V	2V
$\overline{\text{L2CE}}$	P17	Low	Output	–	–
L2CLKOUTA	N15	–	Output	–	–
L2CLKOUTB	L16	–	Output	–	–
L2DATA[0-63]	U14, R13, W14, W15, V15, U15, W16, V16, W17, V17, U17, W18, V18, U18, V19, U19, T18, T17, R19, R18, R17, R15, P19, P18, P13, N14, N13, N19, N17, M17, M13, M18, H13, G19, G16, G15, G14, G13, F19, F18, F13, E19, E18, E17, E15, D19, D18, D17, C18, C17, B19, B18, B17, A18, A17, A16, B16, C16, A14, A15, C15, B14, C14, E13	High	I/O	–	–
L2DP[0-7]	V14, U16, T19, N18, H14, F17, C19, B15	High	I/O	–	–
L2OVDD	D15, E14, E16, H16, J15, L15, M16, P15, R14, R16, T15, F15	–	–	1.8V/2V	3.3V
L2SYNC_IN	L14	–	Input	–	–
L2SYNC_OUT	M14	–	Output	–	–
L2_TSTCLK[2]	F7	High	Input	–	–
L2VSEL[1][3][5][6]	A19	High	Input	GND	3.3V
$\overline{\text{L2WE}}$	N16	Low	Output	–	–
L2ZZ	G17	High	Output	–	–
$\overline{\text{LSSD\_MODE}}$[2]	F9	Low	Input	–	–
$\overline{\text{MCP}}$	B11	Low	Input	–	–
NC (No-Connect)	B3, B4, B5, W19, K9, K11[4], K19[4]	–	–	–	–
OVDD	D5, D8, D12, E4, E6, E9, E11, F5, H4, J5, L5, M4, P5, R4, R6, R9, R11, T5, T8, T12	–	–	1.8V/2V	3.3V
PLL_CFG[0-3]	A4, A5, A6, A7	High	Input	–	–
$\overline{\text{QACK}}$	B2	Low	Input	–	–
$\overline{\text{QREQ}}$	J3	Low	Output	–	–
$\overline{\text{RSRV}}$	D3	Low	Output	–	–
$\overline{\text{SMI}}$	A12	Low	Input	–	–
$\overline{\text{SRESET}}$	E10	Low	Input	–	–
SYSCLK	H9	–	Input	–	–
$\overline{\text{TA}}$	F1	Low	Input	–	–
TBEN	A2	High	Input	–	–
$\overline{\text{TBST}}$	A11	Low	I/O	–	–
TCK	B10	High	Input	–	–
TDI[6]	B7	High	Input	–	–
TDO	D9	High	Output	–	–

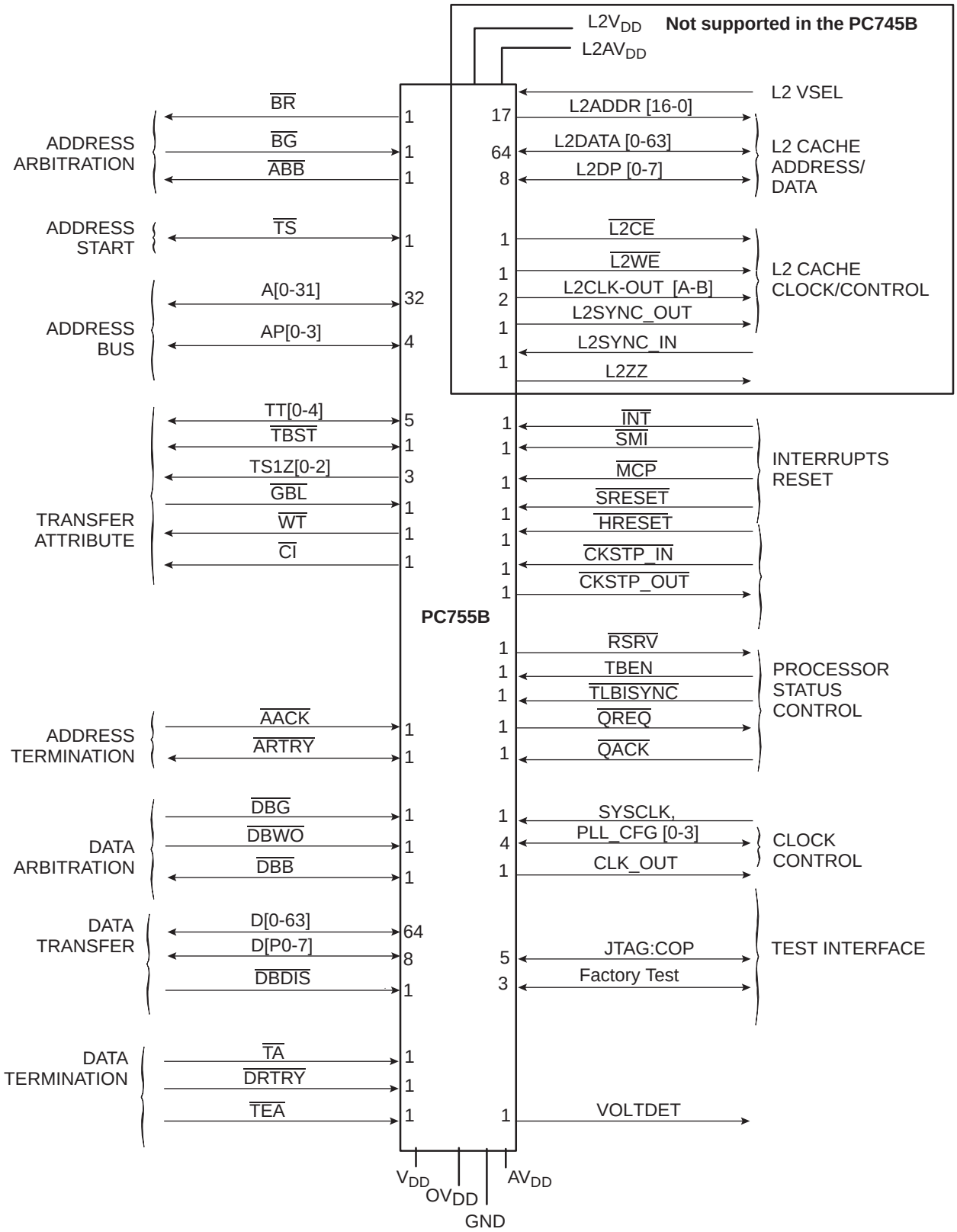
Table 2. Pinout Listing for the PC755, 360 PBGA, CBGA and CI-CGA Packages + HiTCE[8] (Continued)

Signal Name	Pin Number	Active	I/O	I/F Voltages Supported[1]	
				1.8V/2.0V	3.3V
$\overline{TEA}$	J1	Low	Input	–	–
$\overline{TLBISYNC}$	A3	Low	Input	–	–
TMS[6]	C8	High	Input	–	–
$\overline{TRST}$[6]	A10	Low	Input	–	–
$\overline{TS}$	K7	Low	I/O	–	–
TSIZ[0-2]	A9, B9, C9	High	Output	–	–
TT[0-4]	C10, D11, B12, C12, F11	High	I/O	–	–
$\overline{WT}$	C3	Low	Output	–	–
VDD	G8, G10, G12, J8, J10, J12, L8, L10, L12, N8, N10, N12	–	–	2V	2V
VOLTDET[7]	K13	High	Output	–	–

Notes:
1. OV_{DD} supplies power to the processor bus, JTAG, and all control signals except the L2 cache controls (L2CE, L2WE, and L2ZZ); $L2OV_{DD}$ supplies power to the L2 cache interface (L2ADDR[0-16], L2DATA[0-63], L2DP[0-7] and L2SYNC-OUT) and the L2 control signals; and V_{DD} supplies power to the processor core and the PLL and DLL (after filtering to become AV_{DD} and $L2AV_{DD}$ respectively). These columns serve as a reference for the nominal voltage supported on a given signal as selected by the BVSEL/L2VSEL pin configurations of Table 4 and the voltage supplied. For actual recommended value of V_{IN} or supply voltages see Table 5.
2. These are test signals for factory use only and must be pulled up to OV_{DD} for normal machine operation.
3. To allow for future I/O voltage changes, provide the option to connect BVSEL and L2VSEL independently to either OV_{DD} (selects 3.3V) or to OGND (selects 1.8V/2.0V).
4. These pins are reserved for potential future use as additional L2 address pins.
5. Uses one of 9 existing no-connects in PC750's 360-BGA package.
6. Internal pull up on die.
7. Internally tied to $L2OV_{DD}$ in the PC755 360-BGA package to indicate the power present at the L2 cache interface. This signal is not a power supply input.
8. This is different from the PC745 255-BGA package.

Signal Description

Figure 4. PC755 Microprocessor Signal Groups



Detailed Specification

Scope

This drawing describes the specific requirements for the microprocessor PC755, in compliance with Atmel Grenoble standard screening.

Applicable Documents

1) MIL-STD-883: Test methods and procedures for electronics.

2) MIL-PRF-38535 appendix A: General specifications for microcircuits.

Requirements

General

The microcircuits are in accordance with the applicable documents and as specified herein.

Design and Construction

Terminal Connections

Depending on the package, the terminal connections is shown in Table 1, Table 2 and Figure 4.

Absolute Maximum Rating

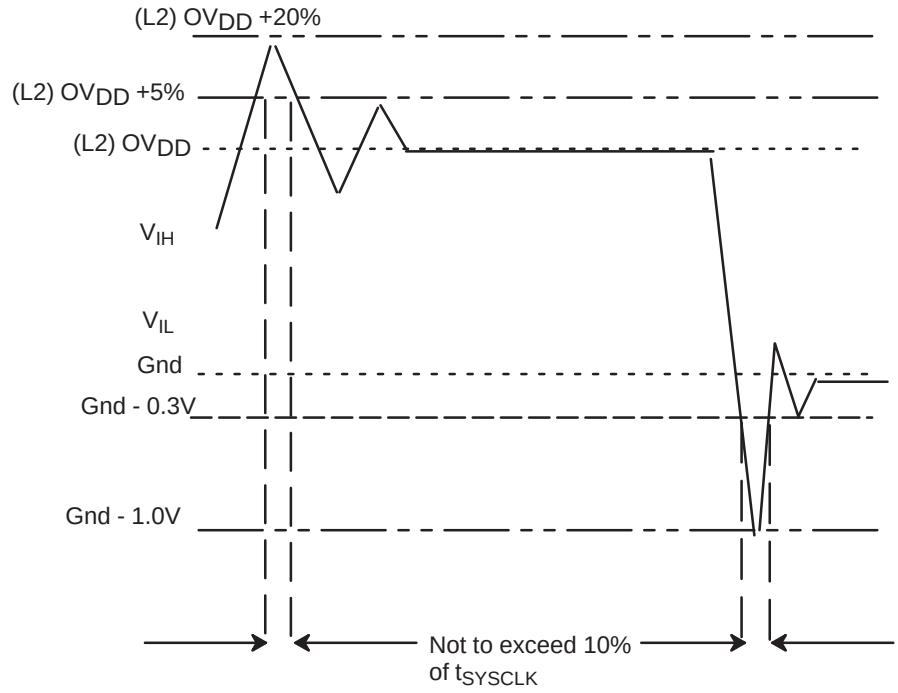
Table 3. Absolute Maximum Ratings(1)

Characteristic		Symbol	Maximum Value	Unit
Core supply voltage(4)		V_{DD}	-0.3 to 2.5	V
PLL supply voltage(4)		AV_{DD}	-0.3 to 2.5	V
L2 DLL supply voltage(4)		$L2AV_{DD}$	-0.3 to 2.5	V
Processor bus supply voltage(3)		OV_{DD}	-0.3 to 3.6	V
L2 bus supply voltage(3)		$L2OV_{DD}$	-0.3 to 3.6	V
Input voltage	Processor bus(2)(5)	V_{in}	-0.3 to OV_{DD} + 0.3V	V
	L2 Bus(2)(5)	V_{in}	-0.3 to $L2OV_{DD}$ + 0.3V	V
	JTAG Signals	V_{in}	-0.3 to 3.6	V
Storage temperature range		T_{stg}	-65 to 150	°C
Rework Temperature		T_{rwk}	220	°C

Notes:
1. Functional and tested operating conditions are given in Table 5. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. Caution: V_{IN} must not exceed OV_{DD} or $L2OV_{DD}$ by more than 0.3V at any time including during power-on reset.
3. Caution: $L2OV_{DD}/OV_{DD}$ must not exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by more than 1.6V during normal operation. During power-on reset and power-down sequences, $L2OV_{DD}/OV_{DD}$ may exceed $V_{DD}/AV_{DD}/L2AV_{DD}$ by up to 3.3V for up to 20 ms, or by 2.5V for up to 40 ms. Excursions beyond 3.3V or 40 ms are not supported.
4. Caution: $V_{DD}/AV_{DD}/L2AV_{DD}$ must not exceed $L2OV_{DD}/OV_{DD}$ by more than 0.4V during normal operation. During power-on reset and power-down sequences, $V_{DD}/AV_{DD}/L2AV_{DD}$ may exceed $L2OV_{DD}/OV_{DD}$ by up to 1.0V for up to 20 ms, or by 0.7V for up to 40 ms. Excursions beyond 1.0V or 40 ms are not supported.
5. This is a DC specifications only. V_{IN} may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 5.

Figure 5 shows the allowable undershoot and overshoot voltage on the PC755 and PC745.

Figure 5. Overshoot/Undershoot Voltage



The PC755 provides several I/O voltages to support both compatibility with existing systems and migration to future systems. The PC755 core voltage must always be provided at nominal 2.0V (see Table 5 for actual recommended core voltage). Voltage to the L2 I/Os and Processor Interface I/Os are provided through separate sets of supply pins and may be provided at the voltages shown in Table 4. The input voltage threshold for each bus is selected by sampling the state of the voltage select pins BVSEL and L2VSEL during operation. These signals must remain stable during part operation and cannot change. The output voltage will swing from GND to the maximum voltage applied to the OV_{DD} or $L2OV_{DD}$ power pins.

Table 4 describes the input threshold voltage setting.

Table 4. Input Threshold Voltage Setting

Part Revision	BVSEL Signal	Processor Bus Interface Voltage	L2VSEL Signal	L2 Bus Interface Voltage
E	0	Not Available	0	Not Available
	1	2.5V/3.3V	1	2.5V/3.3V

Notes: 1. Caution: The input threshold selection must agree with the OV_{DD}/$L2OV_{DD}$ voltages supplied.
2. The input threshold settings above are different for all revisions prior to Rev. 2.8 (Rev. E). For more information, contact your local Atmel sales office.

Table 5. Recommended Operating Conditions[1]

Characteristic		Symbol	Recommended Value				Unit
			300 MHz, 350 MHz		400 MHz		
			Min	Max	Min	Max	
Core supply voltage[3]		V_{DD}	1.80	2.10	1.90	2.10	V
PLL supply voltage[3]		AV_{DD}	1.80	2.10	1.90	2.10	V
L2 DLL supply voltage[3]		$L2AV_{DD}$	1.80	2.10	1.90	2.10	V
Processor bus supply voltage[2][4][5]	BVSEL = 1	OV_{DD}	2.375	2.625	2.375	2.625	V
			3.135	3.465	3.135	3.465	V
L2 bus supply voltage[2][4][5]	L2VSEL = 1	$L2OV_{DD}$	2.375	2.625	2.375	2.625	V
			3.135	3.465	3.135	3.465	V
Input voltage	Processor bus	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V
	L2 Bus	V_{in}	GND	$L2OV_{DD}$	GND	$L2OV_{DD}$	V
	JTAG Signals	V_{in}	GND	OV_{DD}	GND	OV_{DD}	V
Die-junction temperature	Military temperature range	T_j	-55	125	-55	125	°C
	Industrial temperature	T_j	-40	110	-40	110	°C

Notes: 1. These are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.
2. Revisions prior to Rev. 2.8 (Rev. E) offered different I/O voltage support.
3. 2.0V nominal.
4. 2.5V nominal.
5. 3.3V nominal.

Thermal Characteristics

Package Characteristics Table 6 provides the package thermal characteristics for the PC755.

Table 6. Package Thermal Characteristics

Characteristic	Symbol	Value			Unit
		PC755 CBGA	PC755 PBGA	PC745 PBGA	
Junction-to-ambient thermal resistance, natural convection[1][2]	$R\theta_{JA}$	24	31	34	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board[1][3]	$R\theta_{JMA}$	17	25	26	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, single-layer (1s) board[1][3]	$R\theta_{JMA}$	18	25	27	°C/W
Junction-to-ambient thermal resistance, 200 ft./min. airflow, four-layer (2s2p) board[1][3]	$R\theta_{JMA}$	14	21	22	°C/W
Junction-to-board thermal resistance[4]	$R\theta_{JB}$	8	17	17	°C/W
Junction-to-case thermal resistance[5]	$R\theta_{JC}$	< 0.1	< 0.1	< 0.1	°C/W

Notes: 1. Junction temperature is a function of on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per SEMI G38-87 and JEDEC JESD51-2 with the single layer board horizontal.
3. Per JEDEC JESD51-6 with the board horizontal.

4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the calculated case temperature. The actual value of RÉýJC for the part is less than 0.1°C/W.

Note: *R*efer to Section “Thermal Management Information“ page 19 for more details about thermal management.

Package Thermal Characteristics for HiTCE

Table 7 provides the package thermal characteristics for the PC755, HiTCE.

Table 7. Package Thermal Characteristics for HiTCE Package

Characteristic	Symbol	Value	Unit
		PC755 HiTCE	
Junction-to-bottom of balls(1)	$R\theta_J$	6.8	°C/W
Junction-to-ambient thermal resistance, natural convection, four-layer (2s2p) board(1)(2)	$R\theta_{JMA}$	20.7	°C/W
Junction to board thermal resistance	$R\theta_{JB}$	11.0	°C/W

Notes: 1. Simulation, no convection air flow.
2. Per JEDEC JESD51-6 with the board horizontal.

Table 8. Package Thermal Characteristics for CI-CGA

Characteristic	Symbol	Value	Unit
		PC755 CI-CGA	
Junction to board thermal resistance	$R\theta_{JB}$	8.42	°C/W

The board designer can choose between several types of heat sinks to place on the PC755. There are several commercially-available heat sinks for the PC755 provided by the following vendors:

For the exposed-die packaging technology, shown in Table 5, the intrinsic conduction thermal resistance paths are as follows:

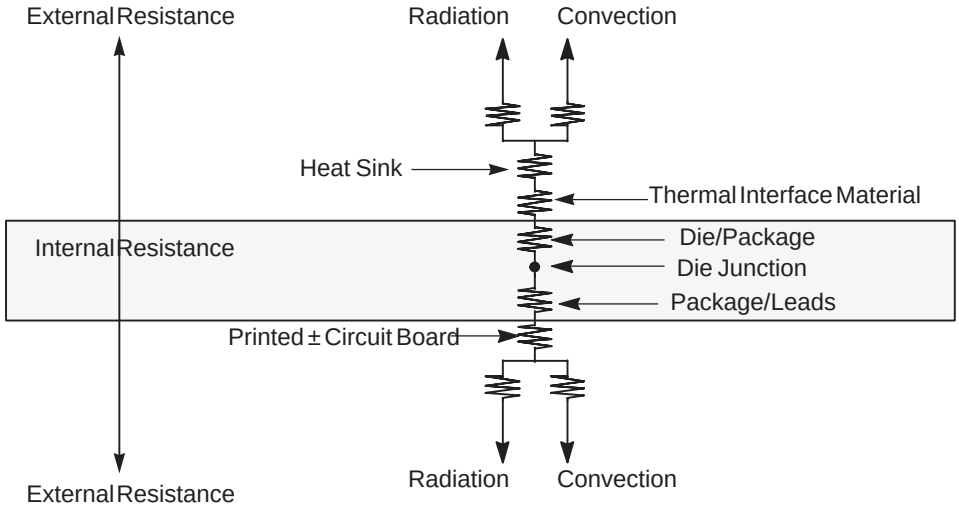
- The die junction-to-case (or top-of-die for exposed silicon) thermal resistance
- The die junction-to-ball thermal resistance

Figure 6 depicts the primary heat transfer path for a package with an attached heat sink mounted to a printed-circuit board.

Heat generated on the active side of the chip is conducted through the silicon, then through the heat sink attach material (or thermal interface material), and finally to the heat sink where it is removed by forced-air convection.

Since the silicon thermal resistance is quite small, for a first-order analysis, the temperature drop in the silicon may be neglected. Thus, the heat sink attach material and the heat sink conduction/convective thermal resistances are the dominant terms.

Figure 6. C4 Package with Head Sink Mounted to a Printed-circuit Board



Note the internal versus external package resistance.

Thermal Management Assistance

The PC755 incorporates a thermal management assist unit (TAU) composed of a thermal sensor, digital-to-analog converter, comparator, control logic, and dedicated special-purpose registers (SPRs). Specifications for the thermal sensor portion of the TAU are found in Table 9. More information on the use of this feature is given in the Motorola PC755 RISC Microprocessor User's manual.

Table 9. Thermal Sensor Specifications at Recommended Operating Conditions (see Table 5)

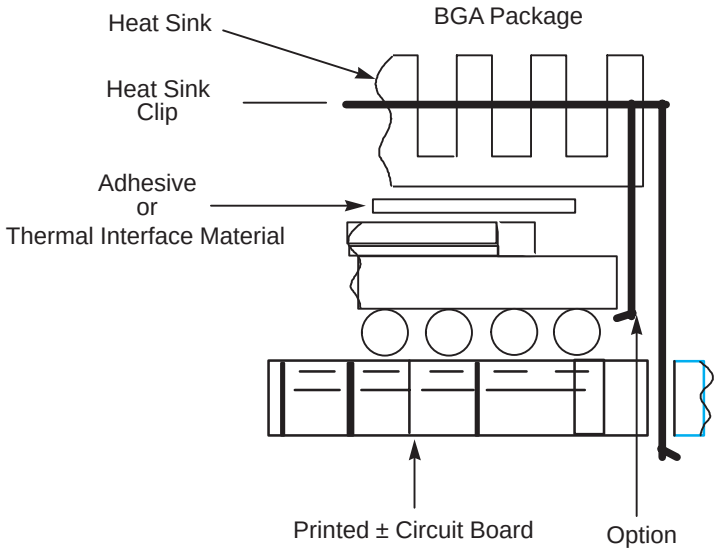
Characteristic	Min	Max	Unit
Temperature range(1)	0	127	°C
Comparator settling time(2)(3)	20	–	s
Resolution(3)	4	–	°C
Accuracy(3)	-12	+12	°C

Notes:
1. The temperature is the junction temperature of the die. The thermal assist unit's raw output does not indicate an absolute temperature, but must be interpreted by software to derive the absolute junction temperature. For information about the use and calibration of the TAU, see Motorola Application Note AN1800/D, "Programming the Thermal Assist Unit in the PC750 Microprocessor".
2. The comparator settling time value must be converted into the number of CPU clocks that need to be written into the THRM3 SPR.
3. Guaranteed by design and characterization.

Thermal Management Information

This section provides thermal management information for the ceramic ball grid array (BGA) package for air-cooled applications. Proper thermal control design is primarily dependent upon the system-level design-the heat sink, airflow and thermal interface material. To reduce the die-junction temperature, heat sinks may be attached to the package by several methods-adhesive, spring clip to holes in the printed-circuit board or package, and mounting clip and screw assembly; see Figure 7. This spring force should not exceed 5.5 pounds of force.

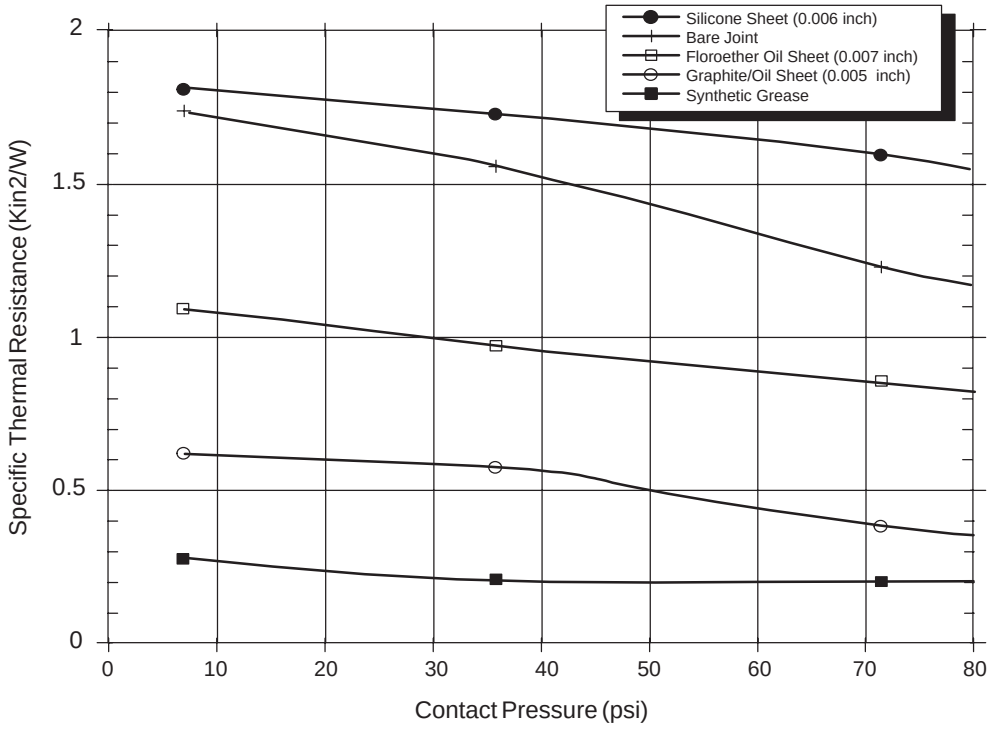
Figure 7. Package Exploded Cross-Sectional View with Several Heat Sink Options



Ultimately, the final selection of an appropriate heat sink depends on many factors, such as thermal performance at a given air velocity, spatial volume, mass, attachment method, assembly, and cost.

Adhesives and Thermal Interface Materials

Figure 8. Thermal Performance of Select Thermal Interface Material



A thermal interface material is recommended at the package lid-to-heat sink interface to minimize the thermal contact resistance. For those applications where the heat sink is attached by spring clip mechanism, Figure 8 shows the thermal performance of three thin-sheet thermal-interface materials (silicone, graphite/oil, floroether oil), a bare joint, and a joint with thermal grease as a function of contact pressure. As shown, the performance of these thermal interface materials improves with increasing contact pressure. The use of thermal grease significantly reduces the interface thermal resistance. That is, the bare joint results in a thermal resistance approximately 7 times greater than the thermal grease joint.

Heat sinks are attached to the package by means of a spring clip to holes in the printed-circuit board (see Figure 7). This spring force should not exceed 5.5 pounds of force. Therefore, the synthetic grease offers the best thermal performance, considering the low interface pressure.

The board designer can choose between several types of thermal interface. Heat sink adhesive materials should be selected based upon high conductivity, yet adequate mechanical strength to meet equipment shock/vibration requirements.

Heat Sink Selection Example

For preliminary heat sink sizing, the die-junction temperature can be expressed as follows:

$$T_j = T_a + T_r + (\theta_{jc} + \theta_{int} + \theta_{sa}) * P_d$$

Where:

T_j is the die-junction temperature

T_a is the inlet cabinet ambient temperature

T_r is the air temperature rise within the computer cabinet

θ_{jc} is the junction-to-case thermal resistance

θ_{int} is the adhesive or interface material thermal resistance

θ_{sa} is the heat sink base-to-ambient thermal resistance

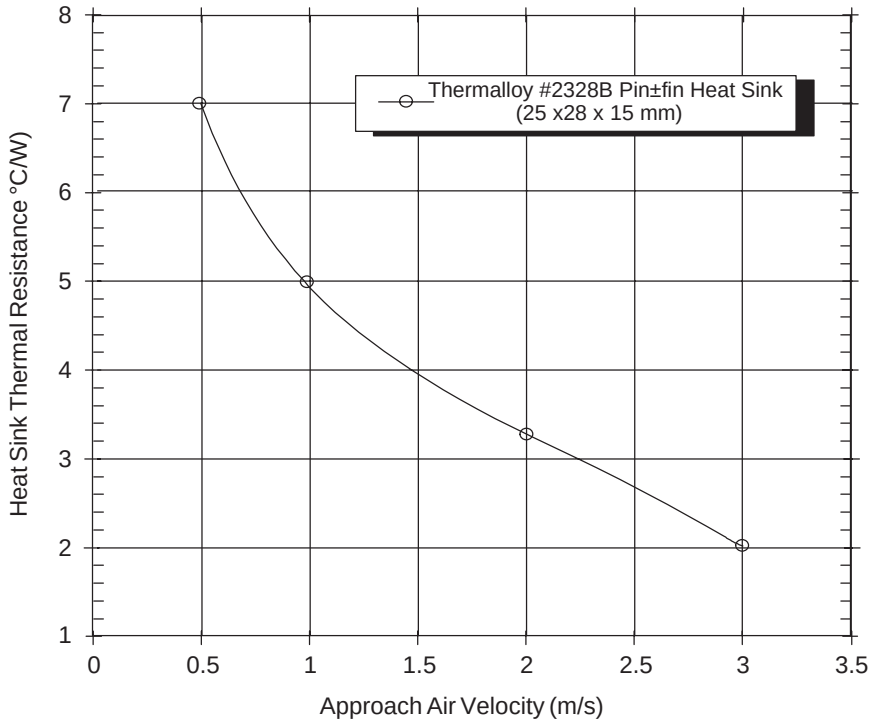
P_d is the power dissipated by the device

During operation the die-junction temperatures (T_j) should be maintained less than the value specified in Table 5. The temperature of the air cooling the component greatly depends upon the ambient inlet air temperature and the air temperature rise within the electronic cabinet. An electronic cabinet inlet-air temperature (T_a) may range from 30 to 40°C. The air temperature rise within a cabinet (T_r) may be in the range of 5 to 10°C. The thermal resistance of the thermal interface material (θ_{int}) is typically about 1°C/W. Assuming a T_a of 30°C, a $T_{r\ of\ 5}$°C, a CBGA package θ_{jc} = 0.03, and a power consumption (P_d) of 5.0 watts, the following expression for T_j is obtained:

Die-junction temperature: $T_j = 30°C + 5°C + (0.03°C/W + 1.0°C/W + \theta_{sa}) * 5.0\ W$

For a Thermalloy heat sink #2328B, the heat sink-to-ambient thermal resistance (θ_{sa}) versus airflow velocity is shown in Figure 9.

Figure 9. Thermalloy #2328B Heat Sink-to-Ambient Thermal Resistance Versus Airflow Velocity



Assuming an air velocity of 0.5 m/s, we have an effective R_{sa} of 7°C/W, thus

$T_j = 30°C + 5°C + (0.03°C/W + 1.0°C/W + 7°C/W) * 5.0\ W,$

resulting in a die-junction temperature of approximately 81°C which is well within the maximum operating temperature of the component.

Other heat sinks offered by Chip Coolers, IERC, Thermalloy, Wakefield Engineering, and Aavid Engineering offer different heat sink-to-ambient thermal resistances, and may or may not need air flow.

Though the die junction-to-ambient and the heat sink-to-ambient thermal resistances are a common figure-of-merit used for comparing the thermal performance of various microelectronic packaging technologies, one should exercise caution when only using this metric in determining thermal management because no single parameter can adequately describe three-dimensional heat flow. The final die-junction operating temperature, is not only a function of the component-level thermal resistance, but the system-level design and its operating conditions. In addition to the component's power consumption, a number of factors affect the final operating die-junction temperature — airflow, board population (local heat flux of adjacent components), heat sink efficiency, heat sink attach, heat sink placement, next-level interconnect technology, system air temperature rise, altitude, etc.

Due to the complexity and the many variations of system-level boundary conditions for today's microelectronic equipment, the combined effects of the heat transfer mechanisms (radiation, convection and conduction) may vary widely. For these reasons, we recommend using conjugate heat transfer models for the board, as well as, system-level designs. To expedite system-level thermal analysis, several "compact" thermal-package models are available within FLOTHERM®. These are available upon request.

Power consideration

Power management

The PC755 provides four power modes, selectable by setting the appropriate control bits in the MSR and HIDO registers. The four power modes are as follows:

- Full-power: This is the default power state of the PC755. The PC755 is fully powered and the internal functional units operate at the full processor clock speed. If the dynamic power management mode is enabled, functional units that are idle will automatically enter a low-power state without affecting performance, software execution, or external hardware.
- Doze: All the functional units of the PC755 are disabled except for the time base/decrementer registers and the bus snooping logic. When the processor is in doze mode, an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or machine check brings the PC755 into the full-power state. The PC755 in doze mode maintains the PLL in a fully powered state and locked to the system external clock input (SYSCLK) so a transition to the full-power state takes only a few processor clock cycles.
- Nap: The nap mode further reduces power consumption by disabling bus snooping, leaving only the time base register and the PLL in a powered state. The PC755 returns to the full-power state upon receipt of an external asynchronous interrupt, a system management interrupt, a decrementer exception, a hard or soft reset, or a machine check input (MCP). A return to full-power state from a nap state takes only a few processor clock cycles. When the processor is in nap mode, if $\overline{\text{QACK}}$ is negated, the processor is put in doze mode to support snooping.
- Sleep: Sleep mode minimizes power consumption by disabling all internal functional units, after which external system logic may disable the PPL and SUSCLK. Returning the PC755 to the full-power state requires the enabling of the PPL and SYSCLK, followed by the assertion of an external asynchronous interrupt, a system management interrupt, a hard or soft reset, or a machine check input (MCP) signal after the time required to relock the PPL.

Power Dissipation

Table 10. Power Consumption for PC755

	Processor (CPU) Frequency			
	300 MHz	**350 MHz**	**400 MHz**	**Unit**
Full-Power Mode				
Typical(1)(3)(4)	3.1	3.6	5.4	W
Maximum(1)(2)	4.5	5.3	8	W
Doze Mode				
Maximum(1)(2)(4)	1.8	2	2.3	W
Nap Mode				
Maximum(1)(2)(4)	1	1	1	W
Sleep Mode				
Maximum(1)(2)(4)	550	550	550	mW
Sleep Mode-PLL and DLL Disabled				
Maximum(1)(2)	510	510	510	mW

Notes:
1. These values apply for all valid processor bus and L2 bus ratios. The values do not include I/O supply power (OV_{DD} and $L2OV_{DD}$) or PLL/DLL supply power (AV_{DD} and $L2AV_{DD}$). OV_{DD} and $L2OV_{DD}$ power is system dependent, but is typically < 10% of V_{DD} power. Worst case power consumption for AV_{DD} = 15 mW and $L2AV_{DD}$ = 15 mW.
2. Maximum power is measured at nominal V_{DD} (see Table 5) while running an entirely cache-resident, contrived sequence of instructions which keep the execution units maximally busy.
3. Typical power is an average value measured at the nominal recommended V_{DD} (see Table 5) and 65×C in a system while running a typical code sequence.
4. Not 100% tested. Characterized and periodically sampled.

Electrical Characteristics

Static Characteristics

Table 11. DC Electrical Specifications at Recommended Operating Conditions (see Table 5)

Characteristic	Nominal bus Voltage(1)	Symbol	Min	Max	Unit
Input high voltage (all inputs except SYSLCK)(2)(3)	2.5	V_{IH}	1.6	(L2)OV_{DD} + 0.3	V
	3.3	V_{IH}	2	(L2)OV_{DD} + 0.3	V
Input low voltage (all inputs except SYSLCK)(2)	2.5	V_{IL}	-0.3	0.6	V
	3.3	V_{IL}	-0.3	0.8	V
SYSCLK input high voltage	2.5	KV_{IH}	1.8	OV_{DD} + 0.3	V
	3.3	KV_{IH}	2.4	OV_{DD} + 0.3	V
SYSCLK input low voltage	2.5	KV_{IL}	-0.3	0.4	V
	3.3	KV_{IL}	-0.3	0.4	V
Input leakage current, (2)(3) V_{IN} = L2OV_{DD}/OV_{DD}		I_{in}	–	10	µA
Hi-Z (off-state) leakage current, (2)(3)(5) V_{IN} = L2OV_{DD}/OV_{DD}		I_{TSI}	–	10	µA
Output high voltage, I_{OH} = -6 mA	2.5	V_{OH}	1.7	–	V
	3.3	V_{OH}	2.4	–	V
Output low voltage, I_{OL} = 6 mA	2.5	V_{OL}	–	0.45	V
	3.3	V_{OL}	–	0.4	V
Capacitance, V_{IN} = 0V, f = 1 MHz (3)(4)		C_{in}	–	5	pF

Notes:
1. Nominal voltages; See Table 5 for recommended operating conditions.
2. For processor bus signals, the reference is OV_{DD} while L2OV_{DD} is the reference for the L2 bus signals.
3. Excludes test signals (LSSD_MODE, L1_TSTCLK, L2_TSTCLK) and IEEE 1149.1 boundary scan (JTAG) signals.
4. Capacitance is periodically sampled rather than 100% tested.
5. The leakage is measured for nominal OV_{DD} and V_{DD}, or both OV_{DD} and V_{DD} must vary in the same direction (for example, both OV_{DD} and V_{DD} vary by either +5% or -5%).

Dynamic Characteristics

After fabrication, parts are sorted by maximum processor core frequency as shown in the “Clock AC Specifications” Section on page 25 and tested for conformance to the AC specifications for that frequency. These specifications are for 275, 300, 333 MHz processor core frequencies. The processor core frequency is determined by the bus (SYSCLK) frequency and the settings of the PLL_CFG[0-3] signals. Parts are sold by maximum processor core frequency.

Clock AC Specifications Table 12 provides the clock AC timing specifications as defined in Table 3.

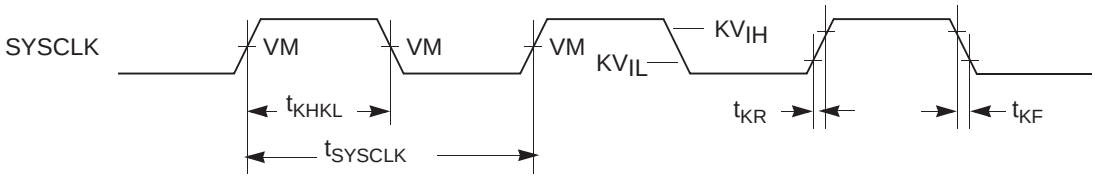
Table 12. Clock AC Timing Specifications at Recommended Operating Conditions (See Table 5)

Characteristic	Symbol	Maximum Processor Core Frequency						Unit
		300 MHz		350 MHz		400 MHz		
		Min	Max	Min	Max	Min	Max	
Processor frequency(1)	f_{core}	200	300	200	350	200	400	MHz
VCO frequency(1)	f_{VCO}	400	600	400	700	400	800	MHz
SYSCLK frequency(1)	f_{SYSCLK}	25	100	25	100	25	100	MHz
SYSCLK cycle time	t_{SYSCLK}	10	40	10	40	10	40	ns
SYSCLK rise and fall time(2)	t_{KR} & t_{KF}	–	2	–	2	–	2	ns
	t_{KR} & t_{KF}	–	1.4	–	1.4	–	1.4	ns
SYSCLK duty cycle measured at $OV_{DD}/2$(3)	t_{KHKL}/t_{SYSCLK}	40	60	40	60	40	60	%
SYSCLK jitter(3)(4)		–	150	–	150	–	150	ps
Internal PLL relock time(3)(5)		–	100	–	100	–	100	µs

Notes:
1. Caution: The SYSCLK frequency and PLL_CFG[0-3] settings must be chosen such that the resulting SYSCLK (bus) frequency, CPU (core) frequency, and PLL (VCO) frequency do not exceed their respective maximum or minimum operating frequencies. Refer to the PLL_CFG[0-3] signal description in Table 18," for valid PLL_CFG[0-3] settings
2. Rise and fall times measurements are now specified in terms of slew rates, rather than time to account for selectable I/O bus interface levels. The minimum slew rate of 1v/ns is equivalent to a 2ns maximum rise/fall time measured at 0.4V and 2.4V or a rise/fall time of 1ns measured at 0.4V to 1.4V.
3. Timing is guaranteed by design and characterization.
4. This represents total input jitter – short term and long term combined and is guaranteed by design.
5. Relock timing is guaranteed by design and characterization. PLL-relock time is the maximum amount of time required for PLL lock after a stable V_{DD} and SYSCLK are reached during the power-on reset sequence. This specification also applies when the PLL has been disabled and subsequently re-enabled during sleep mode. Also note that $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL-relock time during the power-on reset sequence.

Figure 10 provides the SYSCLK input timing diagram.

Figure 10. SYSCLK Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Processor Bus AC Specifications

Table 13 provides the processor bus AC timing specifications for the PC755 as defined in Figure 11 and Figure 13. Timing specifications for the L2 bus are provided in Section “L2 Clock AC Specifications» page 28.

Table 13. Processor Bus Mode Selection AC Timing Specifications(1)
At $V_{DD} = AV_{DD} = 2.0V$ 100 mV; $-55 \le T_j \le +125°C$, $OV_{DD} = 3.3V$ 165 mV and $OV_{DD} = 1.8V \pm 100$ mV and $OV_{DD} = 2.0V$ 100 mV

Parameter	Symbols(2)	All Speed Grades		Unit
		Min	Max	
Mode select input setup to $\overline{\text{HRESET}}$(3)(4)(5)(6)(7)	t_{MVRH}	8	–	t_{SYSCLk}
$\overline{\text{HRESET}}$ to mode select input hold(3)(4)(6)(7)(8)	t_{MXRH}	0	–	ns

Notes:
1. All input specifications are measured from the midpoint of the signal in question to the midpoint of the rising edge of the input SYSCLK. All output specifications are measured from the midpoint of the rising edge of SYSCLK to the midpoint of the signal in question. All output timings assume a purely resistive 50Ω load (See Figure 11). Input and output timings are measured at the pin; time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. THe symbology used for timing specifications herein follows the pattern of $t_{\text{(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(reference)(state)(signal)(state)}}$ for outputs. For example, t_{IVKH} symbolizes the time input signals (I) reach the valid state (V) relative to the SYSCLK reference (K) going to the high (H) state or input setup time. And t_{KHOV} symbolizes the time from SYSCLK(K) going highs) until outputs (O) are valid (V) or output valid time. Input hold time can be read as the time that the input signal (I) went invalid (X) with respect to the rising clock edge (KH) - note the position of the reference and its state for inputs – and output hold time can be read as the time from the rising edge (KH) until the output went invalid (OX). For additional explanation of AC timing specifications in Motorola PowerPC microprocessors, see the application note “Understanding AC Timing Specifications for PowerPC Microprocessors.”
3. The setup and hold time is with respect to the rising edge of $\overline{\text{HRESET}}$ (see Figure 11).
4. This specification is for configuration mode select only. Also note that the $\overline{\text{HRESET}}$ must be held asserted for a minimum of 255 bus clocks after the PLL re-lock time during the power-on reset sequence.
5. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in nanoseconds) of the parameter in question.
6. Mode select signals are BVSEL, L2VSEL, PLL_CFG[0-3]
7. Guaranteed by design and characterization.
8. Bus mode select pins must remain stable during operation. Changing the logic states of BVSEL or L2VSEL during operation will cause the bus mode voltage selection to change. Changing the logic states of the PLL_CFG pins during operation will cause the PLL division ratio selection to change. Both of these conditions are considered outside the specification and are not supported. Once $\overline{\text{HRESET}}$ is negated the states of the bus mode selection pins must remain stable.

Figure 11 provides the mode select input timing diagram for the PC755.

Figure 11. Mode Input Timing Diagram

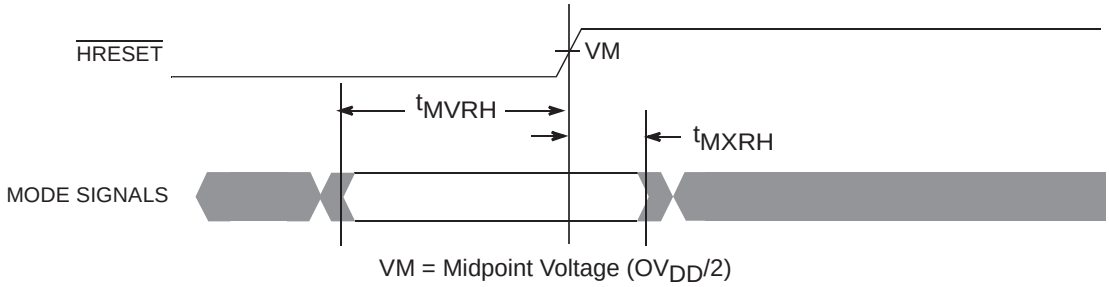


Figure 12 provides the AC test load for the PC755.

Figure 12. AC Test Load

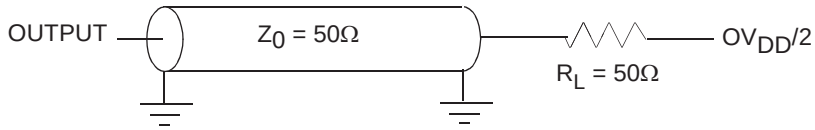


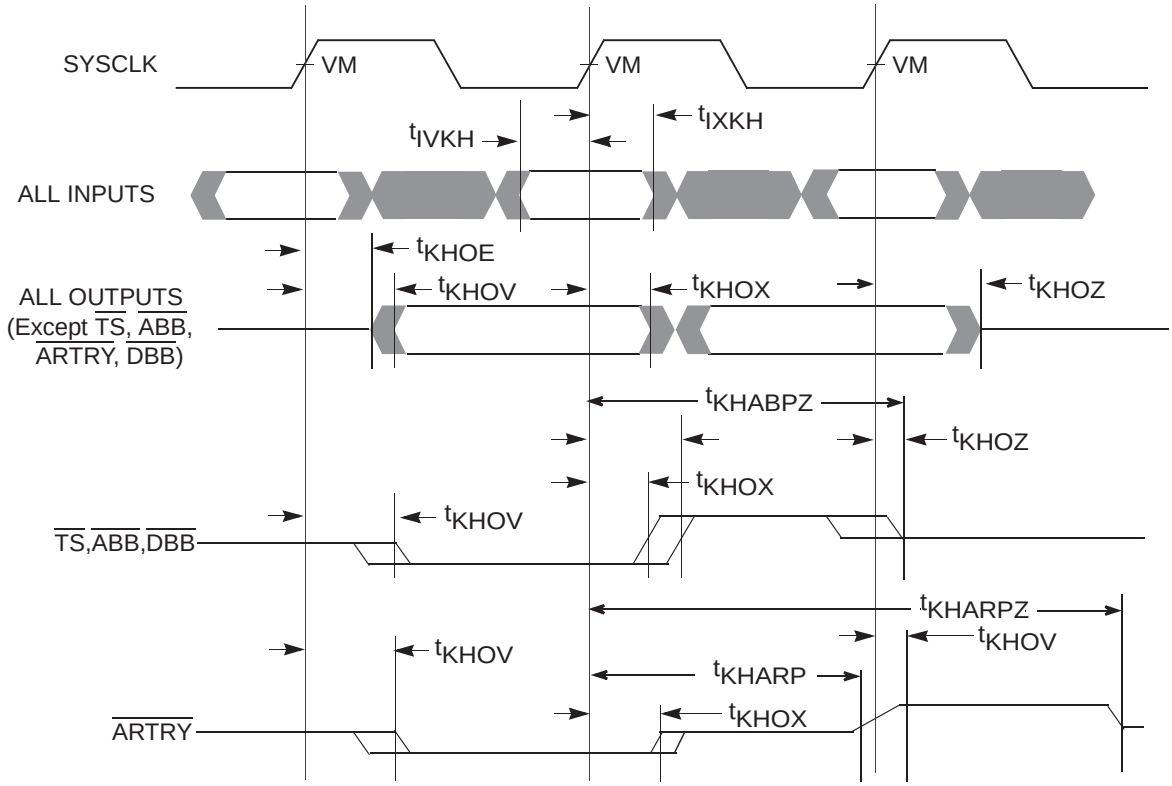
Table 14. Processor Bus AC Timing Specifications[1] at Recommended Operating Conditions

Parameter	Symbols	All Speed Grades		Unit
		Min	Max	
Setup Times: All Inputs	t_{IVKH}	2.5	–	ns
Input Hold Times: $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.6	–	ns
Input Hold Times: All Inputs, except $\overline{\text{TLBISYNC}}$, $\overline{\text{MCP}}$, $\overline{\text{SMI}}$	t_{IXKH}	0.2	–	ns
Valid Times: All Outputs	t_{KHOV}	–	4.1	ns
Output Hold Times: All Outputs	t_{KHOX}	1	–	ns
SYSCLK to Output Enable[2]	t_{KHOE}	0.5	–	ns
SYSCLK to Output High Impedance (all except $\overline{\text{ABB}}$, $\overline{\text{ARTRY}}$, $\overline{\text{DBB}}$)[2]	t_{KHOZ}	–	6	ns
SYSCLK to $\overline{\text{ABB}}$, $\overline{\text{DBB}}$ High Impedance After Precharge[2][3][4]	t_{KHABPZ}	–	1	t_{SYSCLK}
Maximum Delay to $\overline{\text{ARTRY}}$ Precharge[2][3][5]	t_{KHARP}	–	1	t_{SYSCLK}
SYSCLK to $\overline{\text{ARTRY}}$ High Impedance After Precharge[2][3][5]	t_{KHARPZ}	–	2	t_{SYSCLK}

Notes:
1. Revisions prior to Rev 2.8 (Rev E) were limited in performance and did not conform to this specification. Contact your local Motorola sales office for more information.
2. Guaranteed by design and characterization.
3. t_{SYSCLK} is the period of the external clock (SYSCLK) in nanoseconds (ns). The numbers given in the table must be multiplied by the period of SYSCLK to compute the actual time duration (in ns) of the parameter in question.
4. Per the 60x bus protocol, $\overline{\text{TS}}$, $\overline{\text{ABB}}$ and $\overline{\text{DBB}}$ are driven only by the currently active bus master. They are asserted low then precharged high before returning to high-Z as shown in Figure 6. The nominal precharge width for $\overline{\text{TS}}$, $\overline{\text{ABB}}$ or $\overline{\text{DBB}}$ is 0.5 x t_{SYSCLK}, i.e. less than the minimum t_{SYSCLK} period, to ensure that another master asserting $\overline{\text{TS}}$, $\overline{\text{ABB}}$, or $\overline{\text{DBB}}$ on the following clock will not contend with the precharge. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge.The high-Z behavior is guaranteed by design.
5. Per the 60x bus protocol, $\overline{\text{ARTRY}}$ can be driven by multiple bus masters through the clock period immediately following $\overline{\text{AACK}}$. Bus contention is not an issue since any master asserting $\overline{\text{ARTRY}}$ will be driving it low. Any master asserting it low in the first clock following AACK will then go to high-Z for one clock before precharging it high during the second cycle after the assertion of $\overline{\text{AACK}}$. The nominal precharge width for $\overline{\text{ARTRY}}$ is 1.0 t_{SYSCLK}; i.e., it should be high-Z as shown in Figure 6 before the first opportunity for another master to assert $\overline{\text{ARTRY}}$. Output valid and output hold timing is tested for the signal asserted. Output valid time is tested for precharge. The high-Z and precharge behavior is guaranteed by design.

Figure 13 provides the input/output timing diagram for the PC755.

Figure 13. Input/Output Timing Diagram



VM = Midpoint Voltage (OV_{DD}/2 or V_{in}/2)

L2 Clock AC Specifications

The L2CLK frequency is programmed by the L2 Configuration Register (L2CR[4:6]) core-to-L2 divisor ratio. See Table 15 for example core and L2 frequencies at various divisors. Table 15 provides the potential range of L2CLK output AC timing specifications as defined in Figure 14.

The minimum L2CLK frequency of Table 15 is specified by the maximum delay of the internal DLL. The variable-tap DLL introduces up to a full clock period delay in the L2CLKOUTA, L2CLKOUTB, and L2SYNC_OUT signals so that the returning L2SYNC_IN signal is phase aligned with the next core clock (divided by the L2 divisor ratio). Do not choose a core-to-L2 divisor which results in an L2 frequency below this minimum, or the L2CLKOUT signals provided for SRAM clocking will not be phase aligned with the PC755 core clock at the SRAMs.

The maximum L2CLK frequency shown in Table 15 is the core frequency divided by one. Very few L2 SRAM designs will be able to operate in this mode. Most designs will select a greater core-to-L2 divisor to provide a longer L2CLK period for read and write access to the L2 SRAMs. The maximum L2CLK frequency for any application of the PC755 will be a function of the AC timings of the PC755, the AC timings for the SRAM, bus loading, and printed circuit board trace length.

Motorola is similarly limited by system constraints and cannot perform tests of the L2 interface on a socketed part on a functional tester at the maximum frequencies of Table 15. Therefore functional operation and AC timing information are tested at core-to-L2 divisors of 2 or greater. Functionality of core-to-L2 divisors of 1 or 1.5 is verified at less than maximum rated frequencies.

L2 input and output signals are latched or enabled respectively by the internal L2CLK (which is SYSCLK multiplied up to the core frequency and divided down to the L2CLK frequency). In other words, the AC timings of Table 16 and Table 17 are entirely independent of L2SYNC_IN. In a closed loop system, where L2SYNC_IN is driven through the board trace by L2SYNC_OUT, L2SYNC_IN only controls the output phase of L2CLKOUTA and L2CLKOUTB which are used to latch or enable data at the SRAMs. However, since in a closed loop system L2SYNC_IN is held in phase alignment with the internal L2CLK, the signals of Table 16 and Table 17 are referenced to this signal rather than the not-externally-visible internal L2CLK. During manufacturing test, these times are actually measured relative to SYSCLK.

The L2SYNC_OUT signal is intended to be routed halfway out to the SRAMs and then returned to the L2SYNC_IN input of the PC755 to synchronize L2CLKOUT at the SRAM with the processor's internal clock. L2CLKOUT at the SRAM can be offset forward or backward in time by shortening or lengthening the routing of L2SYNC_OUT to L2SYNC_IN. See Motorola Application Note AN179/D "PowerPC™ Backside L2 Timing Analysis for the PCB Design Engineer."

The L2CLKOUTA and L2CLKOUTB signals should not have more than two loads.

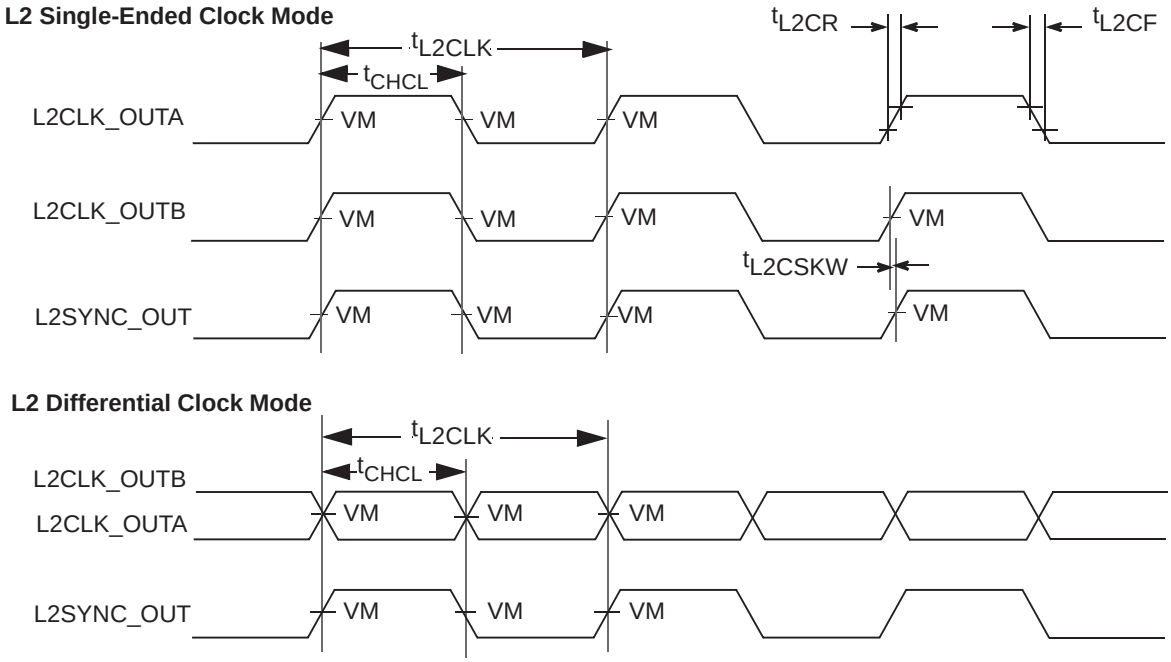
Table 15. L2CLK Output AC Timing Specification. At V_{DD} = AV_{DD} = 2.0V 100 mV; -55 ≤ T_j ≤ +125°C, OV_{DD} = 3.3V 165 mV and OV_{DD} = 1.8V 100 mV and OV_{DD} = 2.0V 100 mV

Parameter	Symbols	All Speed Grades		Unit
		Min	Max	
L2CLK frequency(1)(4)	f_{L2CLK}	80	450	MHz
L2CLK cycle time	t_{L2CLK}	2.5	12.5	ns
L2CLK duty cycle(2)(7)	t_{CHCL}/t_{L2CLK}	45	55	%
Internal DLL-relock time(3)(7)	–	640	–	L2CLK
DLL capture window(5)(7)	–	0	10	ns
L2CLKOUT output-to-output skew(6)(7)	t_{L2CSKW}	–	50	ps
L2CLKOUT output jitter(6)(7)	–	–	±150	ps

Notes:
1. L2CLK outputs are L2CLK_OUTA, L2CLK_OUTB, L2CLK_OUT and L2SYNC_OUT pins. The L2CLK frequency to core frequency settings must be chosen so that the resulting L2CLK frequency and core frequency do not exceed their respective maximum or minimum operating frequencies. The maximum L2LCK frequency will be system dependent. L2CLK_OUTA and L2CLK_OUTB must have equal loading.
2. The nominal duty cycle of the L2CLK is 50% measured at midpoint voltage.
3. The DLL re-lock time is specified in terms of L2CLKs. The number in the table must be multiplied by the period of L2CLK to compute the actual time duration in nanoseconds. Re-lock timing is guaranteed by design and characterization.
4. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz. This adds more delay to each tap of the DLL.
5. Allowable skew between L2SYNC_OUT and L2SYNC_IN.
6. This output jitter number represents the maximum delay of one tap forward or one tap back from the current DLL tap as the phase comparator seeks to minimize the phase difference between L2SYNC_IN and the internal L2CLK. This number must be comprehended in the L2 timing analysis. The input jitter on SYSCLK affects L2CLKOUT and the L2 address/data/control signals equally and therefore is already comprehended in the AC timing and does not have to be considered in the L2 timing analysis.
7. Guaranteed by design.

The L2CLK_OUT timing diagram is shown in Figure 14.

Figure 14. L2CLK_OUT Output Timing Diagram



L2 Bus Input AC Specifications Table 16 provides the L2 bus interface AC timing specifications for the PC755 as defined in Figure 15 and Figure 16 for the loading conditions described in Figure 17.

Table 16. L2 Bus Interface AC Timing Specifications at Recommended Operating Conditions

Parameter	Symbol	All Speed Grades		Unit
		Min	Max	
L2SYNC_IN rise and Fall Time(1)	t_{L2CR} & t_{L2CF}	–	1.0	ns
Setup Times: Data and Parity(2)	t_{DVL2CH}	1.2	-	ns
Input Hold Times: Data and Parity(2)	t_{DXL2CH}	0	-	ns
Valid Times: (3)(4)	t_{L2CHOV}			ns
All Outputs when L2CR[14-15] = 00		-	3.1	
All Outputs when L2CR[14-15] = 01		-	3.2	
All Outputs when L2CR[14-15] = 10		-	3.3	
All Outputs when L2CR[14-15] = 11		-	3.7	
Output Hold Times: (3)	t_{L2CHOX}			ns
All Outputs when L2CR[14-15] = 00		0.5	-	
All Outputs when L2CR[14-15] = 01		0.7	-	
All Outputs when L2CR[14-15] = 10		0.9	-	
All Outputs when L2CR[14-15] = 11		1.1	-	
L2SYNC_IN to High Impedance:(3)(5)	t_{L2CHOZ}			ns
All Outputs when L2CR[14-15] = 00		-	2.4	
All Outputs when L2CR[14-15] = 01		-	2.6	
All Outputs when L2CR[14-15] = 10		-	2.8	
All Outputs when L2CR[14-15] = 11		-	3.0	

Notes:
1. Rise and fall times for the L2SYNC_IN input are measured from 20% to 80% of $L2OV_{DD}$.
2. All input specifications are measured from the midpoint of the signal in question to the midpoint voltage of the rising edge of the input L2SYNC_IN (see Figure 8). Input timings are measured at the pins.
3. All output specifications are measured from the midpoint voltage of the rising edge of L2SYNC_IN to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 10).
4. The outputs are valid for both single-ended and differential L2CLK modes. For pipelined registered synchronous BurstRAMs, L2CR[14-15] = 01 or 10 is recommended. For pipelined late write synchronous BurstRAMs, L2CR[14-15] = 11 is recommended.
5. Guaranteed by design and characterization.
6. Revisions prior to Rev 2.8 (Rev E) were limited in performance.and did not conform to this specification. Contact your local Atmel sales office for more information.

Figure 15 shows the L2 bus input timing diagrams for the PC755.

Figure 15. L2 Bus Input Timing Diagrams

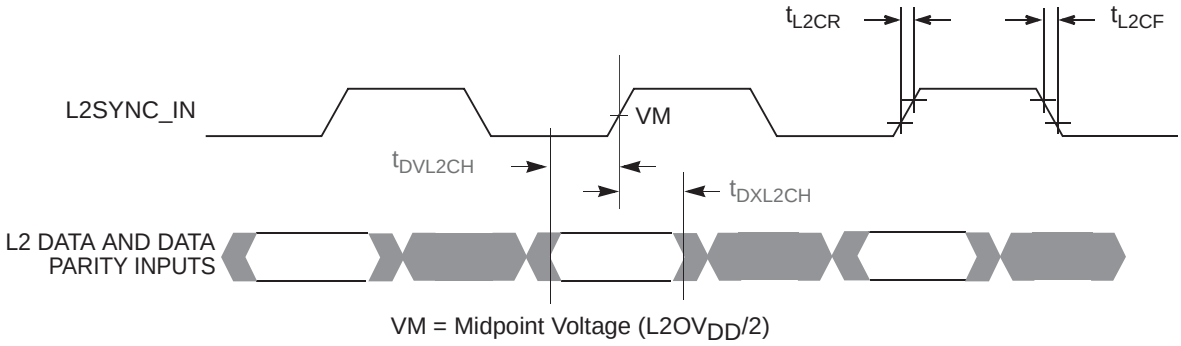


Figure 16 shows the L2 bus output timing diagrams for the PC755.

Figure 16. L2 Bus Output Timing Diagrams

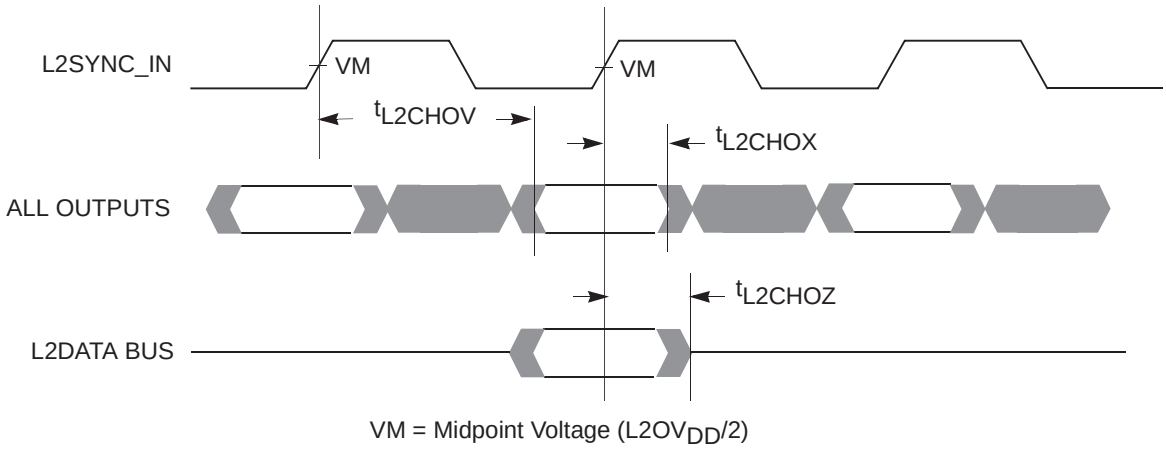
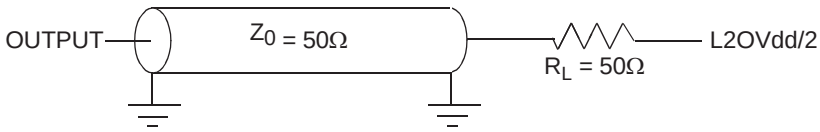


Figure 17 provides the AC test load for L2 interface of the PC755.

Figure 17. AC Test Load for the L2 Interface



Timing Specifications

Table 17 provides the IEEE 1149.1 (JTAG) AC timing specifications as defined in Figure 18, Figure 19, Figure 20, and Figure 21.

Table 17. JTAG AC Timing Specifications (Independent of SYSCLK)[1]

Parameter	Symbol	Min	Max	Unit
TCK Frequency of operation	f_{TCLK}	0	16	MHz
TCK Cycle time	f_{TCLK}	62.5	-	ns
TCK Clock pulse width measured at 1.4V	t_{JHJL}	31	-	ns
TCK Rise and fall times	t_{JR} & t_{JF}	0	2	ns
$\overline{TRST}$ Assert time[2]	$t\overline{TRST}$	25	-	ns
Input Setup Times:[3]				ns
Boundary-scan data	t_{DVJH}	4	-	
TMS, TDI	t_{IVJH}	0	-	
Input Hold Times:[3]				ns
Boundary-scan data	t_{DXJH}	15	-	
TMS, TDI	t_{IXJH}	12	-	
Valid Times:[4]				ns
Boundary-scan data	t_{JLDV}	-	4	
TDO	t_{JLOV}	-	4	
Output Hold Times:[4]				ns
Boundary-scan data	t_{JLDV}	25	-	
TDO	t_{JLOV}	12	-	
TCK to output high impedance:[4][5]				ns
Boundary-scan data	t_{JLDZ}	3	19	
TDO	t_{JLOZ}	3	9	

Notes:
1. All outputs are measured from the midpoint voltage of the falling/rising edge of TCLK to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50Ω load (See Figure 18). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. $\overline{TRST}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
3. Non-JTAG signal input timing with respect to TCK.
4. Non-JTAG signal output timing with respect to TCK.
5. Guaranteed by design and characterization.

Figure 18 provides the AC test load for TDO and the boundary-scan outputs of the PC755.

Figure 18. ALTERNATE AC Test Load for the JTAG Interface

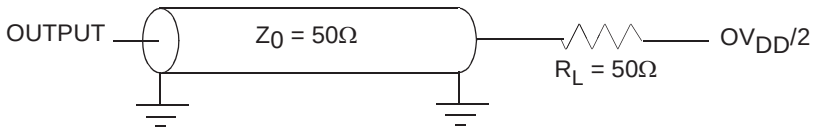
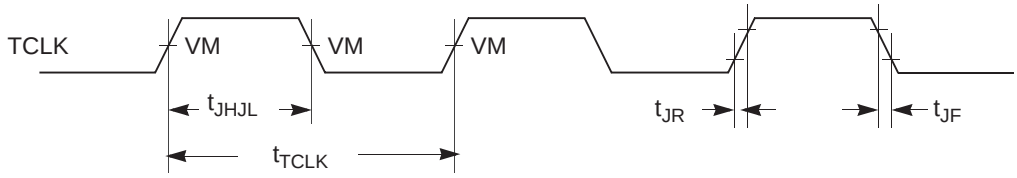


Figure 19 provides the JTAG clock input timing diagram.

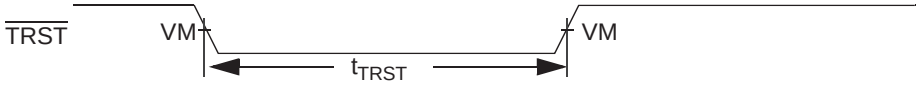
Figure 19. JTAG Clock Input Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 20 provides the $\overline{\text{TRST}}$ timing diagram.

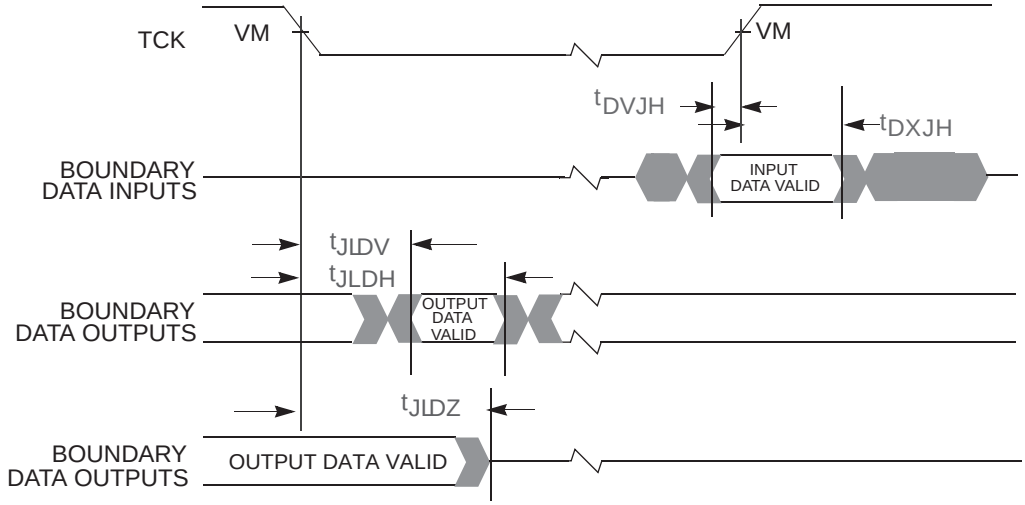
Figure 20. $\overline{\text{TRST}}$ Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 21 provides the boundary-scan timing diagram.

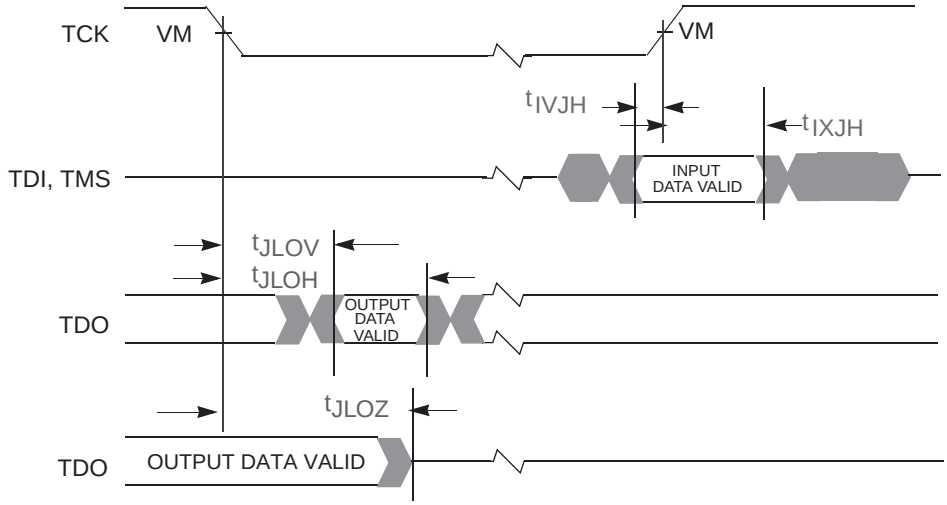
Figure 21. Boundary-Scan Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

Figure 22 provides the test access port timing diagram.

Figure 22. Test Access Port Timing Diagram



VM = Midpoint Voltage ($OV_{DD}/2$)

JTAG Configuration Signals

Boundary scan testing is enabled through the JTAG interface signals. The $\overline{\text{TRST}}$ signal is optional in the IEEE 1149.1 specification, but is provided on all processors that implement the PowerPC architecture. While it is possible to force the TAP controller to the reset state using only the TCK and TMS signals, more reliable power-on reset performance will be obtained if the $\overline{\text{TRST}}$ signal is asserted during power-on reset. Because the JTAG interface is also used for accessing the common on-chip processor (COP) function, simply tying $\overline{\text{TRST}}$ to $\overline{\text{HRESET}}$ is not practical.

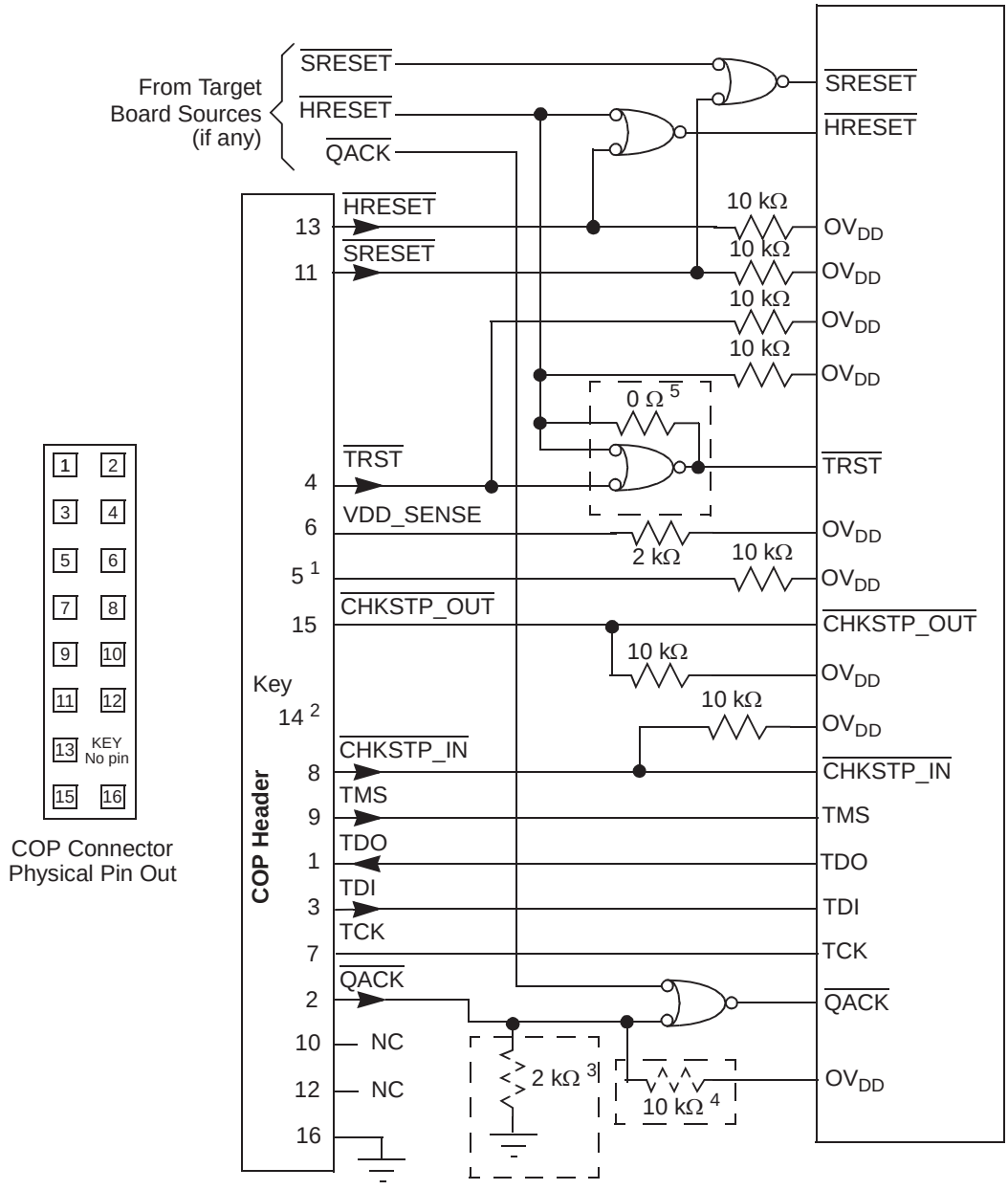
The COP function of these processors allows a remote computer system (typically, a PC with dedicated hardware and debugging software) to access and control the internal operations of the processor. The COP interface connects primarily through the JTAG port of the processor, with some additional status monitoring signals. The COP port requires the ability to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$ in order to fully control the processor. If the target system has independent reset sources, such as voltage monitors, watchdog timers, power supply failures, or push-button switches, then the COP reset signals must bemerged into these signals with logic.

The arrangement shown in Figure 23 allows the COP port to independently assert $\overline{\text{HRESET}}$ or $\overline{\text{TRST}}$, while ensuring that the target can drive $\overline{\text{HRESET}}$ as well. If the JTAG interface and COP header will not be used, $\overline{\text{TRST}}$ should be tied to $\overline{\text{HRESET}}$ through a 0Ω isolation resistor so that it is asserted when the systemreset signal ($\overline{\text{HRESET}}$) is asserted ensuring that the JTAG scan chain is initialized during power-on. While Motorola recommends that the COP header be designed into the system as shown in Figure 23, if this is not possible, the isolation resistor will allow future access to $\overline{\text{TRST}}$ in the casewhere a JTAG interfacemay need to be wired onto the system in debug situations.

The COP header shown in Figure 23 adds many benefits — breakpoints, watchpoints, register and memory examination/modification, and other standard debugger features are possible through this interface — and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

The COP interface has a standard header for connection to the target system, based on the 0.025" square-post 0.100" centered header assembly (often called a Berg header). The connector typically has pin 14 removed as a connector key.

Figure 23. JTAG Interface Connection



Notes:
1. RUN/$\overline{\text{STOP}}$, normally found on pin 5 of the COP header, is not implemented on the PC755. Connect pin 5 of the COP header to OV_{DD} with a 10 kΩ pull-up resistor.
2. Key location; pin 14 is not physically present on the COP header.
3. Component not populated. Populate only if debug tool does not drive $\overline{\text{QACK}}$.
4. Populate only if debug tool uses an open-drain type output and does not actively deassert $\overline{\text{QACK}}$.
5. If the JTAG interface is implemented, connect $\overline{\text{HRESET}}$ from the target source to $\overline{\text{TRST}}$ from the COP header though an AND gate to $\overline{\text{TRST}}$ of the part. If the JTAG interface is not implemented, connect $\overline{\text{HRESET}}$ fromthe target source to $\overline{\text{TRST}}$ of the part through a 0Ω isolation resistor.

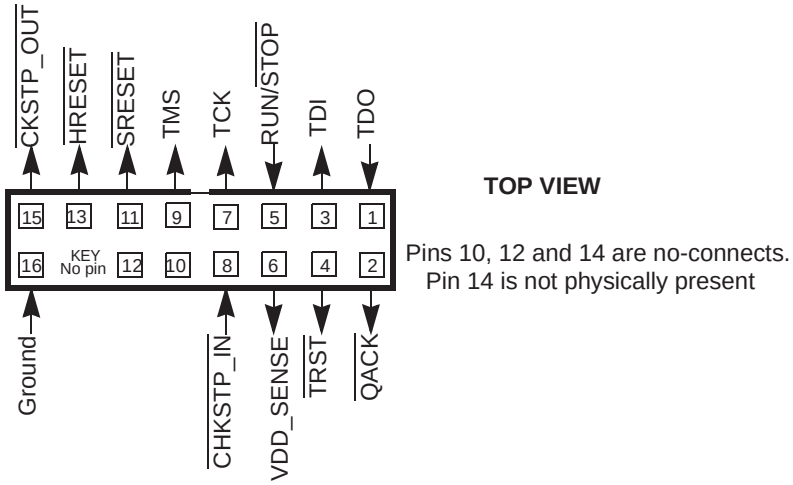
The COP header shown in Figure 24 adds many benefits—breakpoints, watchpoints, register and memory examination/modification and other standard debugger features are possible through this interface – and can be as inexpensive as an unpopulated footprint for a header to be added when needed.

System design information

The COP interface has a standard header for connection to the target system, based on the 0.025” square-post 0.100” centered header assembly (often called a “Berg” header). The connector typically has pin 14 removed as a connector key.

Figure 24 shows the COP connector diagram.

Figure 24. COP Connector Diagram



There is no standardized way to number the COP header shown in Figure 24; consequently, many different pin numbers have been observed from emulator vendors. Some are numbered top-to-bottom then left-to-right, while others use left-to-right then top-to-bottom, while still others number the pins counter clockwise from pin one (as with an IC). Regardless of the numbering, the signal placement recommended in Figure 24 is common to all known emulators.

The $\overline{\text{QACK}}$ signal shown in Table 17 is usually hooked up to the PCI bridge chip in a system and is an input to the PC755 informing it that it can go into the quiescent state. Under normal operation this occurs during a low power mode selection. In order for COP to work the PC755 must see this signal asserted (pulled down). While shown on the COP header, not all emulator products drive this signal. To preserve correct power down operation, $\overline{\text{QACK}}$ should be merged so that it also can be driven by the PCI bridge.

Preparation for Delivery

Packaging

Microcircuits are prepared for delivery in accordance with MIL-PRF-38535.

Certificate of Compliance

Atmel offers a certificate of compliances with each shipment of parts, affirming the products are in compliance either with MIL-PRF-883 and guarantying the parameters not tested at temperature extremes for the entire temperature range.

Handling

MOS devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of static buildup. However, the following handling practices are recommended:

1. Devices should be handled on benches with conductive and grounded surfaces.
2. Ground test equipment, tools and operator.
3. Do not handle devices by the leads.
4. Store devices in conductive foam or carriers.
5. Avoid use of plastic, rubber, or silk in MOS areas.
6. Maintain relative humidity above 50 percent if practical.
7. For CI-CGA packages, use specific tray to take care of the highest height of the package compared with the normal CBGA.

Package Mechanical Data

The following sections provide the package parameters and mechanical dimensions for the PC745, 255 PBGA package as well as the PC755, 360 CBGA and PBGA packages. While both the PC755 plastic and the ceramic packages are described here, both packages are not guaranteed to be available at the same time. All new designs should allow for either ceramic or plastic BGA packages for this device. For more information on designing a common footprint for both plastic and ceramic package types, please contact your local Motorola sales office.

Parameters for the PC745

Package Parameters for the PC745 PBGA

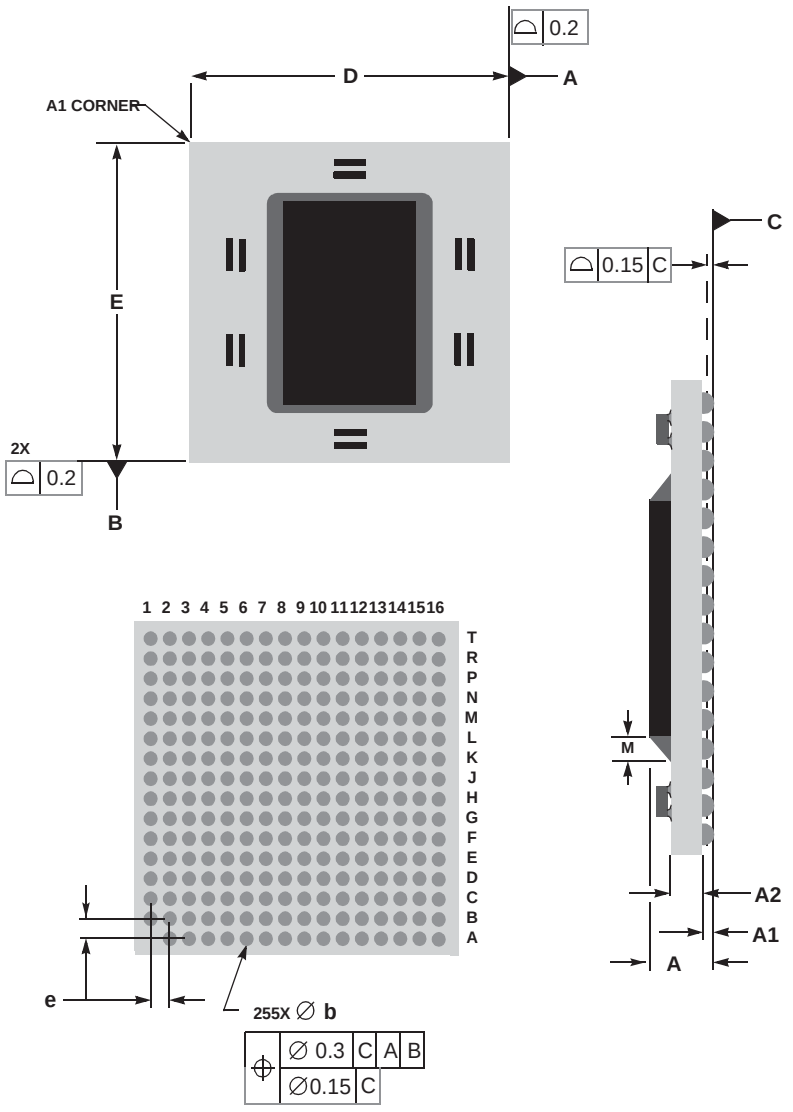
The package parameters are as provided in the following list. The package type is 21 x 21 mm, 255-lead plastic ball grid array (PBGA).

Package outline	21 x 21 mm
Interconnects	255 (16 x 16 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.25 mm
Maximum module height	2.80 mm
Ball diameter (typical)	0.75 mm (29.5 mil)

Mechanical Dimensions of the PC745 PBGA Package

Figure 25 provides the mechanical dimensions and bottom surface nomenclature of the PC745, 255 PBGA package.

Figure 25. Mechanical Dimensions and Bottom Surface Nomenclature of the PC745 PBGA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.
4. CAPACITOR PADS MAY BE UNPOPULATED.

Table 1

	Millimeters	
DIM	**Min**	**Max**
A	2.25	2.80
A1	0.50	0.70
A2	1.00	1.20
b	0.60	0.90
D	21.00 BSC	
E	21.00 BSC	
e	1.27 BSC	

Parameters for the PC755 PBGA

Package Parameter for the PC755 PBGA

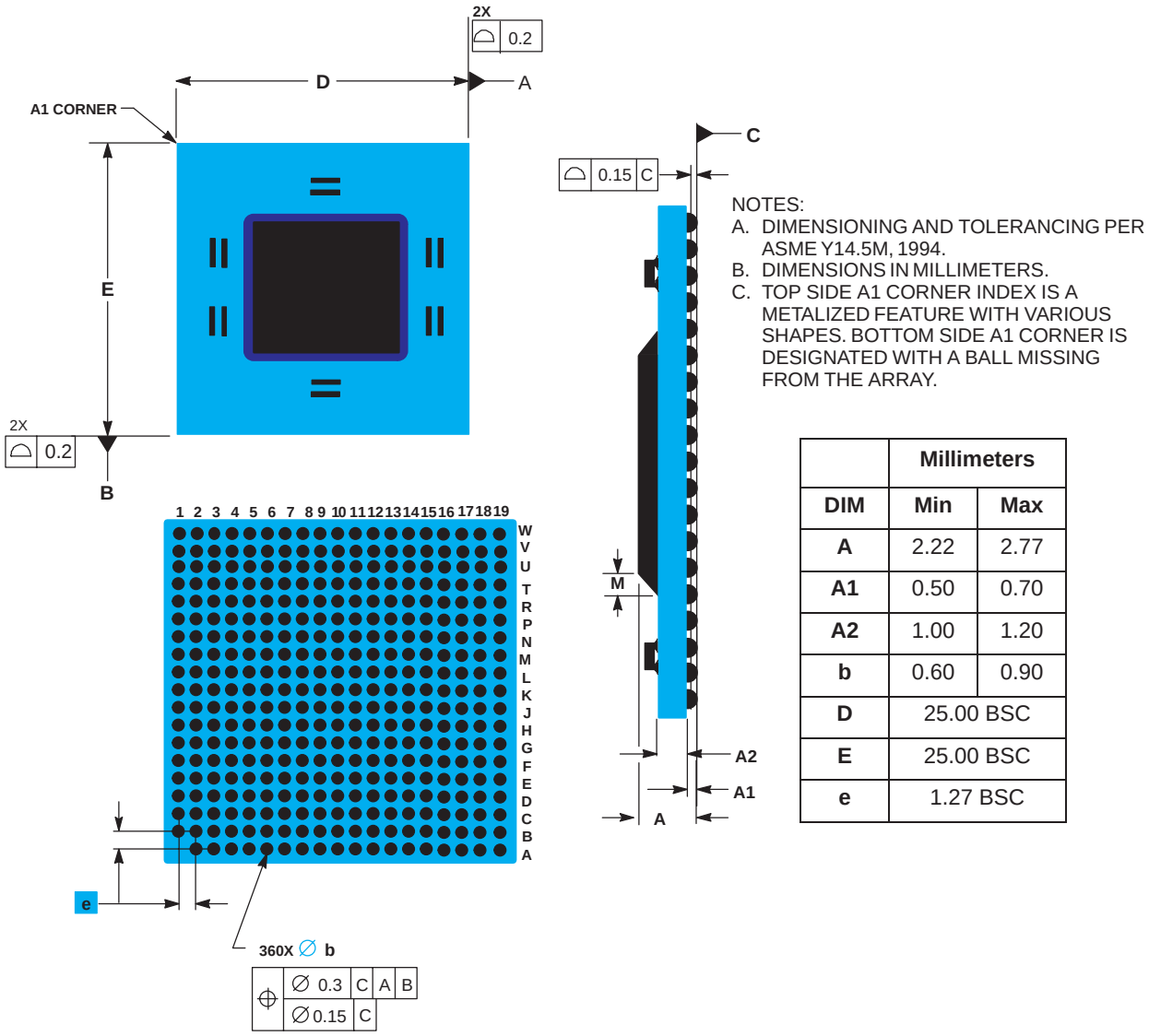
The package parameters are as provided in the following list. The package type is 25 x 25 mm, 360-lead plastic ball grid array (PBGA).

Package outline	25 x 25 mm
Interconnects	360 (19 x 19 ball array – 1)
Pitch	1.27 mm (50 mil)
Minimum module height	2.22 mm
Maximum module height	2.77 mm
Ball diameter	0.75 mm (29.5 mil)

Mechanical Dimensions of the PC755 PBGA

Figure 26 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 PBGA package.

Figure 26. Mechanical Dimensions and Bottom Surface Nomenclature of the PC755 PBGA



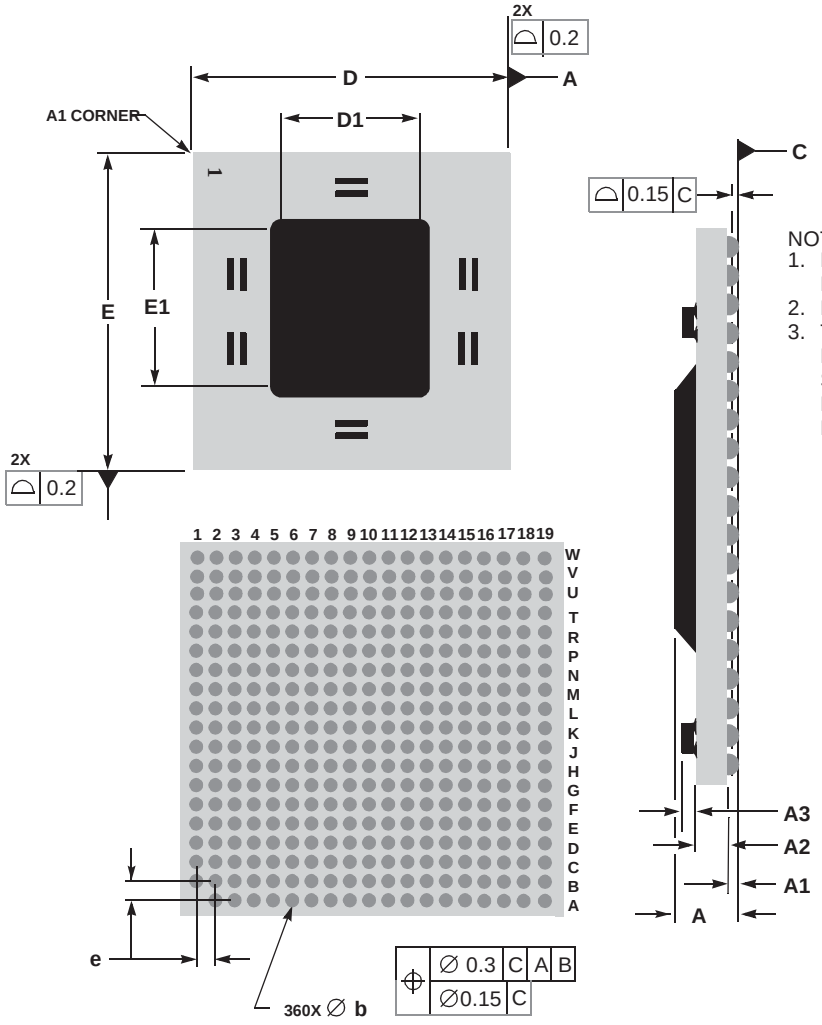
NOTES:
A. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
B. DIMENSIONS IN MILLIMETERS.
C. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	**Min**	**Max**
A	2.22	2.77
A1	0.50	0.70
A2	1.00	1.20
b	0.60	0.90
D	25.00 BSC	
E	25.00 BSC	
e	1.27 BSC	

Mechanical Dimensions of the PC755 CBGA Package

Figure 28 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 CBGA package.

Figure 27. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (CBGA)



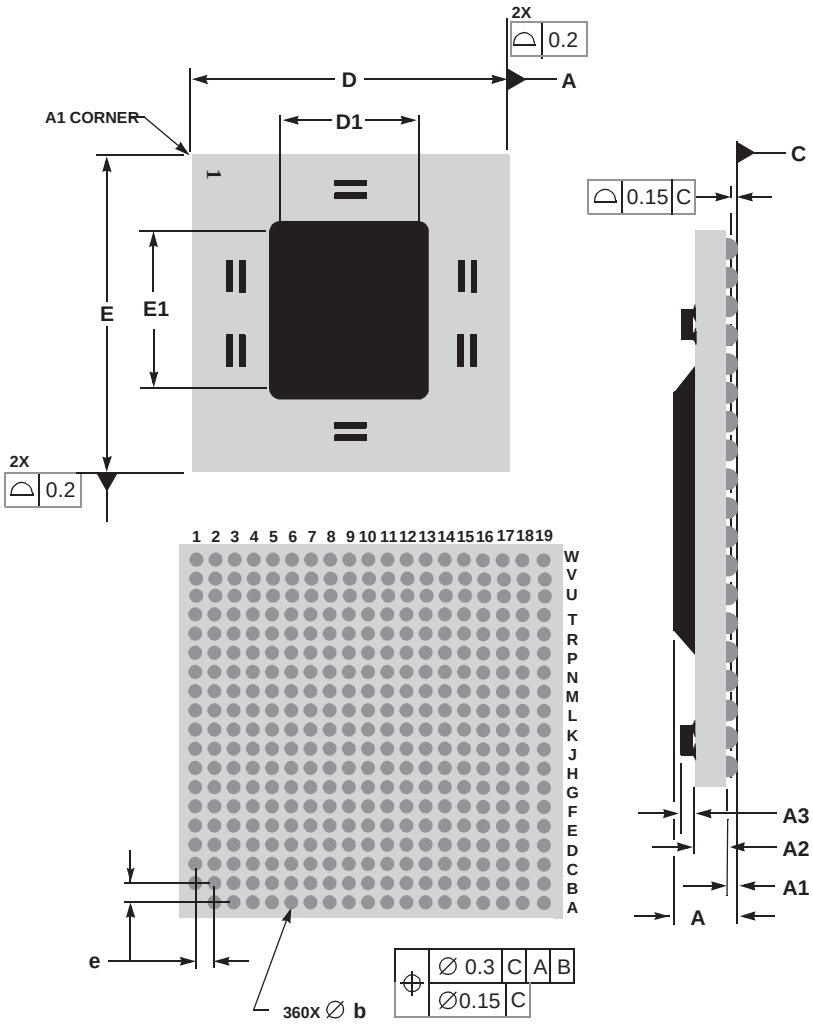
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.20
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Mechanical Dimensions of the PC755 HiTCE Package

Figure 28 provides the mechanical dimensions and bottom surface nomenclature of the PC755, 360 HiTCE package.

Figure 28. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (HiTCE)



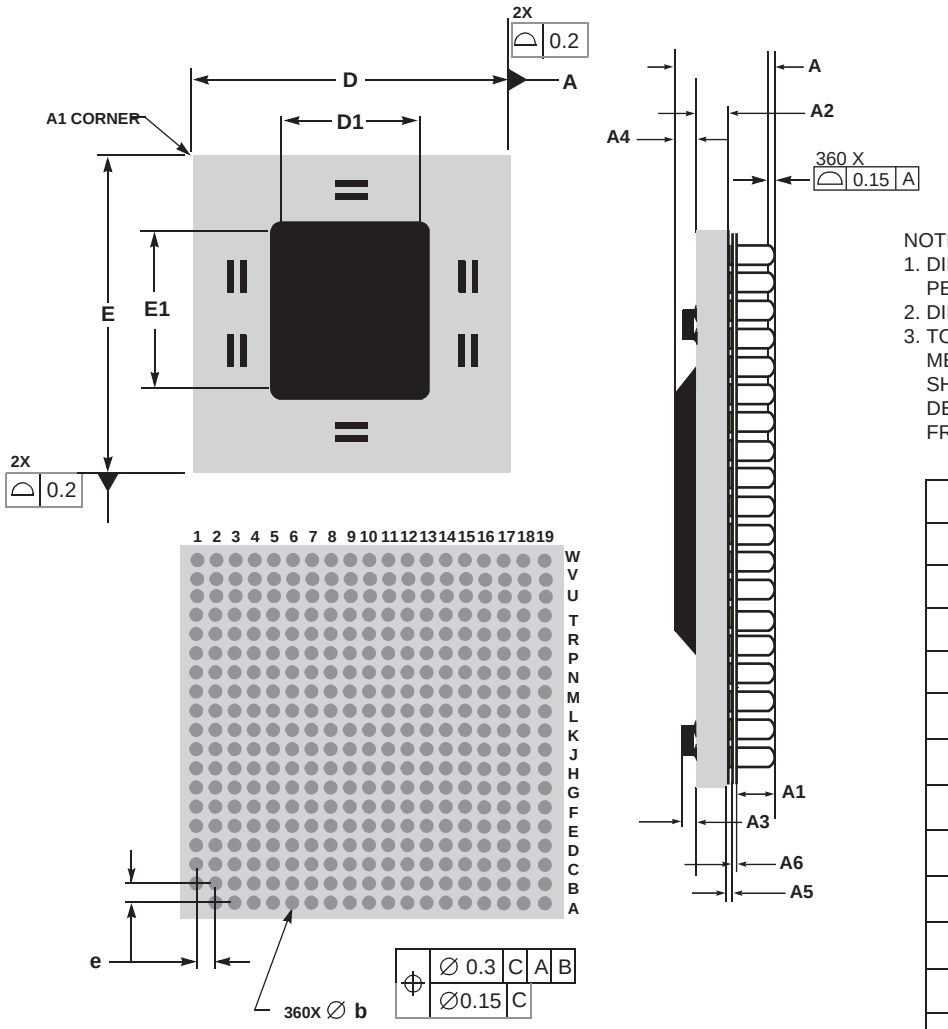
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	**Min**	**Max**
A	2.65	3.24
A1	0.79	0.99
A2	1.10	1.30
A3	—	0.60
b	0.82	0.93
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Mechanical Dimensions of the PC755 CI-CGA Package

Figure 29 provides the mechanical dimensions and bottom surface nomenclature of PC755, 360 CI-CGA package

Figure 29. Mechanical Dimensions and Bottom Surface Nomenclature of PC755 (CI-CGA)



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS IN MILLIMETERS.
3. TOP SIDE A1 CORNER INDEX IS A METALIZED FEATURE WITH VARIOUS SHAPES. BOTTOM SIDE A1 CORNER IS DESIGNATED WITH A BALL MISSING FROM THE ARRAY.

	Millimeters	
DIM	**Min**	**Max**
A	4.04 BSC	
A1	1.545	1.695
A2	1.10	1.30
A3	—	0.60
A4	0.82	0.9
A5	0.10 BSC	
A6	0.25	0.35
b	0.79	0.990
D	25.00 BSC	
D1	6.75	
E	25.00 BSC	
E1	7.87	
e	1.27 BSC	

Clock Relationship Choices

The PC755's PLL is configured by the PLL_CFG[0-3] signals. For a given SYSCLK (bus) frequency, the PLL configuration signals set the internal CPU and VCO frequency of operation. The PLL configuration for the PC755 is shown in Figure 31 for example frequencies.

Table 18. PC755 Microprocessor PLL Configuration

PLL_CFG [0-3]	Example Bus-to-Core Frequency in MHz (VCO Frequency in MHz)							
	Bus-to-Core Multiplier	**Core-to VCO Multiplier**	**Bus 33 MHz**	**Bus 50 MHz**	**Bus 66 MHz**	**Bus 75 MHz**	**Bus 80 MHz**	**Bus 100 MHz**
0100	2x	2x	-	-	-	-	-	200 (400)
1000	3x	2x	-	-	200 (400)	225 (450)	240 (480)	300 (600)
1110	3.5x	2x	-	-	233 (466)	263 (525)	280 (560)	350 (700)
1010	4x	2x	-	200 (400)	266 (533)	300 (600)	320 (640)	400 (800)
0111	4.5x	2x	-	225 (450)	300 (600)	338 (675)	360 (720)	-
1011	5x	2x	-	250 (500)	333 (666)	375 (750)	400 (800)	-
1001	5.5x	2x	-	275 (550)	366 5733°	-	-	-
1101	6x	2x	200 (400)	300 (600)	400 (800)	-	-	-
0101	6.5x	2x	216 (433)	325 (650)	-	-	-	-
0010	7x	2x	233 (466)	350 (700)	-	-	-	-
0001	7.5x	2x	250 (500)	375 (750)	-	-	-	-
1100	8x	2x	266 (533)	400 (800)	-	-	-	-
0110	10x	2x	333 (666)	-	-	-	-	-
0011	PLL off/bypass		PLL off, SYSCLK clocks core circuitry directly, 1x bus-to-core implied					
1111	PLL off		PLL off, no core clocking occurs					

Notes:
1. PLL_CFG[0:3] settings not listed are reserved.
2. The sample bus-to-core frequencies shown are for reference only. Some PLL configurations may select bus, core, or VCO frequencies which are not useful, not supported, or not tested for by the PC755; see Section «Clock AC Specifications» page 25 for valid SYSCLK, core, and VCO frequencies.
3. In PLL-bypass mode, the SYSCLK input signal clocks the internal processor directly, the PLL is disabled, and the bus mode is set for 1:1 mode operation. This mode is intended for factory use and emulator tool use only.
   Note: The AC timing specifications given in this document do not apply in PLL-bypass mode.
4. In PLL off mode, no clocking occurs inside the PC755 regardless of the SYSCLK input.

The PC755 generates the clock for the external L2 synchronous data SRAMs by dividing the core clock frequency of the PC755. The divided-down clock is then phase-adjusted by an on-chip delay-lock-loop (DLL) circuit and should be routed from the PC755 to the external RAMs. A separate clock output, L2SYNC_OUT is sent out half the distance to the SRAMs and then returned as an input to the DLL on pin L2SYNC_IN so that the rising-edge of the clock as seen at the external RAMs can be aligned to the clocking of the internal latches in the L2 bus interface.

The core-to-L2 frequency divisor for the L2 PLL is selected through the L2CLK bits of the L2CR register. Generally, the divisor must be chosen according to the frequency supported by the external RAMs, the frequency of the PC755 core, and the phase adjustment range that the L2 DLL supports. Figure 18 shows various example L2 clock frequencies that can be obtained for a given set of core frequencies. The minimum L2 frequency target is 80 MHz.

Table 19. Sample Core-to-L2 Frequencies

Core Frequency in MHz	1	1.5	2	2.5	3
250	250	166	125	100	83
266	266	177	133	106	89
275	275	183	138	110	92
300	300	200	150	120	100
325	325	217	163	130	108
333	333	222	167	133	111
350	350	233	175	140	117
366	366	244	183	146	122
375	375	250	188	150	125
400	400	266	200	160	133

Note: The core and L2 frequencies are for reference only. Some examples may represent core or L2 frequencies which are not useful, not supported, or not tested for by the PC755; see Section “L2 Clock AC Specifications” page 28 for valid L2CLK frequencies. The L2CR[L2SL] bit should be set for L2CLK frequencies less than 110 MHz.

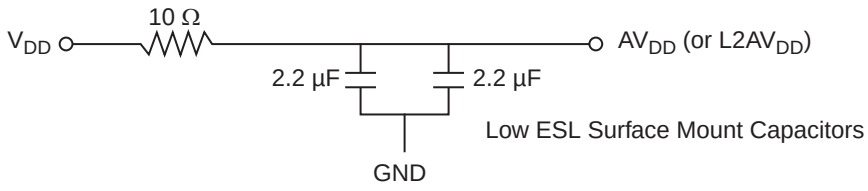
System Design Information

PLL Power Supply Filtering

The AV_{DD} and $L2AV_{DD}$ power signals are provided on the PC755 to provide power to the clock generation phase-locked loop and L2 cache delay-locked loop respectively. To ensure stability of the internal clock, the power supplied to the AV_{DD} input signal should be filtered of any noise in the 500 kHz to 10 MHz resonant frequency range of the PLL. A circuit similar to the one shown in Figure 31 using surface mount capacitors with minimum Effective Series Inductance (ESL) is recommended. Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

The circuit should be placed as close as possible to the AV_{DD} pin to minimize noise coupled from nearby circuits. An identical but separate circuit should be placed as close as possible to the $L2AV_{DD}$ pin. It is often possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of the 360 BGA footprint, without the inductance of vias. The $L2AV_{DD}$ pin may be more difficult to route but is proportionately less critical.

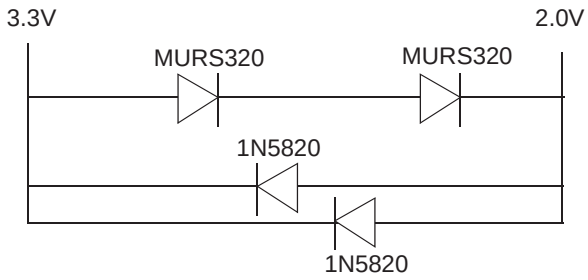
Figure 30. PLL Power Supply Filter Circuit



Power Supply Voltage Sequencing

The notes in Figure 32 contain cautions about the sequencing of the external bus voltages and core voltage of the PC755 (when they are different). These cautions are necessary for the long term reliability of the part. If they are violated, the ESD (Electrostatic Discharge) protection diodes will be forward biased and excessive current can flow through these diodes. If the system power supply design does not control the voltage sequencing, the circuit of Figure 32 can be added to meet these requirements. The MUR420 Schottky diodes of Figure 32 control the maximum potential difference between the external bus and core power supplies on power-up and the 1N5820 diodes regulate the maximum potential difference on power-down.

Figure 31. Example Voltage Sequencing Circuit



Decoupling Recommendations

Due to the PC755's dynamic power management feature, large address and data buses, and high operating frequencies, the PC755 can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the PC755 system, and the PC755 itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each V_{DD}, OV_{DD}, and $L2OV_{DD}$ pin of the PC755. It is also recommended that these decoupling capacitors receive their power from separate V_{DD}, $(L2)OV_{DD}$ and GND power planes in the PCB, utilizing short traces to minimize inductance.

These capacitors should have a value of 0.01 µF or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0508 or 0603 orientations where connections are made along the length of the part.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the V_{DD}, $L2OV_{DD}$, and OV vplanes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors – 100-330 µF (AVX TPS tantalum or Sanyo OSCON).

Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level through a resistor. Unused active low inputs should be tied to OV_{DD}. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

Power and ground connections must be made to all external V_{DD}, OV_{DD}, $L2OV_{DD}$, and GND pins of the PC755.

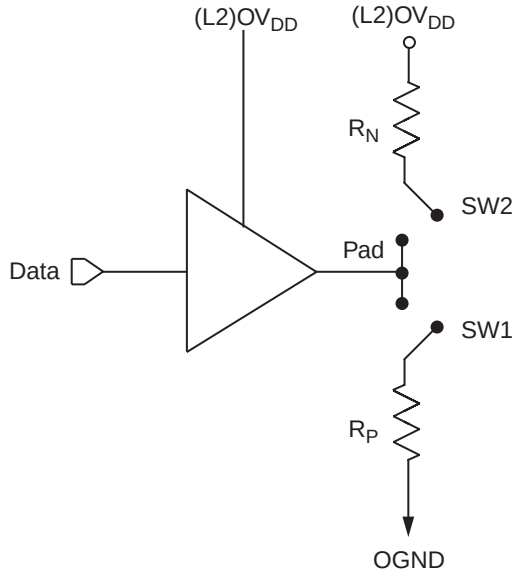
Output Buffer DC Impedance

The PC755 60x and L2 I/O drivers are characterized over process, voltage, and temperature. To measure Z_0, an external resistor is connected from the chip pad to $(L2)OV_{DD}$ or GND. Then, the value of each resistor is varied until the pad voltage is $(L2)OV_{DD}/2$ (See Figure 33).

The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When Data is held low, SW2 is closed (SW1 is open), and R_N is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_N then becomes the resistance of the pull-down devices. When Data is held high, SW1 is closed (SW2 is open), and R_P is trimmed until the voltage at the pad equals $(L2)OV_{DD}/2$. R_P then becomes the resistance of the pull-up devices.

NO TAG describes the driver impedance measurement circuit described above.

Figure 32. Driver Impedance Measurement Circuit



Alternately, the following is another method to determine the output impedance of the PC755. A voltage source, V_{force}, is connected to the output of the PC755 as in Figure 33. Data is held low, the voltage source is set to a value that is equal to (L2)OV_{DD}/2 and the current sourced by V_{force} is measured. The voltage drop across the pull-down device, which is equal to (L2)OV_{DD}/2, is divided by the measured current to determine the output impedance of the pull-down device, R_N. Similarly, the impedance of the pull-up device is determined by dividing the voltage drop of the pull-up, (L2)OV_{DD}/2, by the current sank by the pull-up when the data is high and V_{force} is equal to (L2)OV_{DD}/2. This method can be employed with either empirical data from a test set up or with data from simulation models, such as IBIS.

R_P and R_N are designed to be close to each other in value. Then $Z_0 = (R_P + R_N)/2$.

Figure 33 describes the alternate driver impedance measurement circuit.

Figure 33. Alternate Driver Impedance Measurement Circuit

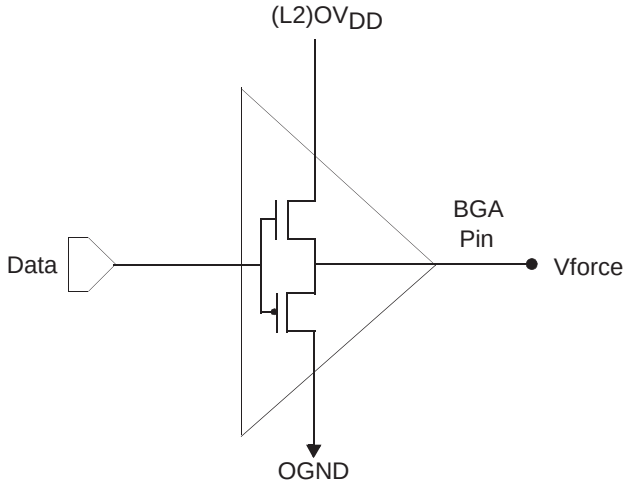


Table 20 summarizes the signal impedance results. The driver impedance values were characterized at 0°C, 65°C, and 105°C. The impedance increases with junction temperature and is relatively unaffected by bus voltage.

Table 20. Impedance Characteristics
V_{DD} = 2.0V, OV_{DD} = 3.3V, T_c = 0 - 105°C

Impedance	Processor bus	L2 bus	Symbol	Unit
RN	25-36	25-36	Z_0	W
RP	26-39	26-39	Z_0	W

Pull–up Resistor Requirements

The PC755 requires pull-up resistors (1 kΩ – 5 kΩ) on several control pins of the bus interface to maintain the control signals in the negated state after they have been actively negated and released by the processor or other bus masters. These pins are $\overline{TS}$, $\overline{ABB}$, $\overline{AACK}$, $\overline{ARTRY}$, $\overline{DBB}$, $\overline{DBWO}$, $\overline{TA}$, $\overline{TEA}$, and $\overline{DBDIS}$. $\overline{DRTRY}$ should also be connected to a pull-up resistor (1 kΩ – 5 kΩ) if it will be used by the system; otherwise, this signal should be connected to $\overline{HRESET}$ to select NO-DRTRY mode.

Three test pins also require pull-up resistors (100Ω – 1 kΩ). These pins are L1_TSTCLK, L2_TSTCLK, and $\overline{LSSD\_MODE}$. These signals are for factory use only and must be pulled up to OV_{DD} for normal machine operation.

In addition, $\overline{\text{CKSTP\_OUT}}$ is an open-drain style output that requires a pull-up resistor (1 kΩ – 5 kΩ) if it is used by the system.

During inactive periods on the bus, the address and transfer attributes may not be driven by any master and may, therefore, float in the high-impedance state for relatively long periods of time. Since the processor must continually monitor these signals for snooping, this float condition may cause additional power draw by the input receivers on the processor or by other receivers in the system. These signals can be pulled up through weak (10 kΩ) pull-up resistors by the system or may be otherwise driven by the system during inactive periods of the bus to avoid this additional power draw, but address bus pull-up resistors are not neccessary for proper device operation. The snooped address and transfer attribute inputs are:
A[0:31], AP[0:3], TT[0:4], $\overline{\text{TBST}}$, and $\overline{\text{GBL}}$.

The data bus input receivers are normally turned off when no read operation is in progress and, therefore, do not require pull-up resistors on the bus. Other data bus receivers in the system, however, may require pull-ups, or that those signals be otherwise driven by the system during inactive periods by the system. The data bus signals are: DH[0:31], DL[0:31], and DP[0:7].

If 32-bit data bus mode is selected, the input receivers of the unused data and parity bits will be disabled, and their outputs will drive logic zeros when they would otherwise normally be driven. For this mode, these pins do not require pull-up resistors, and should be left unconnected by the system to minimize possible output switching.

If address or data parity is not used by the system, and the respective parity checking is disabled through HID0, the input receivers for those pins are disabled, and those pins do not require pull-up resistors and should be left unconnected by the system. If all parity generation is disabled through HID0, then all parity checking should also be disabled through HID0, and all parity pins may be left unconnected by the system.

Definitions

Datasheet Status		**Validity**
Objective specification	This datasheet contains target and goal specification for discussion with customer and application validation.	Before design phase.
Target specification	This datasheet contains target or goal specification for product development.	Valid during the design phase.
Preliminary specification ∝ site	This datasheet contains preliminary data. Additional data may be published later; could include simulation result.	Valid before characterization phase.
Preliminary specification β site	This datasheet contains also characterization results.	Valid before the industrialization phase.
Product specification	This datasheet contains final product specification.	Valid for production purpose.
Limiting Values		
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.		
Application Information		
Where application information is given, it is advisory and does not form part of the specification.		

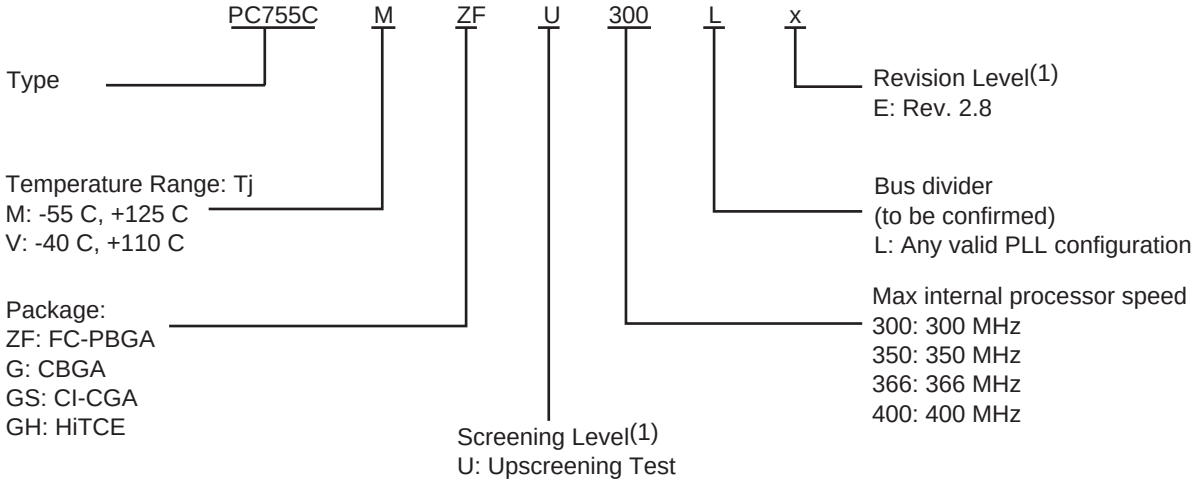
Life Support Applications

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Atmel customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnity Atmel for any damages resulting from such improper use or sale.

Differences with Commercial Part

	Commercial part	Military part
Temperature range	T_j = 0 to 105°C	T_j = -55°C to 125°C

Ordering Information



Note: For availability of different versions, contact your Atmel sales office.

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Europe

Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
Tel: (41) 26-426-5555
Fax: (41) 26-426-5500

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

Zone Industrielle
13106 Rousset Cedex, France
Tel: (33) 4-42-53-60-00
Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom

Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
Tel: (33) 4-76-58-30-00
Fax: (33) 4-76-58-34-80

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e-mail
literature@atmel.com

Web Site
http://www.atmel.com

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