



DOCUMENT NUMBER AND REVISION
VL-FS-MGLS128128-29C REV. B
(MGLS128128T-HT-F-LED WHITE)

DOCUMENT TITLE:
SPECIFICATION
OF
LCD MODULE TYPE

DEPARTMENT	NAME	SIGNATURE	DATE
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DISTRIBUTION LIST: MARKETING



DOCUMENT REVISION HISTORY 1:

DOCUMENT REVISION FROM TO		DATE	DESCRIPTION	CHANGED BY	CHECKED BY
	0.0	2000.08.01	First Release.		
0.0	A	2002.02.28	<p>Items 1 to 7 were updated: (Based on Test Specification: VL-TS-MGLS128128-XX,REV.F, 2003.01.13).</p> <p>1.)(Whole document)The numbers of points were updated. 2.)(Page 4, point 1)“8 K byte display RAM” was added and “1/12bias” was changed to”1/12.4 bias”. 3.)(Page 4, table 1)For outline dimensions, depth (D) was changed from 16.5mm to 14.5mm. “(Note 1)” was deleted. 4.)(Page 5, Fig. 1(A))Drawing was updated from Rev. 0 to Rev. 2. 5.)(Page 6, Fig. 1(B))Backlight Drawing was changed from LBL-128128-5W1 (Rev. 0) to LBL-128128-01A(Rev. 3). 6.)(Page 8, table 2)Supply voltage (Logic), Supply voltage (LCD drive), and Input voltage were updated. 7.)(Page 9, table 5)Supply voltage(LCD), Supply current (Logic & LCD), Supply current(LCD), and Supply voltage of white LED05 backlight were updated.</p>	PHILIP CHENG	YU HAO
A	B	2004.05.31	<p>Items 1 to 8 were updated: (Based on a.) Test Specification:VL-TS-MGLS128128-XX, REV. O, 2004.05.19. b.) VL-QUA-012B, REV. W, 2004.03.20. (According to VL-QUA-012B, LCD size is small because Unit Per Laminate=8 which is more than 6pcs/Laminate.)</p> <p>1.) (Page 3, CONTENTS) “LCD COSMETIC CONDITIONS” was added. 2.) (Page 4, point 1) “FPC” were added. 3.)(Page 4, table 1) The depth of outline dimension was changed from “14.5(D) to 14.5MAX.(D). 4.)(Page 4 & 5) Fig. 1(A) was changed to Fig. 1 and Fig. 1(B) was deleted. 5.) (Page 5, Fig. 1(A)) Drawing was updated. 6.) (Page 8, table 5) Supply current(LCD), and Supply voltage of white LED05 backlight were updated. 7.) (Page 11, point 5) “LCD Cosmetic Conditions” was added. 8.)APPENDIX-LED specifications was deleted.</p>	CHEN HUI JUAN	SUNNY LEE



CONTENTS

	<u>Page No.</u>
1. GENERAL DESCRIPTION	4
2. MECHANICAL SPECIFICATIONS	4
3. ABSOLUTE MAXIMUM RATINGS	6
3.1 ELECTRICAL MAXIMUM RATINGS (Ta=25°C)	6
3.2 ENVIRONMENTAL CONDITION	6
4. ELECTRICAL SPECIFICATIONS	7
4.1 INTERFACE SIGNALS	7
4.2 TYPICAL ELECTRICAL CHARACTERISTICS	8
4.3 TIMING SPECIFICATIONS	8
4.4 TIMING DIAGRAM OF VDD AGAINST VO	10
5. LCD COSMETIC CONDITIONS	11



VARITRONIX LIMITED

Specification of LCD Module Type Model No.: MGLS128128-29C

1. General Description

- 128 x 128 dots FSTN Positive Black & White LCD Graphic Module
- Driving scheme: 1:128 multiplexed drive, 1/12.4 bias
- Viewing direction: 6 o' clock.
- 0.50(W) x 0.50(H) dot size.
- 73.0(W) x 73.0(H) mm viewing area.
- 'Toshiba' T6963C-0101 flat pack or equivalent LCD Controller.
- 'Toshiba' T6A40 flat pack or equivalent LCD Common Drivers.
- 'Toshiba' T6A39 flat pack or equivalent LCD Segment Drivers.
- 8 K byte display RAM.
- White LED05 backlight.
- FPC.

2. Mechanical Specifications

The mechanical detail is shown in Fig. 1 and summarized in Table 1 below.

Table 1

Parameter	Specifications	Unit
Outline dimensions	92.0 (W) x 106.0(H) x 14.5MAX.(D)	mm
Viewing area	73.0(W) x 73.0(H)	mm
Active area	70.35(W) x 70.35(H)	mm
Display format	128 (Horizontal) x 128 (Vertical)	dots
Dot size	0.50(W) x 0.50(H)	mm
Dot spacing	0.05(W) x 0.05(H)	mm
Dot pitch	0.55(W) x 0.55(H)	mm
Weight	Approx. 126.0	grams

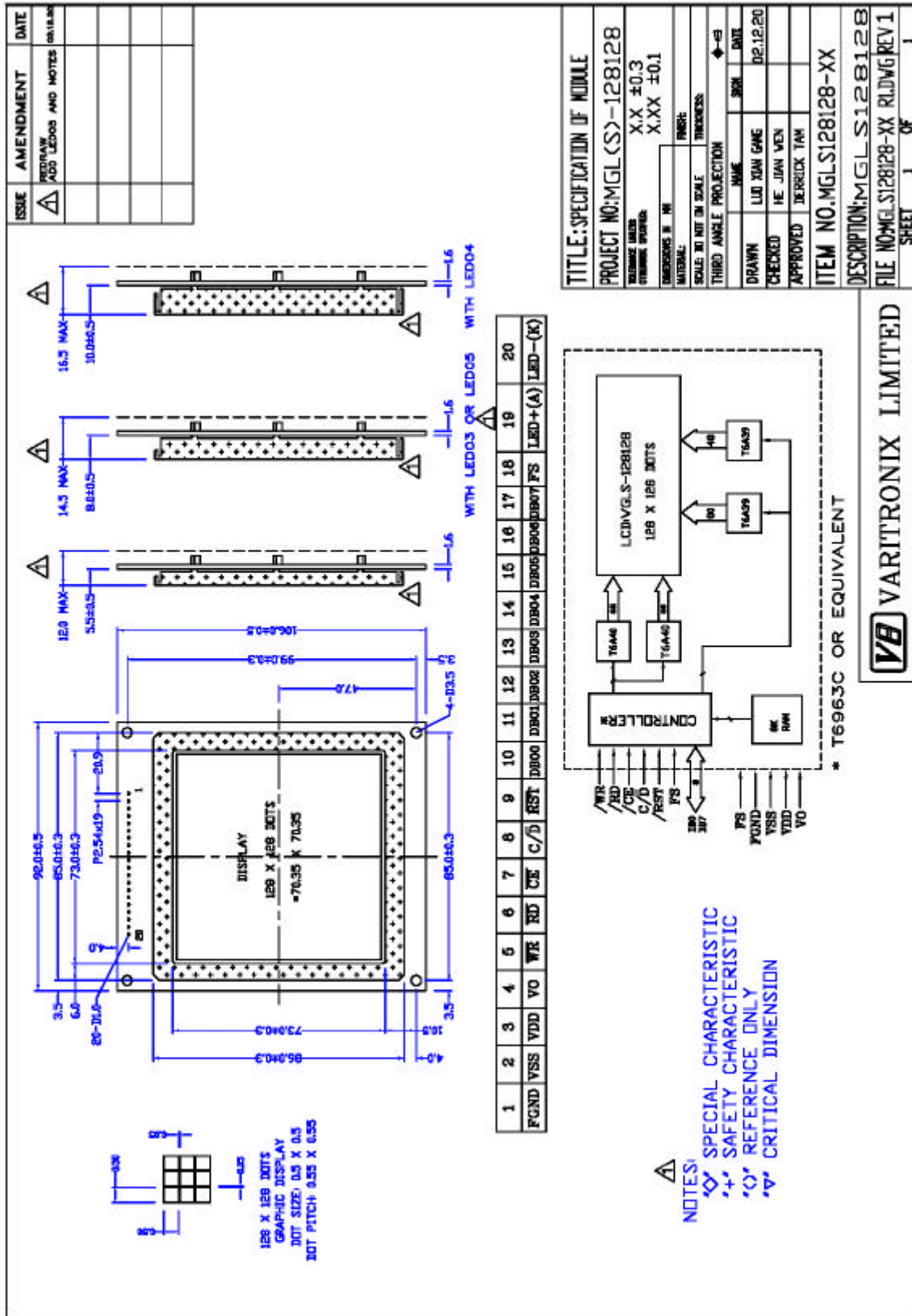


Figure 1: Outline Drawing .



3. Absolute Maximum Ratings

3.1 Electrical Maximum Ratings ($T_a = 25^\circ\text{C}$)

Table 2

Parameter	Symbol	Min.	Max.	Unit
Supply voltage (Logic)	VDD - VSS	-0.3	+7.0	V
Supply voltage (LCD drive)	VLCD=VDD - V0	-0.3	+28.0	V
Input voltage	Vin	-0.3	VDD +0.3	V

Note:

The modules may be destroyed if they are used beyond the absolute maximum ratings.

All voltage values are referenced to VSS = 0V.

3.2 Environmental Condition

Table 3

Item	Operating Temperature (T _{opr})		Storage Temperature (T _{stg})		Remark
	Min.	Max.	Min.	Max.	
Ambient Temperature	-20°C	+70°C	-30°C	+80°C	Dry
Humidity	95% max. RH for $T_a \leq 40^\circ\text{C}$ < 95% RH for $T_a > 40^\circ\text{C}$				no condensation
Vibration (IEC 68-2-6) cells must be mounted on a suitable connector	Frequency: 10 ~ 55 Hz Amplitude: 0.75 mm Duration: 20 cycles in each direction.				3 directions
Shock (IEC 68-2-27) Half-sine pulse shape	Pulse duration: 11 ms Peak acceleration: $981\text{ m/s}^2 = 100\text{g}$ Number of shocks: 3 shocks in 3 mutually perpendicular axes.				3 directions



4. Electrical Specifications

4.1. Interface signals

Table 4

Pin No.	Symbol	Description
1	FGND	Frame Ground (see note 1)
2	VSS	Ground(0V)
3	VDD	Power supply for logic (+5V)
4	V0	Power supply for LCD drive
5	\overline{WR}	Command/Data write to module when "L"
6	\overline{RD}	Command/Data read from module when "L"
7	\overline{CE}	Chip enable of controller when "L"
8	C/D	Command/Data read /write. "H" for command read/write and "L" for data read/write.
9	\overline{RST}	Controller reset when "L"
10	DB00	Data input/output (LSB)
11	DB01	Data input/output
12	DB02	Data input/output
13	DB03	Data input/output
14	DB04	Data input/output
15	DB05	Data input/output
16	DB06	Data input/output
17	DB07	Data input/output (MSB)
18	FS	Font select. "H" for 6 x 8 font & "L" for 8 x 8 font
19	LED+(A)	Anode of LED backlight.
20	LED-(K)	Cathode of LED backlight.

Note 1: This pin is electrically connected to the metal bezel(frame).
User can choose to connect this pin to VSS or leave it open.



4.2 Typical Electrical Characteristics

At $T_a = 25\text{ }^\circ\text{C}$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$.

Table 5

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	$V_{DD} - V_{SS}$		4.75	5.00	5.25	V
Supply voltage (LCD)	$V_{LCD} = V_{DD} - V_0$	$V_{DD} = 5V$, Note 1	19.8	20.3	20.8	V
Input signal voltage	V_{IN}	“H” level	$V_{DD} - 2.2$	-	V_{DD}	V
		“L” level	0	-	0.8	V
Supply current (Logic & LCD)	I_{DD}	Character mode, $V_{DD} = 5V$, Note 1	-	9.1	13.8	mA
		Checker board mode, $V_{DD} = 5V$, Note 1	-	9.6	14.4	mA
Supply current (LCD)	I_0	Character mode, $V_{DD} = 5V$, Note 1	-	3.8	5.7	mA
		Checker board mode, $V_{DD} = 5V$, Note 1	-	4.1	6.1	mA
Supply voltage of white LED05 backlight	V_{LED}	Forward current = 100mA. Number of LED chips = $1 \times 5 = 5$	3.1	3.3	3.5	V

Note 1: There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.



4.3 Timing Specifications

At $T_a = -20^{\circ}\text{C}$ To $+70^{\circ}\text{C}$, $V_{DD} = 5V \pm 5\%$, $V_{SS} = 0V$

Refer to Fig. 2, the bus timing diagram.

Table 6

Parameter	Symbol	Min.	Max.	Unit
C/D Set-up time	t_{CDS}	100	-	ns
C/D Hold Time	t_{CDH}	10	-	ns
/CE,/RD,/WR Pulse Width	t_{CE}, t_{RD}, t_{WR}	80	-	ns
Data Set-up Time	t_{DS}	80	-	ns
Data Hold Time	t_{DH}	40	-	ns
Access Time	t_{ACC}	-	150	ns
Output Hold Time	t_{OH}	10	50	ns

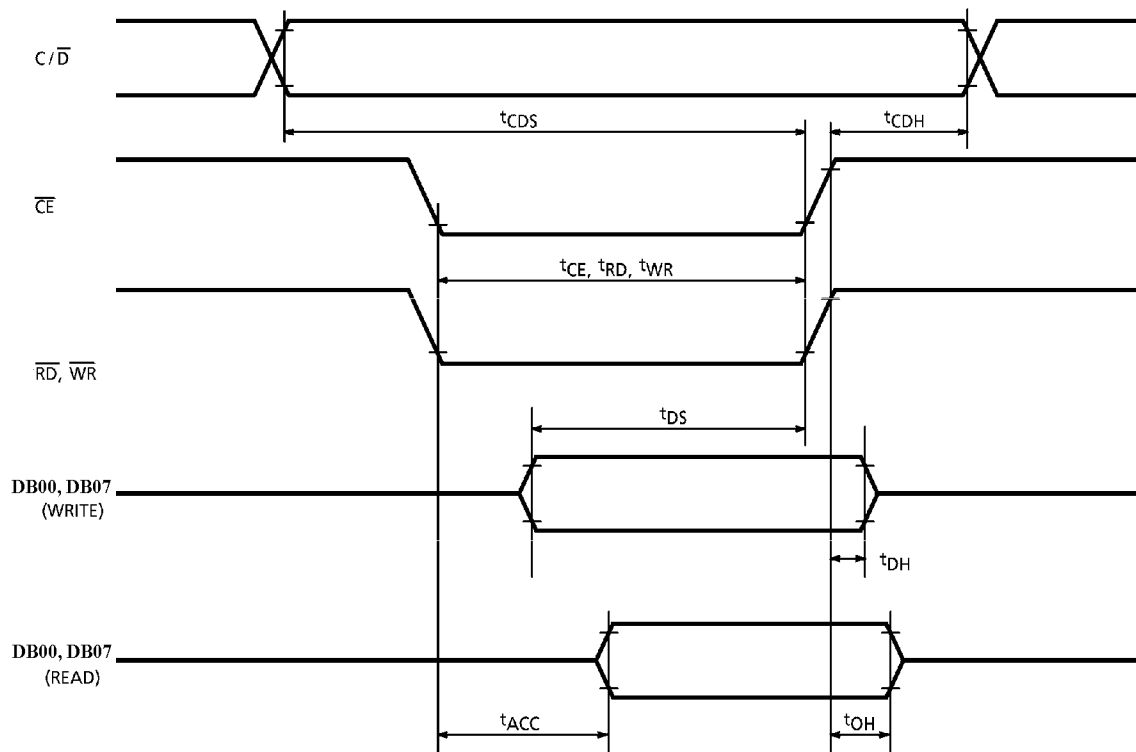


Figure 2: Bus Timing Diagram



4.4 Timing Diagram of VDD Against V0.

Power on sequence shall meet the requirement of Figure 3, the timing diagram of VDD against V0.

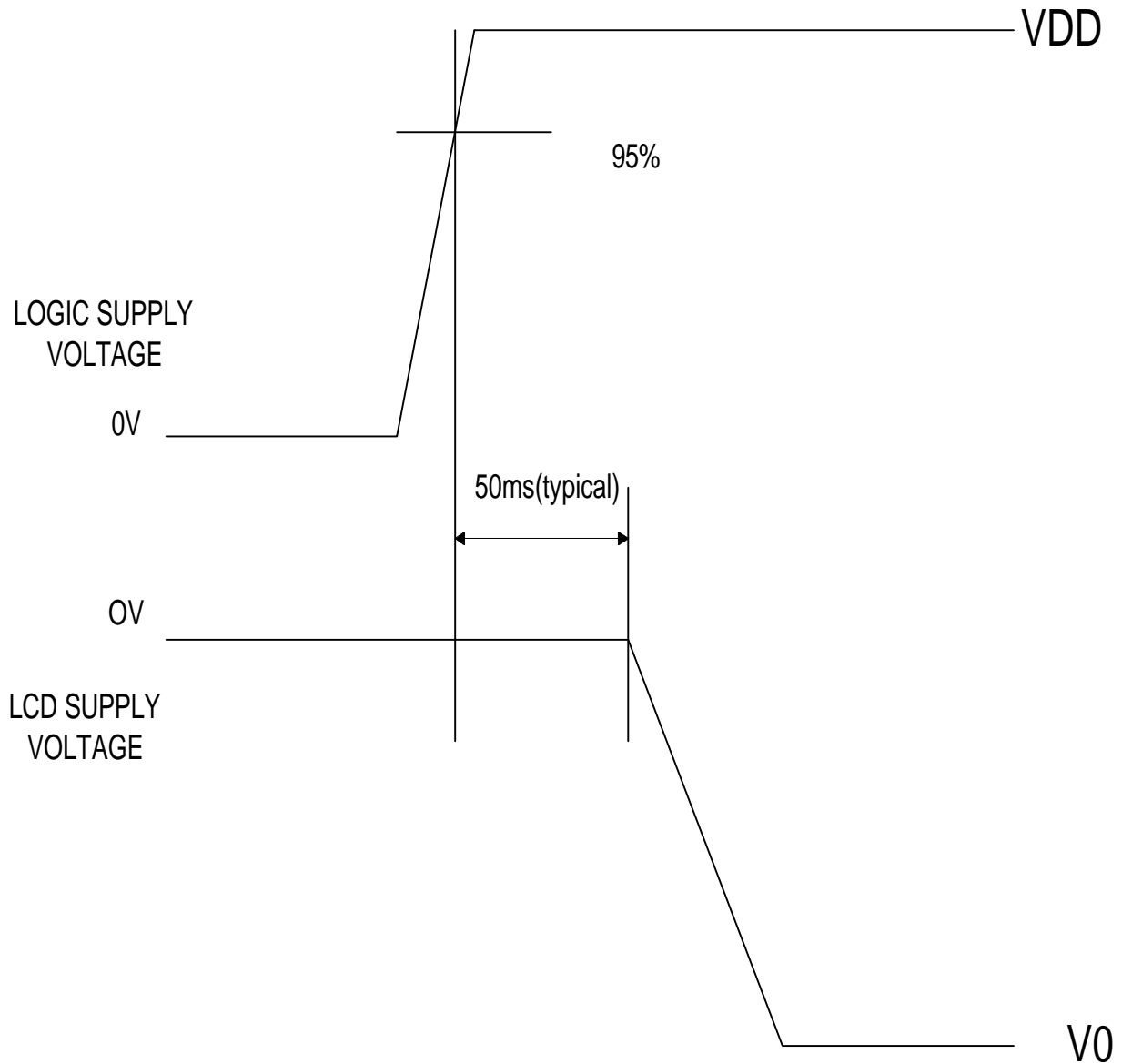


Figure 3: Timing Diagram of VDD Against V0.



5. LCD Cosmetic Conditions

Refer to VL-QUA-012B.

Note: LCD size of the product is small.

“Varitronix Limited reserves the right to change this specification.”

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