2.5 GBIT PORT BYPASS CIRCUIT FOR FIBRE CHANNEL ARBITRATED LOOP S2091

FEATURES

- Supports 2.5 Gbps Data Rates
- Fully differential for minimum jitter accumulation
- TTL Bypass Select
- High speed 50Ω source terminated outputs
- 0.4W Typical power dissipation
- 3.3V power supply
- 20 Pin TSSOP

GENERAL DESCRIPTION

The S2091 is a Port Bypass Circuit (PBC). A single channel Fibre Channel PBC offers designers maximum flexibility in FC-AL disk architectures. The S2091 is designed to minimize jitter accumulation by providing a high bandwidth fully differential signal path. Port Bypass circuits are used to provide resiliency in Fibre Channel Arbitrated Loop (FC-AL) architectures. PBC's are used within FC-AL disk arrays to allow for resiliency and hot swapping of FC-AL drives.

A Port-by-Pass Circuit is a 2:1 Multiplexer with two modes of operations: Normal and Bypass. In Normal mode, the disk drive is connected to the loop. In Bypass mode, the disk drive is either absent or non-functional and data bypasses to the next available disk drive. Normal mode is enabled with a High on the SEL pin and Bypass mode is enable by a Low on the SEL pin. Direct Attach Fibre Channel Disk Drives have an "LRC Interlock" signal defined to control the SEL function. A system diagram showing the S2091 in a single loop of a disk array is illustrated in Figure 2.

The S2091 can be cascaded with the S3040 (Data retimer) for arrays of disk drives greater than 4.

Table 1 is a truth table detailing the data flow through the S2091. Figure 3 shows a timing diagram of the data relationship in the S2091. The primary AC parameter of importance is the deterministic jitter or data eye degradation inserted by the port bypass circuit. The design for the S2091 minimized jitter accumulation by using high bandwidth, low skew fully differential circuits. This provides for symmetric rise and fall delays as well as noise rejection.

Table 1. Truth Table

SEL1	OUT	DDO
0	IN	IN
1	DDI	IN

Figure 1. S2091 Block Diagram

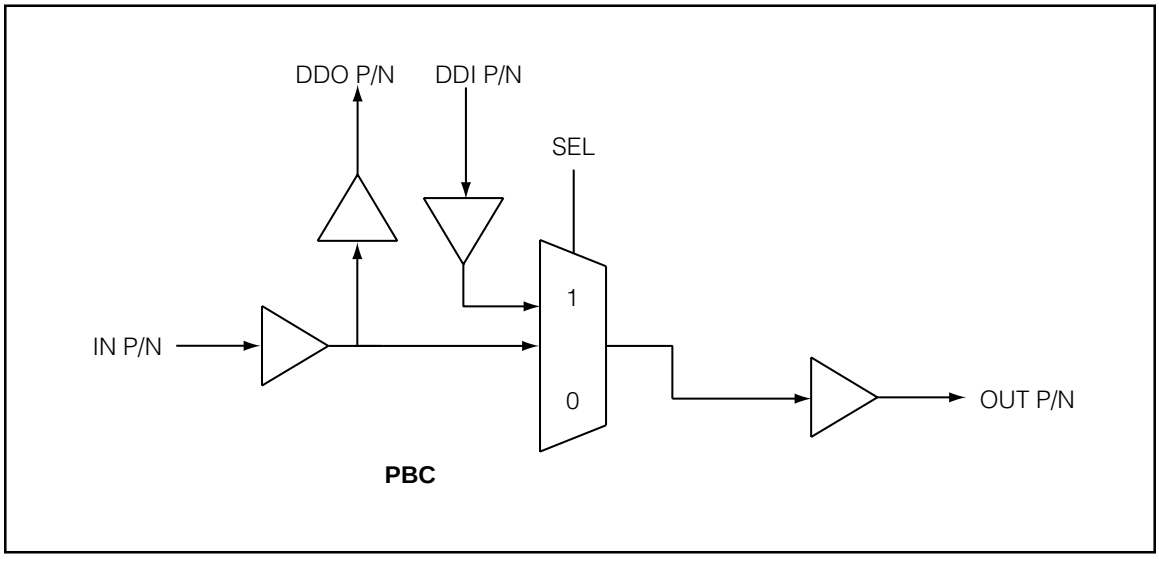


Figure 2. Functional Block Diagram

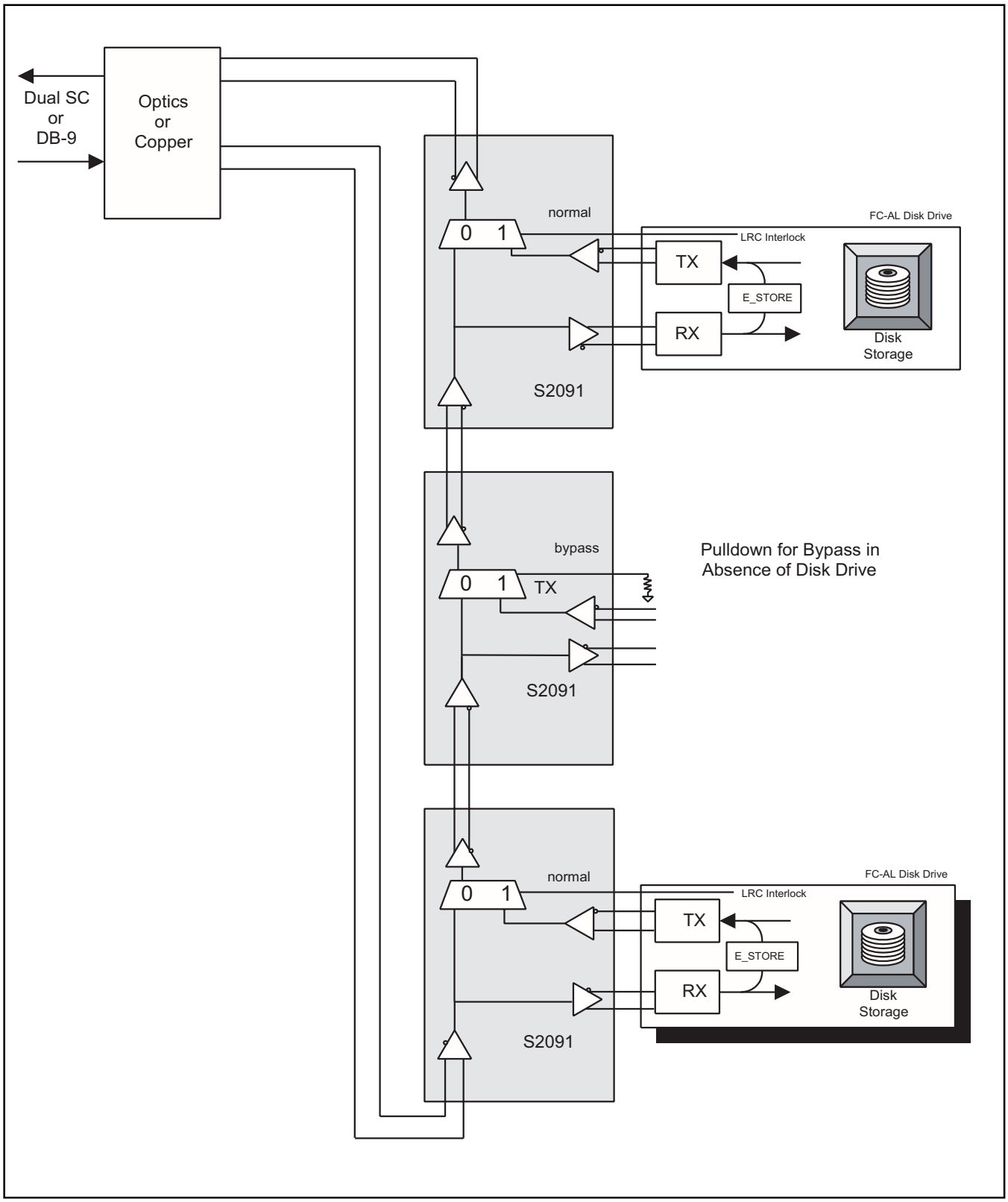


Figure 3. Timing Waveforms

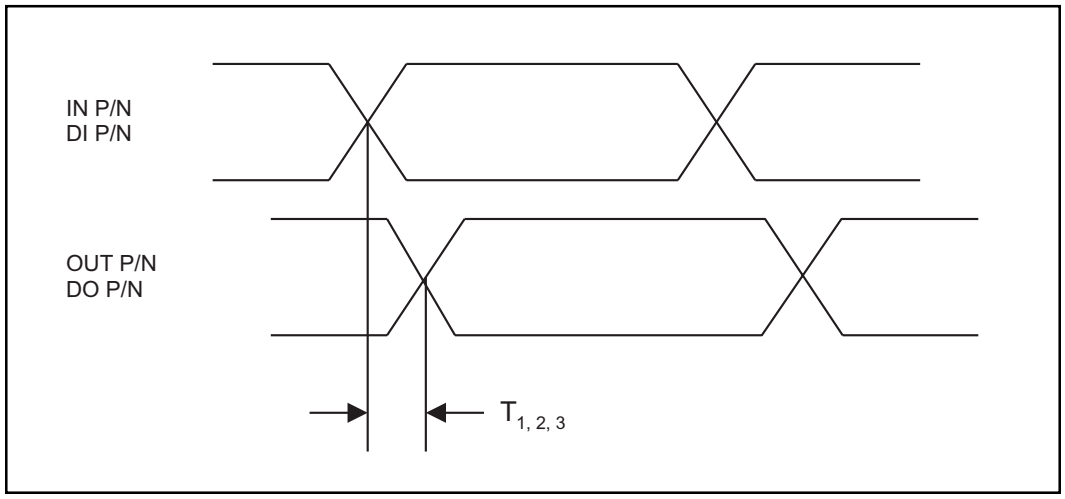


Figure 4. Differential Voltage

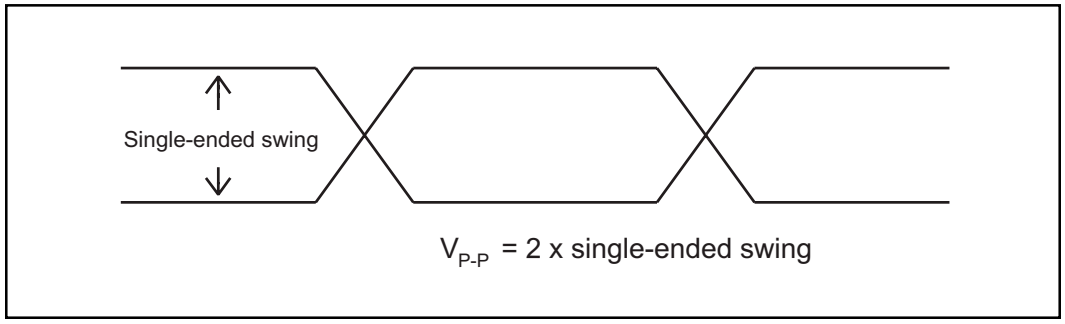


Table 2. Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin#	Description
INP INN	Diff. LVPECL	I	7, 6	Differential inputs from the downstream PBC port.
DDIP DDIN	Diff. LVPECL	I	4, 3	Serial input from the local disk drive.
SEL	LVTTL	I	11	A Low selects the "BYPASS" mode causing the output of the previous port to propagate to the next port or OUT. When High, this signal selects "NORMAL" mode which routes the previous port to the local output, DDO and routes the local input, DDI to the next port or OUT.
DDOP DDON	Diff. CML	O	19, 18	Serial output driving the local disk drive.
OUTP OUTN	Diff. CML	O	15, 14	Serial output driving the upstream PBC port.
VCC			1, 2, 10, 12, 17, 20	Power Supply. 3.3V nominal.
GND			5, 8, 9, 13, 16	Ground. Ground pins are phyisically attached to the die mounting surface, and are an important part of the thermal path. For best thermal performance, all ground pins should be connected to a ground plane, using multiple vias if possible.

Figure 5. S2091 Pinout Package

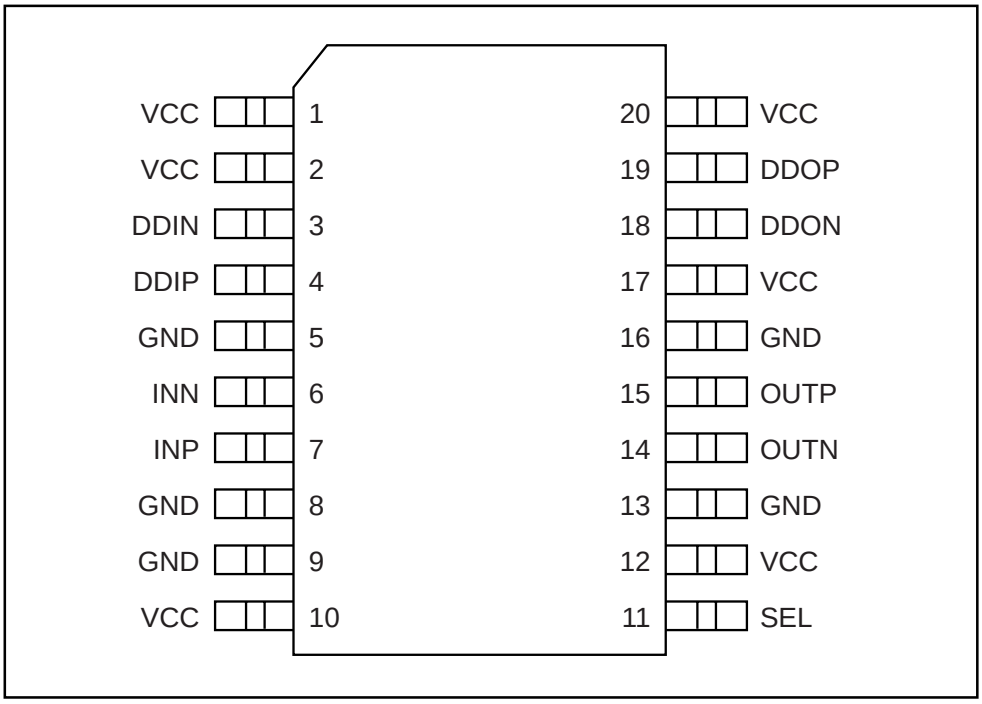
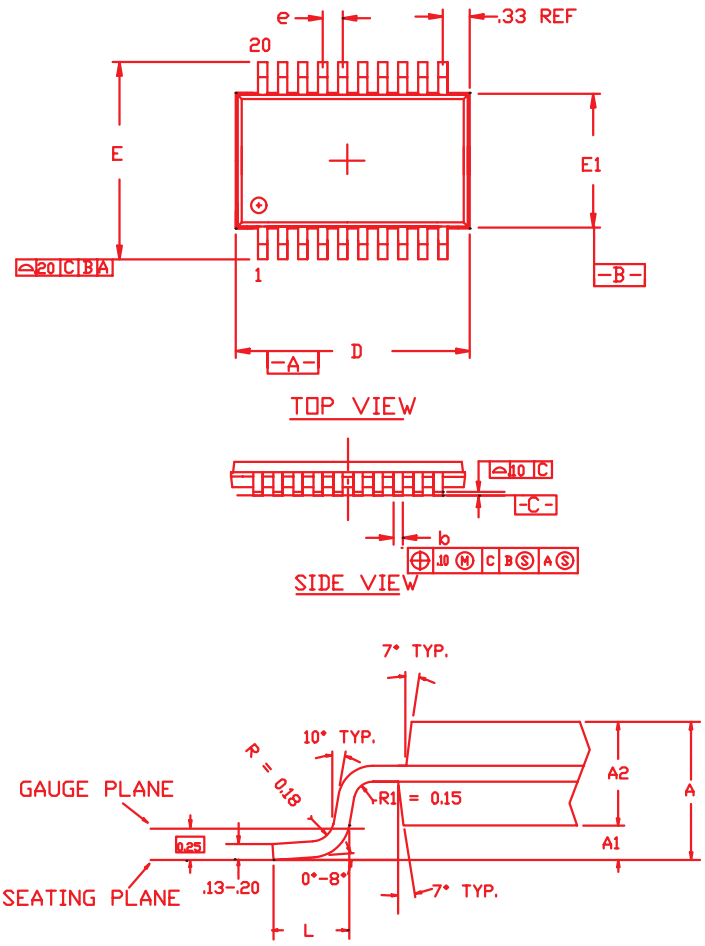


Figure 6. 20 TSSOP Package



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	E	E_1	L	b	e
MIN		0.05		6.45	6.30	4.30	0.50	0.17	0.65 BSC.
NOM			0.90	6.50	6.40	4.40	0.60	0.22	
MAX	1.20	0.10		6.55	6.50	4.50	0.75	0.27	

Thermal Management

Device	Θja (Still Air)	Θjc
S2091A	77 ˚ C/W	25 ˚ C/W

Table 3. AC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Typ	Max	Units	Conditions
T_{R1} T_{F1}	Serial Data rise and fall time (IN to OUT)	105	135	ps	20% to 80% tested on a sample basis. (100Ω line-to-line.)
T_{R2} T_{F2}	Serial Data rise and fall time (IN to DDO)	105	135	ps	20% to 80% tested on a sample basis. (100Ω line-to-line.)
T_{R3} T_{F3}	Serial Data rise and fall time (DDI to OUT)	105	150	ps	20% to 80% tested on a sample basis. (100Ω line-to-line.)
T1	Flow through propagation delay IN to OUT	1.15	1.4	ns	Delay with all circuits bypassed. 50 Ohm load.
T2	Flow through propagation delay IN to DDO	1.15	1.4	ns	Delay with PBC in Normal or Bypass mode. 50 Ohm load.
T3	Flow through propagation delay DDI to OUT	1.15	1.4	ns	Delay with PBC in Normal mode. 50 Ohm load.
$T_{jitterRMS}$	Random jitter accumulation (RMS)	2.2	4	ps	RMS output jitter accumulated with valid 8B/10B code from IN to OUT - PBC in bypass mode. Tested on a sample basis.
$T_{jitterDJ}$	Deterministic jitter accumulation (p-p)	6	±7	ps	Deterministic output jitter accumulated with valid 8B/10B code from IN to OUT, both PBC stages bypassed. Determined by simulation. Actual value not verified due to bandwidth limitation of test equipment.

Table 4. DC Characteristics *(Over recommended operating conditions.)*

Parameter	Description	Min	Typ	Max	Units	Conditions
$V_{IH(ITL)}$	Input HIGH voltage (SEL-TTL)	2.0		VCC	V	
$V_{IL(ITL)}$	Input LOW voltage (SEL-TTL)	0		0.8	V	
$I_{IH(ITL)}$	Input HIGH current (SEL-TTL)			50	µA	V_{IN} = 2.4V
$I_{IL(ITL)}$	Input LOW current (SEL-TTL)	-500		-50	µA	V_{IN} = 0.5V
V_{CC}	Supply Voltage	3.14		3.47	V	V_{CC} = 3.30V ± 5%
I_{CC}	Supply Current		180	230	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		0.4	.8	W	Outputs open, V_{CC} = V_{CC} max
$\Delta V_{IN(DF)}$	Receiver differential peak-to-peak input sensitivity, INP/N & DDIP/N	300		2000	mV_{p-p} [1]	AC Coupled. Internally DC biased V_{CC} - 0.65V
$\Delta V_{OUTN(L\_SO)}$	DDOP/N output differential peak-to-peak voltage swing	1000		1460	mV_{p-p} [1]	100Ω line-to-line
$\Delta V_{OUTN(OUT)}$	OUTP/N output differential peak-to-peak voltage swing	1000		1460	mV_{p-p} [1]	100Ω line-to-line

1. See Figure 4.

Table 5. Absolute Maximum Ratings[1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	0.5		+4	V
PECL DC Input Voltage (V_{INP})	-0.5		V_{CC}+0.5	V
TTL DC Input Voltage (V_{INP})	-0.5		V_{CC}+0.5	V
CML Output Current (I_{OUT}), (DC output High)			90	mA
Case Temperature Under Bias (T_C)	-55		125	C°
Storage Temperature (T_{STG})	-65		150	C°
Static Discharge Voltage			1000	V

1. CAUTION: Stresses listed under “Absolute Maximum Ratings” may be applied one at a time to devices without causing permanent damage. Functionality at or above the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 6. Recommended Operating Conditions[1]

Parameter	Min	Typ	Max	Units
Power Supply Voltage (V_{CC})	+3.14		+3.47	V
Ambient Operating Temperature Range (T)	-40		+85	C°

1. AMCC guarantees the functional and parametric operation of the part under “Recommended Operating Conditions” (except where specifically noted in the AC and DC parametric tables).

Input Structures

Two input structures exist in this part; TTL and high speed, differential inputs. The LVTTL inputs will interface with any LVTTL outputs. The high speed, differential inputs can be AC coupled per the FC-PH specification. Therefore, the high speed, differential input buffers are biased at Vcc -0.65V. Refer to Figure 7 for high speed differential input termination.

Figure 7. Input Termination

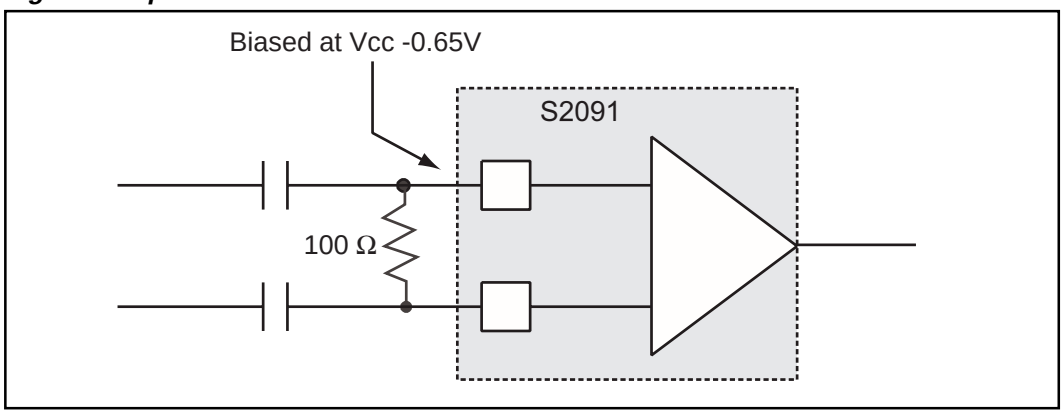
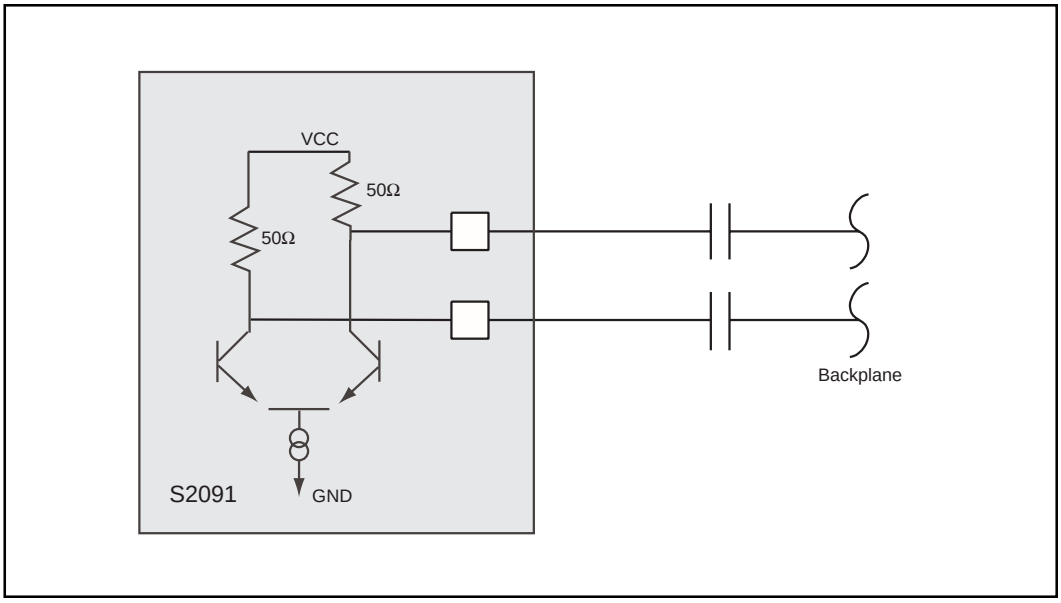


Figure 8. Output



Ordering Information

GRADE	PART NO.	PACKAGE
S- Commercial	2091	A – 20 TSSOP

X Grade XXXX Part No. X Package

ISO 9001 CERTIFIED

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (619) 450-9333 • (800) 755-2622 • Fax: (619) 450-9885
http://www.amcc.com

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