MC10EP445, MC100EP445

3.3V/5V ECL 8-Bit Serial/Parallel Converter

The MC10/100EP445 is an integrated 8–bit differential serial to parallel data converter with asynchronous data synchronization. The device has two modes of operation. CKSEL HIGH mode is designed to operate NRZ data rates of up to 3.3 Gb/s, while CKSEL LOW mode is designed to operate at twice the internal clock data rate of up to 5.0 Gb/s. The conversion sequence was chosen to convert the first serial bit to Q0, the second bit to Q1, etc. Two selectable differential serial inputs, which are selected by SINSEL, provide this device with loop-back testing capability. The MC10/100EP445 has a SYNC pin which, when held high for at least two consecutive clock cycles, will swallow one bit of data shifting the start of the conversion data from D_n to D_{n+1}. Each additional shift requires an additional pulse to be applied to the SYNC pin.

Control pins are provided to reset and disable internal clock circuitry. Additionally, V_{BB} pin is provided for single-ended input condition.

The 100 Series contains temperature compensation.

- 300 ps Propagation Delay
- 5.0 Gb/s Typical Data Rate for CLKSEL LOW Mode
- Differential Clock and Serial Inputs
- V_{BB} Output for Single-Ended Input Applications
- Asynchronous Data Synchronization (SYNC)
- Asynchronous Master Reset (RESET)
- PECL Mode Operating Range: V_{CC} = 3.0 V to 5.5 V with V_{EE} = 0 V
- NECL Mode Operating Range: V_{CC} = 0 V with V_{EE} = -3.0 V to -5.5 V
- Open Input Default State
- CLK ENABLE Immune to Runt Pulse Generation

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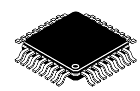
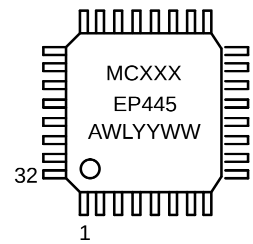
MARKING DIAGRAM*



LQFP-32
FA SUFFIX
CASE 873A

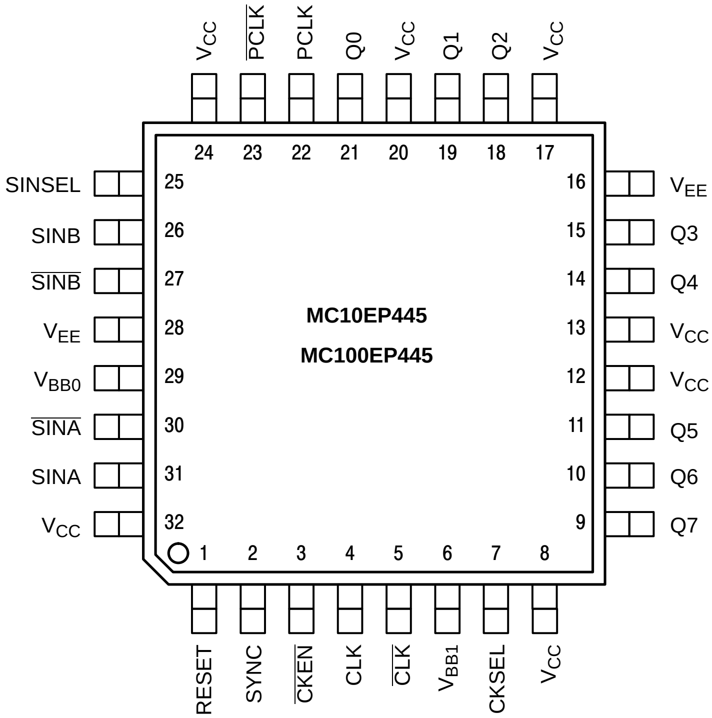


XXX = 10 OR 100
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*For additional information, see Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
MC10EP445FA	LQFP-32	250 Units/Tray
MC10EP445FAR2	LQFP-32	2000/Tape & Reel
MC100EP445FA	LQFP-32	250 Units/Tray
MC100EP445FAR2	LQFP-32	2000/Tape & Reel



Warning: All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.

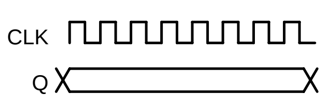
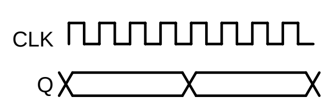
Figure 1. 32-Lead LQFP Pinout (Top View)

PIN DESCRIPTION

PIN	FUNCTION
SINA*, $\overline{\text{SINA}}$*	ECL Differential Serial Data Input A
SINB*, $\overline{\text{SINB}}$*	ECL Differential Serial Data Input B
SINSEL*	ECL Serial Input Selector Pin
Q0-Q7	ECL Parallel Data Outputs
CLK*, $\overline{\text{CLK}}$*	ECL Differential Clock Inputs
PCLK, $\overline{\text{PCLK}}$	ECL Differential Parallel Clock Output
SYNC*	ECL Conversion Synchronizing Input
CKSEL*	ECL Clock Input Selector Pin
$\overline{\text{CKEN}}$*	ECL Clock Enable Pin
RESET*	ECL Reset Pin
V_{BB0}, V_{BB1}	Output Reference Voltage
V_{CC}	Positive Supply
V_{EE}	Negative Supply

* Pins will default logic LOW or differential logic LOW when left open.

TRUTH TABLE

PIN	FUNCTION	
	High	**Low**
SINSEL	Select SINB Input	Select SINA Input
CKSEL	Q: PCLK = 8:1 CLK: Q = 1:1 	Q: PCLK = 8:1 CLK: Q = 1:2 
$\overline{\text{CKEN}}$	Synchronously Disable Internal Clock Circuitry	Synchronously Enable Internal Clock Circuitry
RESET	Asynchronous Master Reset	Synchronous Enable
SYNC	Asynchronously Applied to Swallow a Data Bit	Normal Conversion Process

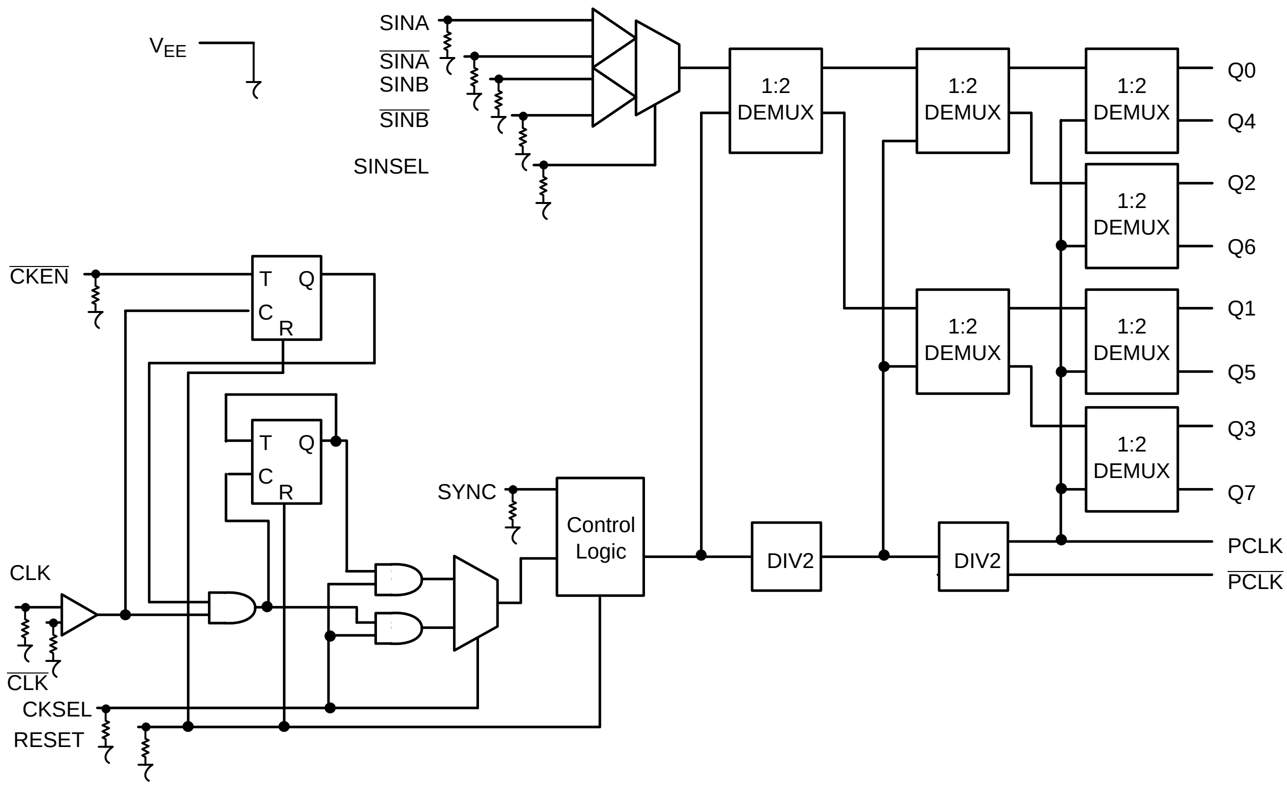


Figure 2. Logic Diagram

ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor		75 kΩ
Internal Input Pull-up Resistor		N/A
ESD Protection	Human Body Model Machine Model Charged Device Model	> 2 kV > 200 V > 2 kV
Moisture Sensitivity (Note 1)		Level 2
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		993 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	PECL Mode Power Supply	V_{EE} = 0 V		6	V
V_{EE}	NECL Mode Power Supply	V_{CC} = 0 V		-6	V
V_I	PECL Mode Input Voltage NECL Mode Input Voltage	V_{EE} = 0 V V_{CC} = 0 V	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
I_{out}	Output Current	Continuous Surge		50 100	mA mA
I_{BB}	V_{BB} Sink/Source			± 0.5	mA
TA	Operating Temperature Range			-40 to +85	°C
T_{stg}	Storage Temperature Range			-65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	32 LQFP 32 LQFP	80 55	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	std bd	32 LQFP	12 to 17	°C/W
T_{sol}	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

10EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 3)

		-40 °C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Power Supply Current	95	119	143	98	122	146	100	125	150	mA
V_{OH}	Output HIGH Voltage (Note 4)	2165	2290	2415	2230	2355	2480	2290	2415	2540	mV
V_{OL}	Output LOW Voltage (Note 4)	1365	1490	1615	1430	1555	1680	1490	1615	1740	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2090		2415	2155		2480	2215		2540	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1365		1690	1460		1755	1490		1815	mV
V_{BB}	Output Voltage Reference	1790	1890	1990	1855	1955	2055	1915	2015	2115	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.
3. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.
4. All loading with 50 Ω to V_{CC} - 2.0 volts.
5. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 6)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 7)	95	119	143	98	122	146	100	125	150	mA
V_{OH}	Output HIGH Voltage (Note 8)	3865	3990	4115	3930	4055	4180	3990	4115	4240	mV
V_{OL}	Output LOW Voltage (Note 8)	3065	3190	3315	3130	3255	3380	3190	3315	3440	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3790		4115	3855		4180	3915		4240	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3065		3390	3130		3455	3190		3515	mV
V_{BB}	Output Voltage Reference	3490	3590	3690	3555	3655	3755	3615	3715	3815	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 9)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

6. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to -0.5 V.
7. Required 500 lfpm air flow when using +5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at $\leq$ 3.3 V.
8. All loading with 50 Ω to V_{CC}-2.0 volts.
9. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

10EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -5.5 V to -3.0 V (Note 10)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 11)	95	119	143	98	122	146	100	125	150	mA
V_{OH}	Output HIGH Voltage (Note 12)	-1135	-1010	-885	-1070	-945	-820	-1010	-885	-760	mV
V_{OL}	Output LOW Voltage (Note 12)	-1935	-1810	-1685	-1870	-1745	-1620	-1810	-1685	-1560	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1210		-885	-1145		-820	-1085		-760	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1935		-1610	-1870		-1545	-1810		-1485	mV
V_{BB}	Output Voltage Reference	-1510	-1410	-1310	-1445	-1345	-1245	-1385	-1285	-1185	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 13)	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V_{EE}+2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

10. Input and output parameters vary 1:1 with V_{CC}.
11. Required 500 lfpm air flow when using -5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at $\leq$ 3.3 V.
12. All loading with 50 Ω to V_{CC}-2.0 volts.
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL V_{CC} = 3.3 V, V_{EE} = 0 V (Note 14)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current	95	119	143	98	122	146	100	125	150	mA
V_{OH}	Output HIGH Voltage (Note 15)	2155	2280	2405	2155	2280	2405	2155	2280	2405	mV
V_{OL}	Output LOW Voltage (Note 15)	1355	1480	1605	1355	1480	1605	1355	1480	1605	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
V_{IL}	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
V_{BB}	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 16)	2.0		3.3	2.0		3.3	2.0		3.3	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

14. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to -2.2 V.
15. All loading with 50 Ω to V_{CC}-2.0 volts.
16. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, PECL V_{CC} = 5.0 V, V_{EE} = 0 V (Note 17)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 18)	95	119	143	98	122	146	100	125	150	mA
V_{OH}	Output HIGH Voltage (Note 19)	3855	3980	4105	3855	3980	4105	3855	3980	4105	mV
V_{OL}	Output LOW Voltage (Note 19)	3055	3180	3305	3055	3180	3305	3055	3180	3305	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	3775		4120	3775		4120	3775		4120	mV
V_{IL}	Input LOW Voltage (Single-Ended)	3055		3375	3055		3375	3055		3375	mV
V_{BB}	Output Voltage Reference	3475	3575	3675	3475	3575	3675	3475	3575	3675	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 20)	2.0		5.0	2.0		5.0	2.0		5.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

17. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +2.0 V to -0.5 V.
18. Required 500 lfpm air flow when using +5 V power supply. For (V_{CC} - V_{EE}) >3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at $\leq$ 3.3 V.
19. All loading with 50 Ω to V_{CC}-2.0 volts.
20. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

100EP DC CHARACTERISTICS, NECL V_{CC} = 0 V, V_{EE} = -5.5 V to -3.0 V (Note 21)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_{EE}	Power Supply Current (Note 22)	95	119	143	98	122	146	100	125	150	mA
V_{OH}	Output HIGH Voltage (Note 23)	-1145	-1020	-895	-1145	-1020	-895	-1145	-1020	-895	mV
V_{OL}	Output LOW Voltage (Note 23)	-1945	-1820	-1695	-1945	-1820	-1695	-1945	-1820	-1695	mV
V_{IH}	Input HIGH Voltage (Single-Ended)	-1225		-880	-1225		-880	-1225		-880	mV
V_{IL}	Input LOW Voltage (Single-Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
V_{BB}	Output Voltage Reference	-1525	-1425	-1325	-1525	-1425	-1325	-1525	-1425	-1325	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential) (Note 24)	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V_{EE} + 2.0		0.0	V
I_{IH}	Input HIGH Current			150			150			150	μA
I_{IL}	Input LOW Current	0.5			0.5			0.5			μA

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

21. Input and output parameters vary 1:1 with V_{CC}.
22. Required 500 lfpm air flow when using -5 V power supply. For (V_{CC} - V_{EE}) > 3.3 V, 5 Ω to 10 Ω in line with V_{EE} required for maximum thermal protection at elevated temperatures. Recommend V_{CC}-V_{EE} operation at ≤ 3.3 V.
23. All loading with 50 Ω to V_{CC} - 2.0 volts.
24. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

AC CHARACTERISTICS V_{CC} = 0 V; V_{EE} = -3.0 V to -5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 25)

Symbol	Characteristic	-40 °C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input CLK Frequency CKSEL = LOW (See Figure 12. F_{max}/JITTER) CKSEL = HIGH	2.0 2.8	2.5 3.3		2.0 2.8	2.5 3.3		1.7 2.8	2.2 3.3		GHz
t_{PLH}, t_{PHL}	Propagation Delay to CLK to Q Output Differential CLK TO PCLK	1230 1000	1450 1240	1660 1490	1300 1050	1530 1310	1760 1580	1400 1140	1650 1420	1900 1710	ps
ts	Setup Time SINA, B+ TO CLK+ (Figure 4) $\overline{CKEN}$+ TO CLK- (Figure 5)	-300 100	-400 50		-300 100	-400 50		-300 100	-400 50		ps
t_h	Hold Time CLK+ TO SINA, B- (Figure 4) CLK- TO $\overline{CKEN}$ (Figure 5)	650 45	550 -35		675 45	575 -35		725 45	625 -35		ps
t_{RR}/t_{RR2}	Reset Recovery (Figure 3)	350	180		350	180		350	180		ps
t_{PW}	Minimum Pulse Width RESET	400			400			400			ps
t_{JITTER}	Cycle-to-Cycle Jitter PCLK (See Figure 12. F_{max}/JITTER)		0.2	< 1		0.2	< 1		0.2	< 1	ps
V_{PP}	Input Voltage Swing (Differential) (Note 26)	150	800	1200	150	800	1200	150	800	1200	mV
t_r t_f	Output Rise/Fall Times Q (20% - 80%)	100	180	250	100	200	300	125	230	325	ps

25. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} - 2.0 V.
26. V_{PP}(min) is the minimum input swing for which AC parameters are guaranteed.

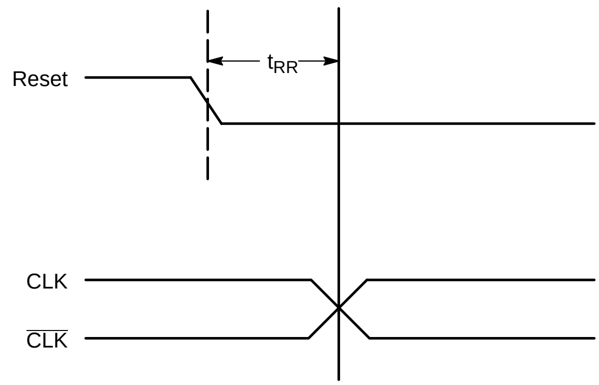


Figure 3. Reset Recovery

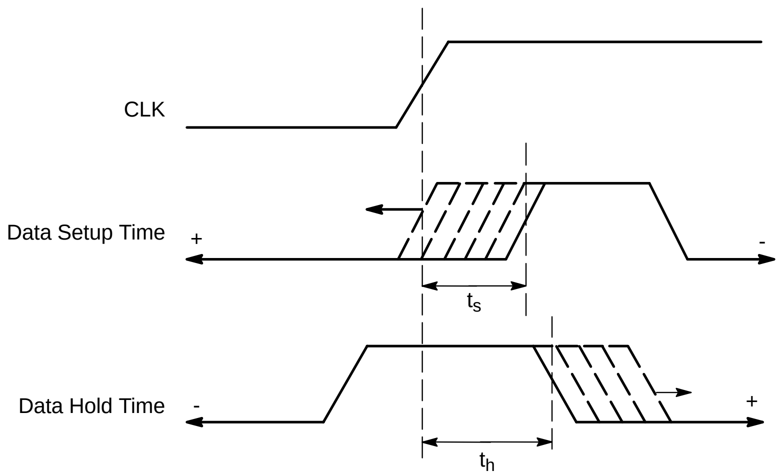


Figure 4. Data Setup and Hold Time

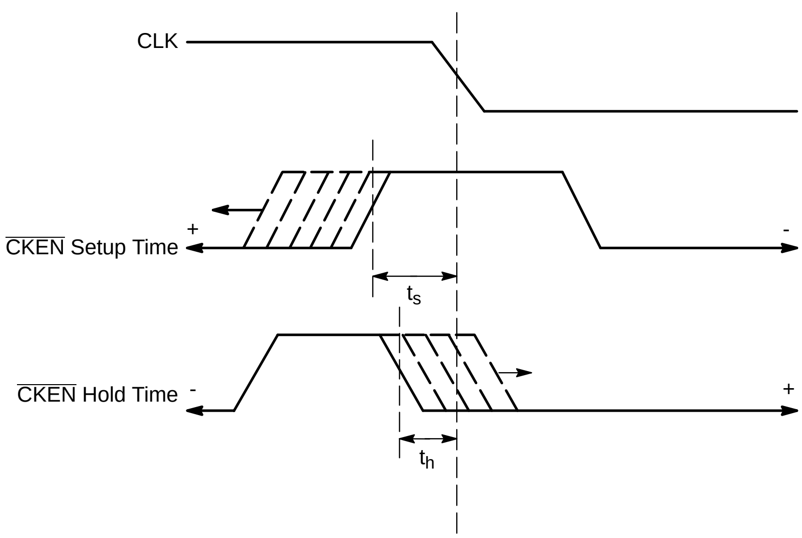


Figure 5. CKEN Setup and Hold Time

APPLICATION INFORMATION

The MC10/100EP445 is an integrated 1:8 serial to parallel converter with two modes of operation selected by CKSEL (Pin 7). CKSEL HIGH mode only latches data on the rising edge of the input CLK and CKSEL LOW mode latches data on both the rising and falling edge of the input CLK. CKSEL LOW is the open default state. Either of the two differential input serial data path provided for this device, SINA and SINB, can be chosen with the SINSEL pin (pin 25). SINA is the default input path when SINSEL pin is left floating. Because of internal pull-downs on the input pins, all input pins will default to logic low when left open. The two selectable serial data paths can be used for loop-back testing as well as the bit error testing.

Upon power-up, the internal flip-flops will attain a random state. To synchronize multiple flip–flops in the device, the Reset (pin 1) must be asserted. The reset pin will disable the internal clock signal irrespective of the CKEN state (CKEN disables the internal clock circuitry). The device will grab the first stream of data after the falling edge of RESET①, followed by the falling edge of CLK②, on second rising edge of CLK③ in either CKSEL modes. (See Figure 6)

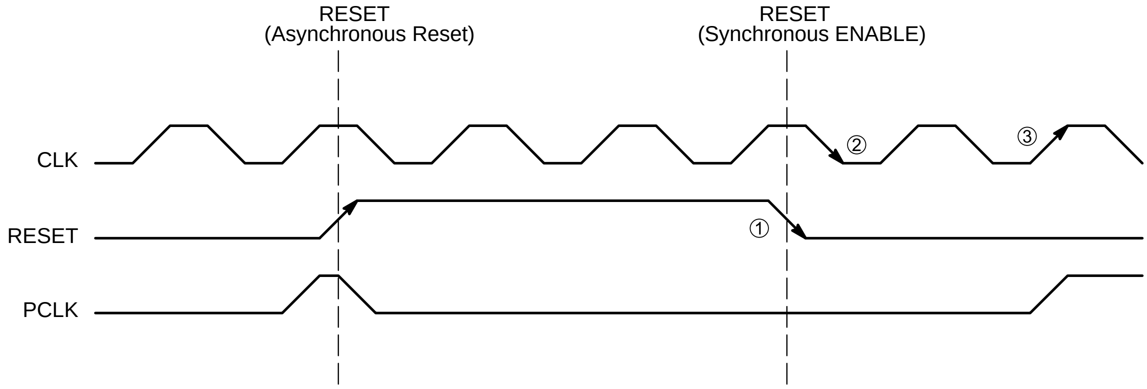


Figure 6. Reset Timing Diagram

For CKSEL LOW operation, the data is latched on both the rising edge and the falling edge of the clock and the time from when the serial data is latched① to when the data is seen on the parallel output② is 6 clock cycles (see Figure 7).

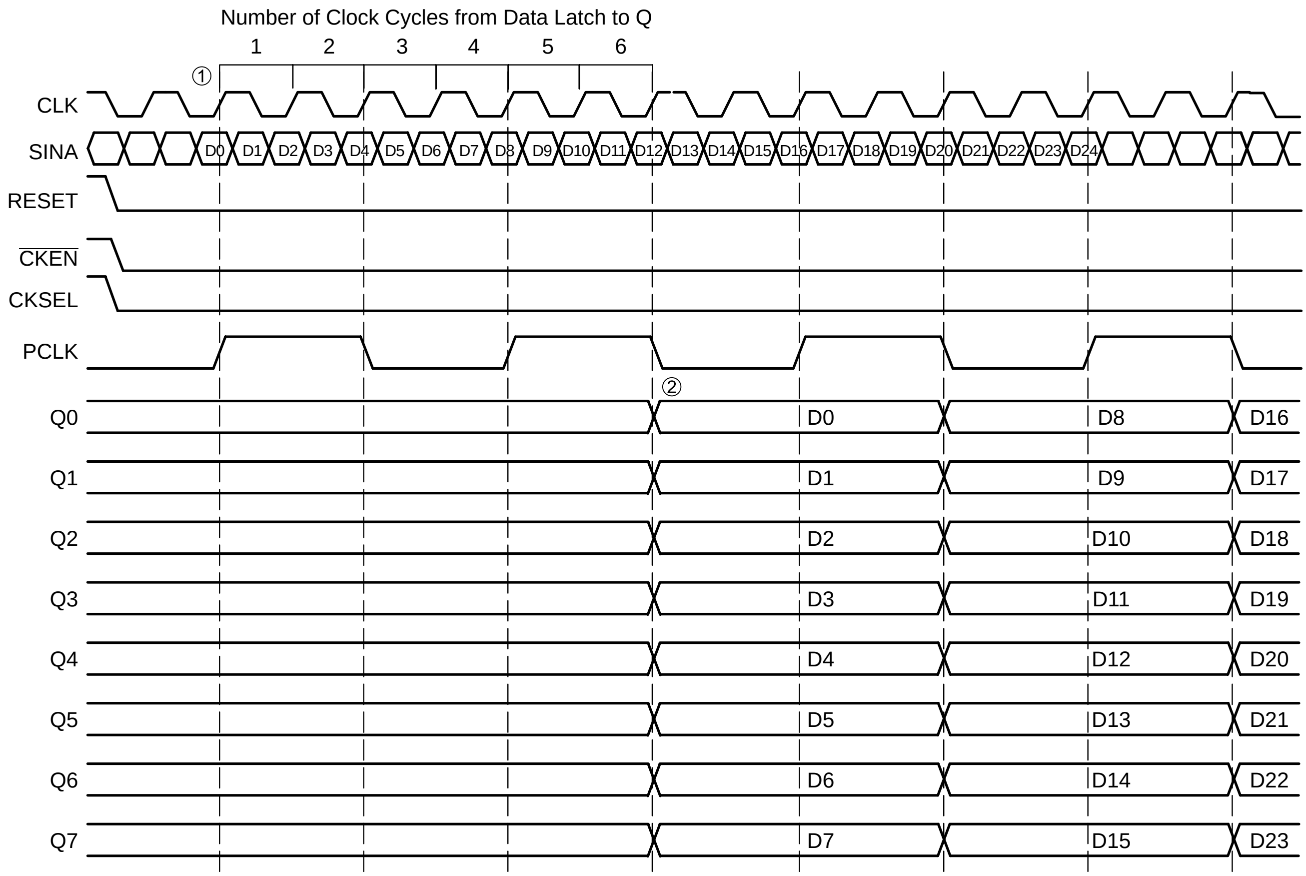


Figure 7. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL LOW

Similarly, for CKSEL HIGH operation, the data is latched only on the rising edge of the clock and the time from when the serial data is latched① to when the data is seen on the parallel output② is 12 clock cycles (see Figure 8).

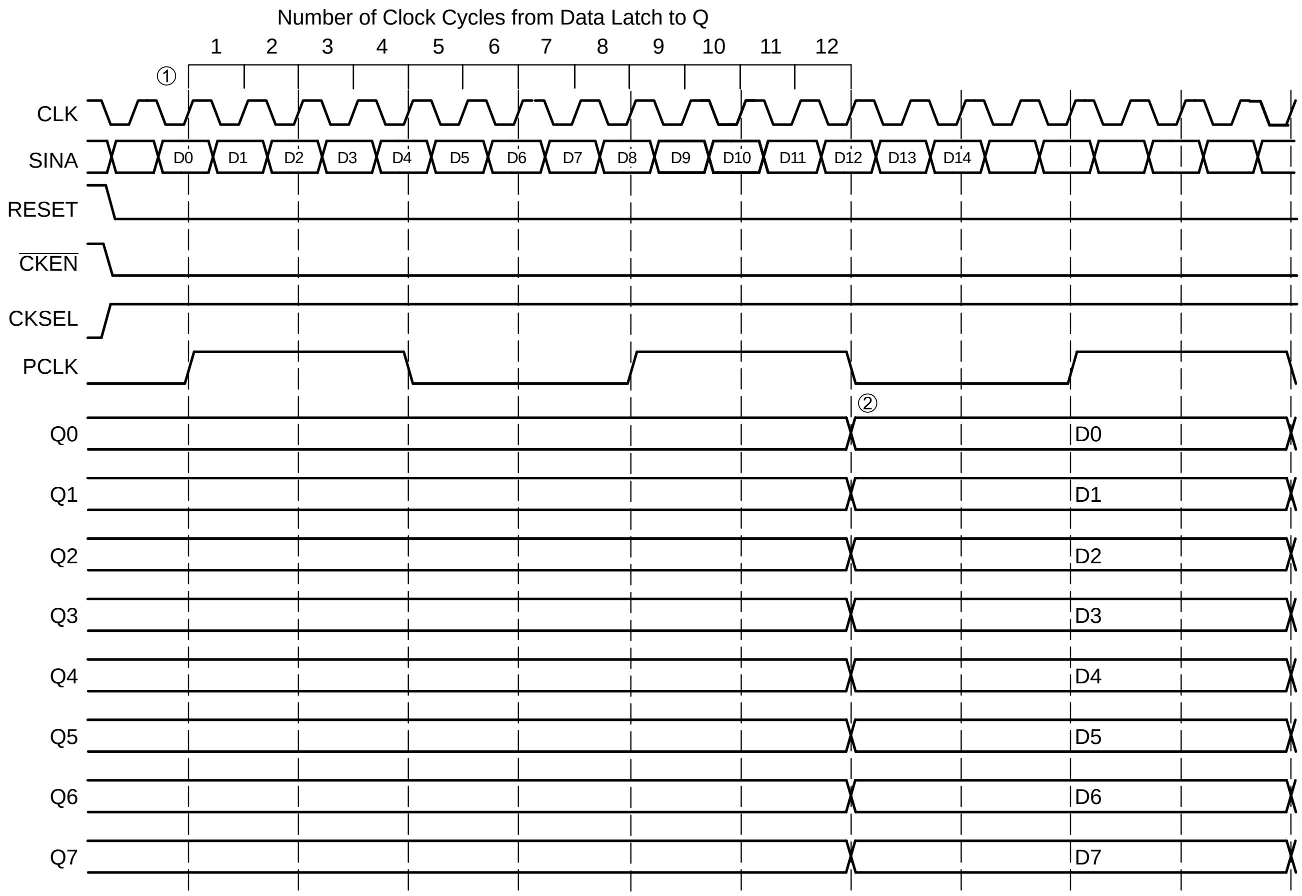


Figure 8. Timing Diagram A. 1:8 Serial to Parallel Conversion with CKSEL HIGH

To allow the user to synchronize the output byte data correctly, the start bit for conversion can be moved using the SYNC input pin (pin 2). Asynchronously asserting the SYNC pin will force the internal clock to swallow a clock pulse, effectively shifting a bit from the Q_n to the Q_{n-1} output as shown in Figure 9 and Figure 10. For CKSEL LOW, a single pulse applied asynchronously for two consecutive clock cycles shifts the start bit for conversion from Q_n to Q_{n-1}. The bit is swallowed following the two clock cycle pulse width of SYNC① on the next triggering edge of clock② (either on the rising or the falling edge of the clock). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 9)

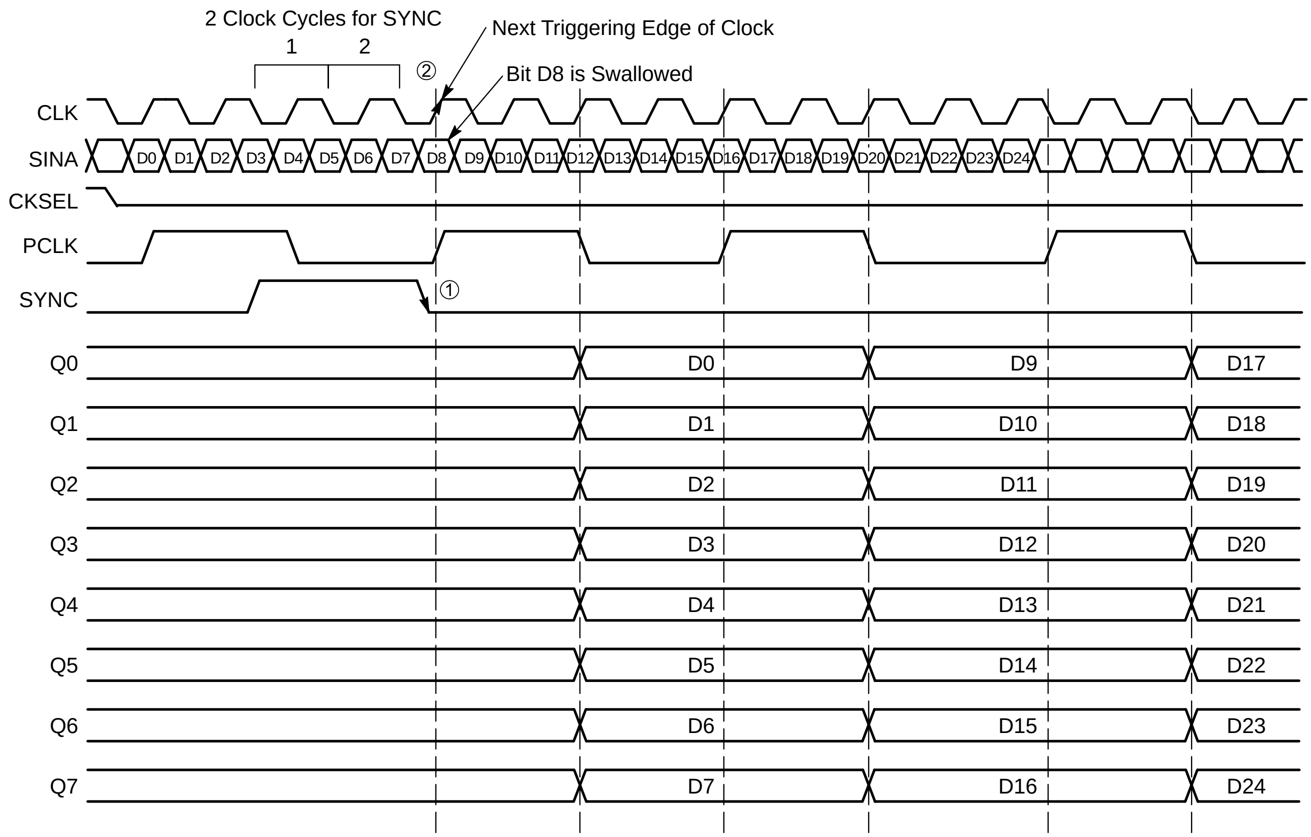


Figure 9. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL LOW

For CKSEL HIGH, a single pulse applied asynchronously for three consecutive clock cycles shifts the start bit for conversion from Q_n to Q_{n-1}. The bit is swallowed following the three clock cycle pulse width of SYNC① on the next triggering edge of clock② (on the rising edge of the clock only). Each additional shift requires an additional pulse to be applied to the SYNC pin. (See Figure 10)

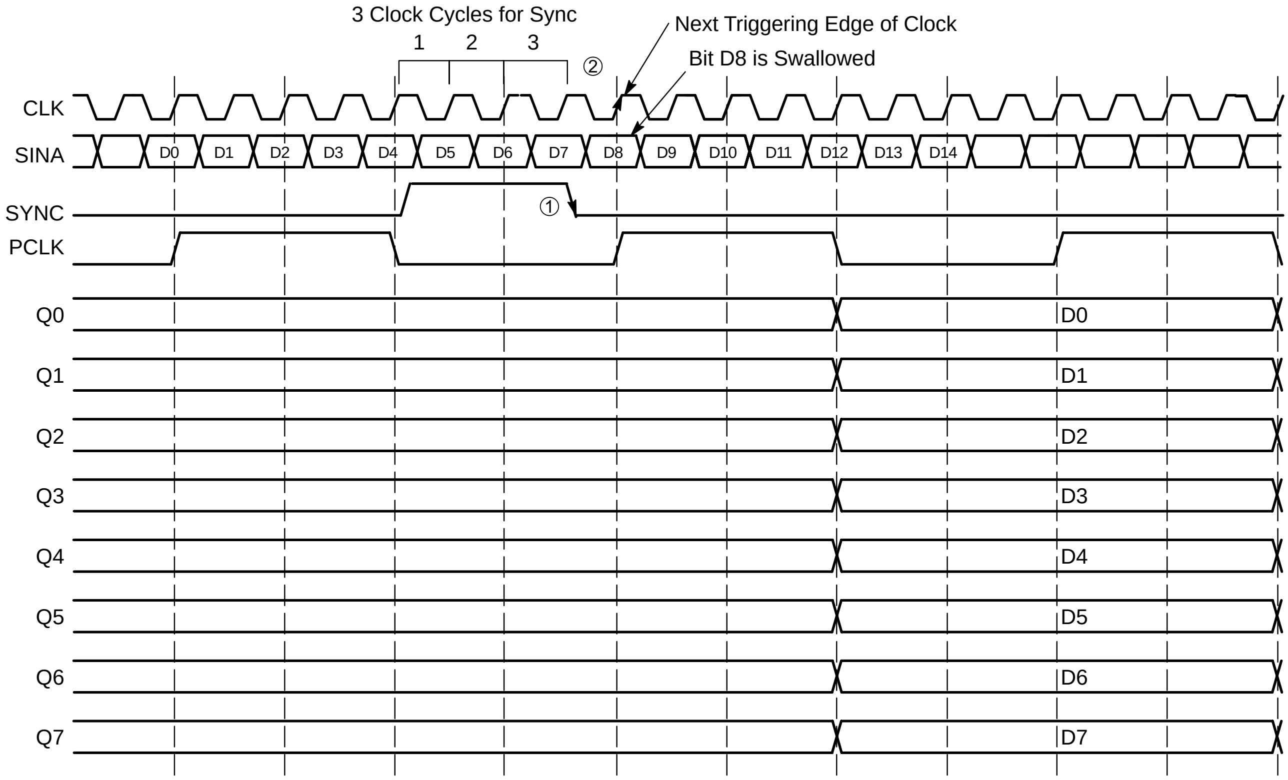


Figure 10. Timing Diagram A. 1:8 Serial to Parallel Conversion with SYNC Pulse at CKSEL HIGH

The synchronous $\overline{CKEN}$ (pin 3) applied with at least one clock cycle pulse length will disable the internal clock signal. The synchronous $\overline{CKEN}$ will suspend all of the device activities and prevent runt pulses from being generated. The rising edge of $\overline{CKEN}$ followed by the falling edge of CLK will suspend all activities. The first data bit will clock on the rising edge, since the falling edge of $\overline{CKEN}$ followed by the falling edge of the incoming clock triggers the enabling of the internal process. (See Figure 11)

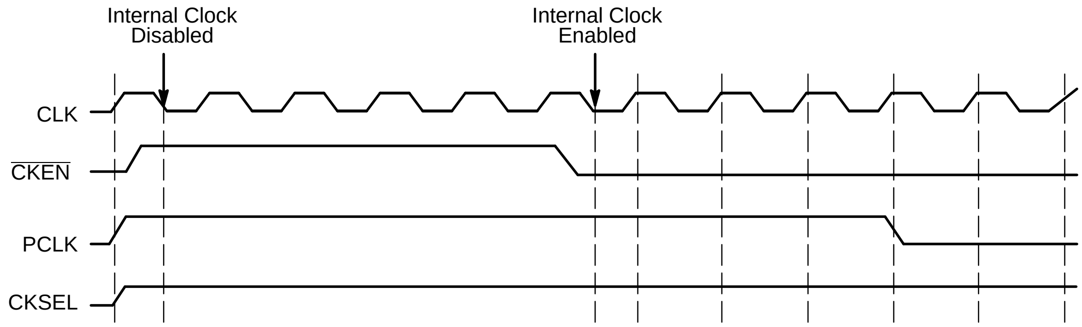


Figure 11. Timing Diagram with CKEN with CKSEL HIGH

The differential PCLK output (pins 22 and 23) is a word framer and can help the user to synchronize the parallel data outputs. During CKSEL LOW operation, the PCLK will provide a divide by 4-clock frequency, which frames the serial data in period of PCLK output. Likewise during CKSEL HIGH operation, the PCLK will provide a divide by 8-clock frequency.

The V_{BB} pin, an internally generated voltage supply, is available to this device only. For single–ended input conditions, the unused differential input is connected to VBB as a switching reference voltage. V_{BB} may also rebias AC coupled inputs. When used, decouple V_{BB} and V_{CC} via a 0.01 μF capacitor, which will limit the current sourcing or sinking to 0.5mA. When not used, V_{BB} should be left open. Also, both outputs of the differential pair must be terminated (50 Ω to $V_{TT} = V_{CC} – 2$ V) even if only one output is used.

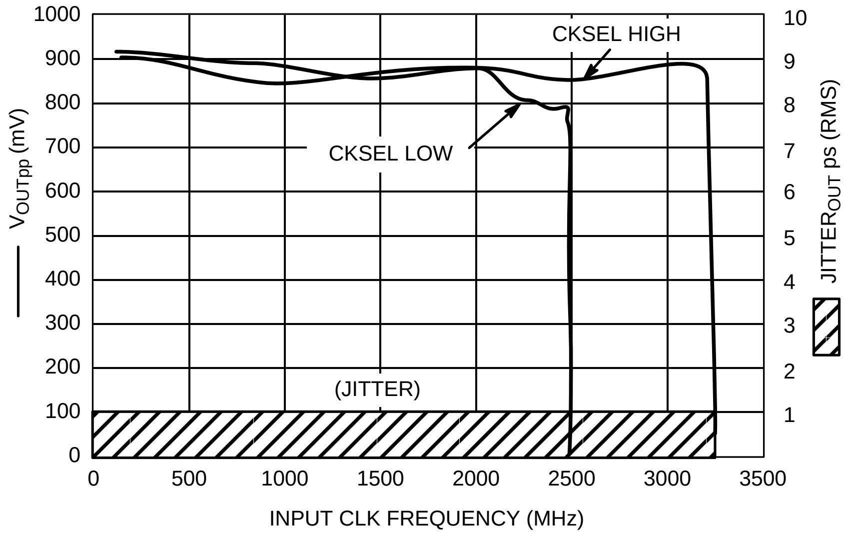


Figure 12. F_{max}/Jitter

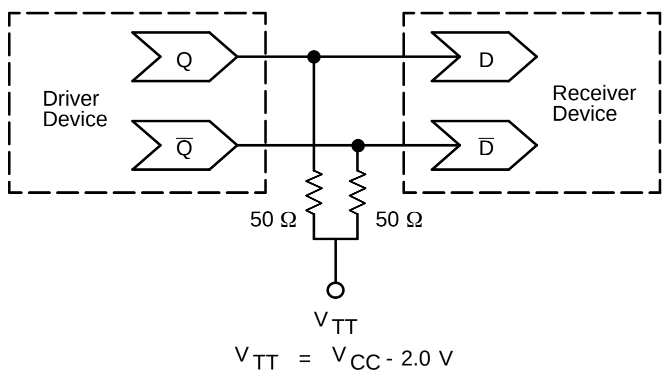


Figure 13. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020 - Termination of ECL Logic Devices.)

Resource Reference of Application Notes

AN1404 - ECLinPS Circuit Performance at Non-Standard V_{IH} Levels

AN1405 - ECL Clock Distribution Techniques

AN1406 - Designing with PECL (ECL at +5.0 V)

AN1504 - Metastability and the ECLinPS Family

AN1568 - Interfacing Between LVDS and ECL

AN1650 - Using Wire-OR Ties in ECLinPS Designs

AN1672 - The ECL Translator Guide

AND8001 - Odd Number Counters Design

AND8002 - Marking and Date Codes

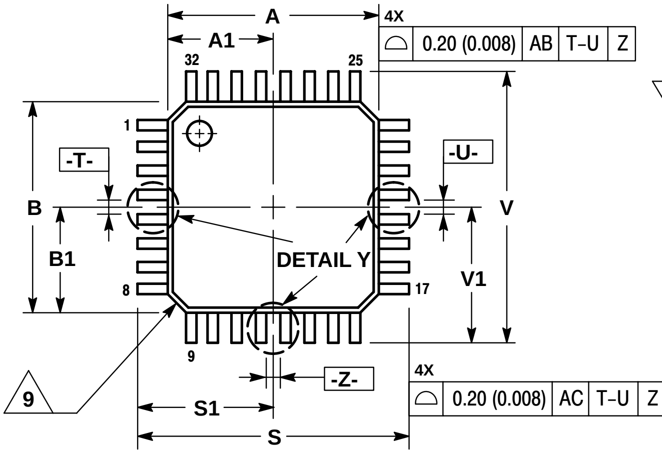
AND8009 - ECLinPS Plus Spice I/O Model Kit

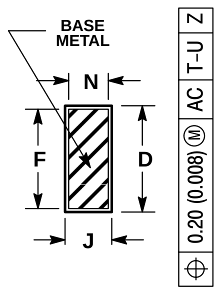
AND8020 - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at http://onsemi.com.

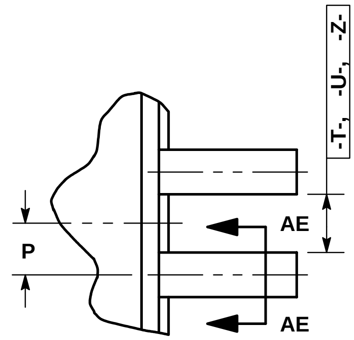
PACKAGE DIMENSIONS

LQFP
FA SUFFIX
32-LEAD PLASTIC PACKAGE
CASE 873A-02
ISSUE A

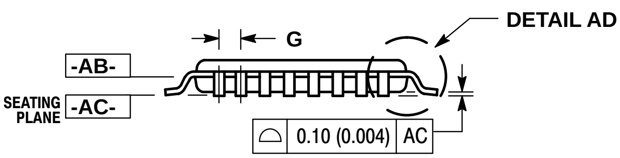


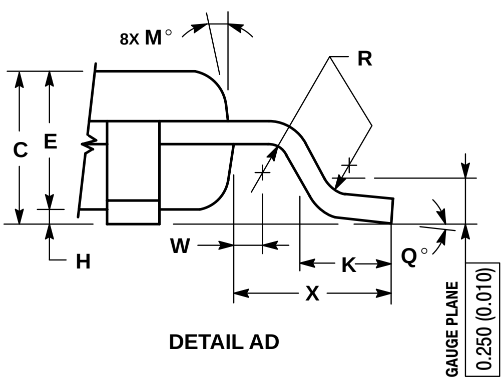


SECTION AE-AE



DETAIL Y





DETAIL AD

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE –AB– IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS –T–, –U–, AND –Z– TO BE DETERMINED AT DATUM PLANE –AB–.
5. DIMENSIONS S AND V TO BE DETERMINED AT SEATING PLANE –AC–.
6. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 (0.010) PER SIDE. DIMENSIONS A AND B DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE –AB–.
7. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE D DIMENSION TO EXCEED 0.520 (0.020).
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076 (0.0003).
9. EXACT SHAPE OF EACH CORNER MAY VARY FROM DEPICTION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	7.000 BSC		0.276 BSC	
A1	3.500 BSC		0.138 BSC	
B	7.000 BSC		0.276 BSC	
B1	3.500 BSC		0.138 BSC	
C	1.400	1.600	0.055	0.063
D	0.300	0.450	0.012	0.018
E	1.350	1.450	0.053	0.057
F	0.300	0.400	0.012	0.016
G	0.800 BSC		0.031 BSC	
H	0.050	0.150	0.002	0.006
J	0.090	0.200	0.004	0.008
K	0.500	0.700	0.020	0.028
M	12° REF		12° REF	
N	0.090	0.160	0.004	0.006
P	0.400 BSC		0.016 BSC	
Q	1°	5°	1°	5°
R	0.150	0.250	0.006	0.010
S	9.000 BSC		0.354 BSC	
S1	4.500 BSC		0.177 BSC	
V	9.000 BSC		0.354 BSC	
V1	4.500 BSC		0.177 BSC	
W	0.200 REF		0.008 REF	
X	1.000 REF		0.039 REF	

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