NBSG14

2.5V/3.3V SiGe Differential 1:4 Clock/Data Driver with RSECL* Outputs

*Reduced Swing ECL

The NBSG14 is a 1−to−4 clock/data distribution chip, optimized for ultra−low skew and jitter.

Inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVTTL, LVCMOS, CML, or LVDS. Outputs are RSECL (Reduced Swing ECL), 400 mV.

- Maximum Input Clock Frequency up to 12 GHz Typical
- Maximum Input Data Rate up to 12 Gb/s Typical
- 30 ps Typical Rise and Fall Times
- 125 ps Typical Propagation Delay
- RSPECL Output with Operating Range: V_{CC} = 2.375 V to 3.465 V with V_{EE} = 0 V
- RSNECL Output with RSNECL or NECL Inputs with Operating Range: V_{CC} = 0 V with V_{EE} = −2.375 V to −3.465 V
- RSECL Output Level (400 mV Peak−to−Peak Output), Differential Output
- 50 Ω Internal Input Termination Resistors
- Compatible with Existing 2.5 V/3.3 V LVEP, EP, and LVEL Devices

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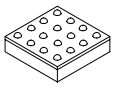
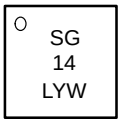
MARKING DIAGRAM*



FCBGA−16
BA SUFFIX
CASE 489



QFN−16
MN SUFFIX
CASE 485G

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

*For further details, refer to Application Note AND8002/D

ORDERING INFORMATION

Device	Package	Shipping
NBSG14BA	4x4 mm FCBGA−16	100 Units/Tray
NBSG14BAR2	4x4 mm FCBGA−16	500 / Tape & Reel
NBSG14MN	3x3 mm QFN−16	123 Units / Rail
NBSG14MNR2	3x3 mm QFN−16	3000 / Tape & Reel

Board	Description
NBSG14BAEVB	NBSG14BA Evaluation Board

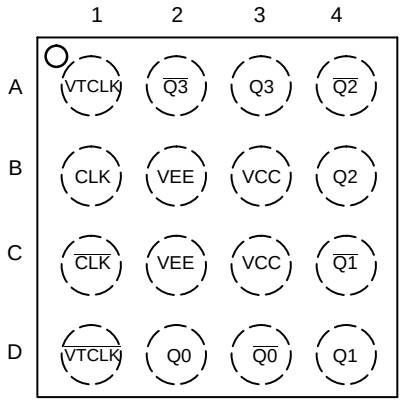


Figure 1. BGA−16 Pinout (Top View)

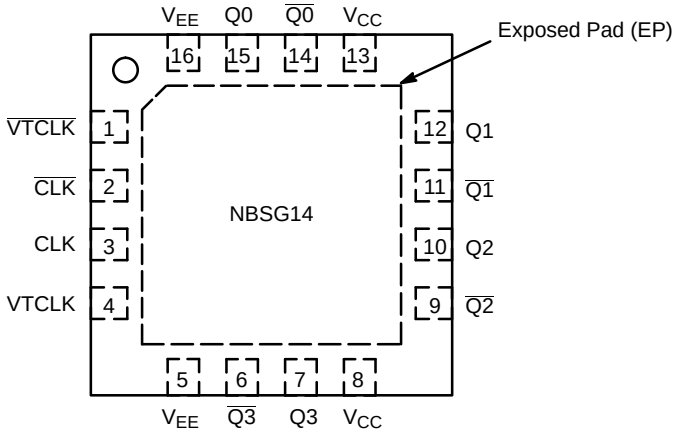


Figure 2. QFN−16 Pinout (Top View)

Table 1. Pin Description

Pin				
BGA	**QFN**	**Name**	**I/O**	**Description**
D1	1	$\overline{\text{VTCLK}}$	−	Internal 50 Ω Termination pin. See Table 2.
C1	2	$\overline{\text{CLK}}$	ECL, CML, LVCMOS, LVDS, LVTTL Input	Inverted Differential Input. Internal 75 kΩ to V_{EE} and 36.5 kΩ to V_{CC}.
B1	3	CLK	ECL, CML, LVCMOS, LVDS, LVTTL Input	Noninverted Differential Input. Internal 75 kΩ to VEE.
A1	4	VTCLK	−	Internal 50 Ω Termination Pin. See Table 2.
B2,C2	5,16	V_{EE}	−	Negative Supply Voltage. All V_{EE} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
A2*	6	$\overline{\text{Q3}}$	RSECL Output	Inverted Differential Output 3. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
A3*	7	Q3	RSECL Output	Noninverted Differential Output 3. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
B3,C3	8,13	V_{CC}	−	Positive Supply Voltage. All V_{CC} Pins must be Externally Connected to Power Supply to Guarantee Proper Operation.
A4*	9	$\overline{\text{Q2}}$	RSECL Output	Inverted Differential Output 2. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
B4*	10	Q2	RSECL Output	Noninverted Differential Output 2. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
C4*	11	$\overline{\text{Q1}}$	RSECL Output	Inverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
D4*	12	Q1	RSECL Output	Noninverted Differential Output 1. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
D3*	14	$\overline{\text{Q0}}$	RSECL Output	Inverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
D2*	15	Q0	RSECL Output	Noninverted Differential Output 0. Typically Terminated with 50 Ω to $V_{TT} = V_{CC} - 2$ V*
N/A	−	EP	−	Exposed Pad. The thermally exposed pad on package bottom (see case drawing) must be attached to a heat−sinking conduit.

1. In the differential configuration when the input termination pins (VTCLK, $\overline{\text{VTCLK}}$) are connected to a common termination voltage, if no signal is applied then the device will be susceptible to self−oscillation.

*Devices in BGA package typically terminated with 50 Ω to $V_{TT} = V_{CC}$−1.5 V.

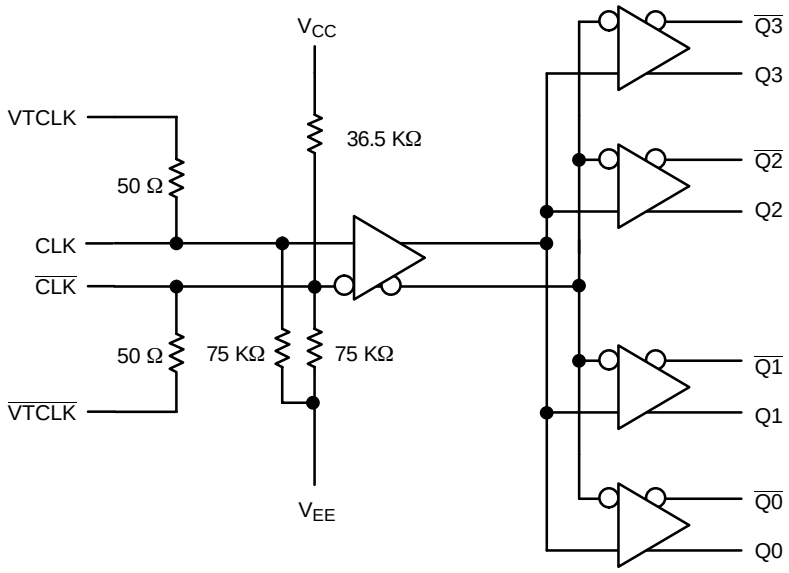


Figure 3. Logic Diagram

Table 2. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTCLK and $\overline{\text{VTCLK}}$ to V_{CC}
LVDS	Connect VTCLK and $\overline{\text{VTCLK}}$ Together
AC−COUPLED	Bias VTCLK and $\overline{\text{VTCLK}}$ Inputs within Common Mode Range (V_{IHCMR})
RSECL, PECL, NECL	Standard ECL Termination Techniques
LVTTL, LVCMOS	An External Voltage (V_{THR}) should be Applied to the Unused Differential Input. Nominal V_{THR} is 1.5 V for LVTTL and V_{CC}/2 for LVCMOS Inputs. This Voltage must be within the V_{THR} Specification.

Table 3. ATTRIBUTES

Characteristics		Value
Internal Input Pulldown Resistor (CLK, $\overline{CLK}$)		75 kΩ
Internal Input Pullup Resistor ($\overline{CLK}$)		36.5 kΩ
ESD Protection	Human Body Model Machine Model	> 2 kV > 100 V
Moisture Sensitivity (Note 1)	FCBGA−16 QFN−16	Level 3 Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count		158
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{CC}	Positive Power Supply	V_{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V_{CC} = 0 V		−3.6	V
V_I	Positive Input Negative Input	V_{EE} = 0 V V_{CC} = 0 V	$V_I \le V_{CC}$ $V_I \ge V_{EE}$	3.6 −3.6	V V
V_{INPP}	Differential Input Voltage |CLK−$\overline{CLK}$|	$V_{CC} - V_{EE} \ge 2.8$ V $V_{CC} - V_{EE} < 2.8$ V		2.8 $\|V_{CC}-V_{EE}\|$	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		45 80	mA mA
I_{OUT}	Output Current	Continuous Surge		25 50	mA mA
T_A	Operating Temperature Range	16 FCBGA 16 QFN		−40 to +70 −40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction−to−Ambient) (Note 3)	0 LFPM 500 LFPM 0 LFPM 500 LFPM	16 FCBGA 16 FCBGA 16 QFN 16 QFN	108 86 41.6 35.2	°C/W °C/W °C/W °C/W
θ_{JC}	Thermal Resistance (Junction−to−Case)	2S2P (Note 3) 2S2P (Note 4)	16 FCBGA 16 QFN	5 4.0	°C/W °C/W
T_{sol}	Wave Solder	< 15 Seconds		225	°C

2. Maximum Ratings are those values beyond which device damage may occur.
3. JEDEC standard 51−6, multilayer board − 2S2P (2 signal, 2 power).
4. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

Table 5. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 2.5 V; V_{EE} = 0 V (Note 5)

		−40°C			25°C			70°C(BGA)/85°C(QFN)**			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 6)	1525	1575	1625	1550	1610	1650	1575	1635	1675	mV
V_{OUTPP}	Output Amplitude Voltage	315	405	495	315	405	495	315	405	495	mV
V_{IH}	Input HIGH Voltage (Single−Ended) (Notes 8 and 10)	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Notes 9 and 10)	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	mV
V_{THR}	Input Threshold Voltage (Single−Ended) (Note 10)	V_{EE} + 1125		V_{CC}− 75	V_{EE} + 1125		V_{CC}− 75	V_{EE} + 1125		V_{CC}− 75	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 7)	1.2		2.5	1.2		2.5	1.2		2.5	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

5. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.125 V to −0.5 V.
6. All outputs loaded with 50 Ω to V_{CC} − 1.5 V for BGA package and V_{CC} − 2 V for QFN package. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).
7. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
8. V_{IH} cannot exceed V_{CC}. $|V_{IH} - V_{THR}| < 2600$ mV.
9. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600$ mV.
10. V_{THR} is the voltage applied to one input when running in single−ended mode.

*Typicals used for testing purposes.

**The device packaged in FCBGA−16 have maximum temperature specification of 70°C and devices packaged in QFN−16 have maximum temperature specification of 85°C.

Table 6. DC CHARACTERISTICS, INPUT WITH RSPECL OUTPUT V_{CC} = 3.3 V; V_{EE} = 0 V (Note 11)

		−40°C			25°C			70°C(BGA)/85°C(QFN)**			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
V_{OH}	Output HIGH Voltage (Note 12)	2325	2375	2425	2350	2410	2450	2375	2435	2475	mV
V_{OUTPP}	Output Amplitude Voltage	350	440	530	350	440	530	350	440	530	mV
V_{IH}	Input HIGH Voltage (Single−Ended) (Notes 14 and 16)	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Notes 15 and 16)	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	mV
V_{THR}	Input Threshold Voltage (Single−Ended) (Note 16)	V_{EE} + 1125		V_{CC}− 75	V_{EE} + 1125		V_{CC}− 75	V_{EE} + 1125		V_{CC}− 75	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13)	1.2		3.3	1.2		3.3	1.2		3.3	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe Circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lfpm is maintained.

11. Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.3 V to −0.165 V.
12. All outputs loaded with 50 Ω to V_{CC} − 1.5 V for BGA package and V_{CC} − 2 V for QFN package. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).
13. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
14. V_{IH} cannot exceed V_{CC}. $|V_{IH} - V_{THR}| < 2600$ mV.
15. V_{IL} always $\geq V_{EE}$. $|V_{IL} - V_{THR}| < 2600$ mV.
16. V_{THR} is the voltage applied to one input when running in single−ended mode.

*Typicals used for testing purposes.

**The device packaged in FCBGA−16 have maximum temperature specification of 70°C and devices packaged in QFN−16 have maximum temperature specification of 85°C.

Table 7. DC CHARACTERISTICS, NECL OR RSNECL INPUT WITH NECL OUTPUT

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V (Note 17)

		−40°C			25°C			70°C(BGA)/85°C(QFN)**			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
I_{EE}	Negative Power Supply Current	45	60	75	45	60	75	45	60	75	mA
VOH	Output HIGH Voltage (Note 18)	−975	−925	−875	−950	−890	−850	−925	−865	−825	mV
V_{OUTPP}	Output Amplitude Voltage −3.465 V ≤ V_{EE} ≤ −3.0 V −3.0 V < V_{EE} ≤ −2.375 V	 350 315	 440 405	 530 495	 350 315	 440 405	 530 495	 350 315	 440 405	 530 495	mV
V_{IH}	Input HIGH Voltage (Single−Ended) (Notes 20 and 22)	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	V_{CC}− 1435	V_{CC}− 1000*	V_{CC}	mV
V_{IL}	Input LOW Voltage (Single−Ended) (Notes 21 and 22)	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	V_{IH}− 2500	V_{CC}− 1400*	V_{IH}− 150	mV
V_{THR}	Input Threshold Voltage (Single−Ended) (Note 22)	V_{EE} + 1125		V_{CC}− 75	V_{EE} + 1125		V_{CC}− 75	V_{EE} + 1125		V_{CC}− 75	mV
V_{IHCMR}	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 19)	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V_{EE} + 1.2		0.0	V
R_{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
I_{IH}	Input HIGH Current (@ V_{IH})		80	150		80	150		80	150	μA
I_{IL}	Input LOW Current (@ V_{IL})		25	100		25	100		25	100	μA

NOTE: SiGe circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained.

17. Input and output parameters vary 1:1 with V_{CC}.
18. All outputs loaded with 50 Ω to V_{CC} −1.5 V for BGA package and V_{CC} − 2 V for QFN package. V_{OH}/V_{OL} measured at V_{IH}/V_{IL} (Typical).
19. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal.
20. V_{IH} cannot exceed V_{CC}. $|V_{IH} - V_{THR}| < 2600$ mV.
21. V_{IL} always ≥ V_{EE}. $|V_{IL} - V_{THR}| < 2600$ mV.
22. V_{THR} is the voltage applied to one input when running in single−ended mode.

*Typicals used for testing purposes.

**The device packaged in FCBGA−16 have maximum temperature specification of 70°C and devices packaged in QFN−16 have maximum temperature specification of 85°C.

Table 8. AC CHARACTERISTICS for FCBGA−16

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		−40°C			25°C			70°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 4) (Note 23)	10.7	12		10.7	12		10.7	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	100	125	150	100	125	150	100	125	150	ps
t_{SKEW}	Duty Cycle Skew (Note 24) Within−Device Skew (Note 25) Device−to−Device Skew (Note 26)		2 6 25	10 15 50		2 6 25	10 15 50		2 6 25	10 15 50	ps
t_{JITTER}	RMS Random Clock Jitter (Figure 4) (Note 28) f_{in} < 10 GHz Peak−to−Peak Data Dependent Jitter (Note 29) f_{in} < 10 Gb/s		0.2	1		0.2 10	1		0.2	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 27)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%) @ 1 GHz	20	30	55	20	30	55	20	30	55	ps

23. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to V_{CC} − 1.5 V. Input edge rates 40 ps (20% − 80%).
24. See Figure 6. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.
25. Within−Device skew is measured between outputs under identical transitions and conditions on any one device.
26. Device−to−device skew for identical transitions at identical V_{CC} levels.
27. V_{INPP} (MAX) cannot exceed V_{CC} − V_{EE} (applicable only when V_{CC}−V_{EE} < 2600 mV).
28. Additive RMS Jitter with 50% duty cycle clock signal at 10 GHz.
29. Additive Peak−to−Peak data dependent jitter with NRZ PRBS 2^{31}−1 data at 10 Gb/s.

Table 9. AC CHARACTERISTICS for QFN−16

V_{CC} = 0 V; V_{EE} = −3.465 V to −2.375 V or V_{CC} = 2.375 V to 3.465 V; V_{EE} = 0 V

		−40°C			25°C			85°C			
Symbol	**Characteristic**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
f_{max}	Maximum Frequency (See Figure 4) (Note 30)	10.5	12		10.5	12		10.5	12		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential	90	125	160	90	125	160	90	125	160	ps
t_{SKEW}	Duty Cycle Skew (Note 31) Within−Device Skew (Note 32) Device−to−Device Skew (Note 33)		3 6 25	15 15 50		3 6 25	15 15 50		3 6 25	15 15 50	ps
t_{JITTER}	RMS Random Clock Jitter (Figure 4) (Note 35) f_{in} < 10 GHz Peak−to−Peak Data Dependent Jitter (Note 36) f_{in} < 10 Gb/s		0.2	1		0.2 10	1		0.2	1	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 34)	75		2600	75		2600	75		2600	mV
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%) @ 1 GHz	15	30	55	20	30	55	20	30	55	ps

30. Measured using a 500 mV source, 50% duty cycle clock source. All outputs loaded with 50 Ω to V_{CC} − 2.0 V. Input edge rates 40 ps (20% − 80%)
31. See Figure 6. $t_{SKEW} = |t_{PLH} - t_{PHL}|$ for a nominal 50% Differential Clock Input Waveform.
32. Within−Device skew is measured between outputs under identical transitions and conditions on any one device.
33. Device−to−device skew for identical transitions at identical V_{CC} levels.
34. V_{INPP} (MAX) cannot exceed $V_{CC} - V_{EE}$ (applicable only when $V_{CC}-V_{EE}$ < 2600 mV).
35. Additive RMS Jitter with 50% duty cycle clock signal at 10 GHz.
36. Additive Peak−to−Peak data dependent jitter with NRZ PRBS $2^{31}-1$ data at 10 Gb/s.

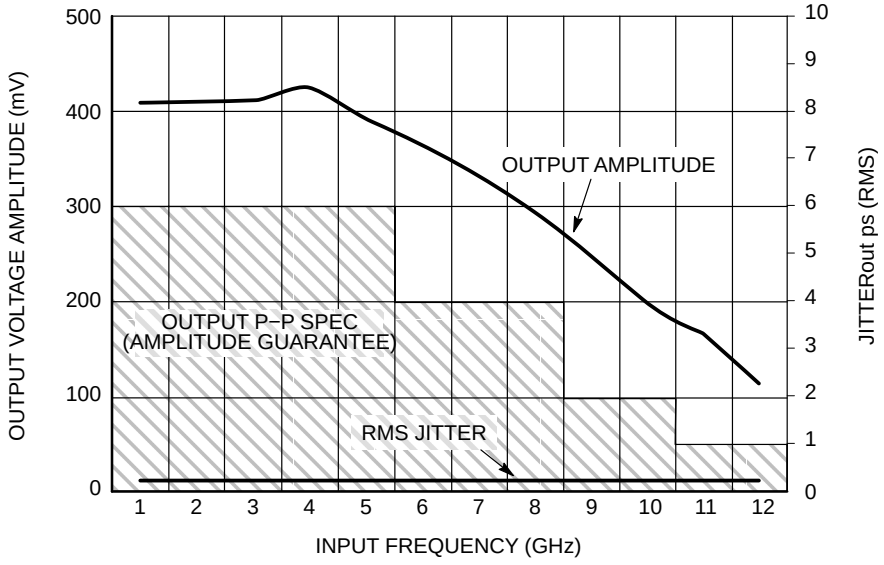
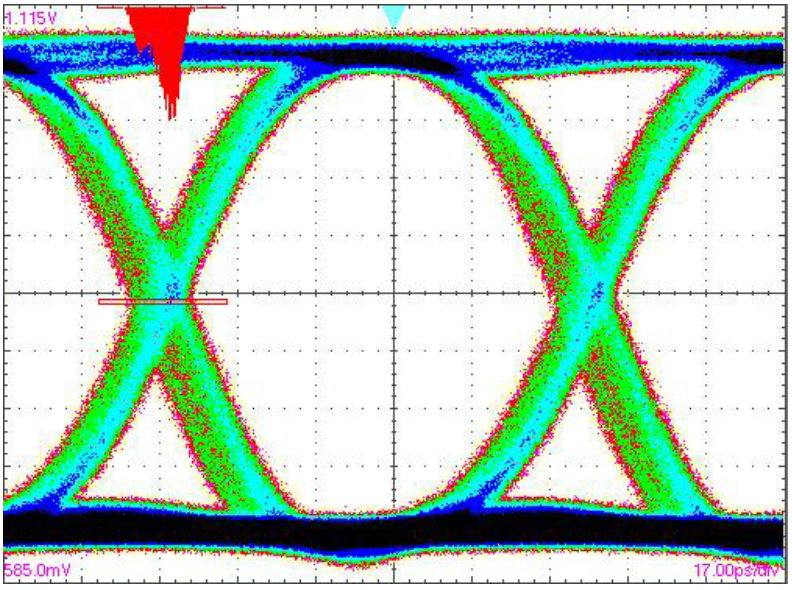


Figure 4. Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) at Ambient Temperature (Typical)



X = 17 ps/DIV, Y = 53 mV/DIV

Figure 5. Eye Diagram at 10.8 Gbps
(V_{CC} − V_{EE} = 3.3 V @ 25°C with Input Data Pattern of 2^31−1 PRBS.
Total Pk−Pk System Jitter Including Signal Generator is 18 ps.
This Data was taken by Acquiring 7000 Waveforms.)

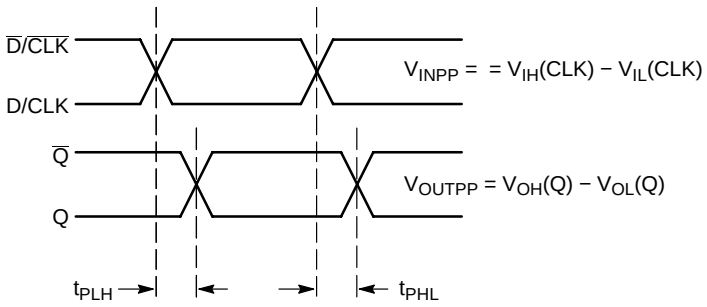
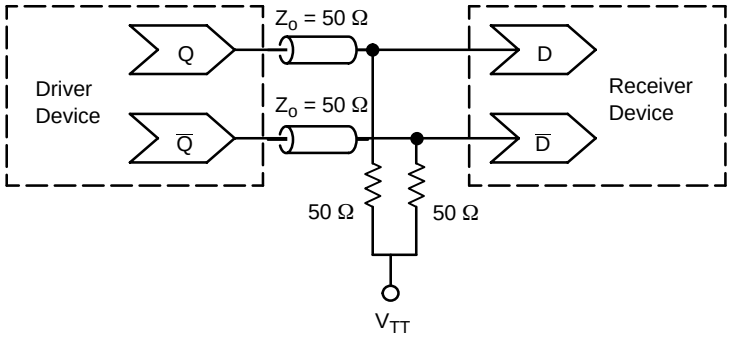


Figure 6. AC Reference Measurement

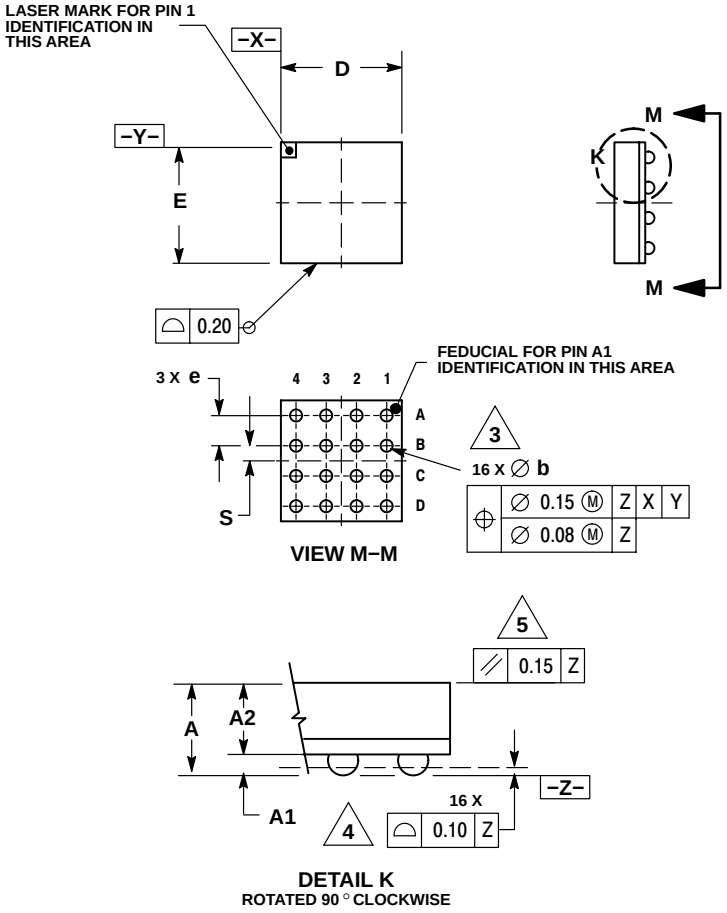


V_{TT} = V_{CC} − 1.5 V (BGA PACKAGE)
V_{TT} = V_{CC} − 2.0 V (QFN PACKAGE)

Figure 7. Typical Termination for Output Driver and Device Evaluation (Refer to Application Note AND8020 − Termination of ECL Logic Devices)

PACKAGE DIMENSIONS

FCBGA−16
BA SUFFIX
PLASTIC 4X4 (mm) BGA FLIP CHIP PACKAGE
CASE 489−01
ISSUE O

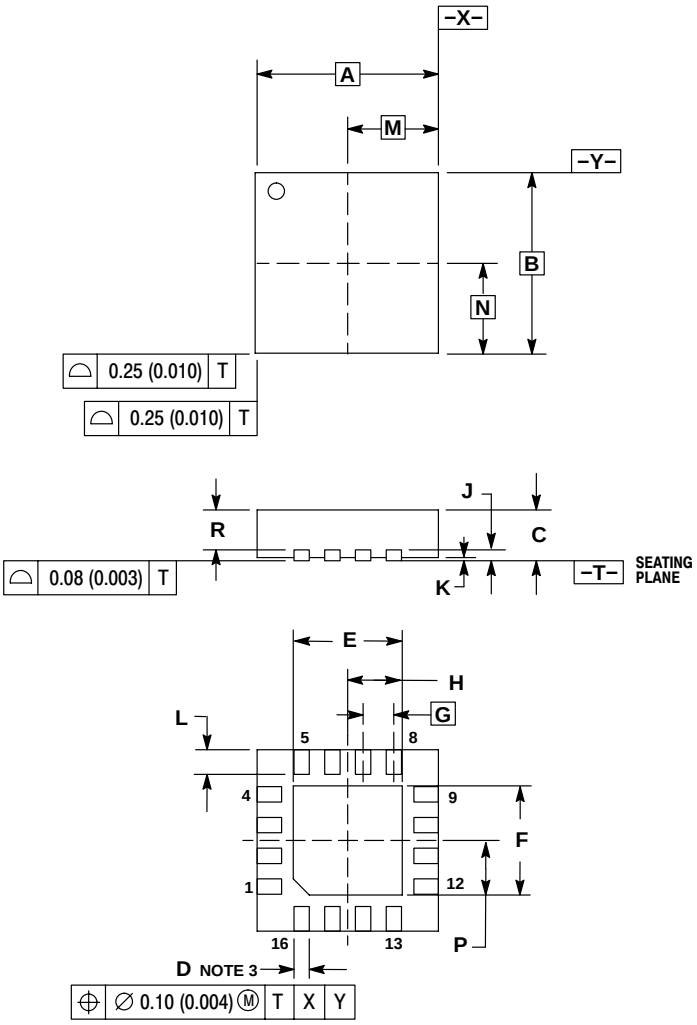


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO DATUM PLANE Z.
4. DATUM Z (SEATING PLANE) IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MILLIMETERS	
DIM	MIN	MAX
A	1.40 MAX	
A1	0.25	0.35
A2	1.20 REF	
b	0.30	0.50
D	4.00 BSC	
E	4.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

PACKAGE DIMENSIONS

16 PIN QFN
MN SUFFIX
CASE 485G−01
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	3.00 BSC		0.118 BSC	
B	3.00 BSC		0.118 BSC	
C	0.80	1.00	0.031	0.039
D	0.23	0.28	0.009	0.011
E	1.75	1.85	0.069	0.073
F	1.75	1.85	0.069	0.073
G	0.50 BSC		0.020 BSC	
H	0.875	0.925	0.034	0.036
J	0.20 REF		0.008 REF	
K	0.00	0.05	0.000	0.002
L	0.35	0.45	0.014	0.018
M	1.50 BSC		0.059 BSC	
N	1.50 BSC		0.059 BSC	
P	0.875	0.925	0.034	0.036
R	0.60	0.80	0.024	0.031

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