

FEATURES

- Hamming code generation
- Extended 100E VEE range of -4.2V to -5.5V
- 8-bit wide
- Expandable for more width
- Provides parity register
- Fully compatible with industry standard 10KH, 100K ECL levels
- Internal 75KΩ input pulldown resistors
- Fully compatible with Motorola MC10E/100E193
- Available in 28-pin PLCC package

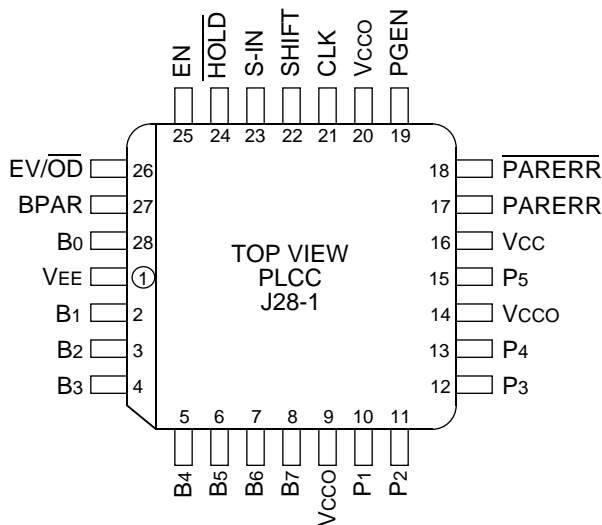
DESCRIPTION

The SY10/100E193 are error detection and correction (EDAC) circuits designed for use in new, high-performance ECL systems. The E193 generates hamming parity codes on an 8-bit word as shown in the block diagram. The P5 output gives the parity of the whole word. PGEN provides word parity after Odd/Even parity control and gating with the BPAR input. PGEN also feeds into a 1-bit shiftable register for use as part of a scan ring.

The combinatorial part of the device generates the same code pattern as the Motorola MC10193.

Used in conjunction with 12-bit parity generators, such as the E160, a SECCED (single error correction, double error detection) error system can be designed for a multiple of an 8-bit word.

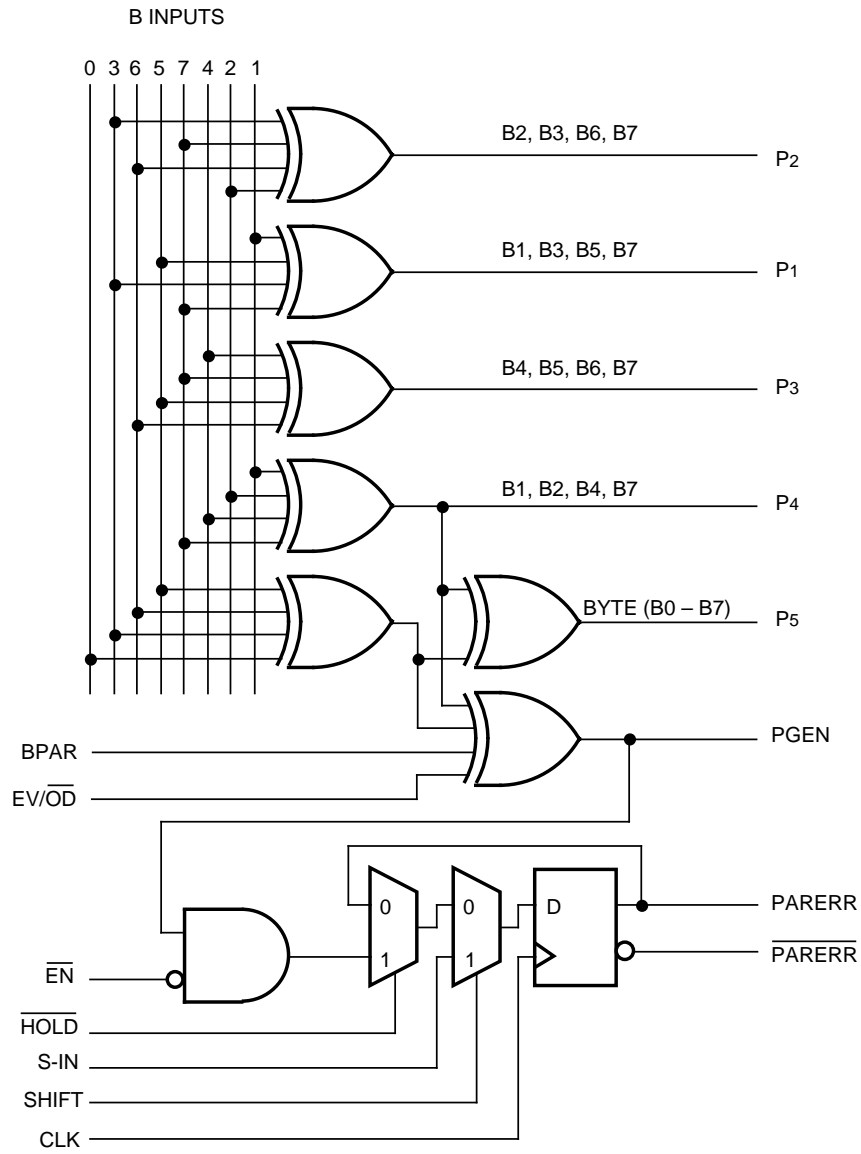
PIN CONFIGURATION



PIN NAMES

Pin	Function
B0-B7	Check Bit Inputs
BPAR	Check Bit Parity Input
EV/OD	Even/Odd Parity Select
EN	Parity Enable
HOLD	Syndrome Hold Input
S-IN	Syndrome Bit Input
SHIFT	Syndrome Bit Shift
CLK	Clock Input
P1-P5	Parity Output
PGEN	Parity Generate Output
PARERR/PARERR	Parity Error Output
VCCO	Vcc to Output

BLOCK DIAGRAM



DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition	
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.			
I _{IH}	Input HIGH Current	—	—	150	—	—	150	—	—	150	μA	—	
I _{EE}	Power Supply Current	10E	—	112	134	—	112	134	—	112	134	mA	—
		100E	—	112	134	—	112	134	—	129	155		

AC ELECTRICAL CHARACTERISTICS

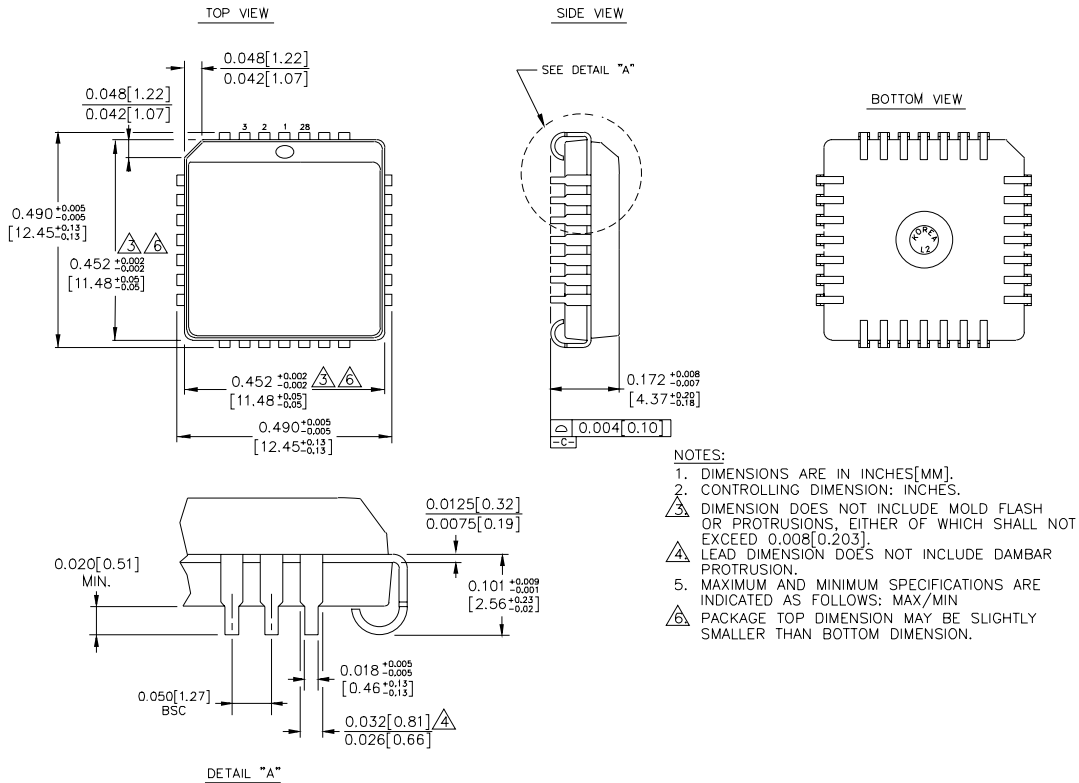
VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

Symbol	Parameter	TA = 0°C			TA = +25°C			TA = +85°C			Unit	Condition
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
t _{PLH} t _{PHL}	Propagation Delay to Output B to P1, P2, P3, P4 B to P5 EV/ \overline{OD} , BPAR to PGEN B to PGEN CLK to PARERR	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	350 400 350 600 300	700 775 650 1000 550	1000 1150 850 1450 850	ps	—
ts	Set-up Time SHIFT S-IN HOLD EN EV/ \overline{OD} BPAR B	400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100	— — — — — — —	400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100	— — — — — — —	400 300 750 500 1300 1300 1700	150 50 350 250 850 850 1100	— — — — — — —	ps	—
th	Hold Time SHIFT S-IN HOLD EN EV/ \overline{OD} BPAR B	200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100	— — — — — — —	200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100	— — — — — — —	200 300 100 100 -200 -200 -300	-150 -50 -350 -250 -850 -850 -1100	— — — — — — —	ps	—
t _r t _f	Rise/Fall Time 20% to 80%	300	700	1100	300	700	1100	300	700	1100	ps	—

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10E193JC	J28-1	Commercial
SY10E193JCTR	J28-1	Commercial
SY100E193JC	J28-1	Commercial
SY100E193JCTR	J28-1	Commercial

28 LEAD PLCC (J28-1)



- NOTES:
1. DIMENSIONS ARE IN INCHES[MM].
 2. CONTROLLING DIMENSION: INCHES.
 3. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008[0.203].
 4. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION.
 5. MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN
 6. PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

Rev. 03

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