QLogic Corporation

FAS366U
Fast Architecture SCSI Processor

Data Sheet

Features

- Compliance with ANSI draft Fast–20 standard
- Compliance with ANSI X3T10/855D SCSI–3 parallel interface (SPI) standard
- Compliance with ANSI SCSI configured automatically (SCAM) protocol levels 1 and 2
- Sustained SCSI data transfer rates of up to:
  - 40 Mbytes/sec synchronous (ultra and wide SCSI)
  - 14 Mbytes/sec asynchronous (wide SCSI)
- Synchronous DMA timing; DMA speed of 50 Mbytes/sec
- $\overline{REQ}$ and $\overline{ACK}$ programmable assertion and deassertion control
- Support for hot plugging
- Target and initiator block transfer sequences
- Bus idle timer
- Split–bus architecture
- Pipelined command structure
- On–chip, single–ended SCSI transceivers (48–mA drivers)
- Initiator and target roles
- Active negation
- 16–bit recommand counter
- Differential mode
- SCSI bus reset watchdog timer

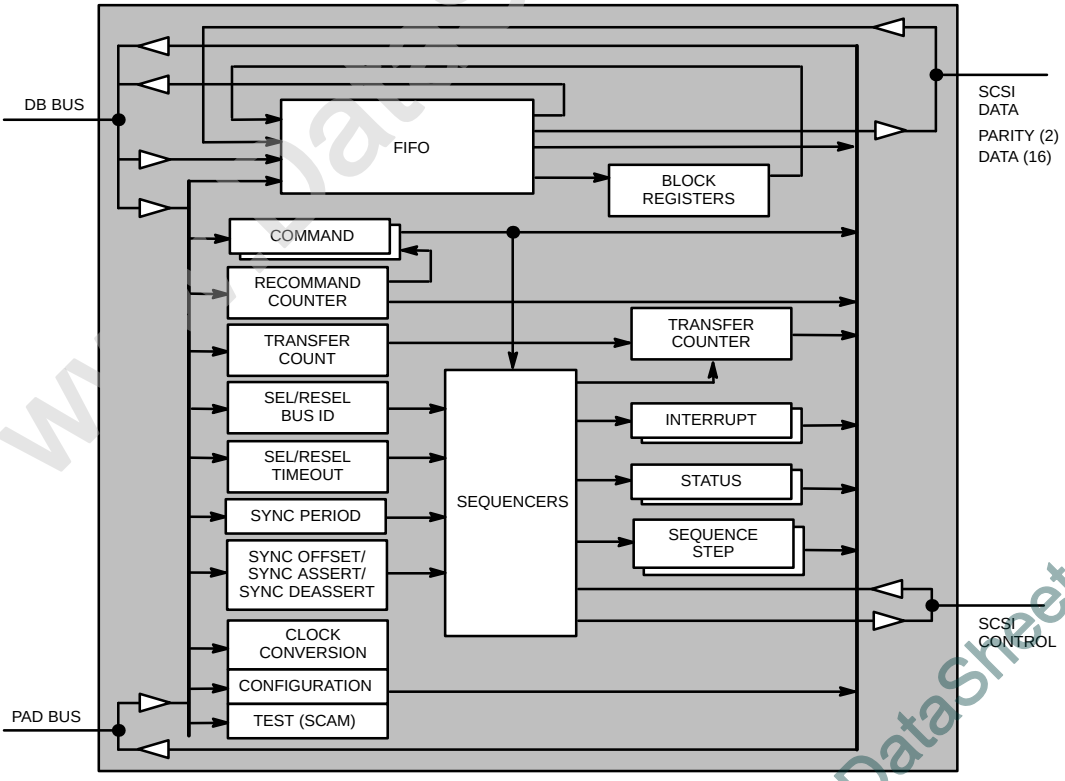


Figure 1. FAS366U Block Diagram

Product Description

The FAS366U is a new addition to the QLogic fast architecture SCSI processor (FAS) chip family. The FAS366U supports advanced SCSI–3 options including ultra SCSI synchronous transfers. Also included is the advanced SCAM level 2 SCSI controller core.

The FAS366U is a single–chip controller for use in host and peripheral applications. It is firmware and pin–out compatible with the QLogic FAS366 chip. The FAS366U block diagram is shown in figure 1.

The FAS366U implements QLogic's new SCSI target and initiator block transfer sequences. The block sequences reduce firmware overhead and are composed of the following new commands: Target Block Sequence (including the bus idle timer), Initiator Block Sequence, Load/Unload Block Registers sequences, Abort Block Sequence, and Disconnect Abort Block Sequence.

The FAS366U supports both single–ended and differential mode SCSI operations and operates in initiator and target roles. The FAS366U has been optimized for interaction with a DMA controller and the controlling microprocessor.

The versatile split–bus architecture supports various microprocessor and DMA bus configurations. A separate 8–bit microprocessor bus (PAD) provides access to all internal registers, and a 16–bit DMA bus (DB) provides a path for DMA transfers through the FIFO. Each bus is protected by a parity bit (byte–wide parity) to improve data integrity. During data transfer, the microprocessor has instant access to status and has the ability to execute commands.

SCAM Implementation

The FAS366U supports levels 1 and 2 of the SCAM protocol. Refer to the latest revision of X3T10/855D, Annex B. The SCAM protocol requires direct access and control over the SCSI data bus and several of the SCSI phase and control signals. The majority of the SCAM protocol can be implemented in firmware at microprocessor speeds. The following SCAM features are supported in the hardware:

- Arbitration without an ID
- Slow response to selection with an unconfirmed ID
- Detection of and response to SCAM selection

Fast DMA Protocol

The fast DMA protocol is required for supporting the full bandwidth of ultra, wide SCSI.

The DREQ signal initiates DMA transfers and runs asynchronous to the user's clock. For read operations, $\overline{\text{DACK}}$ acts as a chip select to enable the FAS366U drivers onto the DMA bus. The chip select role of $\overline{\text{DACK}}$ helps support the burst timing of fast DMA mode. $\overline{\text{DACK}}$ selects the FAS366U after DREQ is asserted and is removed either after DREQ is deasserted or when the DMA transfer is paused.

$\overline{\text{DBRD}}$ requests data from the FAS366U and $\overline{\text{DBWR}}$ validates data sent to the FAS366U. Data is valid around the rising (trailing) edge of $\overline{\text{DBRD}}$ or $\overline{\text{DBWR}}$.

DMA transfers are terminated by deasserting DREQ. Deassertion of DREQ is triggered by the leading edge of $\overline{\text{DBRD}}$ or $\overline{\text{DBWR}}$ (see timing parameter t1 in figures 2 and 3) under any of the following conditions:

- To prevent FIFO overrun conditions
- To prevent FIFO underrun conditions
- When the required amount of data has been transferred

When DREQ is deasserted, the FAS366U ignores $\overline{\text{DBRD}}$ and $\overline{\text{DBWR}}$. Data transfers do not take place unless DREQ is asserted.

The FAS366U does not generate parity on the incoming DMA bus. Correct parity must always be supplied with the data.

The DMA interface signals are given in table 1. DMA timing is given in table 2 and figures 2 and 3.

Table 1. DMA Interface Signals

Pin	Type	Active Level	Description
DREQ	O	High	The FAS366U DMA request line begins and ends DMA cycles.
$\overline{\text{DACK}}$	I	Low	The acknowledge is used as a chip select to activate FAS366U drivers and to acknowledge acceptance of DREQ.
$\overline{\text{DBRD}}$	I	Rising edge	The trailing edge accepts data from the FAS366U for DMA read operations.
$\overline{\text{DBWR}}$	I	Rising edge	The trailing edge strobes data into the FAS366U FIFO on DMA write operations.
DB15–0	I/O	N/A	This is the DMA data bus.

Table 2. DMA Timing

Symbol	Description	Minimum (ns)	Maximum (ns)	Note
t1	$\overline{\text{DBRD}}$/$\overline{\text{DBWR}}$ low to DREQ low		12	a
t2	$\overline{\text{DACK}}$ high to DREQ high	TBD		
t3	$\overline{\text{DACK}}$ high to $\overline{\text{DACK}}$ low	40		
tR1	$\overline{\text{DACK}}$ low to $\overline{\text{DBRD}}$ low	tR5		
tR2	$\overline{\text{DBRD}}$ assertion pulse width	15		
tR3	$\overline{\text{DBRD}}$ deassertion pulse width	15		
tR4	$\overline{\text{DBRD}}$ high to $\overline{\text{DACK}}$ high	tR3		b
tR5	$\overline{\text{DBRD}}$ low to $\overline{\text{DBRD}}$ low cycle	40		
tR6	$\overline{\text{DACK}}$ low to DB15–0 read on	2		c
tR7	$\overline{\text{DACK}}$ high to DB15–0 read off		15	c
tR8	$\overline{\text{DBRD}}$ low to DB15–0 read valid		15	c
tR9	$\overline{\text{DBRD}}$ low to DB15–0 read invalid	0		c
tW1	$\overline{\text{DACK}}$ low to $\overline{\text{DBWR}}$ low	tW5		
tW2	$\overline{\text{DBWR}}$ assertion pulse width	15		
tW3	$\overline{\text{DBWR}}$ deassertion pulse width	15		
tW4	$\overline{\text{DBWR}}$ high to $\overline{\text{DACK}}$ high	tW3		d
tW5	$\overline{\text{DBWR}}$ low to $\overline{\text{DBWR}}$ low cycle	40		
tW6	DB15–0 write setup to $\overline{\text{DBWR}}$ high	10		
tW7	DB15–0 write hold from $\overline{\text{DBWR}}$ high	5		

Table Notes

[a] DREQ loading is 30 pf.

[b] $\overline{\text{DBRD}}$ low to $\overline{\text{DACK}}$ high ≥ tR5

[c] Data loading is 50 pf.

[d] $\overline{\text{DBWR}}$ low to $\overline{\text{DACK}}$ high ≥ tW5

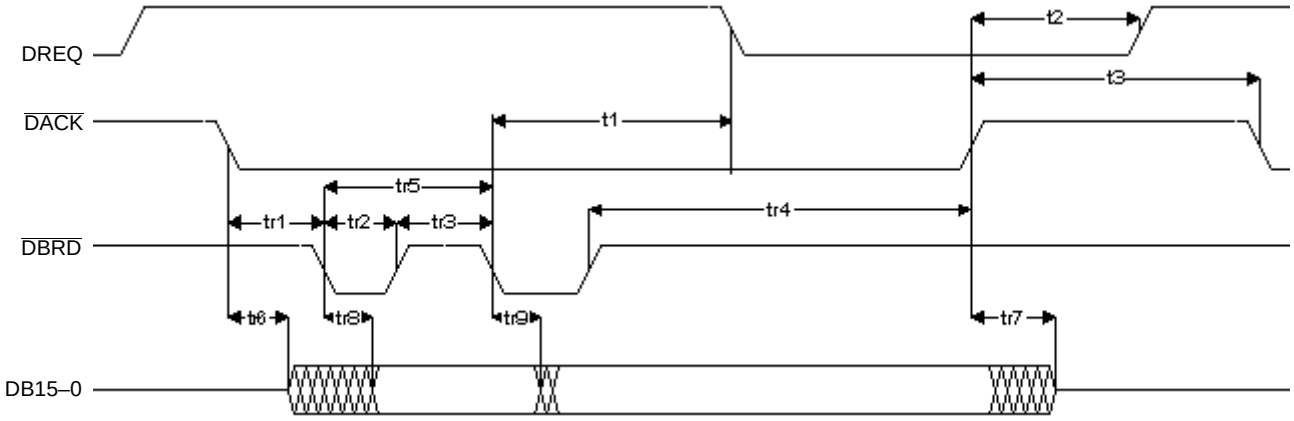


Figure 2. DMA Read Cycle

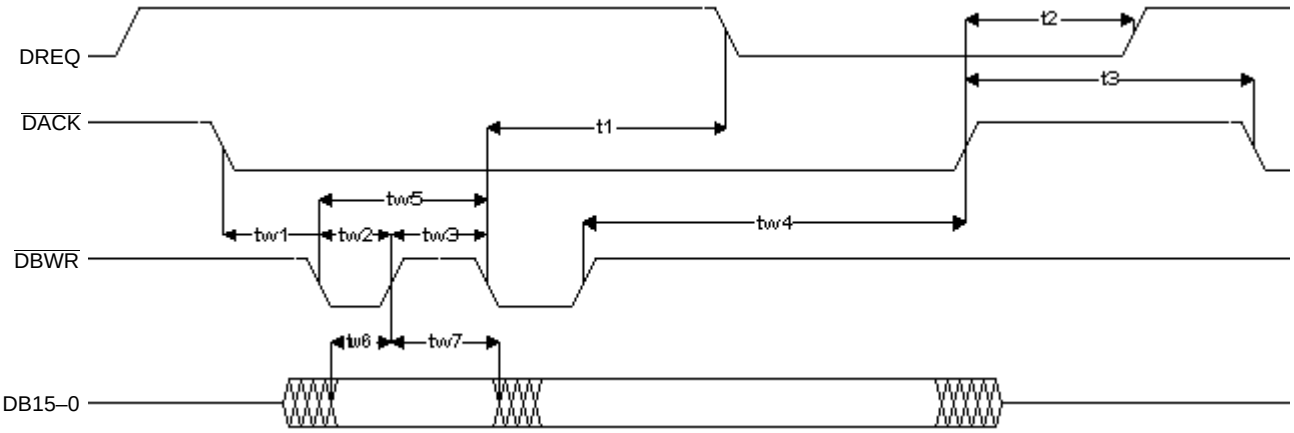
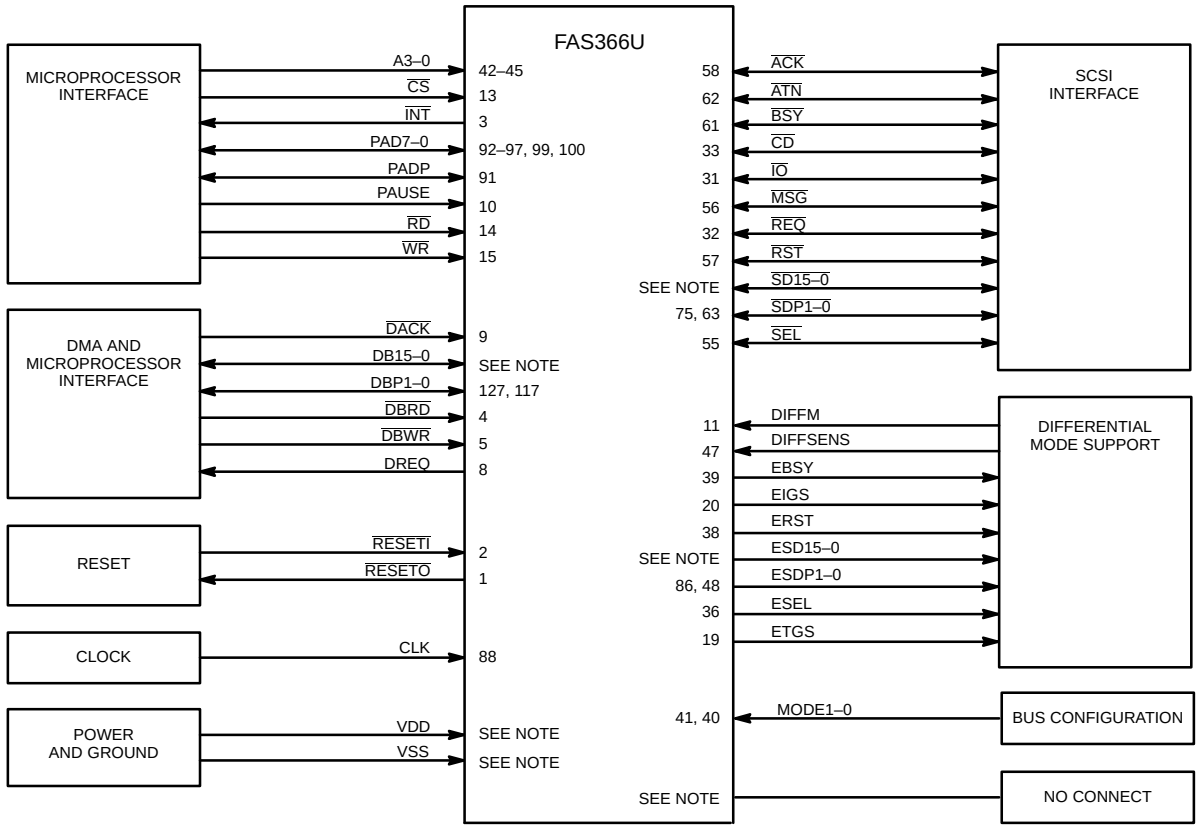


Figure 3. DMA Write Cycle

Interfaces

The FAS366U interfaces consist of the microprocessor bus and the SCSI bus. Pins that support these interfaces and other chip operations are shown in figure 4.



NOTE:
DB15–0 = 126–122, 120–118, 116, 115, 113–108
ESD15–0 = 101–104, 21–24, 49–52, 82–85
NO CONNECT = 16, 37, 53, 60, 67, 90, 105
SD15–0 = 76, 78–80, 26–28, 30, 64, 65, 68–70, 72–74
VDD = 7, 12, 17, 35, 87, 106
VSS = 6, 18, 25, 29, 34, 46, 54, 59, 66, 71, 77, 81, 89, 98, 107, 114, 121, 128

Figure 4. FAS366U Functional Signal Grouping

Packaging

The FAS366U is available in a 128–pin plastic quad flat pack (PQFP). The pin diagram for this package is illustrated in figure 5. The FAS366U package dimensions are shown in figure 6.

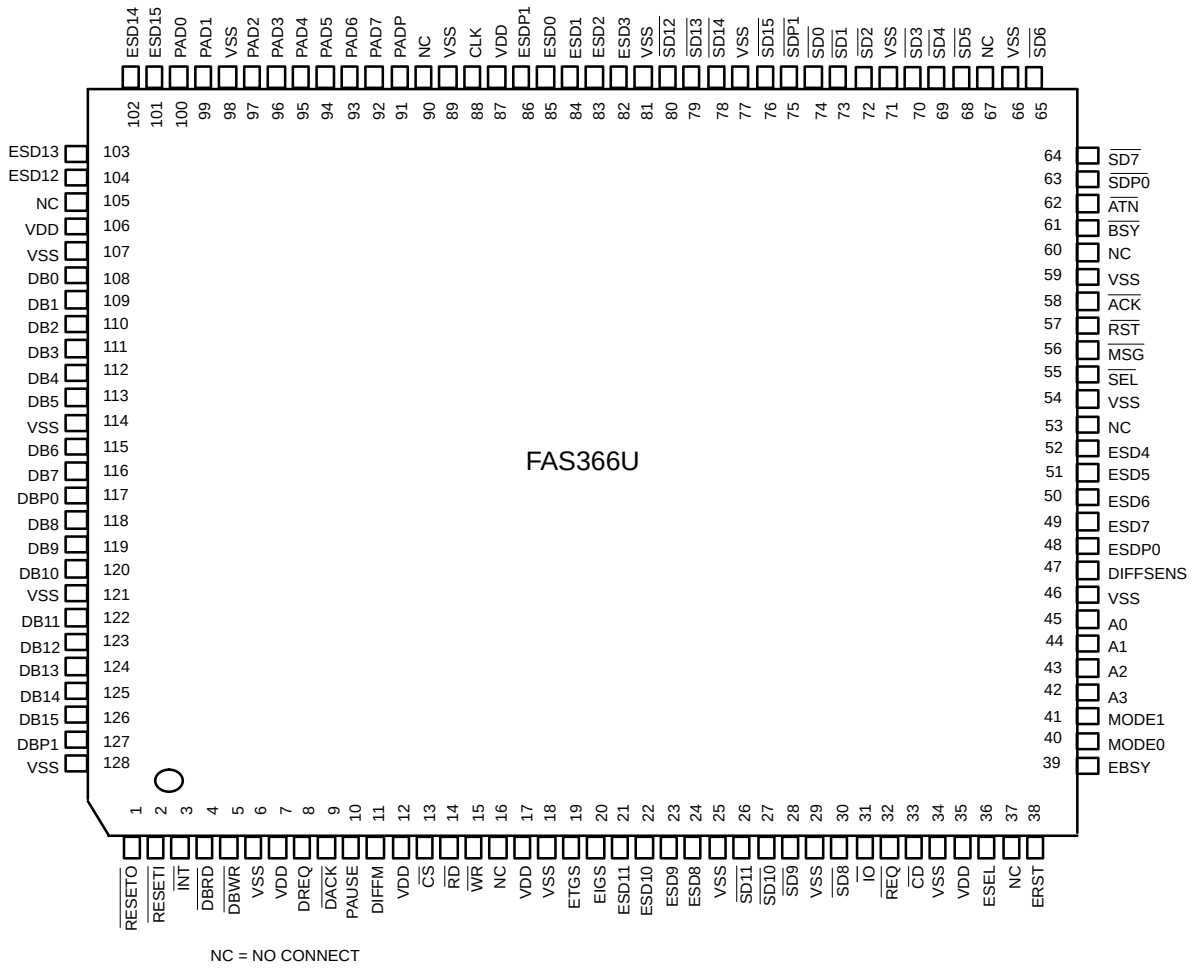


Figure 5. FAS366U Pin Diagram

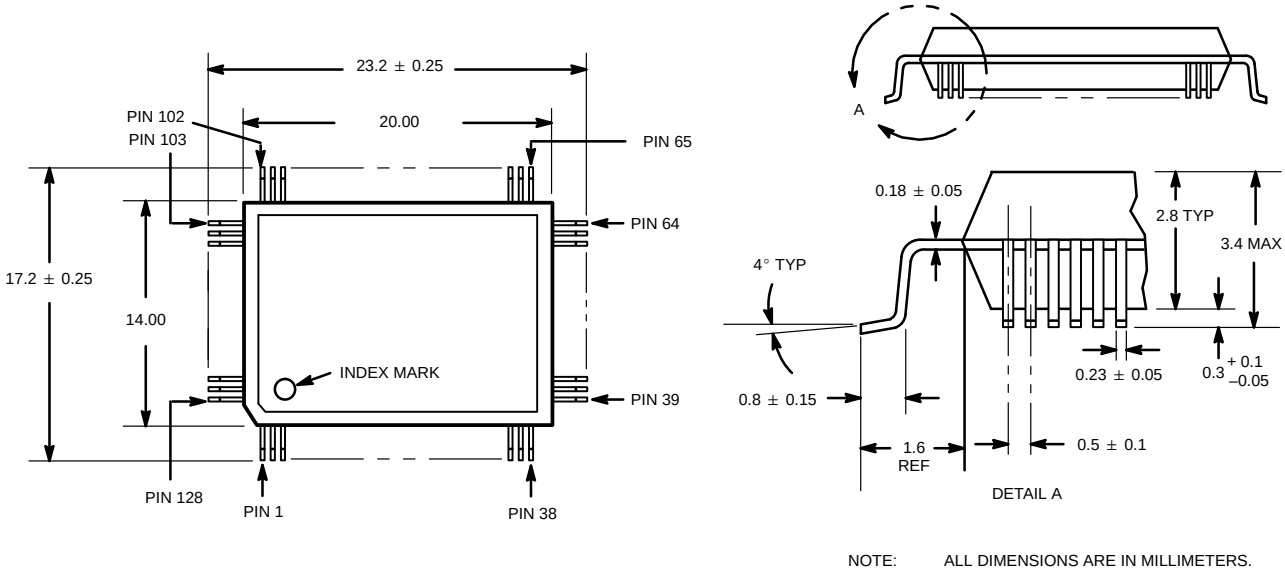


Figure 6. FAS366U Mechanical Drawings

Electrical Characteristics

Table 1. Operating Conditions

Symbol	Description	Minimum	Maximum	Unit
VDD	Supply voltage	4.75	5.25	V
IDD[a]	Supply current (static IDD)		TBD	mA
IDD[b]	Supply current (dynamic IDD)		TBD	mA
TA	Ambient temperature	0	70	°C

Table Notes

Conditions not within the operating conditions but within the absolute maximum stress ratings may cause the chip to malfunction.

[a]Static IDD is measured with no clocks running and all inputs forced to VDD, all outputs unloaded, and all bidirectional pins configured as inputs.

[b]Dynamic IDD is dependent on the application.

Specifications are subject to change without notice.
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