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# HM628512AI Series

524288-word  $\times$  8-bit High Speed CMOS Static RAM

# HITACHI

ADE-203-791 (Z)

Preliminary

Rev. 0.0

Jun. 20, 1997

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## Description

The Hitachi HM628512AI is a 4-Mbit static RAM organized 512-kword  $\times$  8-bit. It realizes higher density, higher performance and low power consumption by employing 0.5  $\mu$ m Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II or 600-mil plastic DIP, is available for high density mounting. L-version is suitable for battery backup system.

## Features

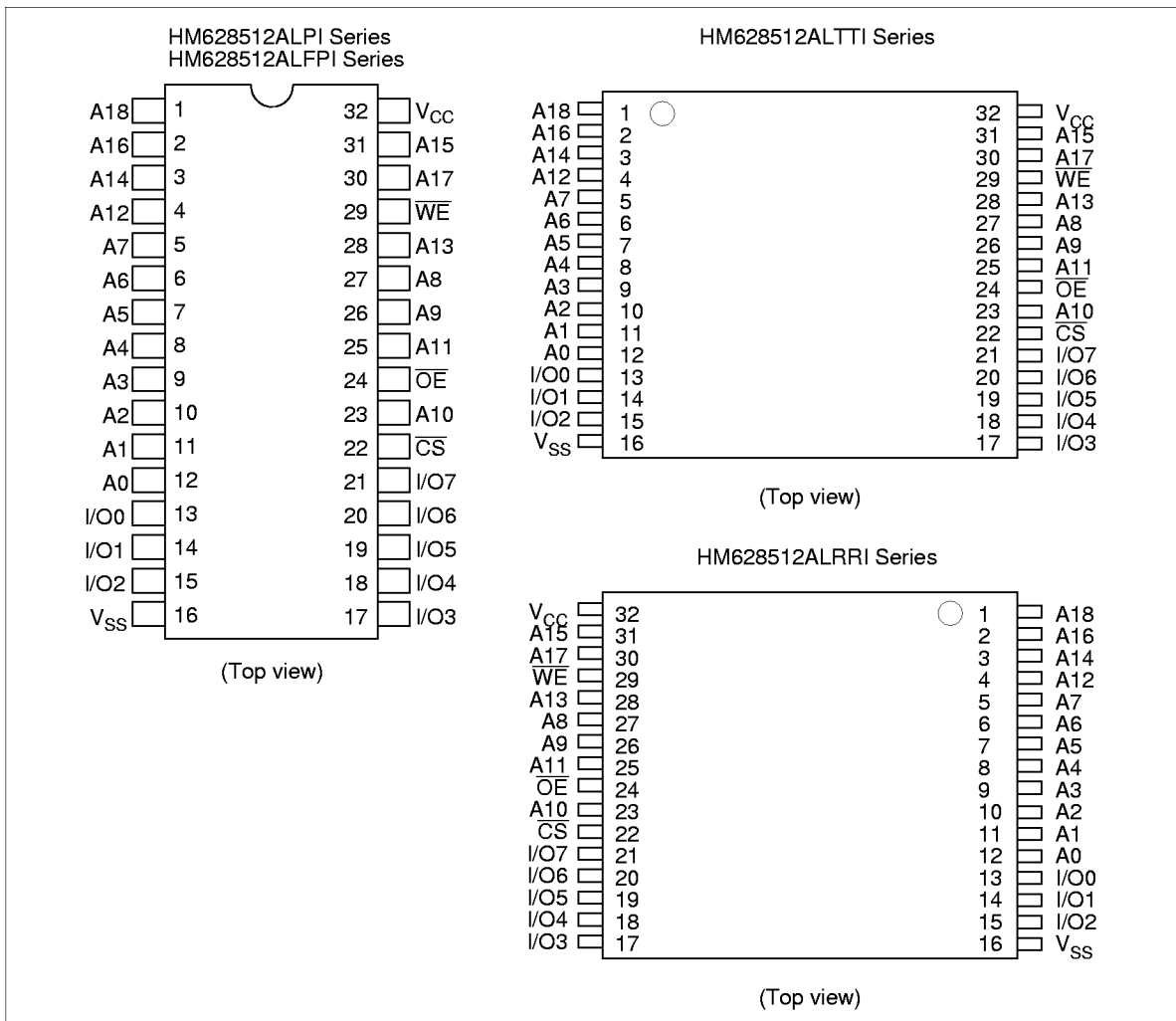
- Single 5 V supply: 5.0 V  $\pm$  10%
- Access time: 70/85 ns (max)
- Power dissipation
  - Active: 50 mW/MHz (typ)
  - Standby: 10  $\mu$ W (typ)
- Completely static memory
  - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation
- Operating temperature:  $-40$  to  $85^{\circ}\text{C}$

# HM628512AI Series

## Ordering Information

Type No.	Access time	Package
HM628512ALPI-7	70 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512ALPI-8	85 ns	
HM628512ALFPI-7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512ALFPI-8	85 ns	
HM628512ALTTI-7	70 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512ALTTI-8	85 ns	
HM628512ALRRI-7	70 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM628512ALRRI-8	85 ns	

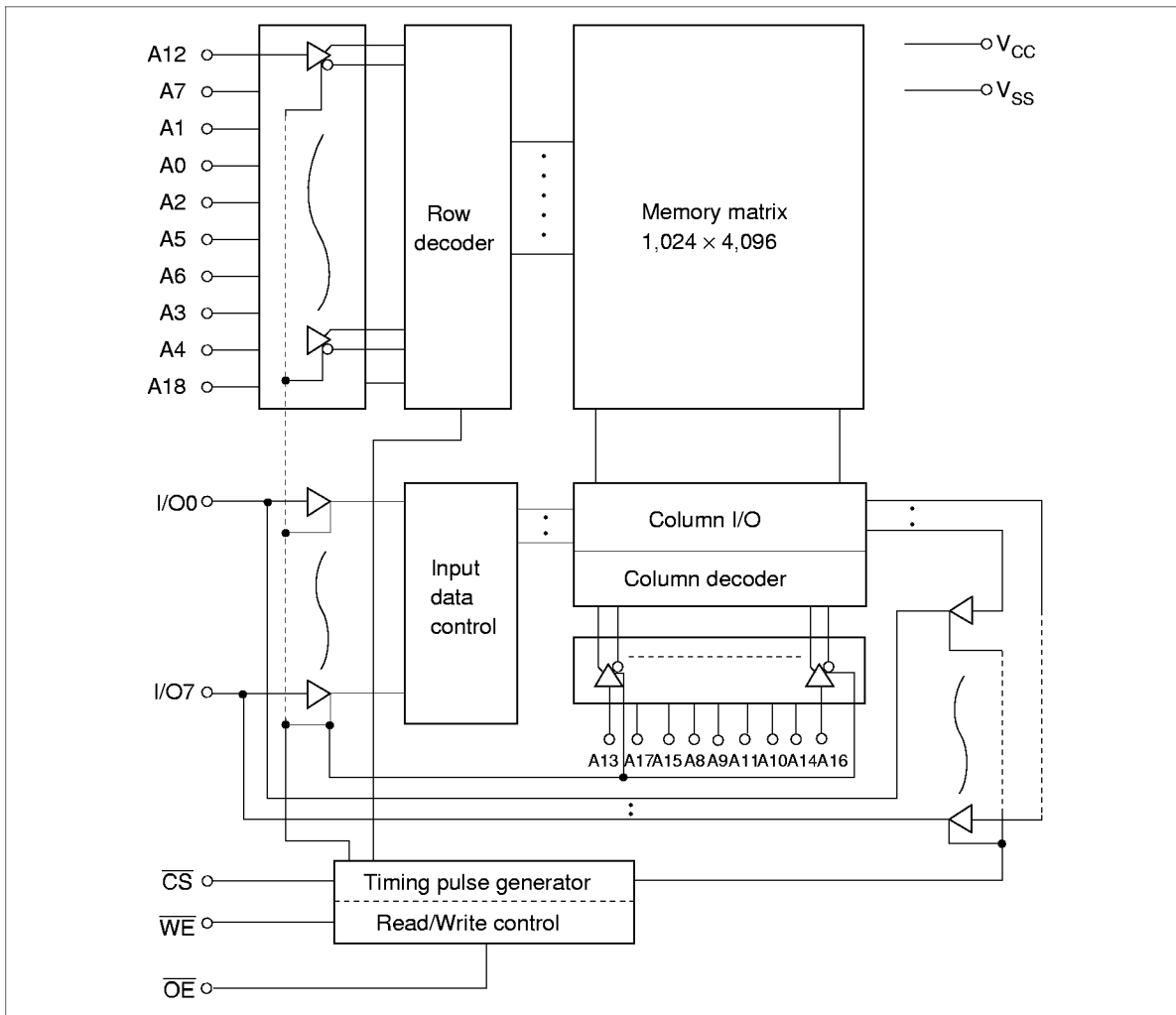
## Pin Arrangement



**Pin Description**

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$V_{CC}$	Power supply
$V_{SS}$	Ground

**Block Diagram**



## HM628512AI Series

### Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
×	H	×	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: ×: H or L

### Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage relative to $V_{SS}$	$V_{CC}$	-0.5 to +7.0	V
Terminal voltage on any pin relative to $V_{SS}$	$V_T$	-0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	-40 to +85	°C
Storage temperature	$T_{stg}$	-55 to +125	°C
Storage temperature under bias	$T_{bias}$	-40 to +85	°C

Notes: 1. -3.0 V for pulse half-width ≤ 30 ns  
 2. Maximum voltage is 7.0 V

### Recommended DC Operating Conditions ( $T_a = -40$ to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.4	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{IL}$	-0.3* <sup>1</sup>	—	0.6	V

Note: 1. -3.0 V for pulse half-width ≤ 30 ns

## HM628512AI Series

### DC Characteristics (Ta = -40 to +85°C, V<sub>CC</sub> = 5 V ±10% , V<sub>SS</sub> = 0 V)

Parameter	Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current	I <sub>LI</sub>	—	—	1	μA	V <sub>in</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Output leakage current	I <sub>LO</sub>	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , V <sub>I/O</sub> = V <sub>SS</sub> to V <sub>CC</sub>
Operating current	I <sub>CC</sub>	—	8	15	mA	$\overline{CS} = V_{IL}$ , others = V <sub>IH</sub> /V <sub>IL</sub> , I <sub>I/O</sub> = 0 mA
Average operating current	I <sub>CC1</sub>	—	45	70	mA	Min cycle, duty = 100% CS = V <sub>IL</sub> , others = V <sub>IH</sub> /V <sub>IL</sub> I <sub>I/O</sub> = 0 mA
	I <sub>CC2</sub>	—	10	20	mA	Cycle time = 1 μs, duty = 100% I <sub>I/O</sub> = 0 mA, $\overline{CS} \leq 0.2$ V V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V
Standby current	I <sub>SB</sub>	—	1	3	mA	$\overline{CS} = V_{IH}$
	I <sub>SB1</sub>	—	2	100	μA	V <sub>in</sub> ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V
Output low voltage	V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 2.1 mA
Output high voltage	V <sub>OH</sub>	2.4	—	—	V	I <sub>OH</sub> = -1.0 mA

Notes: 1. Typical values are at V<sub>CC</sub> = 5.0 V, Ta = +25°C and specified loading, and not guaranteed.

### Capacitance (Ta = 25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	C <sub>in</sub>	—	8	pF	V <sub>in</sub> = 0 V
Input/output capacitance* <sup>1</sup>	C <sub>I/O</sub>	—	10	pF	V <sub>I/O</sub> = 0 V

Note: 1. This parameter is sampled and not 100% tested.

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## HM628512AI Series

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**AC Characteristics** ( $T_a = -40$  to  $+85^\circ\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10$ )

### Test Conditions

- Input pulse levels: 0.5 V to 2.5 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V  
Output load: 1 TTL Gate +  $C_L$  (100 pF)  
(Including scope & jig)

### Read Cycle

Parameter	Symbol	HM628512AI				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Read cycle time	$t_{RC}$	70	—	85	—	ns	
Address access time	$t_{AA}$	—	70	—	85	ns	
Chip select access time	$t_{CO}$	—	70	—	85	ns	
Output enable to output valid	$t_{OE}$	—	35	—	45	ns	
Chip select to output in low-Z	$t_{LZ}$	10	—	10	—	ns	2
Output enable to output in low-Z	$t_{OLZ}$	5	—	5	—	ns	2
Chip deselect to output in high-Z	$t_{HZ}$	0	25	0	30	ns	1, 2
Output disable to output in high-Z	$t_{OHZ}$	0	25	0	30	ns	1, 2
Output hold from address change	$t_{OH}$	10	—	10	—	ns	

**Write Cycle**

Parameter	Symbol	HM628512AI				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Write cycle time	$t_{WC}$	70	—	85	—	ns	
Chip select to end of write	$t_{CW}$	60	—	75	—	ns	4
Address setup time	$t_{AS}$	0	—	0	—	ns	5
Address valid to end of write	$t_{AW}$	60	—	75	—	ns	
Write pulse width	$t_{WP}$	50	—	55	—	ns	3, 12
Write recovery time	$t_{WR}$	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	$t_{WHZ}$	0	25	0	30	ns	1, 2, 7
Data to write time overlap	$t_{DW}$	30	—	35	—	ns	
Data hold from write time	$t_{DH}$	0	—	0	—	ns	
Output active from output in high-Z	$t_{OW}$	5	—	5	—	ns	2
Output disable to output in high-Z	$t_{OHZ}$	0	25	0	30	ns	1, 2, 7

Notes: 1.  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.

4.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.

5.  $t_{AS}$  is measured from the address valid to the beginning of write.

6.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

10. Dout is the read data of next address.

11. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

12. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

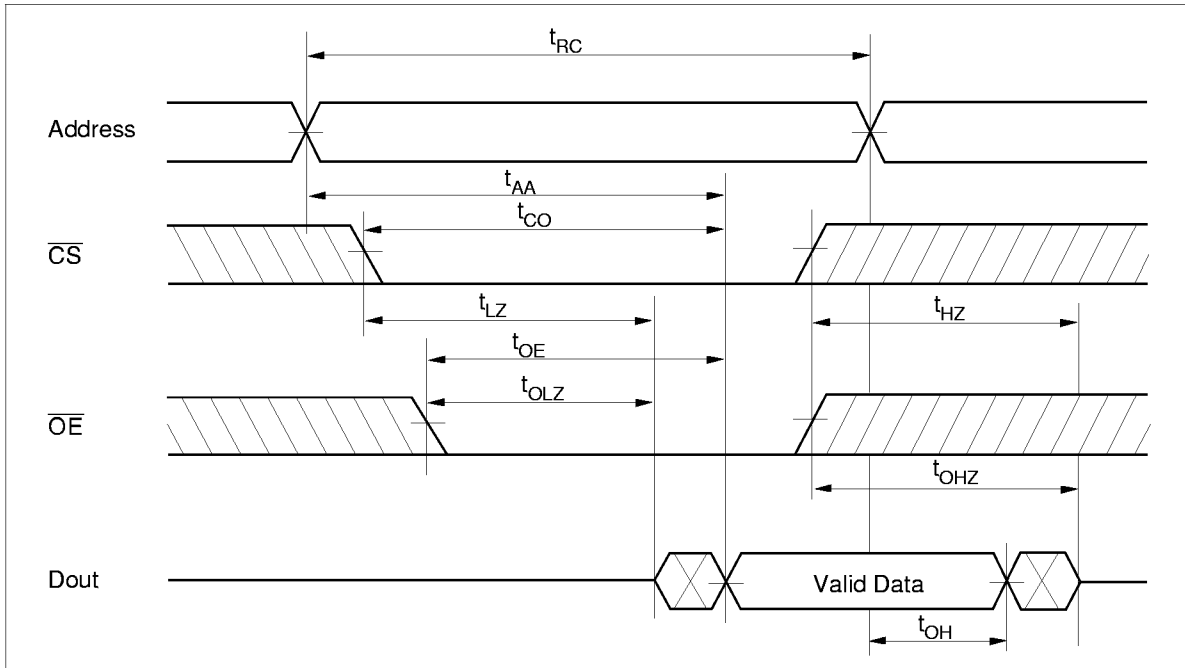
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## HM628512AI Series

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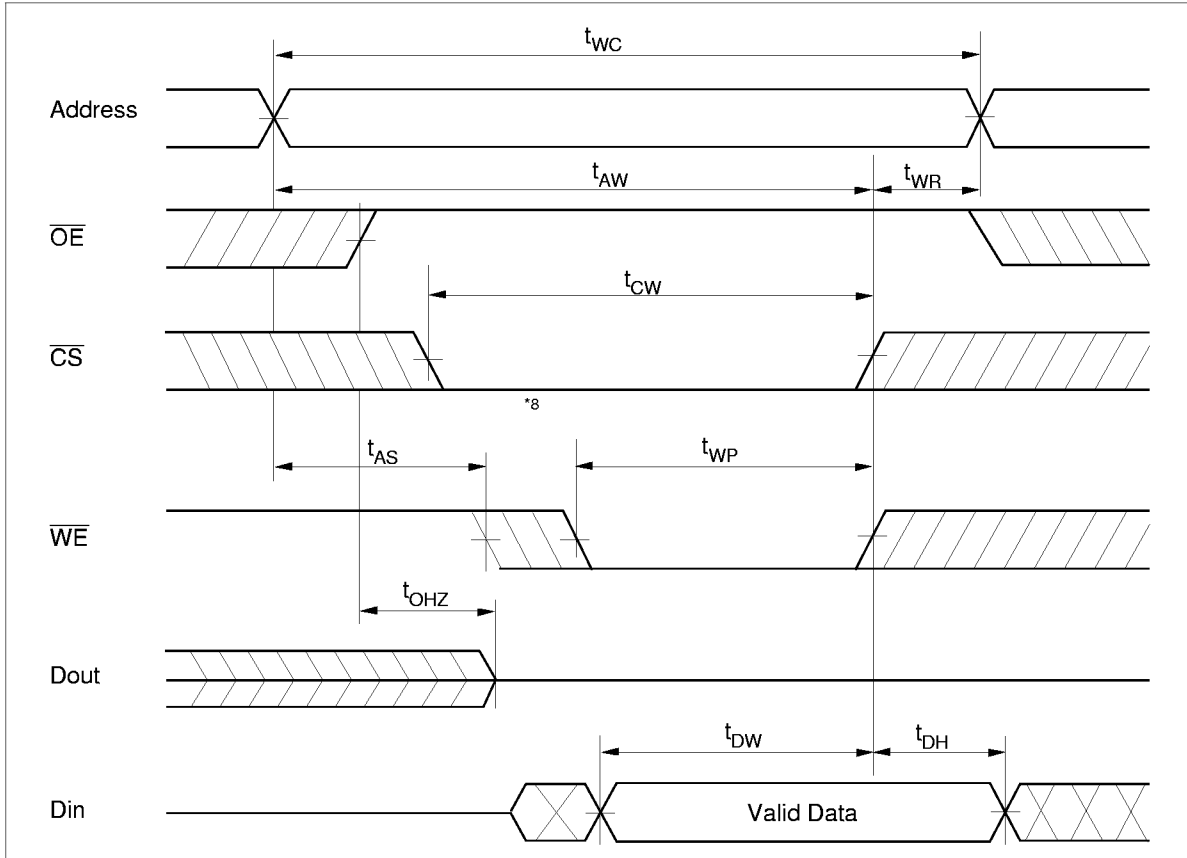
### Timing Waveforms

Read Timing Waveform ( $\overline{WE} = V_{IH}$ )



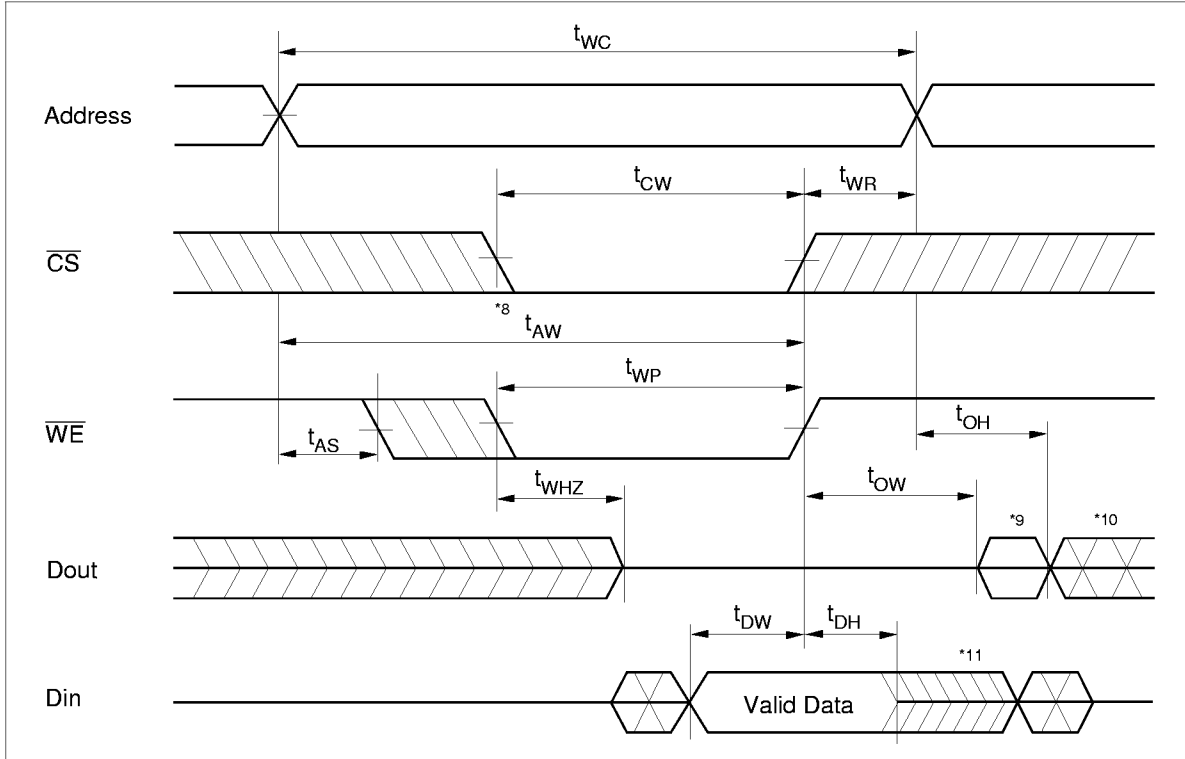


Write Timing Waveform (1) ( $\overline{\text{OE}}$  Clock)



# HM628512AI Series

## Write Timing Waveform (2) ( $\overline{\text{OE}}$ Low Fixed)

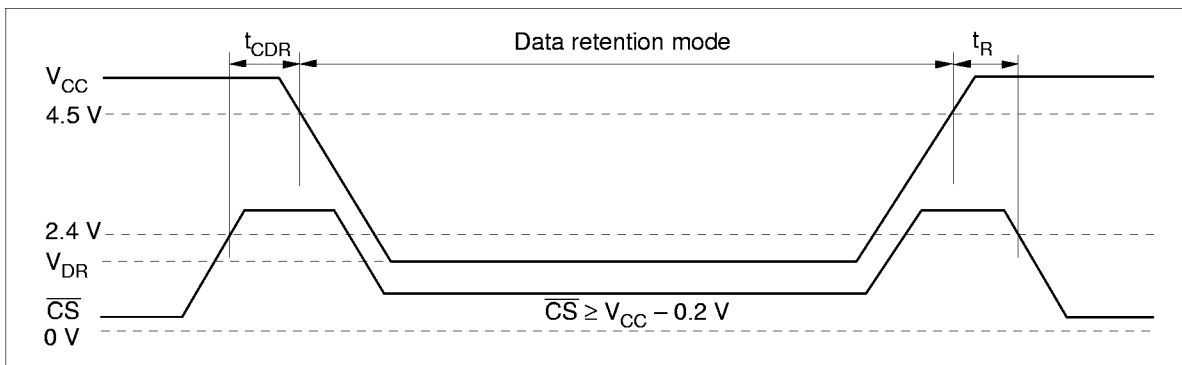


Low  $V_{CC}$  Data Retention Characteristics ( $T_a = -40$  to  $+85^\circ\text{C}$ )

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*2
$V_{CC}$ for data retention	$V_{DR}$	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , $V_{in} \geq 0 \text{ V}$
Data retention current	$I_{CCDR}$	—	1*3	50*1	$\mu\text{A}$	$V_{CC} = 3.0 \text{ V}$ , $V_{in} \geq 0 \text{ V}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	$t_{CDR}$	0	—	—	ns	See retention waveform
Operation recovery time	$t_R$	5	—	—	ms	

- Notes: 1. 20  $\mu\text{A}$  (max) at  $T_a = -40$  to  $40^\circ\text{C}$   
 2.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and  $D_{in}$  buffer. In data retention mode,  $V_{in}$  levels (address,  $\overline{WE}$ ,  $\overline{OE}$ ,  $I/O$ ) can be in the high impedance state.  
 3. Typical values are at  $V_{CC} = 3.0 \text{ V}$ ,  $T_a = 25^\circ\text{C}$  and specified loading, and not guaranteed.

Low  $V_{CC}$  Data Retention Timing Waveform ( $\overline{CS}$  Controlled)

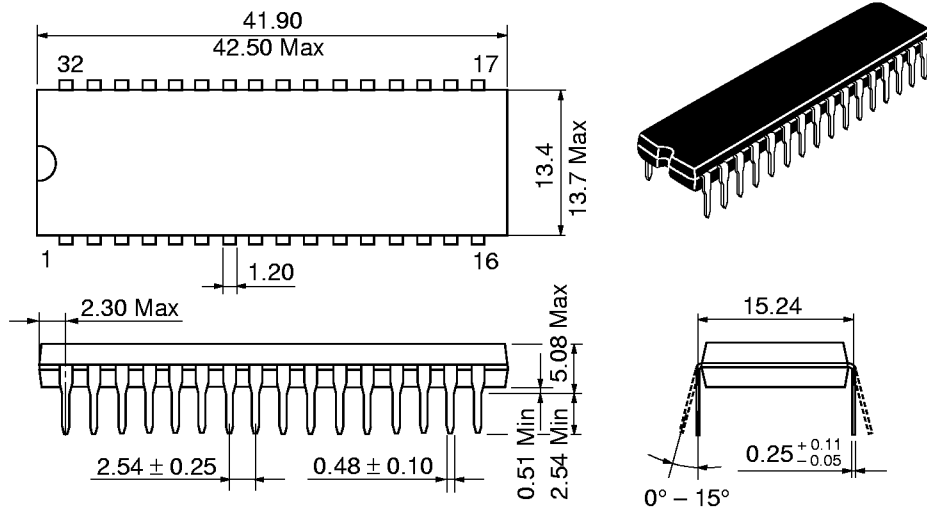


# HM628512AI Series

## Package Dimensions

HM628512ALPI Series (DP-32)

Unit: mm

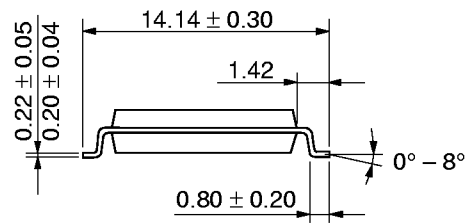
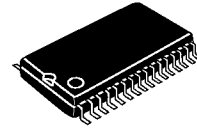
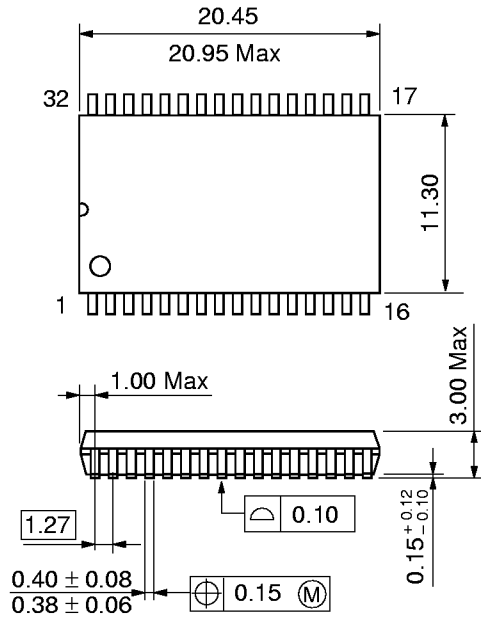


Hitachi Code	DP-32
JEDEC Code	—
EIAJ Code	SC-613
Weight (reference value)	5.1 g

# HM628512AI Series

## HM628512ALFPI Series (FP-32D)

Unit: mm



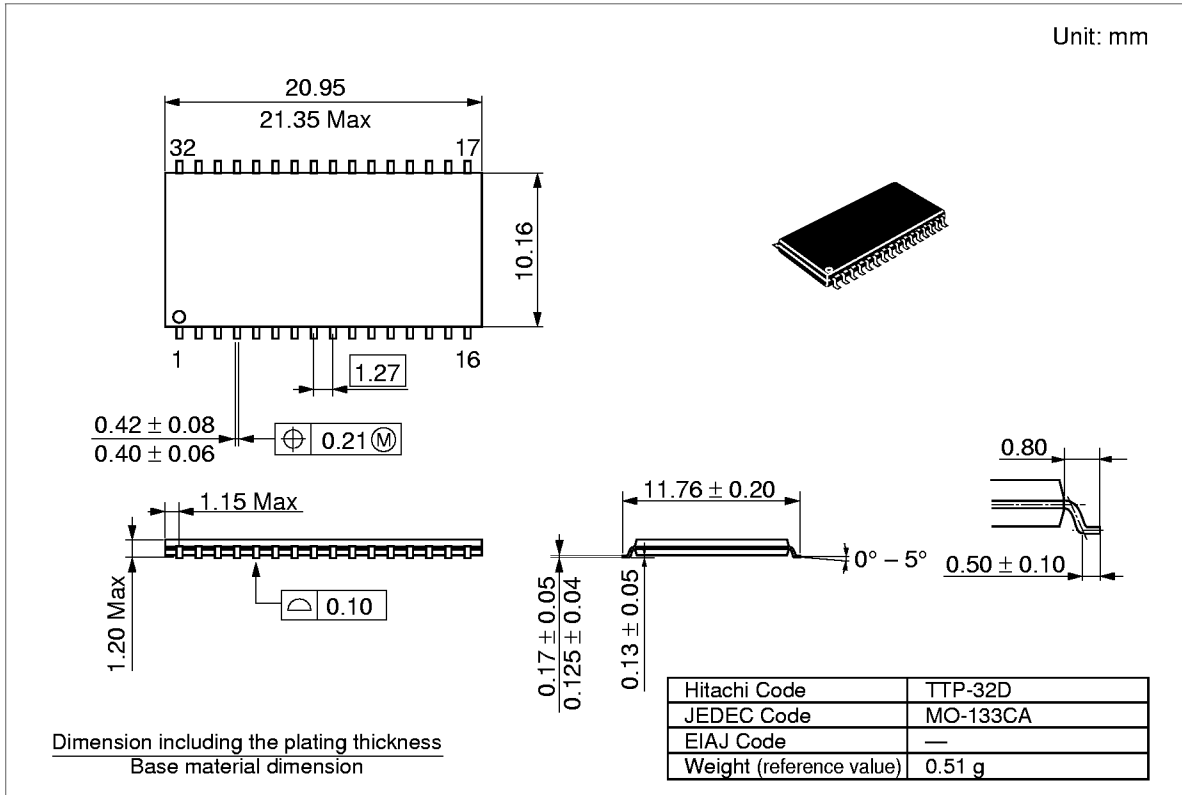
Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-32D
JEDEC Code	MO-099AB
EIAJ Code	—
Weight (reference value)	1.3 g

# HM628512AI Series

## HM628512ALTTI Series (TTP-32D)

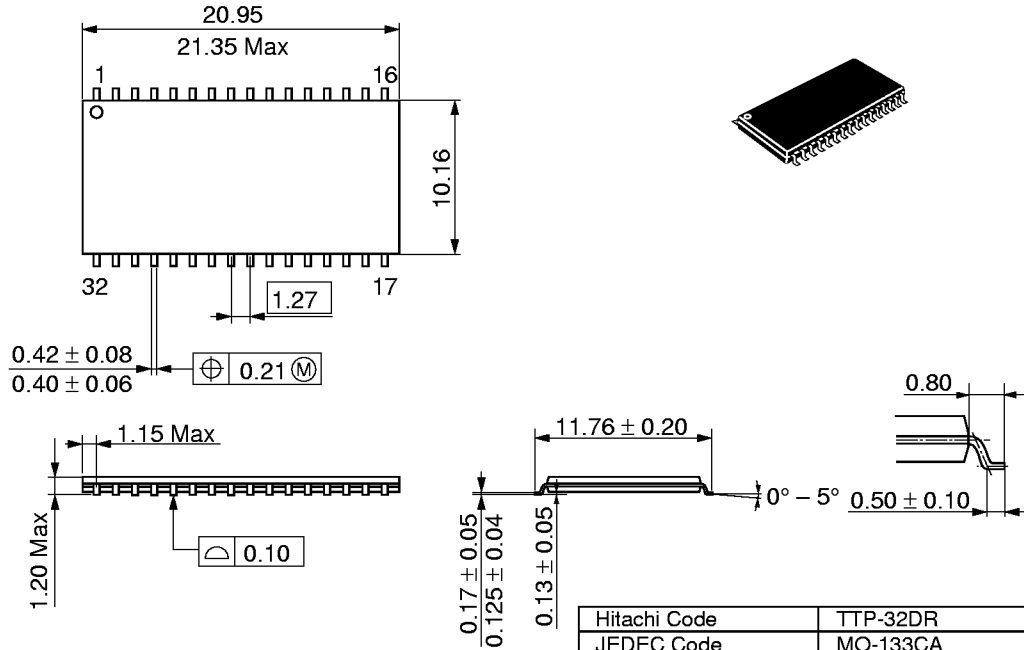
Unit: mm



# HM628512AI Series

## HM628512ALRRI Series (TTP-32DR)

Unit: mm



Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-32DR
JEDEC Code	MO-133CA
EIAJ Code	—
Weight (reference value)	0.51 g

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## HM628512AI Series

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# HITACHI

#### Hitachi, Ltd.

Semiconductor & IC Div.  
Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100, Japan  
Tel: Tokyo (03) 3270-2111  
Fax: (03) 3270-5109

#### For further information write to:

Hitachi America, Ltd.  
Semiconductor & IC Div.  
2000 Sierra Point Parkway  
Brisbane, CA. 94005-1835  
U S A  
Tel: 415-589-8300  
Fax: 415-583-4207

Hitachi Europe GmbH  
Electronic Components Group  
Continental Europe  
Dornacher Straße 3  
D-85622 Feldkirchen  
München  
Tel: 089-9 91 80-0  
Fax: 089-9 29 30 00

Hitachi Europe Ltd.  
Electronic Components Div.  
Northern Europe Headquarters  
Whitebrook Park  
Lower Cookham Road  
Maidenhead  
Berkshire SL6 8YA  
United Kingdom  
Tel: 0628-585000  
Fax: 0628-778322

Hitachi Asia Pte. Ltd.  
16 Collyer Quay #20-00  
Hitachi Tower  
Singapore 0104  
Tel: 535-2100  
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Hitachi Asia (Hong Kong) Ltd.  
Unit 706, North Tower,  
World Finance Centre,  
Harbour City, Canton Road  
Tsim Sha Tsui, Kowloon  
Hong Kong  
Tel: 27359218  
Fax: 27306071

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### Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Jun. 20, 1997	Initial issue		

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