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## S P E C I F I C A T I O N S

Product Type 8M Flash File Memory

### L H 2 8 F 0 0 8 S A T - K 8 5

Model No. (LHF08S17)

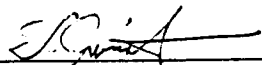
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## LH28F008SAT-K85 8 MBIT (1 MBIT x 8) FLASH MEMORY

### 1. FEATURES

- **High-Density Symmetrically Blocked Architecture**
  - Sixteen 64 KByte Blocks
- **Extended Cycling Capability**
  - 100,000 Block Erase Cycles
  - 1.6 Million Block Erase Cycles per Chip
- **Automated Byte Write and Block Erase**
  - Command User Interface
  - Status Register
- **System Performance Enhancements**
  - $\overline{RY}/\overline{BY}$  Status Output
  - Erase Suspend Capability
- **Deep-Powerdown Mode**
  - 16  $\mu$ A  $I_{CC}$  Maximum
- **Very High-Performance Read**
  - 85 ns Maximum Access Time
- **SRAM-Compatible Write Interface**
- **Hardware Data Protection Feature**
  - Erase/Write Lockout during Power Transitions
- **Industry Standard Packaging**
  - 40-Lead TSOP
- **ETOX™\* V Nonvolatile Flash Technology**
  - 12V Byte Write/Block Erase
- **Not designed or rated as radiation hardened**

SHARP's LH28F008SAT-K85 8 Mbit Flash Memory is the highest density nonvolatile read/write solution for solid state storage. The LH28F008SAXX-KXXX's extended cycling, symmetrically blocked architecture, fast access time, write automation and low power consumption provide a more reliable, lower power, lighter weight and higher performance alternative to traditional rotating disk technology. The LH28F008SAT-K85 brings new capabilities to portable computing. Application and operating system software stored in resident flash memory arrays provide instant-on rapid execute-in-place and protection from obsolescence through in-system software updates. Resident software also extends system battery life and increases reliability by reducing disk drive accesses.

For high density data acquisition applications, the LH28F008SAT-K85 offers a more cost-effective and reliable alternative to SRAM and battery. Traditional high density embedded applications, such as telecommunications, can take advantage of the LH28F008SAXX-KXXX's nonvolatility, blocking and minimal system code requirements for flexible firmware and modular software designs.

The LH28F008SAT-K85 is offered in 40-lead TSOP (standard) package. Pin assignments simplify board layout when integrating multiple devices in a flash memory array or subsystem. This device uses an integrated Command User Interface and state machine for simplified block erasure and byte write. The LH28F008SAT-K85 memory map consists of 16 separately erasable 64 Kbyte blocks.

SHARP's LH28F008SAT-K85 employs advanced CMOS circuitry for systems requiring low power consumption and noise immunity. Its 85 ns access time provides superior performance when compared with magnetic storage media. A deep powerdown mode lowers power consumption to 80  $\mu$ W maximum thru  $V_{CC}$ , crucial in portable computing, handheld instrumentation and other low-power applications. The  $\overline{RP}$  power control input also provides absolute data protection during system powerup/down.

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\* ETOX is a trademark of Intel Corporation.

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## 2. PRODUCT OVERVIEW

The LH28F008SAT-K85 is a high-performance **8 Mbit** (8,388,608 bit) memory organized as **1 Mbyte** (1,048,576 bytes) of 8 bits each. **Sixteen 64 KByte** (65,536 byte) **blocks** are included on the LH28F008SAT-K85. A memory map is shown in Figure 4 of this specification. A block erase operation erases one of the sixteen blocks of memory in typically **1.6 seconds**, independent of the remaining blocks. Each block can be independently erased and written **100,000 cycles**. **Erase Suspend** mode allows system software to suspend block erase to read data or execute code from any other block of the LH28F008SAT-K85.

The LH28F008SAT-K85 is available in the **40-lead TSOP** (Thin Small Outline Package, 1.2 mm thick) package. Pinouts are shown in Figure 2 of this specification.

The **Command User Interface** serves as the interface between the microprocessor or microcontroller and the internal operation of the LH28F008SAT-K85.

**Byte Write and Block Erase Automation** allow byte write and block erase operations to be executed using a two-write command sequence to the Command User Interface. The internal **Write State Machine (WSM)** automatically executes the algorithms and timings necessary for byte write and block erase operations, including verifications, thereby unburdening the microprocessor or microcontroller. Writing of memory data is performed in byte increments typically within **8  $\mu$ s**.  **$I_{pp}$  byte write and block erase currents are 10 mA typical, 30 mA maximum.  $V_{pp}$  byte write and block erase voltage is 11.4V to 12.6V.**

The **Status Register** indicates the status of the WSM and when the WSM successfully completes the desired byte write or block erase operation.

The  **$R\bar{Y}/\bar{B}Y$**  output gives an additional indicator of WSM activity, providing capability for both hardware signal of status (versus software polling) and status masking (interrupt masking for background erase, for example). Status polling using  **$R\bar{Y}/\bar{B}Y$**  minimizes both CPU overhead and system power consumption. When low,  **$R\bar{Y}/\bar{B}Y$**  indicates that the WSM is performing a block erase or byte write operation.  **$R\bar{Y}/\bar{B}Y$**  high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode.

Maximum access time is **85 ns ( $t_{ACC}$ )** over the commercial temperature range (0°C to +70°C) and over  $V_{CC}$  supply voltage range (4.5V to 5.5V and 4.75V to 5.25V).  **$I_{CC}$  active current (CMOS Read) is 20mA typical, 35 mA maximum at 8 MHz.**

When the  **$\bar{C}E$**  and  **$\bar{R}P$**  pins are at  $V_{CC}$ , the  **$I_{CC}$  CMOS Standby** mode is enabled.

A **Deep Powerdown** mode is enabled when the  **$\bar{R}P$**  pin is at GND, minimizing power consumption and providing write protection.  **$I_{CC}$  current** in deep powerdown is **16  $\mu$ A maximum**. Reset time of 400 ns is required from  **$\bar{R}P$**  switching high until outputs are valid to read attempts. Equivalently, the device has a wake time of 1  $\mu$ s from  **$\bar{R}P$**  high until writes to the Command User Interface are recognized by the LH28F008SAT-K85. With  **$\bar{R}P$**  at GND, the WSM is reset and the Status Register is cleared.

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit. In case of reprogramming "0" to the data which has been programmed "1".

- Program "0" for the bit in which you want to change data from "1" to "0".

- Program "1" for the bit which has already been programmed "0".

For example, changing data from "10111101" to "10111100" requires "11111110" programming.

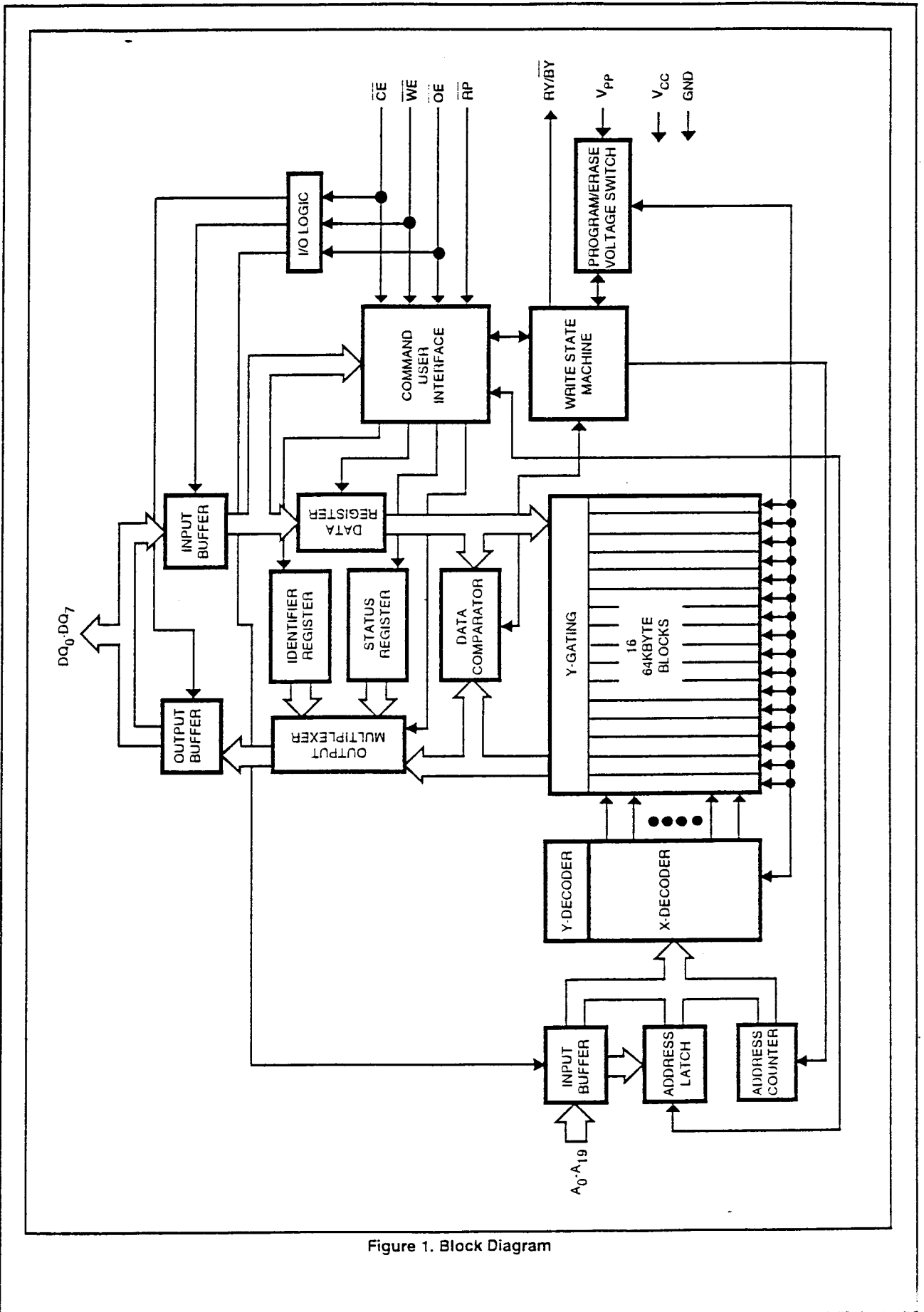


Figure 1. Block Diagram

Table 1. Pin Description

Symbol	Type	Name and Function
$A_0$ - $A_{19}$	INPUT	<b>ADDRESS INPUTS:</b> for memory addresses. Addresses are internally latched during a write cycle.
$DQ_0$ - $DQ_7$	INPUT/OUTPUT	<b>DATA INPUT/OUTPUTS:</b> Inputs data and commands during Command User Interface write cycles; outputs data during memory array, Status Register and Identifier read cycles. The data pins are active high and float to tri-state off when the chip is deselected or the outputs are disabled. Data is internally latched during a write cycle.
$\overline{CE}$	INPUT	<b>CHIP ENABLE:</b> Activates the device's control logic input buffers decoders, and sense amplifiers. $\overline{CE}$ is active low; $\overline{CE}$ high deselects the memory device and reduces power consumption to standby levels.
$\overline{RP}$	INPUT	<b>RESET/POWERDOWN:</b> Puts the device in deep powerdown mode. $\overline{RP}$ is active low; $\overline{RP}$ high gates normal operation. $\overline{RP}$ also locks out block erase or byte write operations when active low, providing data protection during power transitions. $\overline{RP}$ active resets internal automation. Exit from Deep Powerdown sets device to read-array mode.
$\overline{OE}$	INPUT	<b>OUTPUT ENABLE:</b> Gates the device's outputs through the data buffers during a read cycle. $\overline{OE}$ is active low.
$\overline{WE}$	INPUT	<b>WRITE ENABLE:</b> Controls writes to the Command User Interface and array blocks. $\overline{WE}$ is active low. Addresses and data are latched on the rising edge of the $\overline{WE}$ pulse.
$RY/\overline{BY}$	OUTPUT	<b>READY/<math>\overline{BUSY}</math>:</b> Indicates the status of the internal Write State Machine. When low, it indicates that the WSM is performing a block erase or byte write operation. $RY/\overline{BY}$ high indicates that the WSM is ready for new commands, block erase is suspended or the device is in deep powerdown mode. $RY/\overline{BY}$ is always active and does NOT float to tri-state off when the chip is deselected or data outputs are disabled.
$V_{PP}$		<b>BLOCK ERASE/BYTE WRITE POWER SUPPLY:</b> for erasing blocks of the array or writing bytes of each block. <b>NOTE:</b> With $V_{PP} < V_{PPLMAX}$ , memory contents cannot be altered.
$V_{CC}$		<b>DEVICE POWER SUPPLY (5V±10%, 5V±5%)</b>
GND		<b>GROUND</b>

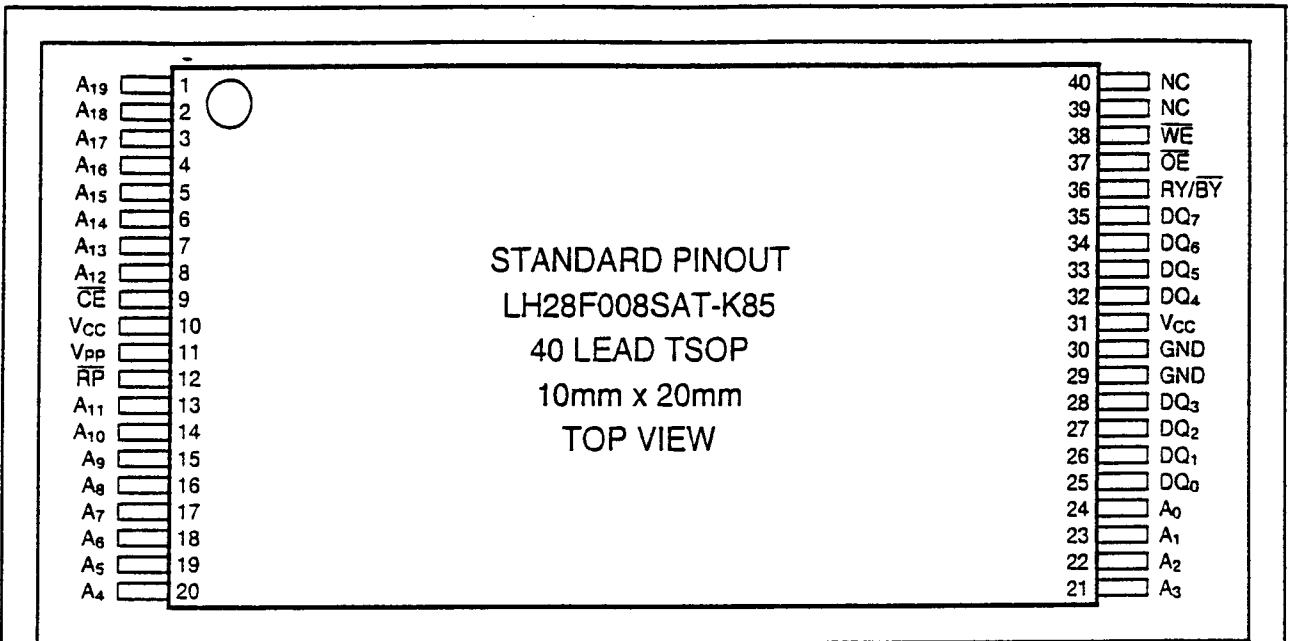


Figure 2. TSOP Lead Configuration



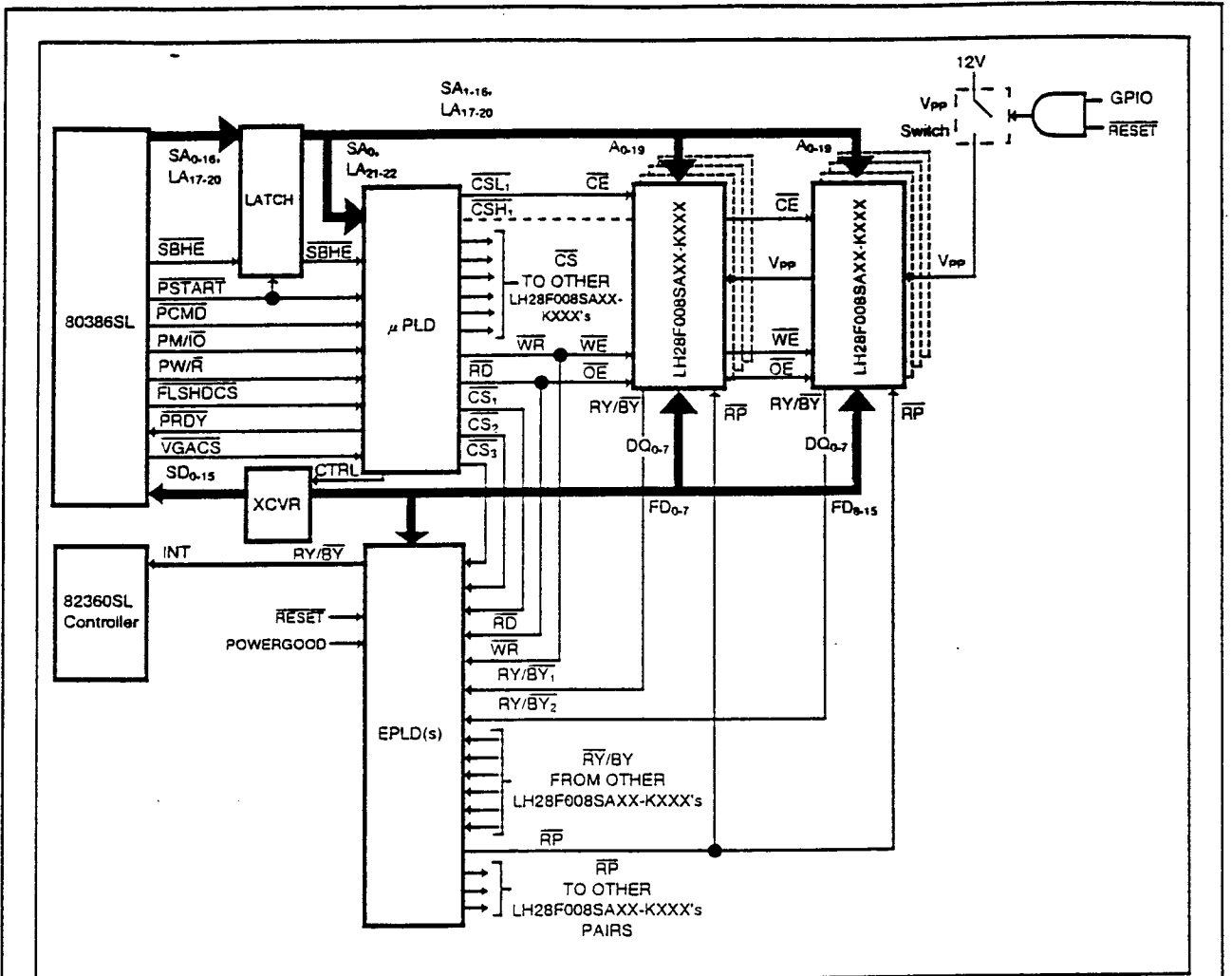


Figure 3. LH28F008SAXX-KXXX Array Interface to 386SL Microprocessor Superset through PI Bus (Including RY/  
 $\bar{B}Y$  Masking and Selective Powerdown), for DRAM Backup during System SUSPEND, Resident O/S and  
 Applications and Motherboard Solid-State Disk.

### 3. PRINCIPLES OF OPERATION

The LH28F008SAT-K85 includes on-chip write automation to manage write and erase functions. The Write State Machine allows for: 100% TTL-level control inputs; fixed power supplies during block erasure and byte write; and minimal processor overhead with SRAM-like interface timings.

After initial device powerup, or after return from deep powerdown mode (see Bus Operations), the LH28F008SAT-K85 functions as a read-only memory. Manipulation of external memory-control pins allow array read, standby and output disable operations. Both Status Register and intelligent identifiers can also be accessed through the Command User Interface when  $V_{PP}=V_{PPL}$ .

This same subset of operations is also available when high voltage is applied to the  $V_{PP}$  pin. In addition, high voltage on  $V_{PP}$  enables successful block erasure and byte writing of the device. All functions associated with altering memory contents — byte write, block erase, status and intelligent identifier — are accessed via the Command User Interface and verified thru the Status Register.

Commands are written using standard microprocessor write timings. Command User Interface contents serve as input to the WSM, which controls the block erase and byte write circuitry. Write cycles also internally latch addresses and data needed for byte write or block erase operations. With the appropriate command written to the register, standard microprocessor read timings output array data, access the intelligent identifier codes, or output byte write and block erase status for verification.

Interface software to initiate and poll progress of internal byte write and block erase can be stored in any of the LH28F008SAT-K85 blocks. This code is copied to, and executed from, system RAM during actual flash memory update. After successful completion of byte write and/or block erase, code/data reads from the LH28F008SAT-K85 are again possible via the Read Array command. Erase suspend/resume capability allows system software to suspend block erase to read data and execute code from any other block.

FFFFF	64 Kbyte Block
F0000	64 Kbyte Block
EFFFF	64 Kbyte Block
E0000	64 Kbyte Block
DFFFF	64 Kbyte Block
D0000	64 Kbyte Block
CFFFF	64 Kbyte Block
C0000	64 Kbyte Block
BFFFF	64 Kbyte Block
B0000	64 Kbyte Block
AFFFF	64 Kbyte Block
A0000	64 Kbyte Block
9FFFF	64 Kbyte Block
90000	64 Kbyte Block
8FFFF	64 Kbyte Block
80000	64 Kbyte Block
7FFFF	64 Kbyte Block
70000	64 Kbyte Block
6FFFF	64 Kbyte Block
60000	64 Kbyte Block
5FFFF	64 Kbyte Block
50000	64 Kbyte Block
4FFFF	64 Kbyte Block
40000	64 Kbyte Block
3FFFF	64 Kbyte Block
30000	64 Kbyte Block
2FFFF	64 Kbyte Block
20000	64 Kbyte Block
1FFFF	64 Kbyte Block
10000	64 Kbyte Block
0FFFF	64 Kbyte Block
00000	64 Kbyte Block

Figure 4. Memory Map

#### Command User Interface and Write Automation

An on-chip state machine controls block erase and byte write, freeing the system processor for other tasks. After receiving the Erase Setup and Erase Confirm commands, the state machine controls block pre-conditioning and erase, returning progress via the Status Register and  $\overline{RY/BY}$  output. Byte write is similarly controlled, after destination address and expected data are supplied. The program and erase algorithms of past standard Flash memories are now regulated by the state machine, including pulse repetition where required and internal verification and margining of data.

### Data Protection

Depending on the application, the system designer may choose to make the  $V_{PP}$  power supply switchable (available only when memory byte writes/block erases are required) or hardwired to  $V_{PPH}$ . When  $V_{PP}=V_{PPL}$ , memory contents cannot be altered. The LH28F008SAT-K85 Command User Interface architecture provides protection from unwanted byte write or block erase operations even when high voltage is applied to  $V_{PP}$ . Additionally, all functions are disabled whenever  $V_{CC}$  is below the write lockout voltage  $V_{LKO}$ , or when  $\overline{RP}$  is at  $V_{IL}$ . The LH28F008SAT-K85 accommodates either design practice and encourages optimization of the processor-memory interface.

The two-step byte write/block erase Command User Interface write sequence provides additional software write protection.

### 4. BUS OPERATION

Flash memory reads, erases and writes in-system via the local CPU. All bus cycles to or from the flash memory conform to standard microprocessor bus cycles.

#### Read

The LH28F008SAT-K85 has three read modes. The memory can be read from any of its blocks, and information can be read from the intelligent identifier or Status Register.  $V_{PP}$  can be at either  $V_{PPL}$  or  $V_{PPH}$ .

The first task is to write the appropriate read mode command to the Command User Interface (array, intelligent identifier, or Status Register). The LH28F008SAT-K85 automatically resets to Read Array mode upon initial device powerup or after exit from deep powerdown. The LH28F008SAT-K85 has four control pins, two of which must be logically active to obtain data at the outputs. Chip Enable ( $\overline{CE}$ ) is the device selection control, and when active enables the selected memory device. Output Enable ( $\overline{OE}$ ) is the data input/output (DQ<sub>0</sub>-DQ<sub>7</sub>) direction control, and when active drives data from the selected memory onto the I/O bus.  $\overline{RP}$  and  $\overline{WE}$  must also be at  $V_{IH}$ . Figure 8 illustrates read bus cycle waveforms.

#### Output Disable

With  $\overline{OE}$  at a logic-high level ( $V_{IH}$ ), the device outputs are disabled. Output pins (DQ<sub>0</sub>-DQ<sub>7</sub>) are placed in a high-impedance state.

#### Standby

$\overline{CE}$  at a logic-high level ( $V_{IH}$ ) places the LH28F008SAT-K85 in standby mode. Standby operation disables much of the LH28F008SAXX-KXXX's circuitry and substantially reduces device power consumption. The outputs (DQ<sub>0</sub>-DQ<sub>7</sub>) are placed in a high-impedance state independent of the status of  $\overline{OE}$ . If the LH28F008SAT-K85 is deselected during block erase or byte write, the device will continue functioning and consuming normal active power until the operation completes.

Table 2. Bus Operations

Mode	Notes	$\overline{RP}$	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$A_0$	$V_{PP}$	DQ <sub>0-7</sub>	RY/BY
Read	1,2,3	$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	X	X	D <sub>OUT</sub>	X
Output Disable	3	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	X	X	High Z	X
Standby	3	$V_{IH}$	$V_{IH}$	X	X	X	X	High Z	X
Deep PowerDown		$V_{IL}$	X	X	X	X	X	High Z	$V_{OH}$
Intelligent Identifier (Mfr)		$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	X	89H	$V_{OH}$
Intelligent Identifier (Device)		$V_{IH}$	$V_{IL}$	$V_{IL}$	$V_{IH}$	$V_{IH}$	X	A2H	$V_{OH}$
Write	3,4,5	$V_{IH}$	$V_{IL}$	$V_{IH}$	$V_{IL}$	X	X	D <sub>IN</sub>	X

#### NOTES:

1. Refer to DC Characteristics. When  $V_{PP}=V_{PPL}$ , memory contents can be read but not written or erased.
2. X can be  $V_{IL}$  or  $V_{IH}$  for control pins and addresses, and  $V_{PPL}$  or  $V_{PPH}$  for  $V_{PP}$ . See DC Characteristics for  $V_{OPL}$  and  $V_{OCH}$  voltages.
3. RY/ $\overline{BY}$  is  $V_{OL}$  when the Write State Machine is executing internal block erase or byte write algorithms. It is  $V_{OH}$  when the WSM is not busy, in Erase Suspend mode or deep powerdown mode.
4. Command writes involving block erase or byte write are only successfully executed when  $V_{PP}=V_{PPH}$ .
5. Refer to Table 3 for valid D<sub>IN</sub> during a write operation.

### Deep Power-Down

The LH28F008SAT-K85 offers a deep powerdown feature, entered when  $\overline{RP}$  is at  $V_{IL}$ . Current draw thru  $V_{CC}$  is 16  $\mu$ A maximum in deep powerdown mode, with current draw through  $V_{PP}$  maximal 5 $\mu$ A. During read modes,  $\overline{RP}$ -low de-selects the memory, places output drivers in a high-impedance state and turns off all internal circuits. The LH28F008SAT-K85 requires time  $t_{PHQV}$  (see AC Characteristics-Read-Only Operations) after return from powerdown until initial memory access outputs are valid. After this wakeup interval, normal operation is restored. The Command User Interface is reset to Read Array, and the upper 5bits of the Status Register are cleared to value 10000, upon return to normal operation.

During block erase or byte write modes,  $\overline{RP}$  low will abort either operation. Memory contents of the block being altered are no longer valid as the data will be partially written or erased. Time  $t_{PHWL}$  after  $\overline{RP}$  goes to logic-high ( $V_{IH}$ ) is required before another command can be written.

### Intelligent Identifier Operation

The intelligent identifier operation outputs the manufacturer code, 89H; and the device code, A2H for the LH28F008SAT-K85. The system CPU can then automatically match the device with its proper block erase and byte write algorithms.

The manufacturer- and device-codes are read via the Command User Interface. Following a write of 90H to the Command User Interface, a read from address location 00000H outputs the manufacturer code (89H). A read from address 00001H outputs the device code (A2H). It is not necessary to have high voltage applied to  $V_{PP}$  to read the intelligent identifiers from the Command User Interface.

### Write

Writes to the Command User Interface enable reading of device data and intelligent identifiers. They also control inspection and clearing of the Status Register. Additionally, when  $V_{PP}=V_{PPH}$ , the Command User Interface controls block erasure and byte write. The contents of the interface register serve as input to the internal state machine.

Table 3. Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Operation	Address	Data	Operation	Address	Data
Read Array/Reset	1	1	Write	X	FFH			
Intelligent Identifier	3	2,3,4	Write	X	90H	Read	IA	IID
Read Status Register	2	3	Write	X	70H	Read	X	SRD
Clear Status Register	1		Write	X	50H			
Erase Setup/Erase Confirm	2	2	Write	BA	20H	Write	BA	D0H
Erase Suspend/Erase Resume	2		Write	X	80H	Write	X	D0H
Byte Write Setup/Write	2	2,3,5	Write	WA	40H	Write	WA	WD
Alternate Byte Write Setup/Write	2	2,3,5	Write	WA	10H	Write	WA	WD

#### NOTES:

1. Bus operations are defined in Table 2.
2. IA=Identifier Address: 00H for manufacturer code, 01H for device code.  
BA=Address within the block being erased.  
WA=Address of memory location to be written.
3. SRD=Data read from Status Register. See Table 4 for a description of the Status Register bits.  
WD=Data to be written at location WA. Data is latched on the rising edge of  $\overline{WE}$ .  
IID=Data read from intelligent identifiers.
4. Following the intelligent identifier command, two read operations access manufacture and device codes.
5. Either 40H or 10H are recognized by the WSM as the Byte Write Setup command.
6. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

The Command User Interface itself does not occupy an addressable memory location. The interface register is a latch used to store the command and address and data information needed to execute the command. Erase Setup and Erase Confirm commands require both appropriate command data and an address within the block to be erased. The Byte Write Setup command requires both appropriate command data and the address of the location to be written, while the Byte Write command consists of the data to be written and the address of the location to be written.

The Command User Interface is written by bringing  $\overline{WE}$  to a logic-low level ( $V_{IL}$ ) while  $\overline{CE}$  is low. Addresses and data are latched on the rising edge of  $\overline{WE}$ . Standard microprocessor write timings are used.

Refer to AC Write Characteristics and the AC Waveforms for Write Operations, Figure 9, for specific timing parameters.

## 5. COMMAND DEFINITIONS

When  $V_{PPL}$  is applied to the  $V_{PP}$  pin, read operations from the Status Register, intelligent identifiers, or array blocks are enabled. Placing  $V_{PPH}$  on  $V_{PP}$  enables successful byte write and block erase operations as well.

Device operations are selected by writing specific commands into the Command User Interface. Table 3 defines the LH28F008SAT-K85 commands.

### Read Array Command

Upon initial device powerup and after exit from deep powerdown mode, the LH28F008SAT-K85 defaults to Read Array mode. This operation is also initiated by writing FFH into the Command User Interface. Microprocessor read cycles retrieve array data. The device remains enabled for reads until the Command User Interface contents are altered. Once the internal Write State Machine has started a block erase or byte write operation, the device will not recognize the Read Array command, until the WSM has completed its operation. The Read Array command is functional when  $V_{PP}=V_{PPL}$  or  $V_{PPH}$ .

### Intelligent Identifier Command

The LH28F008SAT-K85 contains an intelligent identifier operation, initiated by writing 90H into the Command User Interface. Following the command write, a read cycle from address 00000H retrieves the manufacturer code of 89H. A read cycle from address 00001H returns the device code of A2H. To terminate the operation, it is necessary to write another valid command into the register. Like the Read Array command, the intelligent identifier command is functional when  $V_{PP}=V_{PPL}$  or  $V_{PPH}$ .

Table 4. Status Register Definitions

WSMS	ESS	ES	BWS	VPPS	R	R	R
7	6	5	4	3	2	1	0

**SR. 7 = WRITE STATE MACHINE STATUS (WSMS)**  
 1 = Ready  
 0 = Busy

**SR. 6 = ERASE SUSPEND STATUS (ESS)**  
 1 = Erase Suspended  
 0 = Erase in Progress/Completed

**SR. 5 = ERASE STATUS (ES)**  
 1 = Error in Block Erasure  
 0 = Successful Block Erase

**SR. 4 = BYTE WRITE STATUS (BWS)**  
 1 = Error in Byte Write  
 0 = Successful Byte Write

**SR. 3 =  $V_{PP}$  STATUS (VPPS)**  
 1 =  $V_{PP}$  Low Detect: Operation Abort  
 0 =  $V_{PP}$  OK

**SR. 2-0 = RESERVED FOR FUTURE (R) ENHANCEMENTS**

**NOTES:**

RY/ $\overline{BY}$  or the Write State Machine Status bit must first be checked to determine byte write or block erase completion, before the Byte Write or Erase Status bit are checked for success. If the Byte Write AND Erase Status bits are set to "1"s during a block erase attempt, an improper command sequence was entered. Attempt the operation again.

If  $V_{PP}$  low status is detected, the Status Register must be cleared before another byte write or block erase operation is attempted. The  $V_{PP}$  Status bit, unlike an A/D converter, does not provide continuous indication of  $V_{PP}$  level. The WSM interrogates the  $V_{PP}$  level only after the byte write or block erase command sequences have been entered and informs the system if  $V_{PP}$  has not been switched on. The  $V_{PP}$  Status bit is not guaranteed to report accurate feedback between  $V_{PDL}$  and  $V_{PPH}$ .

These bits are reserved for future use and should be masked out when polling the Status Register.

### Read Status Register Command

The LH28F008SAT-K85 contains a Status Register which may be read to determine when a byte write or block erase operation is complete, and whether that operation completed successfully. The Status Register may be read at any time by writing the Read Status Register command (70H) to the Command User Interface. After writing this command, all subsequent read operations output data from the Status Register, until another valid command is written to the Command User Interface. The contents of the Status Register are latched on the falling edge of  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs last in the read cycle.  $\overline{OE}$  or  $\overline{CE}$  must be toggled to  $V_{IH}$  before further reads to update the Status Register latch. The Read Status Register command functions when  $V_{PP}=V_{PPL}$  or  $V_{PPH}$ .

### Clear Status Register Command

The Erase Status and Byte Write Status bits are set to "1"s by the Write State Machine and can only be reset by the Clear Status Register Command. These bits indicate various failure conditions (see Table 4). By allowing system software to control the resetting of these bits, several operations may be performed (such as cumulatively writing several bytes or erasing multiple blocks in sequence). The Status Register may then be polled to determine if an error occurred during that sequence. This adds flexibility to the way the device may be used.

Additionally, the  $V_{PP}$  Status bit (SR.3) MUST be reset by system software before further byte writes or block erases are attempted. To clear the Status Register, the Clear Status Register command (50H) is written to the Command User Interface. The Clear Status Register command is functional when  $V_{PP}=V_{PPL}$  or  $V_{PPH}$ .

### Erase Setup/Erase Confirm Commands

Erase is executed one block at a time, initiated by a two-cycle command sequence. An Erase Setup command (20H) is first written to the Command User Interface, followed by the Erase Confirm command (D0H). These commands require both appropriate sequencing and an address within the block to be erased to FFH. Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After the two-command erase sequence is written to it, the LH28F008SAT-K85 automatically outputs Status Register data when read (see Figure 6; Block Erase Flowchart). The CPU can detect the completion of the erase event by ana-

lyzing the output of the RY/ $\overline{BY}$  pin, or the WSM Status bit of the Status Register.

When erase is completed, the Erase Status bit should be checked. If erase error is detected, the Status Register should be cleared. The Command User Interface remains in Read Status Register mode until further commands are issued to it.

This two-step sequence of set-up followed by execution ensures that memory contents are not accidentally erased. Also, reliable block erasure can only occur when  $V_{PP}=V_{PPH}$ . In the absence of this high voltage, memory contents are protected against erasure. If block erase is attempted while  $V_{PP}=V_{PPL}$ , the  $V_{PP}$  Status bit will be set to "1". Erase attempts while  $V_{PPL}<V_{PP}<V_{PPH}$  produce spurious results and should not be attempted.

### Erase Suspend/Erase Resume Commands

The Erase Suspend command allows block erase interruption in order to read data from another block of memory. Once the erase process starts, writing the Erase Suspend command (B0H) to the Command User Interface requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The LH28F008SAT-K85 continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended (both will be set to "1"). RY/ $\overline{BY}$  will also transition to  $V_{OH}$ .

At this point, a Read Array command can be written to the Command User Interface to read data from blocks other than that which is suspended. The only other valid commands at this time are Read Status Register (70H) and Erase Resume (D0H), at which time the WSM will continue with the erase process. The Erase Suspend Status and WSM Status bits of the Status Register will be automatically cleared and RY/ $\overline{BY}$  will return to  $V_{OL}$ . After the Erase Resume command is written to it, the LH28F008SAT-K85 automatically outputs Status Register data when read (see Figure 7; Erase Suspend/Resume Flowchart).  $V_{PP}$  must remain at  $V_{PPH}$  while the LH28F008SAT-K85 is in Erase Suspend.

### Byte Write Setup/Write Commands

Byte write is executed by a two-command sequence. The Byte Write Setup command (40H or 10H) is written to the Command User Interface, followed by a second write specifying the address and data (latched on the rising edge of  $\overline{WE}$ ) to be written. The WSM then takes over, controlling the byte write and write verify algorithms internally. After the two-command byte write sequence is written to it, the LH28F008SAT-K85 automatically outputs Status Register data when read (see Figure 5; Byte Write Flowchart). The CPU can detect the completion of the byte write event by analyzing the output of the RY/ $\overline{BY}$  pin, or the WSM Status bit of the Status Register. Only the Read Status Register command is valid while byte write is active.

When byte write is complete, the Byte Write Status bit should be checked. If byte write error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for "1"s that do not successfully write to "0"s. The Command User Interface remains in Read Status Register mode until further commands are issued to it. If byte write is attempted while  $V_{PP}=V_{PPL}$ , the  $V_{PP}$  Status bit will be set to "1". Byte write attempts while  $V_{PPL}<V_{PP}<V_{PPH}$  produce spurious results and should not be attempted.

### 6. EXTENDED BLOCK ERASE/BYTE WRITE CYCLING

The LH28F008SAT-K85 is designed for 100,000 byte write/block erase cycles on each of the sixteen 64 Kbyte blocks. Low electric fields, advanced oxides and minimal oxide area per cell subjected to the tunneling electric field combine to greatly reduce oxide stress and the probability of failure. A 20 Mbyte solid-state drive using an array of LH28F008SAXX-KXXX's has a MTBF (Mean Time Between Failure) of 33.3 million hours<sup>(1)</sup>, over 600 times more reliable than equivalent rotating disk technology.

### 7. AUTOMATED BYTE WRITE

The LH28F008SAT-K85 integrates the Quick-Pulse programming algorithm using the Command User Interface, Status Register and Write State Machine (WSM). On-chip integration dramatically simplifies system software and provides processor interface timings to the Command User Interface and Status Register. WSM operation, internal verify and  $V_{PP}$  high voltage presence are monitored and reported via the RY/ $\overline{BY}$  output and appropriate Status Register bits. Figure 5 shows a system software flowchart for device byte write. The entire sequence is performed with  $V_{PP}$  at  $V_{PPH}$ .

Byte write abort occurs when  $\overline{RP}$  transitions to  $V_{IL}$ , or  $V_{PP}$  drops to  $V_{PPL}$ . Although the WSM is halted, byte data is partially written at the location where byte write was aborted. Block erasure, or a repeat of byte write, is required to initialize this data to a known value.

### 8. AUTOMATED BLOCK ERASE

As above, the Quick-Erase algorithm is now implemented internally, including all preconditioning of block data. WSM operation, erase success and  $V_{PP}$  high voltage presence are monitored and reported through RY/ $\overline{BY}$  and the Status Register. Additionally, if a command other than Erase Confirm is written to the device following Erase Setup, both the Erase Status and Byte Write Status bits will be set to "1"s. When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 6 shows a system software flowchart for block erase.

Erase typically takes 1.6 seconds per block. The Erase Suspend/Erase Resume command sequence allows suspension of this erase operation to read data from a block other than that in which erase is being performed. A system software flowchart is shown in Figure 7.

The entire sequence is performed with  $V_{PP}$  at  $V_{PPH}$ . Abort occurs when  $\overline{RP}$  transitions to  $V_{IL}$  or  $V_{PP}$  falls to  $V_{PPL}$ , while erase is in progress. Block data is partially erased by this operation, and a repeat of erase is required to obtain a fully erased block.

### 9. DESIGN CONSIDERATIONS

#### Three-Line Output Control

The LH28F008SAT-K85 will often be used in large memory arrays. SHARP provides three control inputs to accommodate multiple memory connections. Three-line control provides for:

- lowest possible memory power dissipation
- complete assurance that data bus contention will not occur

To efficiently use these control inputs, an address decoder should enable  $\overline{CE}$  while  $\overline{OE}$  should be connected to all memory devices and the system's  $\overline{READ}$  control line. This assures that only selected memory devices have active outputs while deselected memory devices are in Standby Mode. Finally,  $\overline{RP}$  should either be tied to the system  $\overline{RESET}$ , or connected to  $V_{CC}$  if unused.

(1) Assumptions: 10 Kbyte file written every 10 minutes. (20 Mbyte array)/(10 Kbyte file) = 2,000 file writes before erase required.  
 (2000 files writes/erase) x (100,000 cycles per LH28F008SAT-K85 block) = 200 million file writes.  
 (200 x 10<sup>6</sup> file writes) x (10 min/write) x (1 hr/60 min) = 33.3 x 10<sup>6</sup> MTBF

## RY/ $\overline{\text{BY}}$ and $\overline{\text{BY}}$ Write/Block Erase Polling

RY/ $\overline{\text{BY}}$  is a full CMOS output that provides a hardware method of detecting byte write and block erase completion. It transitions low time  $t_{\text{WHRL}}$  after a write or erase command sequence is written to the LH28F008SAT-K85, and returns to  $V_{\text{OH}}$  when the WSM has finished executing the internal algorithm.

RY/ $\overline{\text{BY}}$  can be connected to the interrupt input of the system CPU or controller. It is active at all times, not tristated if the LH28F008SAT-K85  $\overline{\text{CE}}$  or  $\overline{\text{OE}}$  inputs are brought to  $V_{\text{IH}}$ . RY/ $\overline{\text{BY}}$  is also  $V_{\text{OH}}$  when the device is in Erase Suspend or deep powerdown modes.

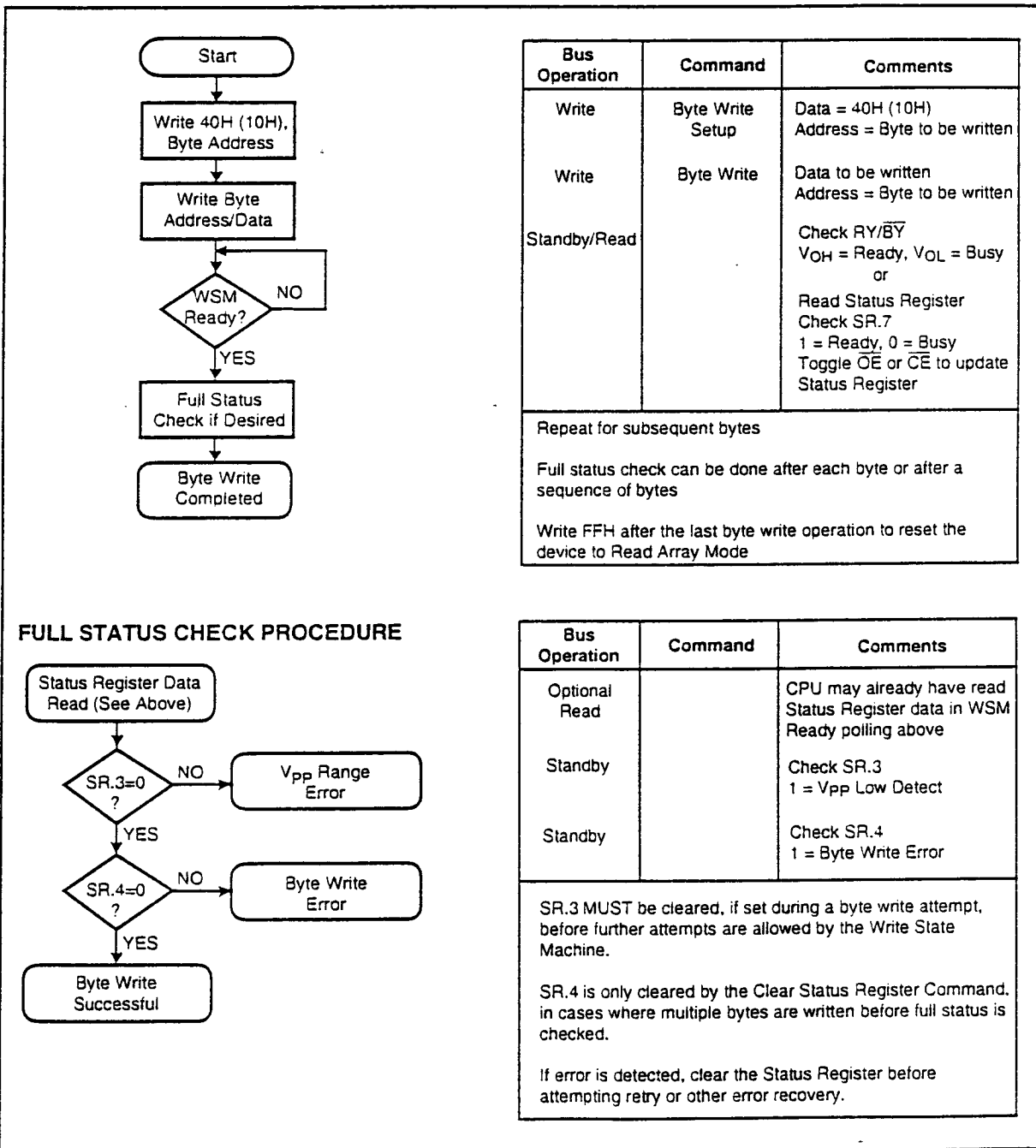
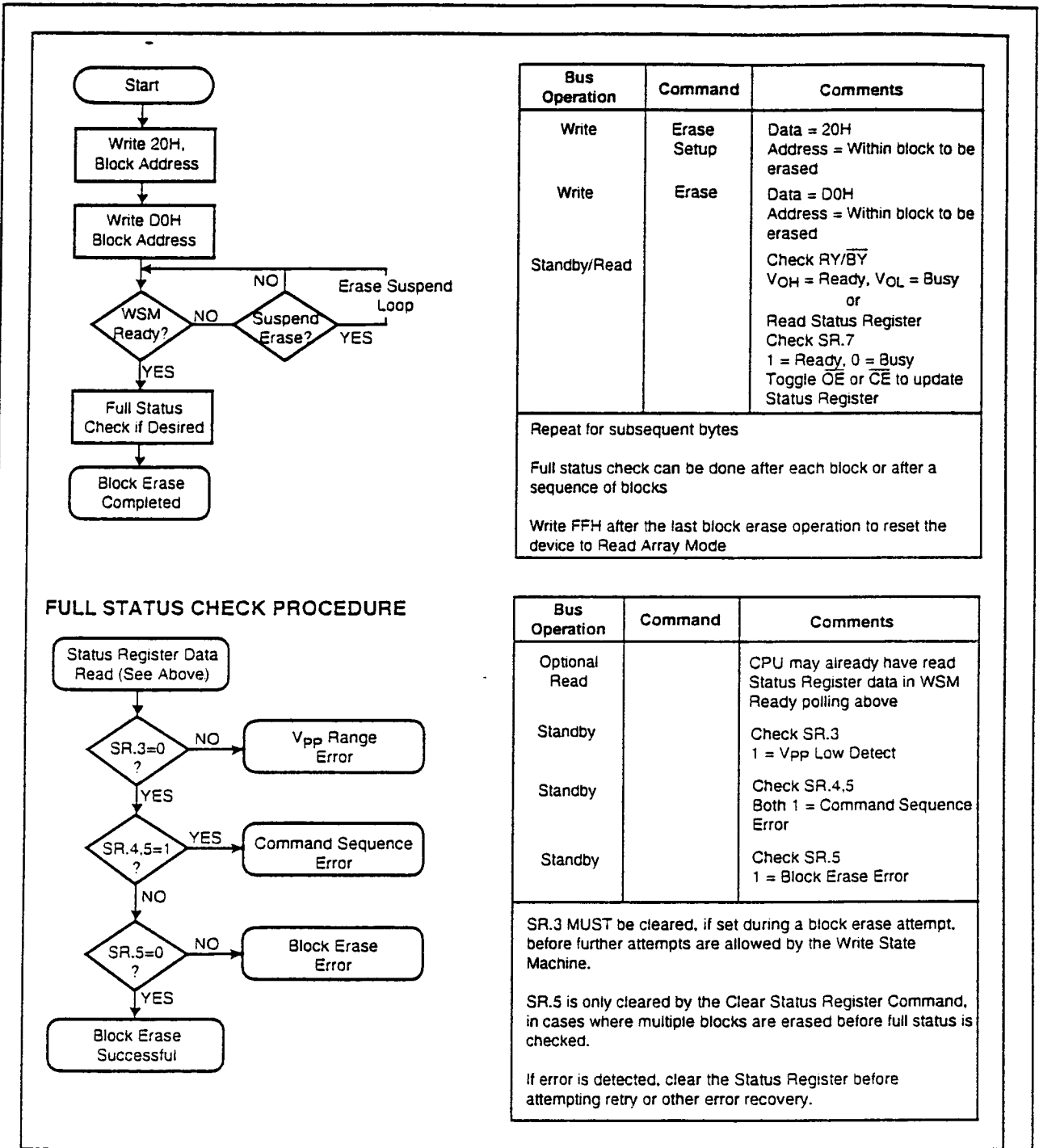


Figure 5. Automated Byte Write Flowchart





Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Address = Within block to be erased
Write	Erase	Data = D0H Address = Within block to be erased
Standby/Read		Check $\overline{RY}/\overline{BY}$ $V_{OH}$ = Ready, $V_{OL}$ = Busy or Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle OE or CE to update Status Register

Repeat for subsequent bytes

Full status check can be done after each block or after a sequence of blocks

Write FFH after the last block erase operation to reset the device to Read Array Mode

Bus Operation	Command	Comments
Optional Read		CPU may already have read Status Register data in WSM Ready polling above
Standby		Check SR.3 1 = Vpp Low Detect
Standby		Check SR.4.5 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during a block erase attempt, before further attempts are allowed by the Write State Machine.

SR.5 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 6. Automated Block Erase Flowchart

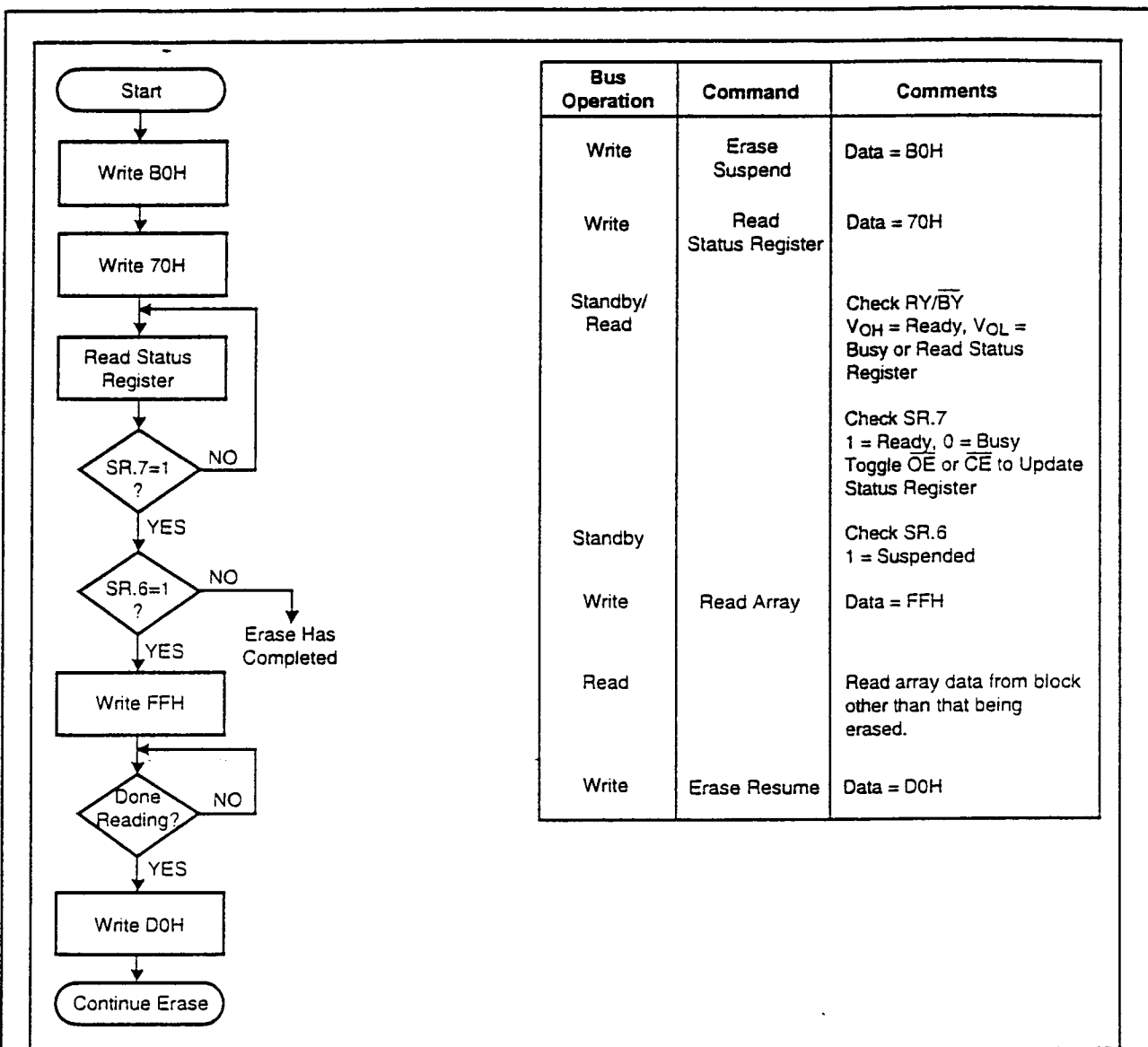


Figure 7. Erase Suspend/Resume Flowchart

### Power Supply Decoupling

Flash memory power switching characteristics require careful device decoupling. System designers are interested in 3 supply current issues: standby current levels ( $I_{\text{SB}}$ ), active current levels ( $I_{\text{CC}}$ ) and transient peaks produced by falling and rising edges of  $\overline{\text{CE}}$ . Transient current magnitudes depend on the device outputs' capacitive and inductive loading. Two-line control and proper decoupling capacitor selection will suppress transient voltage peaks. Each device should have a 0.1  $\mu\text{F}$  ceramic capacitor connected between each  $V_{\text{CC}}$  and GND, and between its  $V_{\text{PP}}$  and GND. These high frequency, low inherent-inductance capacitors should be placed as close as possible to package leads. Addition-

ally, for every 8 devices, a 4.7  $\mu\text{F}$  electrolytic capacitor should be placed at the array's power supply connection between  $V_{\text{CC}}$  and GND. The bulk capacitor will overcome voltage slumps caused by PC board trace inductances.

### $V_{\text{PP}}$ Trace on Printed Circuit Boards

Writing flash memories, while they reside in the target system, requires that the printed circuit board designer pay attention to the  $V_{\text{PP}}$  power supply trace. The  $V_{\text{PP}}$  pin supplies the memory cell current for writing and erasing. Use similar trace widths and layout considerations given to the  $V_{\text{CC}}$  power bus. Adequate  $V_{\text{PP}}$  Supply traces and decoupling will decrease  $V_{\text{PP}}$  voltage spikes and overshoots.

### $V_{CC}$ , $V_{PP}$ , $\overline{RP}$ Transitions and the Command/Status Registers

Byte write and block erase completion are not guaranteed if  $V_{PP}$  drops below  $V_{PPH}$ . If the  $V_{PP}$  Status bit of the Status Register (SR.3) is set to "1", a Clear Status Register command MUST be issued before further byte write/block erase attempts are allowed by the WSM. Otherwise, the Byte Write (SR.4) or Erase (SR.5) Status bits of the Status Register will be set to "1"s if error is detected.  $\overline{RP}$  transitions to  $V_{IL}$  during byte write and block erase also abort the operations. Data is partially altered in either case, and the command sequence must be repeated after normal operation is restored. Device poweroff, or  $\overline{RP}$  transitions to  $V_{IL}$ , clear the Status Register to initial value 10000 for the upper 5 bits.

The Command User Interface latches commands as issued by system software and is not altered by  $V_{PP}$  or  $\overline{CE}$  transitions or WSM actions. Its state upon powerup, after exit from deep powerdown or after  $V_{CC}$  transitions below  $V_{LKO}$ , is Read Array Mode.

After byte write or block erase is complete, even after  $V_{PP}$  transitions down to  $V_{PPL}$ , the Command User Interface must be reset to Read Array mode via the Read Array command if access to the memory array is desired.

### Power Up/Down Protection

The LH28F008SAT-K85 is designed to offer protection against accidental block erasure or byte writing during power transitions. Upon power-up, the LH28F008SAT-K85 is indifferent as to which power supply,  $V_{PP}$  or  $V_{CC}$ , powers up first. Power supply sequencing is not required. Internal circuitry in the LH28F008SAT-K85 ensures that the Command User Interface is reset to the Read Array mode on power up.

A system designer must guard against spurious writes for  $V_{CC}$  voltages above  $V_{LKO}$  when  $V_{PP}$  is active. Since both  $\overline{WE}$  and  $\overline{CE}$  must be low for a command write, driving either to  $V_{IH}$  will inhibit writes. The Command User Interface architecture provides an added level of protection since alteration of memory contents only occurs after successful completion of the two-step command sequences.

Finally, the device is disabled until  $\overline{RP}$  is brought to  $V_{IH}$ , regardless of the state of its control inputs. This provides an additional level of memory protection.

### Power Dissipation

When designing portable systems, designers must consider battery power consumption not only during device operation, but also for data retention during system idle time. Flash nonvolatility increases usable battery life, because the LH28F008SAT-K85 does not consume any power to retain code or data when the system is off.

In addition, the LH28F008SAXX-KXXX's deep powerdown mode ensures extremely low power dissipation even when system power is applied. For example, portable PCs and other power sensitive applications, using an array of LH28F008SAXX-KXXX's for solid-state storage, can lower  $\overline{RP}$  to  $V_{IL}$  in standby or sleep modes, producing negligible power consumption. If access to the LH28F008SAT-K85 is again needed, the part can again be read, following the  $t_{PHQV}$  and  $t_{PHWL}$  wakeup cycles required after  $\overline{RP}$  is first raised back to  $V_{IH}$ . See AC Characteristics — Read-Only and Write Operations and Figures 8 and 9 for more information.

### 10. ABSOLUTE MAXIMUM RATINGS\*

Operating Temperature	
During Read	.....0°C to +70°C <sup>(1)</sup>
During Block Erase/Byte Write	.....0°C to +70°C
Temperature Under Bias	.....-10°C to +80°C
Storage Temperature	.....-65°C to +125°C
Voltage on Any Pin (except V <sub>CC</sub> and V <sub>PP</sub> )	
with Respect to GND	.....-2.0V to +7.0V <sup>(2)</sup>
V <sub>PP</sub> Program Voltage with Respect to GND during Block Erase/Byte Write	.....-2.0V to +14.0V <sup>(2,3)</sup>
V <sub>CC</sub> Supply Voltage with Respect to GND	.....-2.0V to +7.0V <sup>(2)</sup>
Output Short Circuit Current	.....100mA <sup>(4)</sup>

\* WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.

#### NOTES:

1. Operating temperature is for commercial product defined by this specification.
2. Minimum DC voltage is -0.5V on input/output pins. During transitions, this level may undershoot to -2.0V for periods < 20ns. Maximum DC voltage on input/output pins is V<sub>CC</sub>+0.5V which, during transitions, may overshoot to V<sub>CC</sub>+2.0V for periods < 20ns.
3. Maximum DC voltage on V<sub>PP</sub> may overshoot to +14.0V for periods < 20ns.
4. Output shorted for no more than one second. No more than one output shorted at a time.

### 11. OPERATING CONDITIONS

Symbol	Parameter	Notes	Min.	Max.	Unit
T <sub>A</sub>	Operating Temperature		0	+70	°C
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (10%)	1	4.50	5.50	V
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage (5%)	1	4.75	5.25	V

#### NOTE:

1. 5% V<sub>CC</sub> specifications reference the LH28F008SAXX-KX85 in its High Speed configuration. 10% V<sub>CC</sub> specifications reference the LH28F008SAXX-KX85 in its Standard configuration.

### 12. DC CHARACTERISTICS

T<sub>A</sub>=0~+70°C

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Condition
I <sub>LI</sub>	Input Load Current	1			±1.0	μA	V <sub>CC</sub> =V <sub>CC</sub> Max V <sub>IN</sub> =V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current	1			±10	μA	V <sub>CC</sub> =V <sub>CC</sub> Max V <sub>OUT</sub> =V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current	1, 3		1.0	2.0	mA	V <sub>CC</sub> =V <sub>CC</sub> Max CE=RP=V <sub>IH</sub>
				30	100	μA	V <sub>CC</sub> =V <sub>CC</sub> Max CE=RP=V <sub>CC</sub> ±0.2V
I <sub>CCD</sub>	V <sub>CC</sub> Deep PowerDown Current	1		0.2	16	μA	RP=GND ±0.2V I <sub>OUT</sub> (RY/BY)=0mA
I <sub>CCR</sub>	V <sub>CC</sub> Read Current	1		20	35	mA	V <sub>CC</sub> =V <sub>CC</sub> Max, CE=GND f=8MHz, I <sub>OUT</sub> =0mA CMOS Inputs
				25	50	mA	V <sub>CC</sub> =V <sub>CC</sub> Max, CE=V <sub>IL</sub> f=8MHz, I <sub>OUT</sub> =0mA TTL Inputs

## DC CHARACTERISTICS (Continued)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Condition
$I_{CCW}$	$V_{CC}$ Byte Write Current	1		10	30	mA	Byte Write In Progress
$I_{CCE}$	$V_{CC}$ Block Erase Current	1		10	30	mA	Block Erase In Progress
$I_{CCES}$	$V_{CC}$ Erase Suspend Current	1,2		5	10	mA	Block Erase Suspended $\overline{CE}=V_{IH}$
$I_{PPS}$	$V_{PP}$ Standby Current	1			+15/ -300	$\mu$ A	$V_{PP}=GND$
$I_{PPD}$	$V_{PP}$ Deep PowerDown Current	1		0.1	5.0	$\mu$ A	$\overline{RP}=GND \pm 0.2V$
$I_{PPR}$	$V_{PP}$ Read Current	1			200	$\mu$ A	$V_{PP}>V_{CC}$
$I_{PPW}$	$V_{PP}$ Byte Write Current	1		10	30	mA	$V_{PP}=V_{PPH}$ Byte Write in Progress
$I_{PPE}$	$V_{PP}$ Block Erase Current	1		10	30	mA	$V_{PP}=V_{PPH}$ Block Erase in Progress
$I_{PPES}$	$V_{PP}$ Erase Suspend Current	1		90	200	$\mu$ A	$V_{PP}=V_{PPH}$ Block Erase Suspended
$V_{IL}$	Input Low Voltage		-0.5		0.8	V	
$V_{IH}$	Input High Voltage		2.0		$V_{CC}+0.5$	V	
$V_{OL}$	Output Low Voltage	3			0.45	V	$V_{CC}=V_{CC}$ Min $I_{OL}=5.8mA$
$V_{OH1}$	Output High Voltage (TTL)	3	2.4			V	$V_{CC}=V_{CC}$ Min $I_{OH}=-2.5mA$
$V_{OH2}$	Output High Voltage (CMOS)		$0.85V_{CC}$			V	$I_{OH}=-2.5\mu A$ $V_{CC}=V_{CC}$ Min
			$V_{CC}-0.4$				$I_{OH}=-100\mu A$ $V_{CC}=V_{CC}$ Min
$V_{PPL}$	$V_{PP}$ during Normal Operations	4	0.0		6.5	V	
$V_{PPH}$	$V_{PP}$ during Erase/Write Operations		11.4	12.0	12.6	V	
$V_{LKO}$	$V_{CC}$ Erase/Write Lock Voltage		2.0			V	

## NOTES:

- All currents are in RMS unless otherwise noted. Typical values at  $V_{CC}=5.0V$ ,  $V_{PP}=12.0V$ ,  $T_A=+25^\circ C$ . These currents are valid for all product versions (package and speeds).
- $I_{CCES}$  is specified with the device deselected. If read while in Erase Suspend Mode, current draw is the sum of  $I_{CCES}$  and  $I_{CCR}$ .
- Includes  $\overline{RY}/\overline{BY}$ .
- Block Erases/Byte Writes are inhibited when  $V_{PP}=V_{PPL}$  and not guaranteed in the range between  $V_{PPH}$  and  $V_{PPL}$ .

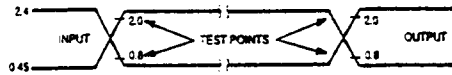
13. CAPACITANCE<sup>(1)</sup> $T_A=+25^\circ C$ ,  $f=1MHz$ 

Symbol	Parameter	Typ.	Max.	Unit	Condition
$C_{IN}$	Input Capacitance	6	8	pF	$V_{IN}=0V$
$C_{OUT}$	Output Capacitance	8	12	pF	$V_{OUT}=0V$

## NOTE:

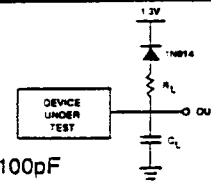
- Sampled, not 100% tested.

### AC INPUT/OUTPUT REFERENCE WAVEFORM(1)



AC test inputs are driven at  $V_{OH}$  (2.4V<sub>TTL</sub>) for a Logic "1" and  $V_{OL}$  (0.45V<sub>TTL</sub>) for a Logic "0". Input timing begins at  $V_{IH}$  (2.0V<sub>TTL</sub>) and  $V_{IL}$  (0.8V<sub>TTL</sub>). Output timing ends at  $V_{IH}$  and  $V_{IL}$ . Input rise and fall times (10% to 90%) < 10ns.

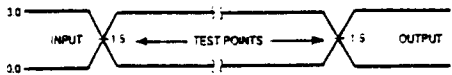
### AC TESTING LOAD CIRCUIT(1)



$C_L=100\text{pF}$   
 $C_L$  Includes Jig Capacitance  
 $R_L=3.3\text{k}\Omega$

### HIGH SPEED

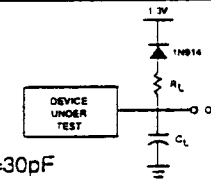
### AC INPUT/OUTPUT REFERENCE WAVEFORM(2)



AC test inputs are driven at 3.0V for a Logic "1" and 0.0V for a Logic "0". Input timing begins, and output timing ends, at 1.5V. Input rise and fall times (10% to 90%) < 10ns.

### HIGH SPEED

### AC TESTING LOAD CIRCUIT(2)



$C_L=30\text{pF}$   
 $C_L$  Includes Jig Capacitance  
 $R_L=3.3\text{k}\Omega$

### NOTES:

1. Testing characteristics for LH28F008SAXX-KX85 in Standard configuration.
2. Testing characteristics for LH28F008SAXX-KX85 in High Speed configuration.

### 14. AC CHARACTERISTICS — Read-Only Operations<sup>(1)</sup>

Versions		Parameter	Notes	LH28F008SAXX-KX85 <sup>(4)</sup>		LH28F008SAXX-KX85 <sup>(5)</sup>		Unit
				$V_{CC}\pm 5\%$	$V_{CC}\pm 10\%$	Min.	Max.	
$t_{AVAV}$	$t_{RC}$	Read Cycle Time		85		90		ns
$t_{AVQV}$	$t_{ACC}$	Address to Output Delay			85		90	ns
$t_{ELQV}$	$t_{CE}$	$\overline{CE}$ to Output Delay	2		85		90	ns
$t_{PHQV}$	$t_{PWH}$	$\overline{RP}$ High to Output Delay			400		400	ns
$t_{GLQV}$	$t_{OE}$	$\overline{OE}$ to Output Delay	2		40		45	ns
$t_{ELQX}$	$t_{LZ}$	$\overline{CE}$ to Output Low Z	3	0		0		ns
$t_{EHQZ}$	$t_{HZ}$	$\overline{CE}$ High to Output High Z	3		55		55	ns
$t_{GLQX}$	$t_{OLZ}$	$\overline{OE}$ to Output Low Z	3	0		0		ns
$t_{GHQZ}$	$t_{DF}$	$\overline{OE}$ High to Output High Z	3		30		30	ns
	$t_{OH}$	Output Hold from Addresses, $\overline{CE}$ or $\overline{OE}$ Change, Whichever is First	3	0		0		ns

### NOTES:

1. See AC Input/Output Reference Waveform for timing measurements.
2.  $\overline{OE}$  may be delayed up to  $t_{CE}-t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$ .
3. Sampled, not 100% tested.
4. See High Speed AC Input/Output Reference Waveforms and High Speed AC Testing Load circuits for testing characteristics.
5. See AC Input/Output Reference Waveforms and AC Testing Load Circuits for testing characteristics.

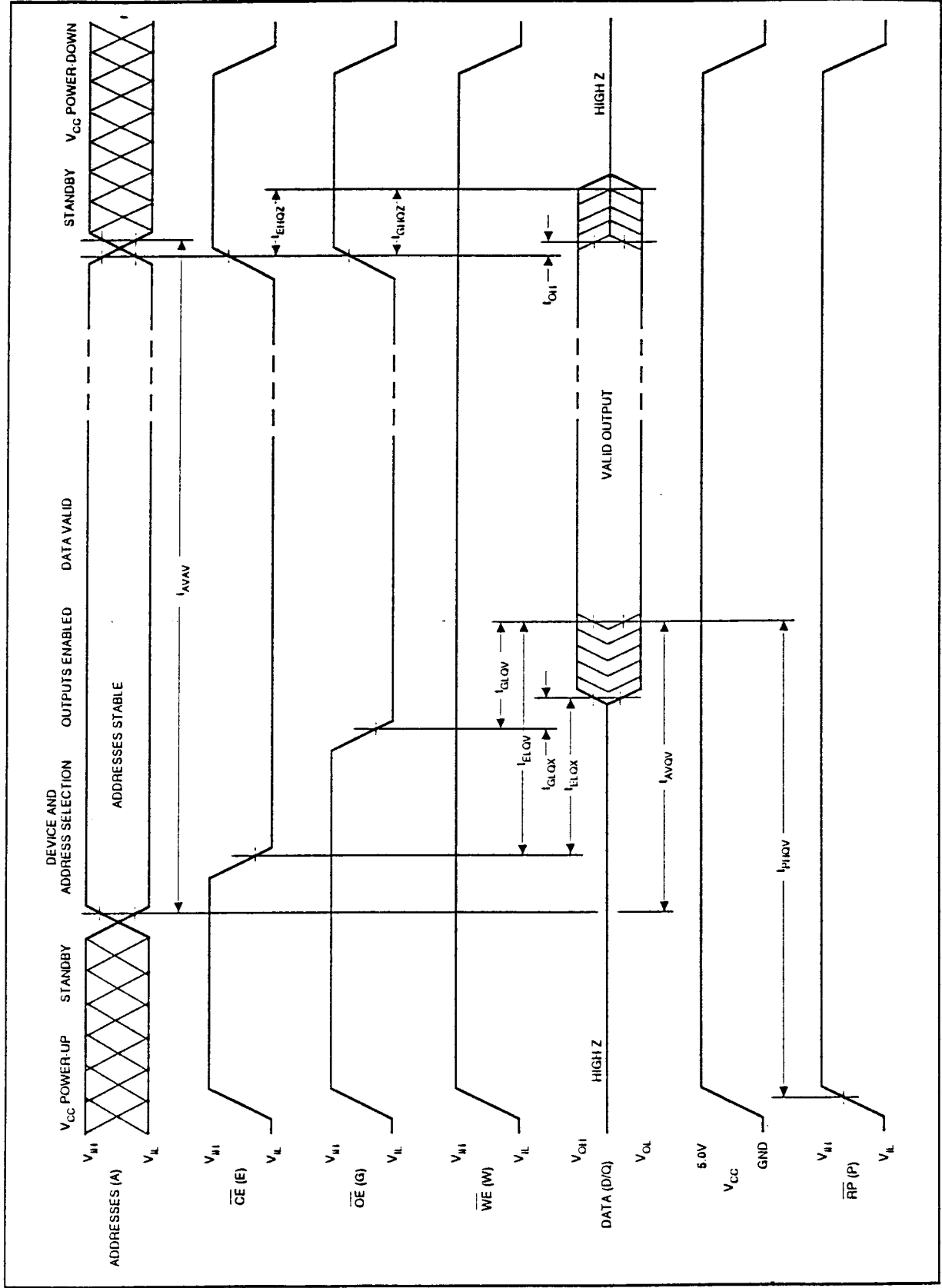


Figure 8. AC Waveform for Read Operations

AC CHARACTERISTICS - Write Operations<sup>(1)</sup>

Versions		Parameter	Notes	LH28F008SAXX-KX85 <sup>(7)</sup>		LH28F008SAXX-KX85 <sup>(8)</sup>		Unit
				V <sub>CC</sub> ±5%		Min.	Max.	
Symbol				Min.	Max.	Min.	Max.	
t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time		85		90		ns
t <sub>PHWL</sub>	t <sub>PS</sub>	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	2	1		1		μs
t <sub>ELWL</sub>	t <sub>CS</sub>	$\overline{CE}$ Setup to $\overline{WE}$ Going Low		10		10		ns
t <sub>WLWH</sub>	t <sub>WP</sub>	$\overline{WE}$ Pulse Width		40		40		ns
t <sub>VPWH</sub>	t <sub>VPS</sub>	V <sub>PP</sub> Setup to $\overline{WE}$ Going High	2	100		100		ns
t <sub>AVWH</sub>	t <sub>AS</sub>	Address Setup to $\overline{WE}$ Going High	3	40		40		ns
t <sub>DVWH</sub>	t <sub>DS</sub>	Data Setup to $\overline{WE}$ Going High	4	40		40		ns
t <sub>WHDX</sub>	t <sub>DH</sub>	Data Hold from $\overline{WE}$ High		5		5		ns
t <sub>WHAX</sub>	t <sub>AH</sub>	Address Hold from $\overline{WE}$ High		5		5		ns
t <sub>WHEH</sub>	t <sub>CH</sub>	$\overline{CE}$ Hold from $\overline{WE}$ High		10		10		ns
t <sub>WHWL</sub>	t <sub>WPH</sub>	$\overline{WE}$ Pulse Width High		30		30		ns
t <sub>WHRL</sub>		$\overline{WE}$ High to RY/ $\overline{BY}$ Going Low			100		100	ns
t <sub>WHQV1</sub>		Duration of Byte Write Operation	5, 6	6		6		μs
t <sub>WHQV2</sub>		Duration of Block Erase Operation	5, 6	0.3		0.3		s
t <sub>WHGL</sub>		Write Recovery before Read		0		0		ns
t <sub>QVVL</sub>	t <sub>VPH</sub>	V <sub>PP</sub> Hold from Valid SRD, RY/ $\overline{BY}$ High	2, 6	0		0		ns

## NOTES:

1. Read timing characteristics during erase and byte write operations are the same as during read-only operations. Refer to AC Characteristics for Read-Only Operations.
2. Sampled, not 100% tested.
3. Refer to Table 3 for valid A<sub>W</sub> for byte write or block erasure.
4. Refer to Table 3 for valid D<sub>W</sub> for byte write or block erasure.
5. The on-chip Write State Machine incorporates all byte write and block erase system functions and overhead of standard SHARP flash memory, including byte program and verify (byte write) and block precondition, precondition verify, erase and erase verify (block erase).
6. Byte write and block erase durations are measure to completion (SR.7=1, RY/ $\overline{BY}$ =V<sub>OH</sub>). V<sub>PP</sub> should be held at V<sub>PPH</sub> until determination of byte write/block erase success (SR.3/4/5=0).
7. See High Speed AC Input/Output Reference Waveforms and High Speed AC Testing Load Circuits for testing characteristics.
8. See AC Input/Output Reference Waveforms and AC Testing Load Circuits for testing characteristics.



## 15. BLOCK-ERASE AND BYTE WRITE PERFORMANCE

Parameter	Notes	LH28F008SAXX-KXXX			Unit
		Min.	Typ. <sup>(1)</sup>	Max.	
Block Erase Time	2		1.6	10	s
Block Write Time	2		0.6	2.1	s
Byte Write Time			8	(Note 3)	μs

## NOTES:

1. 25°C, 12.0V V<sub>pp</sub>.
2. Excludes System-Level Overhead.
3. Contact your SHARP representative for information on the maximum byte write specification.

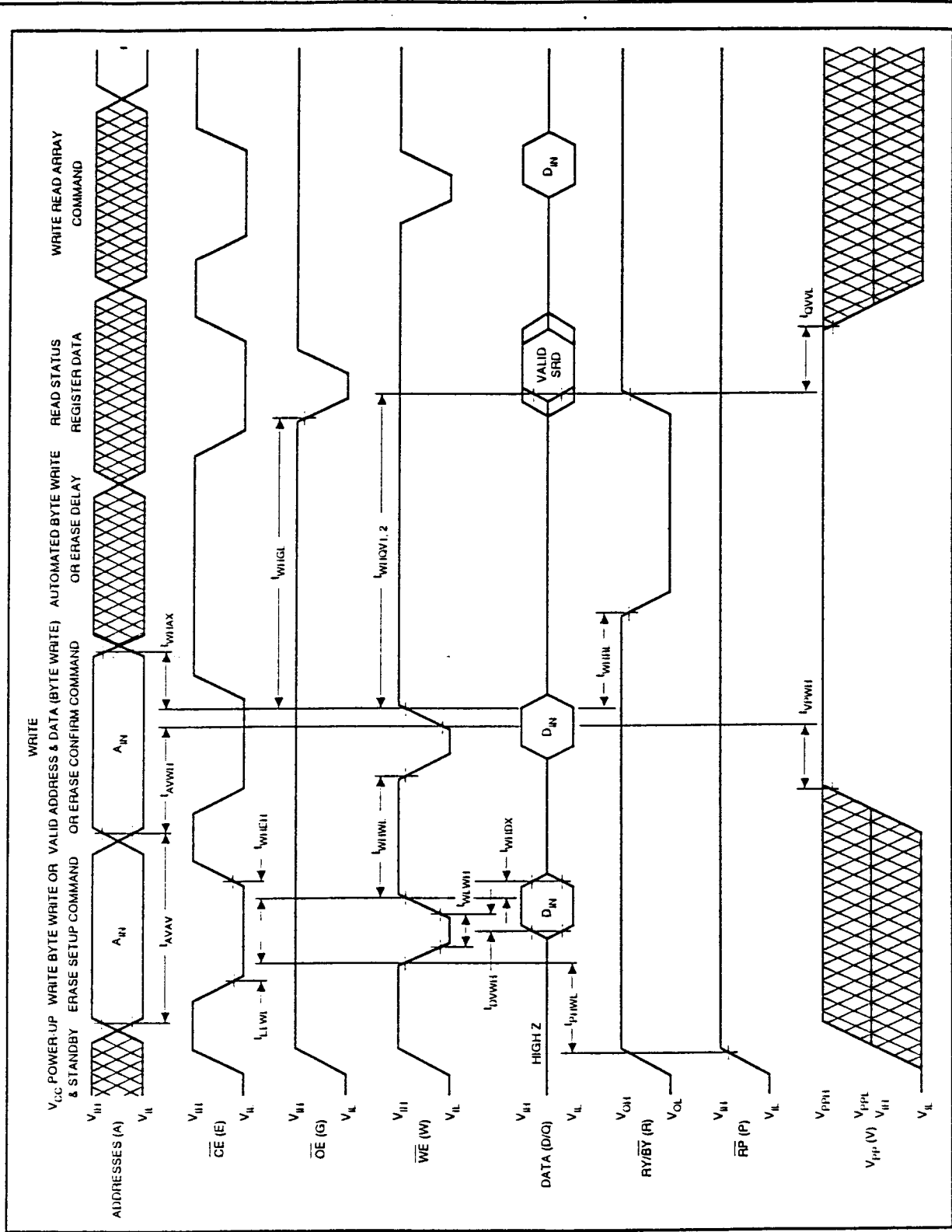


Figure 9. AC Waveform for Write Operations

16. ALTERNATIVE  $\overline{CE}$ -CONTROLLED WRITES<sup>(1)</sup>

Versions		Parameter	Notes	LH28F008SAXX-KX85 <sup>(6)</sup>		LH28F008SAXX-KX85 <sup>(7)</sup>		Unit
				$V_{CC}\pm 5\%$		$V_{CC}\pm 10\%$		
Symbol				Min.	Max.	Min.	Max.	
$t_{AVAV}$	$t_{WC}$	Write Cycle Time		85		90		ns
$t_{PHEL}$	$t_{PS}$	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	2	1		1		$\mu s$
$t_{WLEL}$	$t_{WS}$	$\overline{WE}$ Setup to $\overline{CE}$ Going Low		0		0		ns
$t_{ELEH}$	$t_{CP}$	$\overline{CE}$ Pulse Width		50		50		ns
$t_{VPEH}$	$t_{VPS}$	$V_{PP}$ Setup to $\overline{CE}$ Going High	2	100		100		ns
$t_{AVEH}$	$t_{AS}$	Address Setup to $\overline{CE}$ Going High	3	40		40		ns
$t_{DVEH}$	$t_{DS}$	Data Setup to $\overline{CE}$ Going High	4	40		40		ns
$t_{EHDX}$	$t_{DH}$	Data Hold from $\overline{CE}$ High		5		5		ns
$t_{EHAX}$	$t_{AH}$	Address Hold from $\overline{CE}$ High		5		5		ns
$t_{EHWH}$	$t_{WH}$	$\overline{WE}$ Hold from $\overline{CE}$ High		0		0		ns
$t_{EHEL}$	$t_{EPH}$	$\overline{CE}$ Pulse Width High		25		25		ns
$t_{EHRL}$		$\overline{CE}$ High to $\overline{RY}/\overline{BY}$ Going Low			100		100	ns
$t_{EHQV1}$		Duration of Byte Write Operation	5	6		6		$\mu s$
$t_{EHQV2}$		Duration of Block Erase Operation	5	0.3		0.3		s
$t_{EHGL}$		Write Recovery before Read		0		0		ns
$t_{QVVL}$	$t_{VPH}$	$V_{PP}$ Hold from Valid SRD, $\overline{RY}/\overline{BY}$ High	2,5	0		0		ns

## NOTES:

- Chip-Enable Controlled Writes: Write operations are driven by the valid combination of  $\overline{CE}$  and  $\overline{WE}$ . In systems where  $\overline{CE}$  defines the write pulsewidth (within a longer  $\overline{WE}$  timing waveform), all setup, hold and inactive  $\overline{WE}$  times should be measured relative to the  $\overline{CE}$  waveform.
- Sampled, not 100% tested.
- Refer to Table 3 for valid  $A_N$  for byte write or block erasure.
- Refer to Table 3 for valid  $D_N$  for byte write or block erasure.
- Byte write and block erase durations are measured to completion (SR.7=1,  $\overline{RY}/\overline{BY}=V_{OH}$ ).  $V_{PP}$  should be held at  $V_{PPH}$  until determination of byte write/block erase success (SR.3/4,5=0).
- See High Speed AC Input/Output Reference Waveforms and High Speed AC Testing Load Circuits for testing characteristics.
- See AC Input/Output Reference Waveforms and AC Testing Load Circuits for testing characteristics.



17 Package and packing specification

1. Package Outline Specification

Refer to drawing No. AA1105

2. Markings

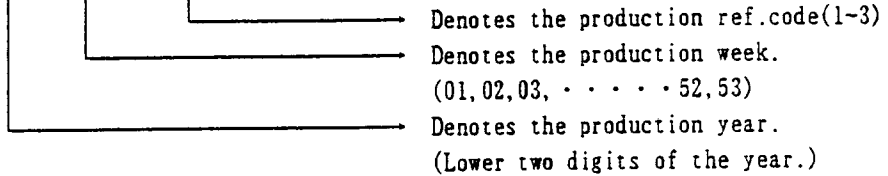
2-1. Marking contents

(1) Product name : LH28F008SAT-K85

(2) Company name : SHARP

(3) Date code

(Example) YY WW XXX Indicates the product was manufactured in the WWth week of 19YY.



(4) The marking of "JAPAN" indicates the country of origin.

2-2. Marking layout

Refer drawing No. AA1105

(This layout does not define the dimensions of marking character and marking position.)

3. Packing Specification (Dry packing for surface mount packages)

Dry packing is used for the purpose of maintaining IC quality after mounting packages on the PCB (Printed Circuit Board).

When the epoxy resin which is used for plastic packages is stored at high humidity, it may absorb 0.15% or more of its weight in moisture. If the surface mount type package for a relatively large chip absorbs a large amount of moisture between the epoxy resin and insert material (e.g. chip, lead frame) this moisture may suddenly vaporize into steam when the entire package is heated during the soldering process (e.g. VPS). This causes expansion and results in separation between the resin and insert material, and sometimes cracking of the package. This dry packing is designed to prevent the above problem from occurring in surface mount packages.

3-1. Packing Materials

Material Name	Material Specificaiton	Purpose
Tray	Conductive plastic (50devices/tray)	Fixing of device
Upper cover tray	Conductive plastic (1tray/case)	Fixing of device
Laminated aluminum bag	Aluminum polyethylene (1bag/case)	Drying of device
Desiccant	Silica gel	Drying of device
P P band	Polypropylene (3pcs/case)	Fixing of tray
Inner case	Card board (500devices/case)	Packaging of device
Label	Paper	Indicates part number, quantity and date of manufacture
Outer case	Card board	Outer packing of tray

(Devices shall be placed into a tray in the same direction.)

- 3-2. Outline dimension of tray  
Refer to attached drawing

#### 4. Storage and Opening of Dry Packing

- 4-1. Store under conditions shown below before opening the dry packing

- (1) Temperature range : 5~40°C  
(2) Humidity : 80% RH or less

- 4-2. Notes on opening the dry packing

- (1) Before opening the dry packing, prepare a working table which is grounded against ESD and use a grounding strap.  
(2) The tray has been treated to be conductive or anti-static. If the device is transferred to another tray, use a equivalent tray.

- 4-3. Storage after opening the dry packing

Perform the following to prevent absorption of moisture after opening.

- (1) After opening the dry packing, store the ICs in an environment with a temperature of 5~25°C and a relative humidity of 60% or less and mount ICs within 72 hours after opening dry packing.

- 4-4. Baking (drying) before mounting

- (1) Baking is necessary  
(A) If the humidity indicator in the desiccant becomes pink  
(B) If the procedure in section 4-3 could not be performed  
(2) Recommended baking conditions  
If the above conditions (A) and (B) are applicable, bake it before mounting. The recommended conditions are 16~24 hours at 120°C.  
Heat resistance tray is used for shipping tray.

#### 5. Surface Mount Conditions

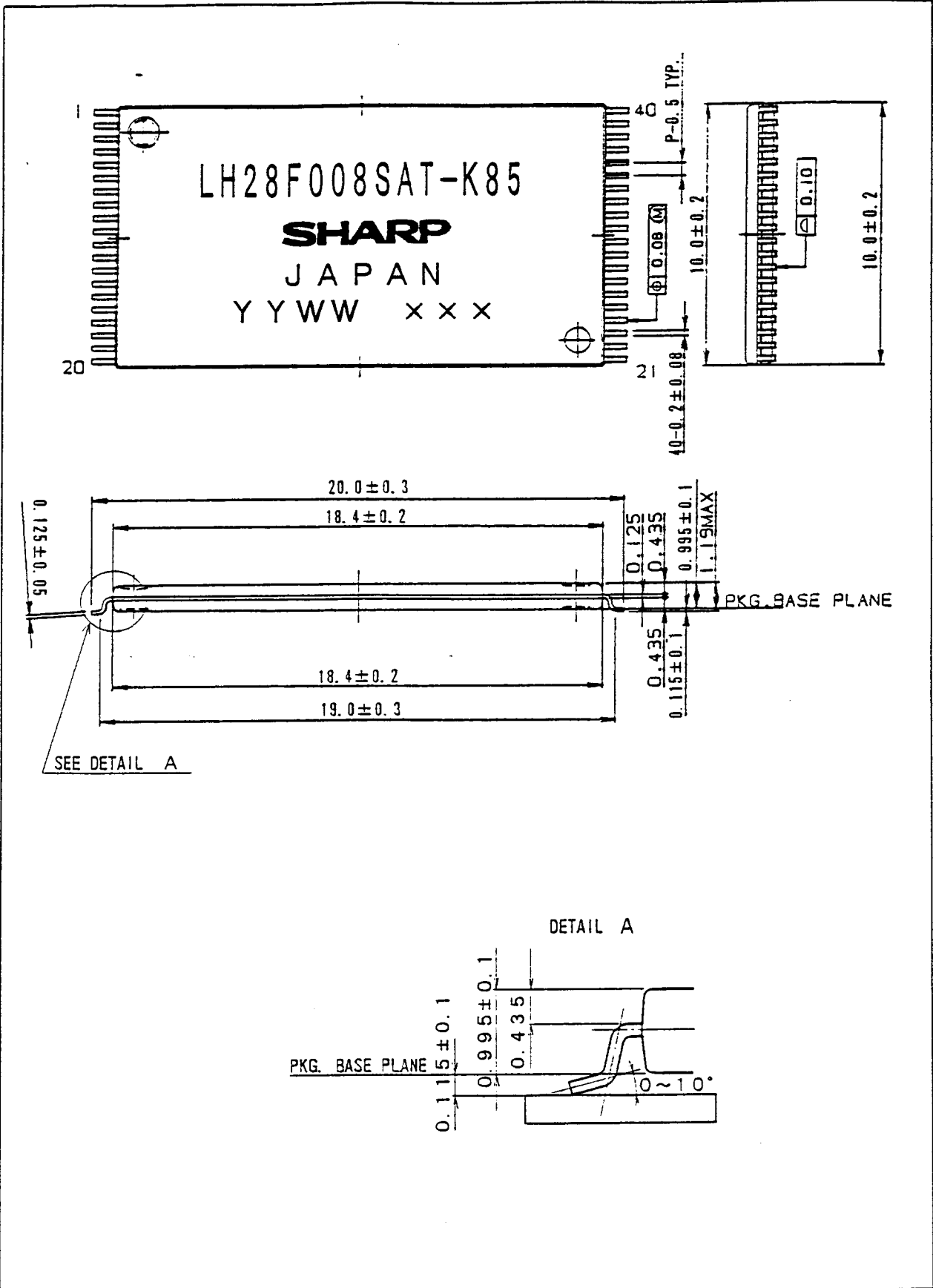
Please perform the following conditions when mounting ICs not to deteriorate IC quality.

- 5-1. Soldering conditions (The following conditions are valid only for one time soldering.)

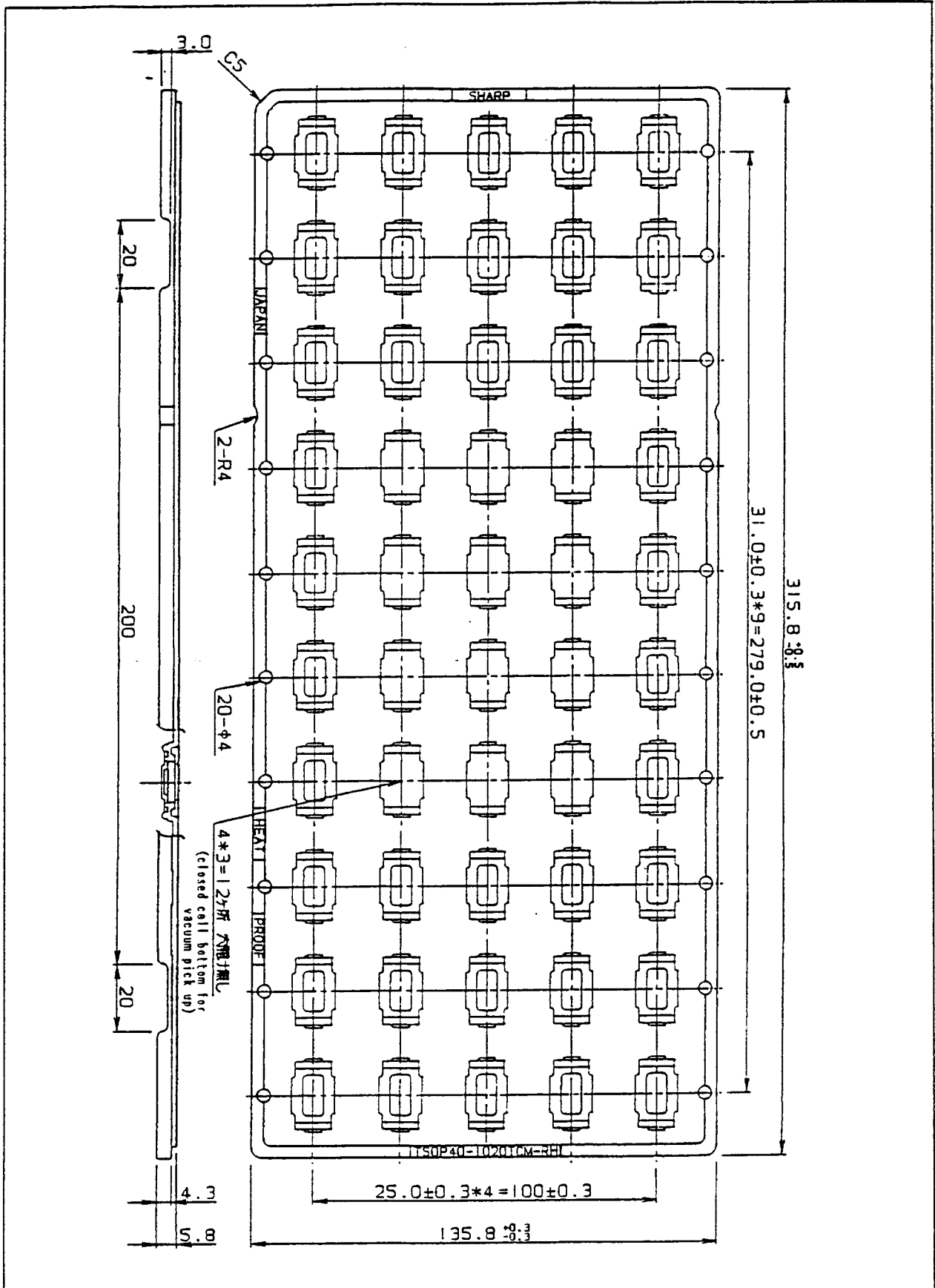
Mounting Method	Temperature and Duration	Measurement Point
Reflow soldering (air)	Peak temperature of 230°C or less, duration of less than 15 seconds. 200°C or over, duration of less than 40 seconds. Temperature increase rate of 1~4°C/second	IC package surface
Manual soldering (soldering iron)	260°C or less, duration of less than 10 seconds.	IC outer lead surface

- 5-2. Conditions for removal of residual flux

- (1) Ultrasonic washing power : 25 Watts/liter or less  
(2) Washing time : Total 1 minute maximum  
(3) Solvent temperature : 15~40°C



名称	リード仕上	TIN-LEAD	備考
NAME TSOP40-P-1020	LEAD FINISH	PLATING	プラスチックパッケージ外形寸法は、バリを含まないものとする。 NOTE Plastic body dimensions do not include burr of resin.
DRAWING NO.	単位	UNIT	mm
AA1105	UNIT	mm	



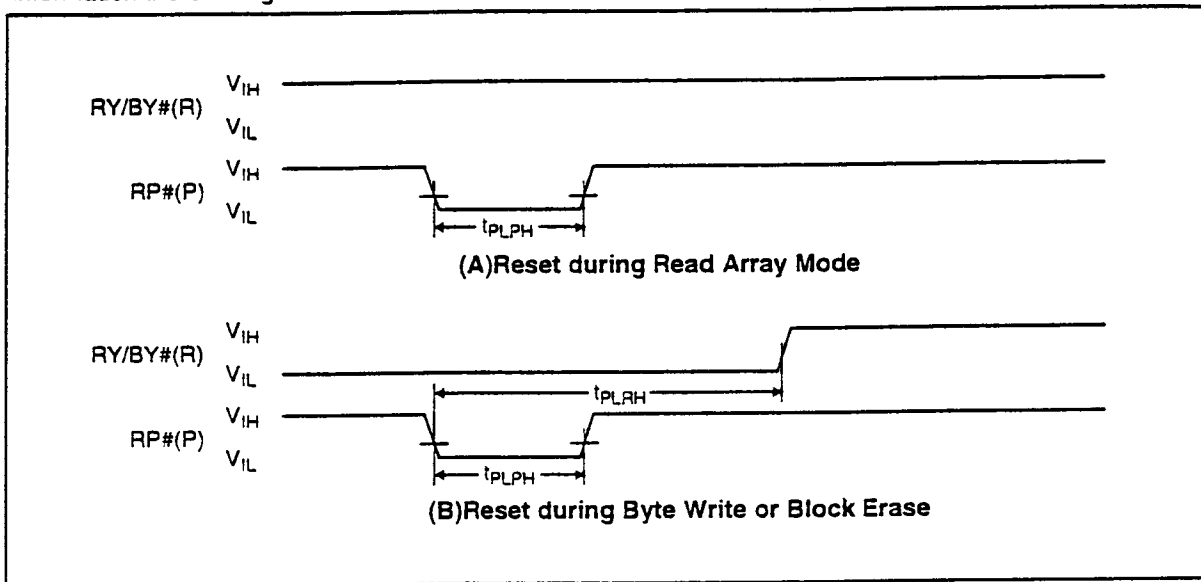
名称 NAME	TSOP40-1020TCM-RH	備考 NOTE
DRAWING NO.	CV644	UNIT mm



## SPECIFICATION CHANGES

### Reset Specifications for the LH28F008SAXX-KXXX

**PROBLEM:** Two reset specifications have been added to the LH28F008SAXX-KXXX. Please add this information the existing datasheet. The next datasheet revision will incorporate these reset specifications.



AC Waveform for Reset Operation

### Reset AC Specifications<sup>(1)</sup>

Sym	Parameter	Notes	V <sub>CC</sub> =5V		Unit
			Min.	Max.	
t <sub>PLPH</sub>	RP# Pulse Low Time (If RP# is tied to V <sub>CC</sub> , this specification is not applicable)		100		ns
t <sub>PLRH</sub>	RP# Low to Reset during Block Erase or Byte Write (If RP# is tied to V <sub>CC</sub> , this specification is not applicable)	2,3		12	s

#### NOTES:

1. These specifications are valid for all product versions (packages and speeds).
2. If RP# is asserted while a block erase or byte write operation is not executing, the reset will complete within 100 ns.
3. A reset time, t<sub>PHQV</sub>, is required from the latter of RY/BY# or RP# going high until outputs are valid.

In read modes, RP#-low deselects the memory, places output drivers in a high impedance state and turns off all internal circuits. RP# must be held low for a minimum of 100 ns. Time t<sub>PHQV</sub> is required after return from power-down until initial memory access outputs are valid. After this wake-up interval, normal operation is restored. The CUI is reset to read array mode and status register is set to 80H.

During block erase or byte write, RP#-low will abort the operation. RY/BY# remains low until the reset operation is complete. Memory contents being altered are no longer valid; the data may be partially erased or written.

**AFFECTED PRODUCTS:** All A- $\chi$  stepping material is affected.

LH28Fxxx FLASH MEMORY FLASH NON-VOLATILE MEMORY FLASH E2ROM FLASH ROM  
READ ONLY MEMORY ETOX LH28F008SAT-K85 8M (1Mx8) Dual Voltage