MGCM02

TDMA/AMPS IF and Baseband Interface

Data Sheet

April 2003

Features

- Complete IF to Baseband for IS136
- 100dB Gain Control
- Channel Filtering (30kHz)
- FM Demodulator
- RSSI Output
- Dual IF Synthesisers
- Fully Programmable via serial bus
- 3 Volt operation
- 49 Ball BGA package (7 x 7 mm)

Ordering Information

MGCM02/KG/BP1N

MGCM02/KG/BP1Q

Applications

- Dual Mode TDMA/AMPS Mobile telephones
- Dual Band (PCS1900/900) TDMA/AMPS Mobile telephones
- PCS 1900 TDMA Mobile Telephones

Description

The MGCM02 provides the complete IF to baseband I and Q including channel filtering for IS136/AMPS.

The receive input is at an IF frequency up to 200MHz. This is downconverted to an internal IF of 60kHz and filtered by a switched capacitor bandpass filter which also provides image rejection. The 60kHz signal is then demodulated to give baseband I and Q signals. Over 100dB of gain control is provided. The baseband outputs can be input directly to an A to D converter.

The internal FM discriminator can be used for demodulating AMPS signals. The receive path also provides RSSI.

Transmit I and Q baseband signals from D to A converters can be input directly to MGCM02 which provides reconstruction filters and a variable gain buffer.

The two PLL synthesisers are used for generation of the receive and transmit IF LO signals.

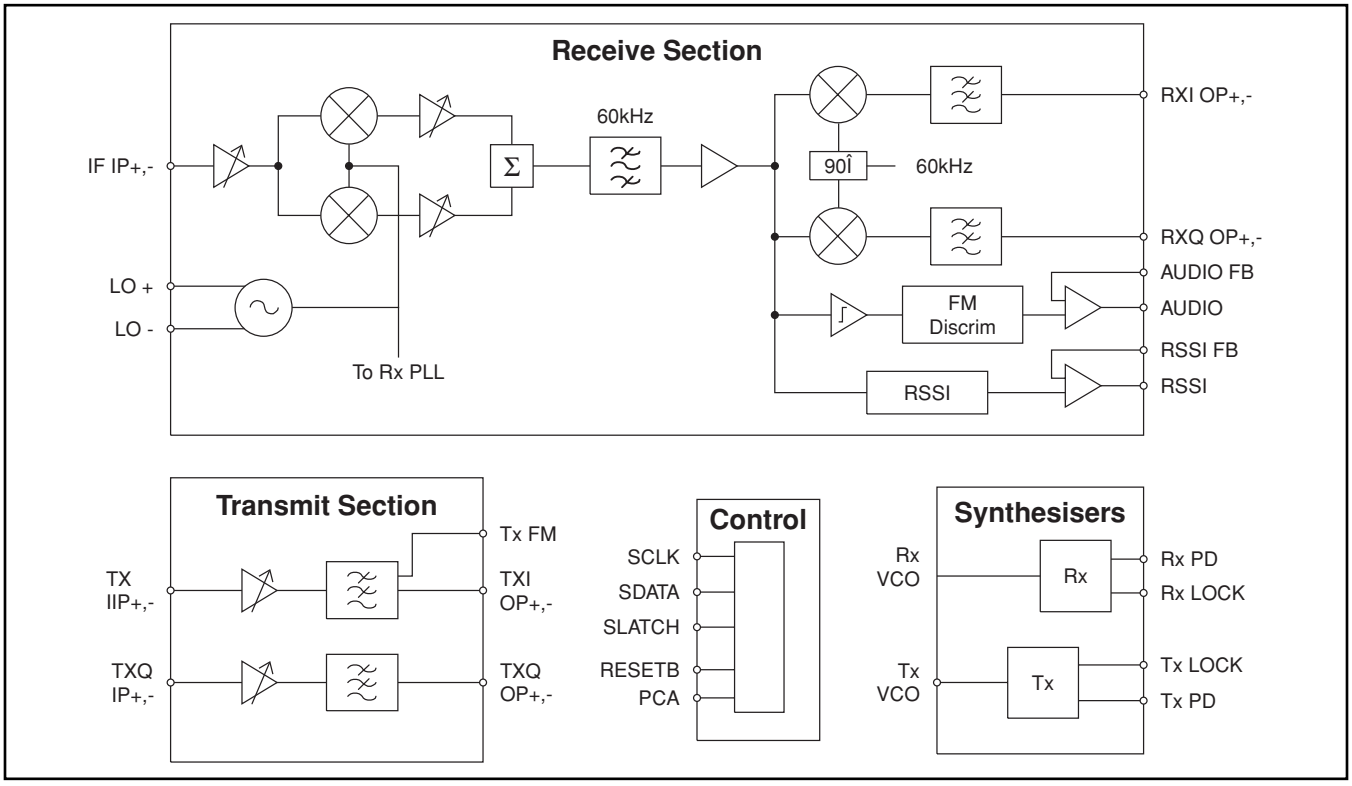


Figure 1 - Block Diagram

Pad Assignment

No	Pin Name	Type	Description
A1	RTUNE		Bias Reference - connect 100kΩ to ground
A2	VBG		Bandgap Reference Decoupling
A3	PCA	Input	Power Control Assert
A4	SDATA	Input	Serial Interface, Serial Data In
A5	VDD	Power	Power Supply - Digital
A6	TCXO	Input	19.44MHz Reference from TCXO
A7	GND (TX)	Ground	Ground - Transmit Section
B1	RXI OP+	Output	Baseband Receive I Output +
B2	RXI OP-	Output	Baseband Receive I Output -
B3	SCLK	Input	Serial Interface, Clock
B4	GND	Input	Ground Digital
B5	RESETB	Input	Reset (active low)
B6	TXQ IP-	Input	Transmit Q Input -
B7	TXQ IP+	Input	Transmit Q Input +
C1	RXQ OP-	Output	Baseband Receive Q Output -
C2	GND	Ground	Ground - Receive Section
C3	AGC	Input	AGC control voltage
C4	SLATCH	Input	Serial Interface, Latch
C5	LOCK DET	Output	Synthesiser Lock Detect
C6	TXI IP-	Input	Transmit I Input -
C7	TXI IP+	Input	Transmit I Input +
D1	RX IP+	Input	Receive IF Input +
D2	RXQ OP+	Output	Baseband Receive Q Output +
D3	GND	Ground	Ground (Substrate Connection)
D4	NC		Not Connected
D5	GND	Ground	Ground (Substrate Connection)
D6	TXI OP+	Output	Transmit I Output +
D7	VDD	Power	Power Supply - Transmit Section
E1	RX IP-	Input	Receive IF Input -

No	Pin Name	Type	Description
E2	VDD	Power	Power Supply - RSSI and Demodulator
E3	RSSI	Output	RSSI Output
E4	UHF LOCK	Input	UHF Synth Lock Input
E5	TX FM	Output	Transmit FM Output
E6	TXQ OP+	Output	Transmit Q Output +
E7	TXI OP-	Output	Transmit I Output -
F1	AUDIO FB	Input	Demodulator Feedback
F2	GND	Ground	Ground RSSI/Demodulator
F3	RSSI FB	Input	RSSI Feedback
F4	RX PD	Output	Receive PLL Charge Pump Output
F5	GND	Ground	Ground - Synthesiser
F6	VDD	Power	Power Supply - Synthesiser
F7	TXQ OP-	Output	Transmit Q Output -
G1	AUDIO	Output	Demodulator Audio/Data Output
G2	VDD	Power	Power Supply - Receive Section
G3	GND	Ground	Ground (Substrate Connection)
G4	VHF RESB	Input	VHF VCO resonator
G5	VHF RES	Input	VHF VCO resonator
G6	TX VCO	Input	Transmit IF PLL Input
G7	TX PD	Output	Transmit PLL Charge Pump Output

Absolute Maximum Ratings

Supply Voltage	-0.3 to 3.9V
Voltage applied to any pin	-0.3 to Vcc + 0.3 V
Operating Temperature	-40 °C to 100 °C
Storage Temperature	-55 °C to 150 °C
Max Junction Temperature	150 °C
ESD (Human Body Model)	2kV

Electrical Characteristics

Tamb = -40°C to +85°C, VDD = 3V +/- 10%. VEE = 0V. These characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage ranges unless otherwise stated.

Characteristics	Value			Units	Comments
	Min	Typ	Max		
Supply Current					
Sleep		20	100	µA	
Powerdown		550		µA	
Powerdown - Rx PLL on				mA	
Powerdown - Tx PLL on				mA	
Receive Section (I/Q)			25	mA	
Receive Section (FM)			26	mA	
Receive Section (I/Q)		17	18.5	mA	T = 25°C, Vdd = 3V
Receive Section (FM)		17	19.5	mA	T = 25°C, Vdd = 3V
Transmit Section (I/Q)		6	9	mA	
Transmit Section (FM)		3.5	6.5	mA	
Logic Inputs					
Input Voltage High - VIH	0.8Vdd			Volts	
Input Voltage Low - VOL			0.2Vdd	Volts	
Input Current			10	nA	Vin = 0 to Vdd
Input Capacitance			10	pF	
Logic Outputs					
Output Voltage Low			0.4Vdd	Volts	
Output Voltage High	0.6Vdd			Volts	
Output Current			+/-1	mA	
Serial Control Timing					See Fig 7
SDATA Set Up t1	20			ns	
SDATA Hold t2	20			ns	
SCLK Pulse Width t3	50			ns	
SLATCH Set up t4	20		t3 - 20	ns	
SLATCH Pulse Width t5	50			ns	
SCLK Period	100			ns	

Characteristics	Value			Units	Comments
	Min	Typ	Max		
Switch on/off times					
Tx Turn on time			0.5	ms	
Tx Turn off time			0.5	ms	
Rx Turn on time			1.0	ms	
Rx Turn off time			1.0	ms	
TCXO Input					
Input Resistance	10			kΩ	
Input Capacitance	10			pF	
Input Sensitivity	0.5		2	V p-p	ac coupled
Frequency		19.44		MHz	
Receive - General					
Input Impedance	8	12	16	kΩ	Differential
Input Frequency	40		200	MHz	
Output Impedance		2		kΩ	Differential
Output Voltage RXI,RXQ		1.25		Volts	Selected by programming
Output Voltage RXI,RXQ		Vdd/2		Volts	
Receive (IQ Mode)					
Min Gain		-17		dB	
Max Gain		96.5		dB	
Gain	tbd	80	tbd	dB	Vagc = tbd
Gain Resolution		0.5		dB	
Gain Control Slope	tbd	68	tbd	dB/V	
I/Q Gain Matching	-0.5		+0.5	dB	
I/Q Phase Balance			+/- 1	deg	
Group Delay Ripple		14	16	µs p-p	0 to 12.5 kHz
Gain Ripple		1.5	2.2	dB p-p	0 to 12.5 kHz
Noise Figure			12.5	dB	Rs = 850 ohms
Input IP3 (Max Gain)		-35		dBm	Note 2
Input IP3 (Gain = 80dB)		-20		dBm	Note 3
Output 1dB Compression	3			V p-p	Differential
Receive (FM Mode)					
Input Sensitivity		-108		dBm	Rs = 850 Ω Note 4
Noise Figure		13		dB	Rs = 850 Ω
Input IP3 (High Gain)		-20		dBm	Note 5
Audio Output			500	mV	Defined by external components

Characteristics	Value			Units	Comments
	Min	Typ	Max		
Receive LO VCO					
Operating Frequency	100		400	MHz	
LO Phase Noise		-92		dBc/Hz	Offset = 30 kHz
Receive Filter					Note 6
Centre Frequency		60		kHz	Fig 3
3dB Bandwidth	+/- 16		+/- 18	kHz	
Stop Band Attenuation					Relative to signal at 60kHz
0 to 3 kHz	67	69		dB	
3 kHz to 10 kHz	61	63		dB	
10 kHz to 22 kHz	48	51		dB	
38 kHz	18	20		dB	Note 7
82 kHz	18	20		dB	Note 7
98 kHz to 110 kHz	48	50		dB	
110 kHz to 117 kHz	61	63		dB	
117 kHz to 123 kHz	68	70		dB	
123 kHz to 1.36 MHz	71	73		dB	
1.36 MHz to 1.52 MHz	36	48		dB	
1.52 MHz to 10 MHz	71	73		dB	
Image Attenuation					Fig 4
0 to -10kHz	61			dB	
-10 kHz to -42 kHz	40			dB	
- 42 kHz to -78 kHz	25	28		dB	
- 78 kHz to -105 kHz	40			dB	
-105 kHz to -1.36 MHz	61			dB	
-1.36 MHz to -1.52 MHz	36	48		dB	
-1.52 MHz to -10 MHz	61			dB	
Gain Ripple		1.0	1.5	dB	Peak
RSSI (FM Mode)					
Dynamic Range		75		dB	Note 8
Accuracy	-3		+3	dB	
RSSI Slope		20		mV/dB	
Input Signal - Min		-100		dBm	Rs = 850Ω
Input Signal - Max		-25		dBm	Rs = 850Ω
RSSI Output Level	Vdd/2-1.2		Vdd/2+1.2	V	Fig 6
RSSI Output Impedance		1		kΩ	

Characteristics	Value			Units	Comments
	Min	Typ	Max		
Transmit (I/Q and FM)					
Gain	11	12	13	dB	
	8.5	9	9.5	dB	
	5.5	6	6.5	dB	
	2.5	3	3.5	dB	
	-0.5	0	0.5	dB	
Input dc Voltage		0.8		V	
Output dc Voltage		1.25		V	Selected by programming
Output dc Voltage		Vdd/2		V	
Input Signal Range			2	V p-p	Differential Note 9
Ouput Signal Range			2	V p-p	Differential Note 9
Input Signal - FM			1	V p-p	Single-ended
Output Signal - FM			1	V p-p	
Output Amplitude Balance	-0.3		0.3	dB	
Output Phase Balance			0.7	deg	
Output dc offset		20	30	mV p-p	
3dB Filter bandwidth	22	25	29	kHz	
Gain Ripple			1	dB	0 to 12.5kHz
Group Delay Variation			10	µs	0 to 12.5kHz
Stop Band Attenuation	30			dB	100kHz to 2MHz
	40			dB	> 2MHz
Noise - in band			-50	dBc	Note 10
Noise 20 to 45 kHz			-60	dBc	BW = 300Hz
Noise 45 to 60 kHz			-75	dBc	BW = 300Hz
Noise => 60 kHz			-85	dBc	BW = 300Hz
Synthesisers					
Transmit PLL Frequency	1		115	MHz	
Receive PLL Frequency	80		400	MHz	From receive LO VCO
Tx PLL Input Sensitivity	100			mV	
Charge Pump Current	400	496	600	µA	Default mode
	140	176	210	µA	
	75	96	115	µA	
	13	16	19	µA	
Charge Pump Output	0.5		Vdd -0.5	Volts	Io +/-15%
Charge Pump sink/source mismatch			+/- 15	%	
Charge Pump off state current			5	nA	

Notes on Electrical Characteristics

1. All signal voltages are differential rms unless stated otherwise
2. Intermodulation tones at offsets of 120kHz and 240kHz. Level = -61dBm
3. Gain set to 80 dB - typically max gain required in application
4. Output SINAD = 12dB. Input modulation is 1kHz tone with 8kHz deviation. Standard gain FM mode.
5. Intermodulation tones at offsets of 60kHz and 120kHz. Level = - 55dBm
6. These filter characteristics are for the 60kHz band pass filter in narrow band mode. This provides all the filtering in FM mode. There is additional filtering in I/Q mode provided by the baseband low pass filters. Details are shown in fig 2
7. Extrapolate linearly between 22kHz - 38kHz, 82kHz - 98kHz
8. Standard gain FM mode - RSSI switched internally
9. The input and output signal ranges are the maximum available. For example if the input signal is 2V pk-pk then the programmed gain can only be 0dB
10. Noise relative to full scale signal

Operating Description

Receive

Basic Architecture

The MGCM02 provides a highly integrated receive solution for dual mode IS136/AMPS mobile telephones. The input to MGCM02 is normally from the output of the first IF filter. The signal is amplified by a variable gain amplifier before being downconverted in a quadrature mixer to a low IF of 60kHz as I (In phase) and Q (Quadrature) signals. The local oscillator for this mixer is generated from an on chip VCO using external tank components. This oscillator operates at twice the LO frequency to allow the generation of accurate quadrature LO signals for the mixer. High side or low side LO injection is programmable. Further stages of voltage controlled gain are then provided at 60kHz with matched amplifiers in the I and Q channels.

Gain control is provided from an external analogue control signal. This signal is digitised by an on chip 8 bit analog to digital converter. The digital outputs are then used to control the amplifiers. Figure 2 shows the amplifier configuration in more detail. The preamplifier has 4 gain settings and there are four amplifier stages at 60 kHz each providing -12 to +12dB gain in 0.5 dB steps. The gain control range will be more than adequate for most TDMA applications. The digitally controlled amplifiers provide a highly accurate and linear control of gain. The conversion rate of the analog to digital converter is 45 kHz.

The I and Q signals are then combined and passed through a switched capacitor polyphase bandpass filter. This filter is a fifth order Chebyshev. The advantage of using a switched capacitor filter is that it gives very stable performance and no calibration is required. The circuit also provides rejection of the image frequency following the down conversion to 60kHz.

TDMA IS136 Mode

Following the bandpass filter the signal is mixed down to baseband I and Q signals which are output from differential outputs. There is additional baseboard filtering to remove spurii from the downconverters and clock breakthrough from the switched capacitor filters. Further detail of the MGCM02 receive path is shown in Fig 2. The baseboard outputs can be fed directly into analog to digital converters in a baseband circuit.

AMPS FM Mode

FM demodulation can be done using the I and Q baseband signals if supported by the baseband however the MGCM02 contains a FM demodulator.

In FM mode the baseband I and Q output stages are disabled and the 60 kHz IF signal from the bandpass filter is input to a limiting amplifier and FM discriminator. The FM discriminator consists of a shift register acting as a delay line. The output of the discriminator is a digital signal which must be filtered to recover the audio signal. The discriminator output is routed through the cascaded baseband I and Q low pass smoothing filters and finally through an output buffer stage. The cut-off frequency of the low pass switched capacitor filters can be set at 25kHz for optimum filtering. External components can be used to optimise the gain and frequency response of the output amplifier.

There are two methods of controlling the amplifier gain in FM Mode.

1) Fixed gain. The amplifier gain is set to a preset level. This gain level (Pre-amplifier and VGA gain = 26dB) allows the minimum sensitivity requirements to be met, but at high signal levels the gain is automatically reduced by 32.5 dB. This optimises the signal levels through the bandpass filter preventing overload and excessive phase distortion. Further details on this are given in the following RSSI section.

2) AGC Control. In this mode the gain is controlled by the VGA control input. The RSSI level is monitored by the baseband controller and the gain level set appropriately. This mode gives improved performance in strong fading environments.

RSSI

The MGCM02 also contains RSSI circuitry. This would normally be used when using the FM discriminator to provide the received signal strength to the phone microcontroller. This RSSI circuit has over 70dB dynamic range.

A block diagram of the RSSI circuit is shown in figure 5. The switched capacitor filter has a limited dynamic range of approximately 50dB due to aliased noise from the sampling process used. In order to enable the RSSI to operate over a larger dynamic range gain control is required in the amplifiers before the

band pass filter. This can be provided in two ways as described in the preceding FM section.

In the fixed gain FM mode the RSSI output is input to a comparator. The output of this comparator then reduces the IF amplifier gain by 32.5dB thus enabling a larger dynamic range for the RSSI. Hysteresis is built in to prevent oscillation when close to the threshold level. Fig 6 shows the RSSI characteristic. At low signal levels the RSSI output increases with signal level, however at high signal level when the gain is reduced in the input path, the RSSI output is mirrored around Vdd/2 and decreases with increasing signal level. The slope is the same at high level as at low level but is of course negative. The actual slope (or gain) and settling time for the RSSI are set by external components as shown in fig 5.

The RSSI output from the MGCM02 will normally be input into an a to d converter. This, together with the baseboard controller can convert the RSSI signal to a monotonic digital output as required by the IS136 specifications. Calibration will be required to determine the slope, offset at low and high signal levels, and threshold level of the RSSI characteristic. For example if the RSSI output is less than Vdd/2 then the RSSI slope is positive; if greater than Vdd/2 than the RSSI slope is negative.

If the AGC mode is used for FM then this automatic RSSI switching is disabled and the RSSI is only operated over the lower segment of the characteristic. The actual signal level must then be calculated by the baseband using the measured RSSI level and the applied AGC signal.

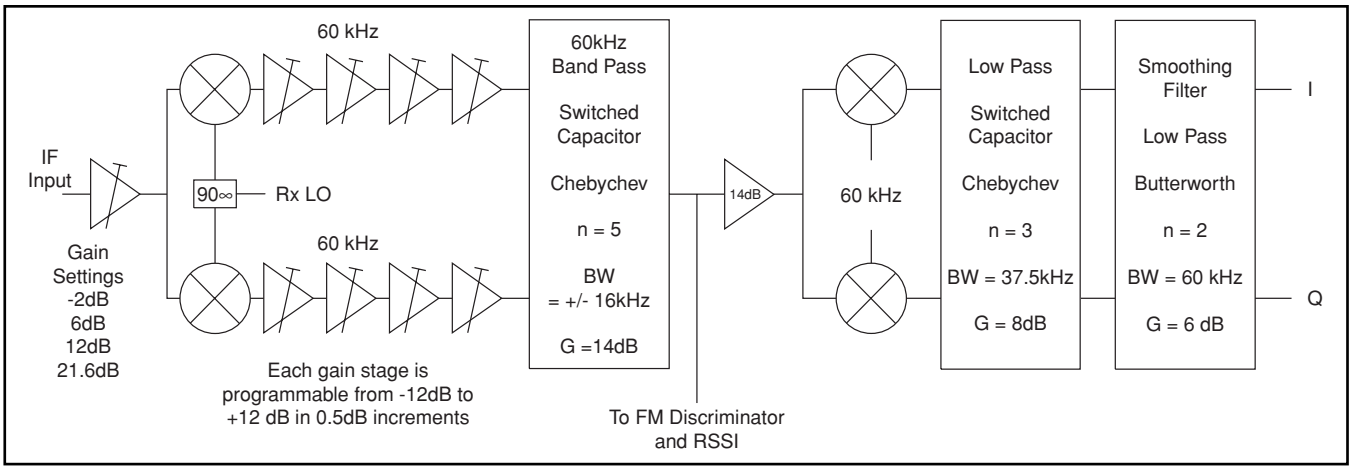


Figure 2 - Receive Path Block Diagram showing Gain Plan and Filters

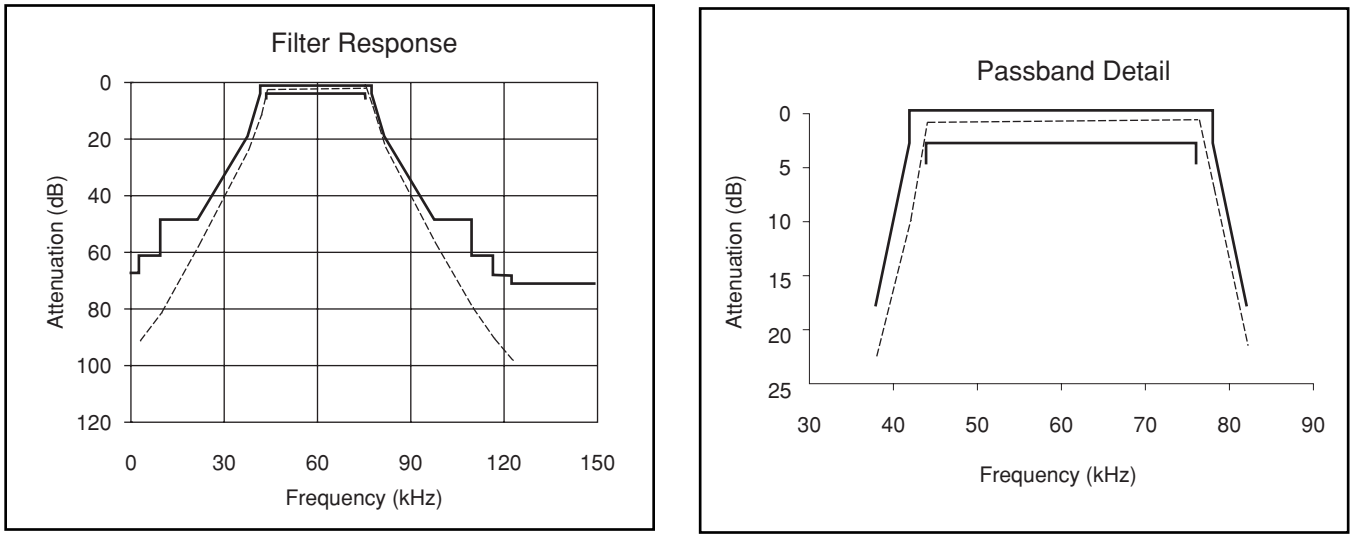


Figure 3 - Band Pass Filter Response

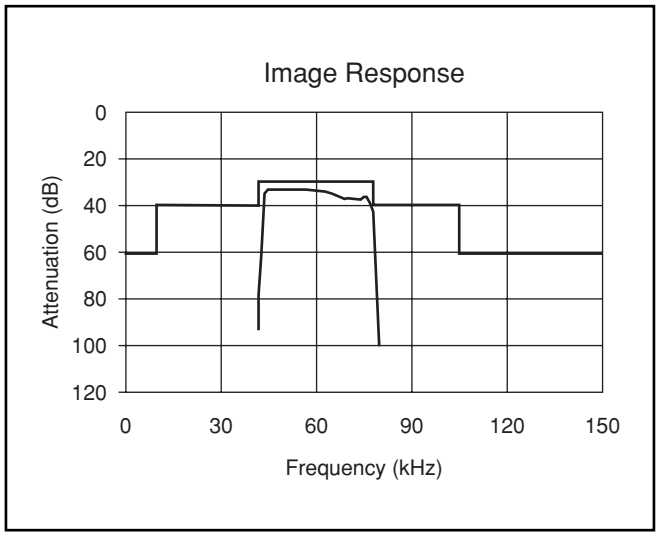


Figure 4 - Band Pass Filter - Image Response

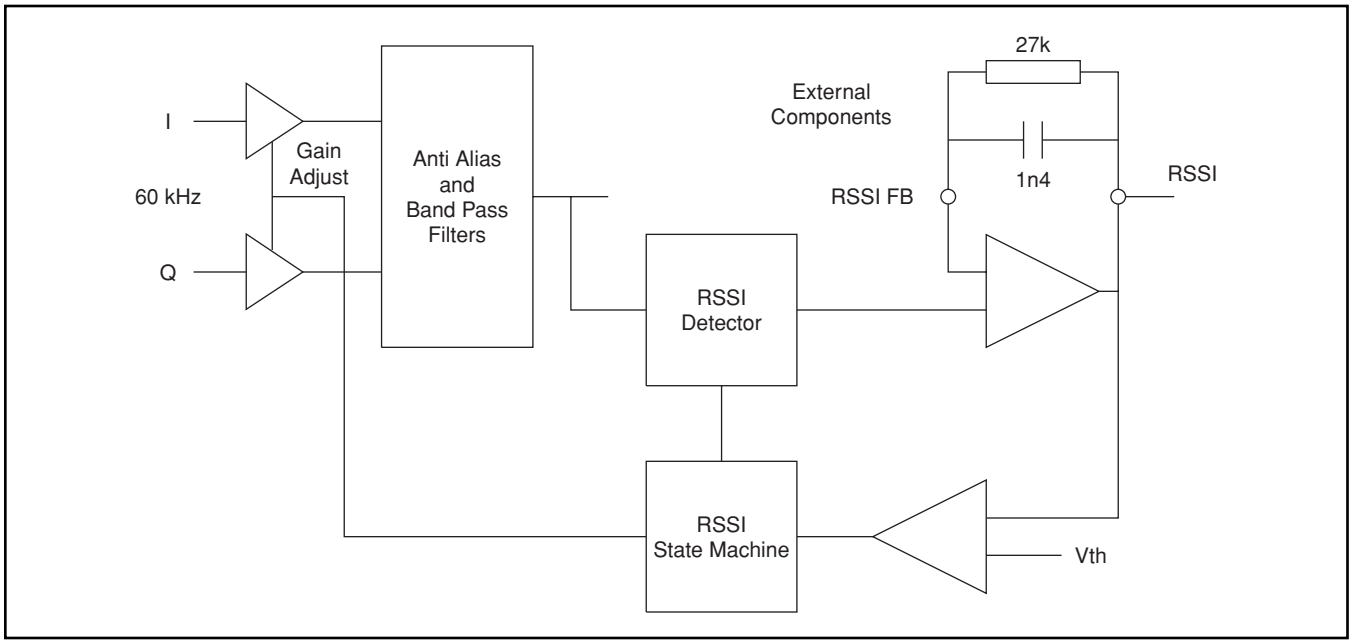


Figure 5 - RSSI Block Diagram

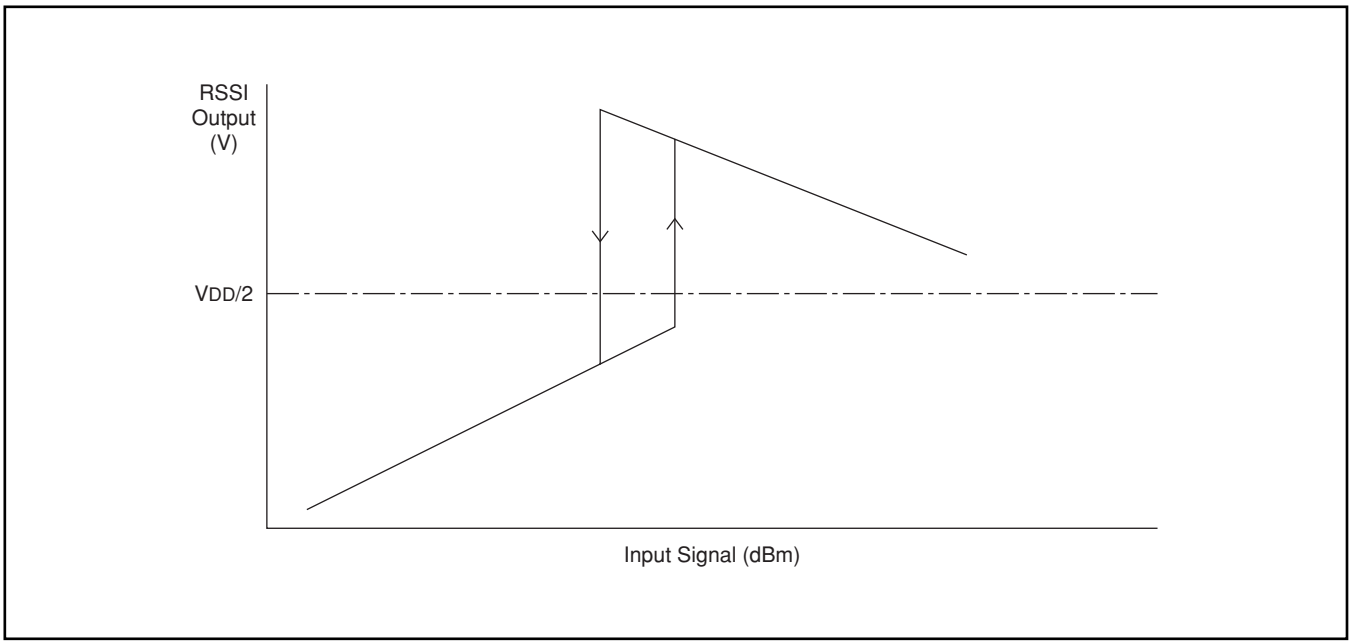


Figure 6 - RSSI Characteristic

Transmit

TDMA IS136 Mode I/Q Modulation

The inputs to MGCM02 are derived from baseband digital to analog converters. These signals are passed through variable gain buffers. The gain of these buffers can be programmed from 0 to 12 dB in 3 dB increments allowing compatibility with a number of baseband and transmit modulator devices.

The buffers are followed by reconstruction filters to remove spurious responses from preceding digital to analog converters. These filters are third order Butterworth with 25kHz cut off. The filters contain automatic calibration to set the cut off frequency. This can be controlled via the serial programming bus.

All inputs and outputs are differential

AMPS FM mode

There is a choice of modes available to accommodate the modulation technique used and different baseband interfaces.

If I,Q modulation is used for FM modulation then the same mode is used as for TDMA ie differential input and differential output on the I and Q channels.

If direct modulation of the transmit IF VCO is used then the TX FM (E5) single-ended output is used. The I+,Q+ outputs are switched high and the I-,Q- outputs are switched low to set the IQ modulator in a transmit device such as the Zarlink MGCT04 into FM mode. When using the MGCT04 the transmit IF VCO will be operating at twice the IF frequency. The frequency deviation therefore required on the VCO will be twice that required at the transmit output of that device.

The input to the MGCM02 can be programmed to be either differential or single ended using the I channel inputs and the Q channel inputs are powered down. The differential input mode is the same as for TDMA. In the single ended mode only the TXI+ input is active and the FM signal must be capacitively coupled into this pin. This mode would only be used where the FM signal is from a different source to the I channel. When using this mode the differential I outputs from a baseband device must be in high impedance state.

The transmit filtering used for FM mode is the same as for TDMA mode.

Synthesisers and VCO

Two VHF PLL synthsisers are included for the generation of receive and transmit IF LO signals. The two synthesisers are identical.

The input to the receive PLL is from the on chip VCO. This operates at twice the LO frequency. An external tank circuit is required - typically a parallel capacitor and inductor with a varactor for tuning.

The synthesisers include 2 modulus prescalers programmable from 8/9 to 128/129 followed by a 11 bit programmable counter and 7 bit swallow counter to control the 2 modulus prescaler. The reference divider is a fully programmable 15 bit counter. The reference frequency is a 19.44MHz TCXO.

The synthesiser charge pumps can be programmed to four current levels to drive the appropriate loop filters.

The synthesisers also provide lock detect outputs. There is also a lock detect input pin (E4) which can be connected to the system UHF synthesiser and is then gated with the MGCM02 lock detect to give a combined lock detect output to the baseband controller via Lock Detect output pin (C5). This logic can use either the receive or transmit lock detect which is selected via the serial bus.

Programming

The MGCM02 features very flexible programming via a 3 wire serial bus. Data is clocked in 24 bit words with a latch pulse following the final data bit (see fig 7). The latch input must be held low at all other times.

The serial bus not only programmes the modes of operation but also enables unused sections of the device to be powered on and off as required. This is particularly important in a TDMA system when the phone does not receive or transmit all of the time. An added feature is the PCA (Power Control Assert) pin which allows the MGCM02 to alternate between receive and transmit modes without reloading commands via the serial bus and gives more accurate timing.

Details of the serial bus are shown below. A total of 8 words can be programmed but some of these are for test purposes only and are not required in normal applications.

Bit	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Word 1	X	X	X	RXDIV <17:0>																		0	0	0
Word 2	X	X	X	TXDIV <17:0>																		0	0	1
Word 3	X	X	X	0	TLI	RLI	REFRX <14:0>															0	1	0
Word 4	X	X	X	0	0	TPP	REFTX <14:0>															0	1	1
Word 5	X	X	X	RPP	0	0	TPR <2:0>			RPR <2:0>			TCC	RTC	TCP <1:0>		RCO <1:0>		LDC	0	0	1	0	0
Word 6	X	X	X	X	X	X	X	TDC	X	0	TXG <2:0>			TXC	TX <1:0>		X	TC <3:0>				1	0	1
Word 7	X	X	X	0	0	0	PCS <3:0>				X	X	RSS	RX	X	CONT <3:0>				VPD	LOI	1	1	0
Word 8	CALCO <7:0>								LPC <1:0>		PDF <1:0>		RDC	TEST				0	VGA <2:0>			1	1	1

X	Not used
RXDIV	Receive Synthesiser (LO2) Divide Ratio
TXDIV	Transmit Synthesiser Divide Ratio
REFRX	Receive Synthesiser Reference Divide Ratio
REFTX	Transmit Synthesiser Reference Divide Ratio
RCP,TCP<1:0>	Receive, Transmit synthesiser Charge Pump Current control
RTC,TTC	Receive, Transmit synthesiser Charge Pump Tristate control
RPR,TPR<2:0>	Receive, Transmit synthesiser prescaler ratio
RPP,TPP	Receive, Transmit synthesiser phase detector polarity
TLI,RLI	Receive, Transmit lock detect invert
LDC	Lock Detect Select
TX<1,0>	Transmit Control
PCS<2:0>	Power Control System
RX	Receive Mode
LOI	Select low/high side LO
TXG<2:0>	Transmit Gain
RSS<2:0>	RSSI Control
CONT<3:0>	Receive Control
TXC	Transmit Calibrate
TC<3:0>	Transmit Calibrate control - set to 1000
CALCO<3:0>	Sets transmit cut off frequency - set to 00001100 for standard 25kHz cutoff
LPC	Set FM Audio filter cut off frequency
PDF	Enables additional FM Audio filtering
VPD	LO Oscillator power down
TDC	Selects transmit output bias voltage
RDC	Selects receive output bias voltage
VGA<2:0>	Selects VGA Mode - primarily used for test purposes

The programming will be described in more detail in the following sections. Serial bus timing is shown in figure 5.

Receive Programming

MGCM02 has two basic receive modes:

1. I/Q mode. The 60 kHz IF signal is mixed down to baseband I and Q signals. This mode is used for IS136 TDMA and may also be used for AMPS.

2. FM mode. The baseband I/Q path is powered down and the MGCM02 discriminator is used for demodulation. This mode can be used for AMPS.

These modes are selected by the RX mode bit - Word 7, Bit 11

RX	Mode
0	I / Q
1	FM

Additional control is provided by the receive control bits - Word 7 Bits 9:6. These program MGCM02 gain in I and Q mode and allow the input attenuator to be manually controlled.

CONT <3:0>				Mode
X	X	0	0	Gain +0dB
X	X	0	1	Gain +12dB
X	X	1	0	Gain +15dB
X	X	1	1	Gain +18dB
X	0	X	X	+/- 20kHz Bandwidth
X	1	X	X	+/- 16kHz Bandwidth
0	X	X	X	FM Low Gain
1	X	X	X	FM High Gain

Normally the standard gain setting of CONT<1:0> = 00 should be used. The extra gain is provided in the amplifier after the bandpass filter and the low pass baseband filter.

CONT<2> sets the bandwidth of the 60 kHz bandpass filter. The low bandwidth mode (CONT<2> = 1) should be used for FM mode however the higher bandwidth mode (+/-20 kHz) may be used in TDMA operation.

The FM gain control CONT<3> is inactive unless RSS <0> is set to 1 as described in the next section.

CONT<2> sets the bandwidth of the 60 kHz bandpass filter. The low bandwidth mode (CONT<2> = 1) should be used for FM mode however the higher bandwidth mode (+/-20 kHz) may be used in TDMA operation.

RSS allows manual control of the input attenuator in conjunction with CONT<3>.

RSS	Operation
0	Normal FM Mode
1	Manual 32 dB Gain Enable

LOI - Word 7 bit 3 - is used to select high side or low side LO injection for the downconverter to 60kHz. The internal 60 kHz I and Q signals are also reversed to take account of this and enable the image rejection to operate correctly.

LOI	Operation
0	High side LO
1	Low side LO

Extra post discriminator filtering can be programmed using LPC<1:0> and PDF<1:0> - Word 8 Bits 15-12. The PDF bits connect the switched capacitor baseband filters after the FM discriminator and are used to improve the discriminator output performance. The LPF bits allow the cut-off frequency to be reduced to 25 kHz. The LPC and PDF bits should only be used in FM mode. In TDMA mode they should be set to zero.

LPC <1:0>		Operation
0	0	Both filters 37.5kHz cut-off
0	1	Filter 2 - 37.5kHz, filter 1 - 25kHz
1	0	Filter 2 - 25kHz, filter 1 - 37.5kHz
1	1	Both filters 25kHz cut-off

PDF <1:0>		Operation
0	0	No extra filtering
0	1	Filter 1 only
1	0	Filter 2 only
1	1	Both filters

The dc level for the baseband I and Q outputs can be selected by RDC - Word 8 Bit 11

RDC	Operation
0	Output Bias = 1.25 Volts
1	Output Bias = Vdd/2

The VGA<2:0> - Word 8 Bits 5-3, are used to set FM gain mode and for test purposes.

VGAWD <2:0>			Operation
0	0	0	Standard Mode. AGC Control for TDMA, Fixed gain for FM
1	1	0	AGC Control for FM

The other states are used for test purposes. In TDMA mode VGAWD should always be set to 000.

Transmit Programming

MGCM02 has two basic transmit modes.

1. I / Q mode. I and Q signals from baseband digital to analog converter are filtered and buffered. This mode is used for IS136 TDMA.
2. FM Mode. This is used for direct FM modulation of transmit IF oscillator.

These modes are controlled by TX <1:0> - Word 6 Bits 9:8

TX <1:0>		Mode
0	0	TDMA
0	1	FM - Differential input
1	X	FM - Single-ended input

A calibration of the transmit filters can be initialised by setting TXC - Word 6 Bit 10 to 1. After calibration the internal register for this bit is reset to 0

The transmit gain can be programmed by TXG<2:0> - Word 6 Bits 13:11

TXG <2:0>			Gain (dB)
X	X	1	0
0	0	0	3
0	1	0	6
1	0	0	9
1	1	0	12

The dc level for the transmit I and Q outputs can be selected by TDC - Word 8 Bit 12

TDC	Operation
0	Output Bias = 1.25 Volts
1	Output Bias = Vdd/2

Transmit Calibration

This is initiated by setting TXC - Word 6 Bit 10 high. Calibration takes approximately 0.6ms. In order for the calibration to give the required cutoff, CALCO - Word 8 Bits 23:16 must be set to 00001100. The calibration code is then stored in TC<3:0> Word 6 Bits 6:3, and TXC is reset low. If TC<3:0> is overwritten then a further calibration is required.

Synthesisers

The receive and transmit synthesisers are a similar design and use identical programming. Each synthesiser includes a dual modulus (N,N+1) prescaler followed by 'A and M' counters giving a total divide ratio of MN + A.

M is a 11 bit number

A is a 7 bit number

N is the prescaler modulus - this can also be programmed.

The value of A must be less than N

The A and M values are combined to give the RXDIV, TXDIV values in Words 1 and 2.

Receive Synthesiser

M value is programmed in Word 1Bits 20:10

A value is programmed in Word 1 Bits 9:3

The reference divider REFRX, a 15 bit number, is programmed in Word 3 bits 17:3

The dual modulus prescaler is programmed by RPR<2:0> - Word 5 Bits 14:12

RPR <2:0>			Prescaler Ratio
0	X	X	8/9
1	0	0	16/17
1	0	1	32/33
1	1	0	64/65
1	1	1	128/129

Transmit Synthesiser

M value is programmed in Word 2 Bits 20:10

A value is programmed in Word 2 Bits 9:3

The reference divider REFTX, a 15 bit number, is programmed in Word 4 bits 17:3

The dual modulus prescaler is programmed by TPR<2:0> - Word 5 Bits 17:15

TPR <2:0>			Prescaler Ratio
0	X	X	8/9
1	0	0	16/17
1	0	1	32/33
1	1	0	64/65
1	1	1	128/129

Synthesiser Control

The transmit and receive synthesiser control programming is independent but has the same format.

Charge Pump Current

Four charge pump currents for each synthesiser can be programmed using RCP,TCP<1:0>. Word 5 bits 7:6 and bits 9:8. This allows additional flexibility when optimising loop filters and overall synthesiser performance.

RCP, TCP <1:0>		Current (μA)
0	0	496
0	1	176
1	0	96
1	1	16

Charge Pump Output control

The charge pump can be inverted using RPP -Word 5 Bit 20 for the receive synthesiser and TPP - Word 4 Bit 18 for the transmit synthesiser.

RPP, TPP	Mode
0	Normal
1	Inverted

The charge pump outputs can also be put into a high impedance inactive state using RTC,TTC - word 5 Bits 11,10. This can be used to minimise settling time when the synthesiser is idle for short periods

RTC, TTC	Mode
0	Normal
1	Tristate

Lock Detect Output Polarity

The Lock detect output polarity can be inverted using RLI, TLI - Word3 Bits 18,19. In normal operation lock detect outputs are high when locked.

RLI, TLI	Mode
0	Normal
1	Invert

Lock Detect Output Control

The receive or transmit lock detect output can be selected for gating with the UHF lock detect input using the LDC bit - Word 5 Bit 5. The gating for the total lock detect function is shown below. The RLI and TLI bits should be set to 0. The combined lock detect output is available on Pin 38

UHF LOCK	RX/TX LOCK	LOCK DET	Mode
0	X	0	UHF Unlocked
1	0	0	UHF Locked, Rx or Tx Unlocked
1	1	1	All PLLs Locked

MGCM02 Power Control

MGCM02 features flexible power control using the PCS<2:0> Word 7 - Bits 17:15 using the serial bus in conjunction with the PCA pin.

PCS <3:0>				Mode
0	0	0	0	Deep Sleep
0	1	0	0	Standby
0	0	1	0	TX
0	1	1	0	RX
0	0	0	1	Duplex
0	1	0	1	Alt Rx/Tx
0	0	1	1	RSSI On
0	1	1	1	RSSI Off
1	0	0	0	TX PLL ON
1	1	0	0	TX PLL OFF
1	0	1	0	RX PLL ON
1	1	1	0	RX PLL OFF

Description of Power Control Modes

Deep Sleep - In this mode all circuitry is powered down except the power control circuits.

Powerdown - As deep sleep but voltage reference circuits active. PLL and VCO circuit can still be active (see TX,RX PLL ON modes)

RX - Receive Channel powered on. Operates in conjunction with RX mode control.

TX - Transmit Channel powered on. Operates in conjunction with TX mode control.

Duplex - Receive and Transmit channels active.

Alt RX/TX - Receive and transmit under control of the PCA control. Receive on when PCA = 0, Transmit on when PCA = 1

RSSI on. RSSI circuitry is activated when receive mode subsequently selected. This mode must be

selected if RSSI is required in TDMA mode. The RSSI is always powered on in FM mode

RSSI off. RSSI circuitry off when TDMA receive mode selected. This is the default state in TDMA mode

TX PLL ON. Transmit PLL circuits remain powered on in powerdown mode.

TX PLL OFF. Transmit PLL circuits are powered off in powerdown mode.

RX PLL ON. Receive PLL and VCO circuits remain powered on in powerdown mode.

RX PLL OFF. Receive PLL and VCO circuits are powered off in powerdown mode.

These power control modes are activated by the PCA pin. The PCA pin must normally be held low whilst a power control instruction is loaded via the serial bus. The power mode is not activated however until the PCA line is taken high. This allows accurate timing of the power modes. The exception is the Alt RX/TX mode which is loaded while PCA is low. The receive and transmit modes can then be toggled with the PCA pin.

In addition the receive LO Oscillator can be powered down by setting VPD (Word 7 - Bit 4) to one. This allows the LO to be provided differentially from an external oscillator.

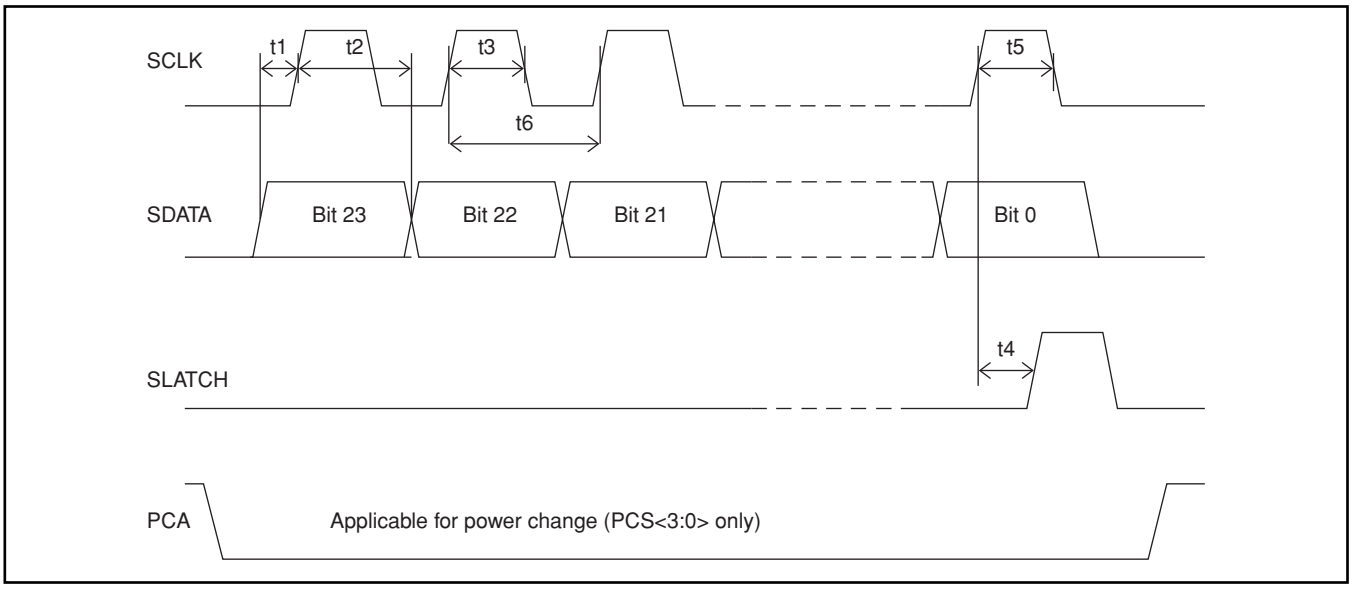


Figure 7 - Serial Programming

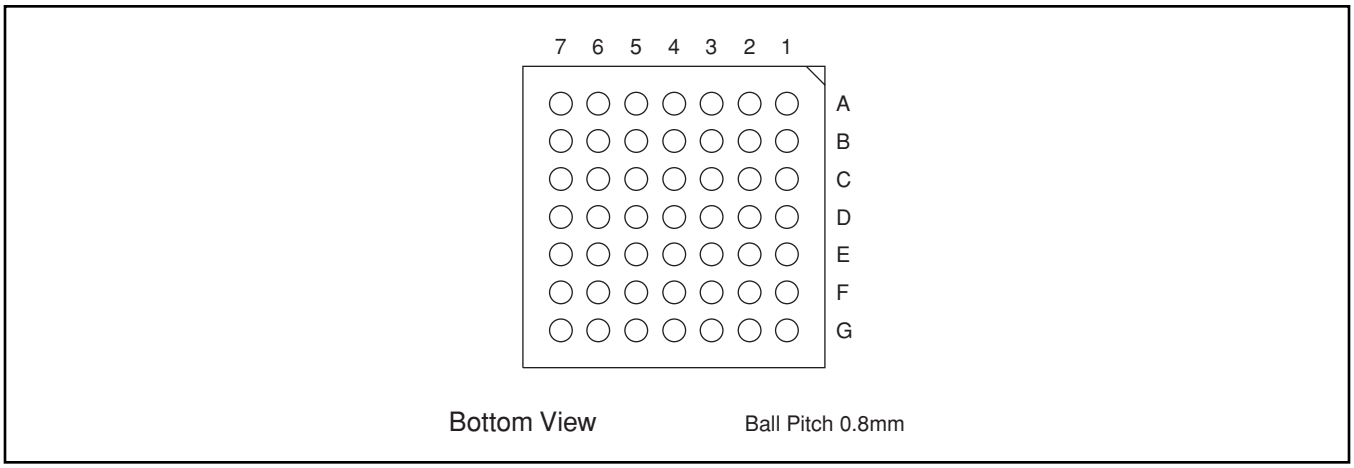


Figure 8 - Package Ball Layout

Applications Information

MGCM02 requires a minimal number of external components in a typical application. The TCXO input should be ac coupled using 10 nF capacitor. Internal currents in the device are set by a reference resistor connected from pin 48 to ground. The recommended value for this resistor is 100kΩ. External components on the discriminator and RSSI pins control the output characteristics of these functions. The recommended components are shown in figures 9 and 10.

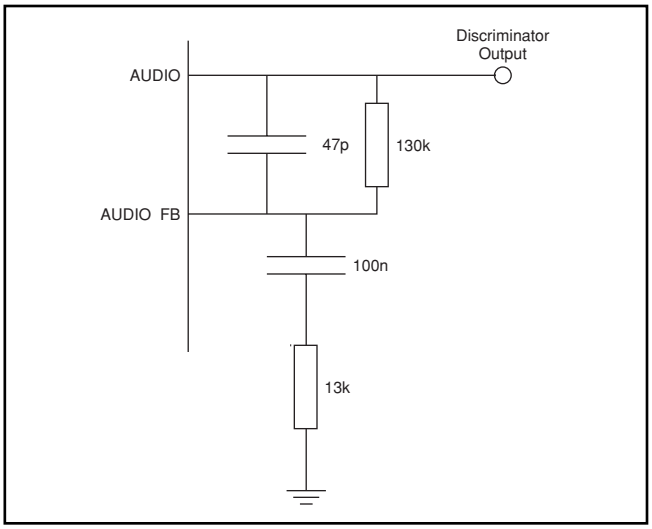


Figure 9 - Discrminator Output Components

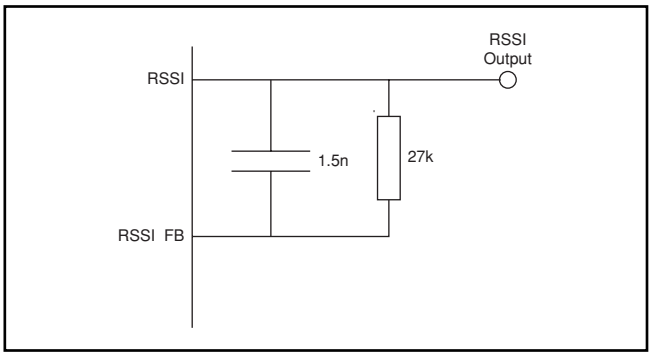


Figure 10 - RSSI Output Components

Fig 11 shows the external tank circuit required for the receive VCO. These components should be mounted as close as possible to the device. The actual component values will be dependent on the required operating frequency.

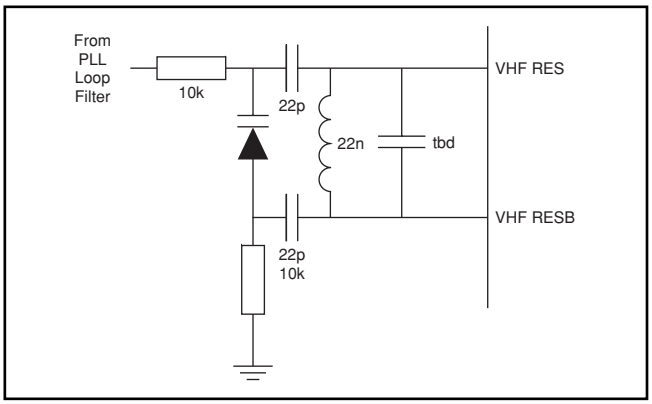


Figure 11 - External Tank Circuit

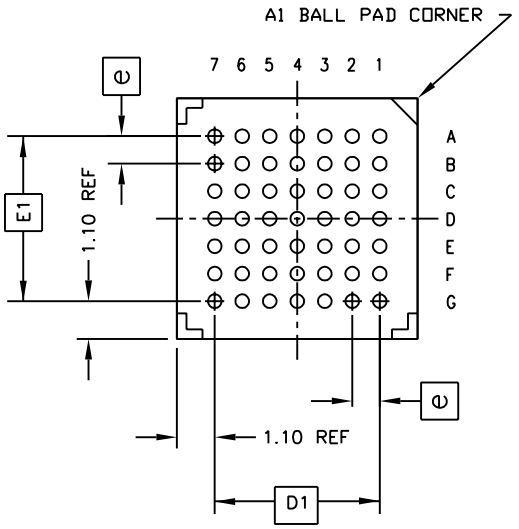
The MGCM02 transmit circuits are fully compatible with transmit products from Zarlink Semiconductor such as MGCT02 and MGCT04.

FM Operation in Fading Environment

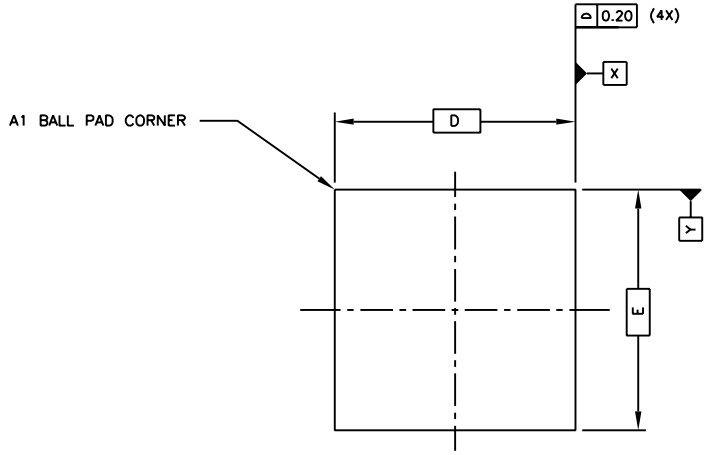
In a severe fading environment the FM performance is improved by operating in the AGC mode. This eliminates the switching transients using the fixed gain FM mode, when the gain is switched by 32.5 dB which can cause ringing and distortion in the bandpass filter.

The FM agc mode can be selected by setting VGAWD in Word 8 to '110'. The RSSI switching should be disabled by setting CONT<3> and RSS bits to '1'

At low signal levels the gain should be set as for the fixed gain FM mode (Pre-amp plus VGA = 26 dB), and the agc loop should not be activated until the RSSI output voltage is approximately 1.2 volts. This maintains optimum intermodulation performance and tolerance to 'down fades'.



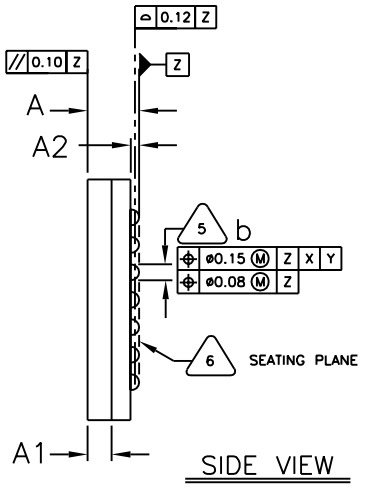
BOTTOM VIEW
(49 SOLDER BALLS)



TOP VIEW

DIMENSION	MIN	MAX
A	1.30	1.50
A1	0.65	0.75
A2	0.31	0.41
D	7.00 BSC	
D1	4.80 BSC	
E	7.00 BSC	
E1	4.80 BSC	
b	0.41	0.51
e	0.80 BSC	
N	49	
	2 LAYERS	

JEDEC No. to be confirmed



SIDE VIEW

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. DIMENSIONS IN MILLIMETERS.
3. NOT TO SCALE.
4. THE MAXIMUM ALLOWABLE NUMBER ("N") OF SOLDER BUMPS IS 49.
5. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. THE MAXIMUM SOLDER BALL MATRIX SIZE IS 7 X 7.
8. THE BASIC SOLDER BUMP GRID PITCH IS 0.80mm.

ISSUE	1	2		
ACN	208543	212492		
DATE	20Mar00	8Apr02		
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes
BP / G

Package Code GA

Package Outline for 49 lead PBGA (7 x 7mm)

GPD00720

For more information about all Zarlink products
visit our Web Site at

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