C67401 C67401A C67402 C67402A

First-In First-Out (FIFO)
64x4, 64x5 Cascadable Memory

Advanced Micro Devices

DISTINCTIVE CHARACTERISTICS

- **Choice of 15 and 10 MHz shift-out/shift-in rates**
- **Choice of 4-bit or 5-bit data width**
- **TTL inputs and outputs**
- **Readily expandable in the word and bit dimensions**
- **Structured pinouts. Output pins directly opposite corresponding input pins**
- **Asynchronous operation**

ORDERING INFORMATION

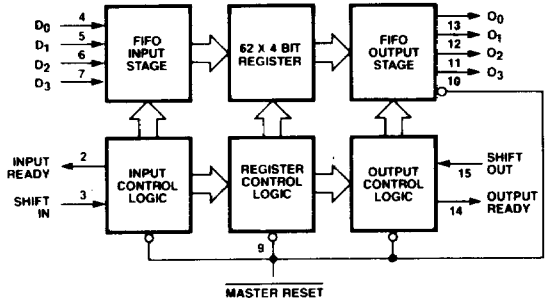
Part Number	Package	Temp	Description
C67401	CD 016,PD 016,PL 020	Com	10 MHz 64x4 FIFO
C67402	CD 018,PD 018,PL 020	Com	10 MHz 64x5 FIFO
C67401A	CD 016,PD 016,PL 020	Com	15 MHz 64x4 FIFO
C67402A	CD 018,PD 018,PL 020	Com	15MHz 64x5 FIFO

GENERAL DESCRIPTION

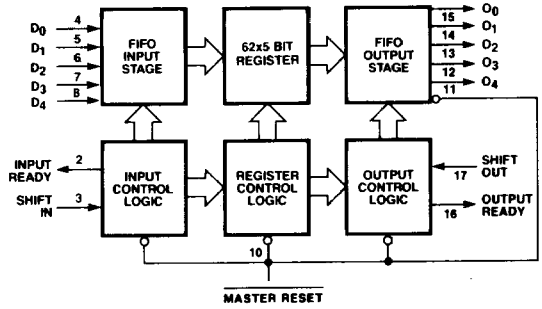
The C67401/2/1A/2A are "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4 bits and 64 words by 5 bits respectively. A 15 MHz data rate allows usage in high speed tape or disc controllers and communications buffer applications. Both word length and FIFO depth are expandable.

BLOCK DIAGRAMS

C67401A 64x4

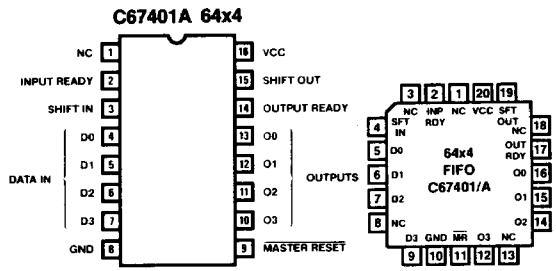


C67402A 64x5

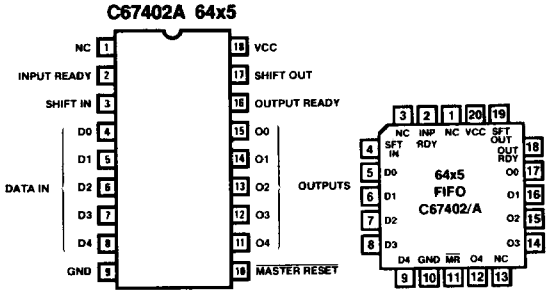


CONNECTION DIAGRAMS

C67401A 64x4



C67402A 64x5



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Issue Date: January 1989

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} .....–0.5 V to + 7.0 V
Input voltage .....–1.5 V to + 7.0 V
Off-state output voltage .....–0.5 V to + 5.5 V
Storage temperature .....–65°C to + 150°C

OPERATING CONDITIONS

Symbol	Parameter	Figure	C67401A/2A Min.	Typ.	Max.	C67401/2 Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	0		75	°C
t_{SIH}†	Shift in HIGH time	1	23			23			ns
t_{SIL}	Shift in LOW time	1	25			35			ns
t_{IDS}	Input data setup	1	0			0			ns
t_{IDH}	Input data hold time	1	40			45			ns
t_{SOH}†	Shift Out HIGH time	5	23			23			ns
t_{SOL}	Shift Out LOW time	5	25			35			ns
t_{MRW}	Master Reset pulse	10	35			35			ns
t_{MRS}	Master Reset to SI	10	35			35			ns

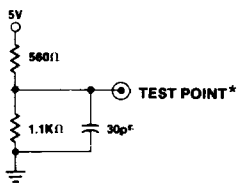
SWITCHING CHARACTERISTICS Over Operating Conditions

Symbol	Parameter	Figure	C67401A/2A Min.	Typ.	Max.	C67401/2 Min.	Typ.	Max.	Unit
f_{IN}	Shift In rate	1	15			10			MHz
t_{IRL}	Shift In to Input Ready LOW	1			40			45	ns
t_{IRH}	Shift In to Input Ready HIGH	1			40			45	ns
f_{OUT}	Shift Out rate	5	15			10			MHz
t_{ORL}†	Shift Out to Output Ready LOW	5			45			55	ns
t_{ORH}†	Shift Out to Output Ready HIGH	5			50			60	ns
t_{ODH}	Output Data Hold (previous word)	5	10			10			ns
t_{ODS}	Output Data Shift (next word)	5			45			55	ns
t_{PT}	Data throughput or "fall through"	4,8			1.6			3	µs
t_{MRORL}	Master Reset to OR LOW	10			60			60	ns
t_{MRIRH}	Master Reset to IR HIGH	10			60			60	ns
t_{IPH}	Input Ready pulse HIGH	4	23			23			ns
t_{OPH}*	Output Ready pulse HIGH	8	23			23			ns

† See AC test and High Speed application note.

*This parameter applies to FIFOs communicating with each other in a cascaded mode.

SWITCHING TEST CIRCUIT



Input Pulse 0 to 3 V
Input Rise and Fall Time (10% - 90%)
5 ns minimum
Measurements made at 1.5 V

* The "TEST POINT" is driven by the output under test, and observed by instrumentation.

DC CHARACTERISTICS Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}	Low-level input voltage						0.8†	V
V_{IH}	High-level input voltage				2†			V
V_{IC}	Input clamp voltage		V_{CC} = MIN	I_I = −18mA			−1.5	V
I_{IL1}	Low-level input current	D_0-D_n, $\overline{MR}$	V_{CC} = MAX	V_I = 0.45V			−0.8	mA
I_{IL2}		SI, SO					−1.6	mA
I_{IH}	High-level input current		V_{CC} = MAX	V_I = 2.4V			50	μA
I_I	Maximum input current		VCC = MAX	V_I = 5.5V			1	mA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8mA			0.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = −0.9mA	2.4			V
I_{OS}	Output short-circuit current *		V_{CC} = MAX	V_0 = 0V	−20		−90	mA
I_{CC}	Supply current		V_{CC} = MAX, All inputs low, All outputs open.	C67401†			160	mA
				C67402			180	
				C67401A			170	
				C6702A			190	

*Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
†There are absolute voltage with respect to device GND (Pin 8 or 9) and includes all overshoots due to test equipment

FUNCTIONAL DESCRIPTION

Data Input

After power up the Master Reset is pulsed low (Fig. 10) to prepare the FIFO to accept data in the first location. When Input Ready (IR) is HIGH the location is ready to accept data from the D_X inputs. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. The first word is present at the outputs before a shift out is applied. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front.

t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the O_X outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the FIFO is emptied, OR stays LOW, and O_X remains as before, (i.e. data does not change if FIFO is empty). Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

AC TEST AND HIGH-SPEED APP. NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. The internal shift rate of the FIFO typically exceeds 20 MHz in operation. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitance and/or poor supply decoupling and grounding. We recommend a monolithic ceramic capacitor of 0.1 μF directly between V_{CC} and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift In-Input Ready combination, as well as the Shift Out-Output Ready combination, timing measurements may be misleading, i.e. rising edge of the Shift-In pulse is not recognized until Input-Ready is High. If Input-Ready is not high due to too high a frequency or FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going High. This same type of problem is also related to t_{IRH}, t_{ORL} and t_{ORH} as related to Shift-Out.

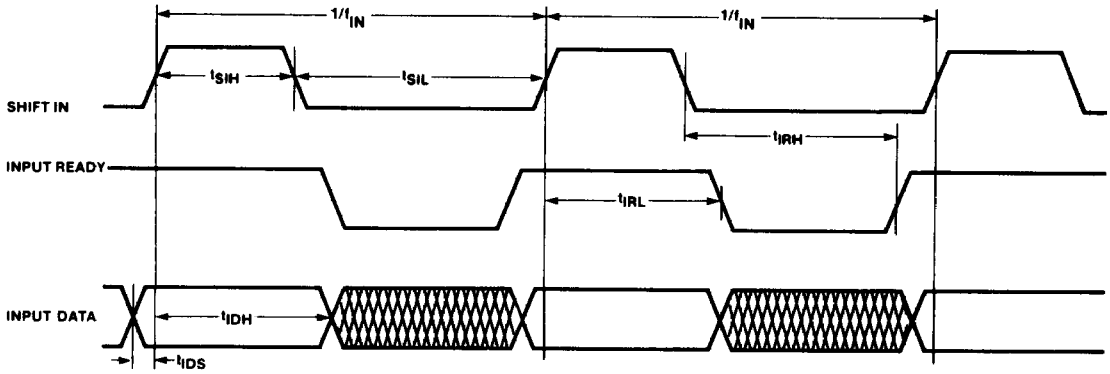


Figure 1. Input Timing

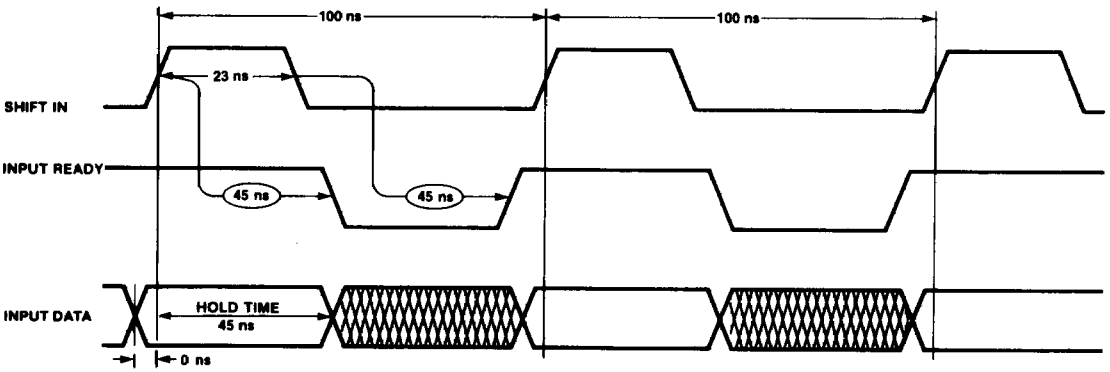


Figure 2. Typical Waveforms for 10 MHz Shift In Data Rate

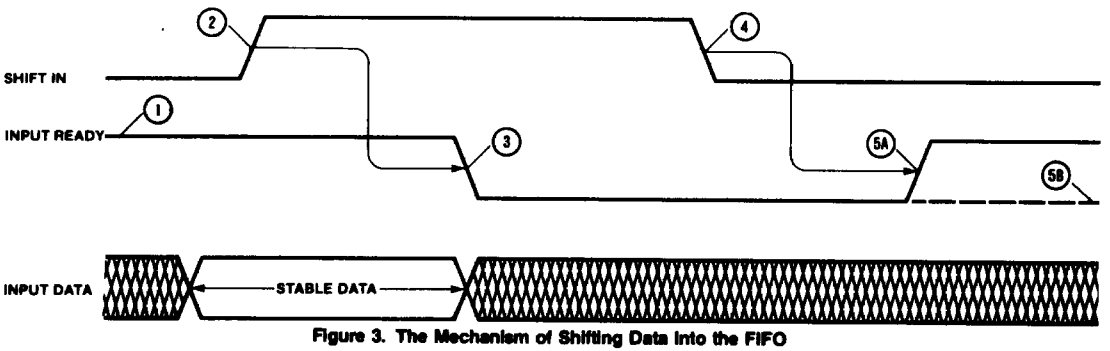


Figure 3. The Mechanism of Shifting Data into the FIFO

(1) Input Ready HIGH indicates space is available and a Shift In pulse may be applied.

(2) Input Data is loaded into the first word.

(3) Input Ready goes LOW indicating the first word is full.

(4) The Data from the first word is released for "fall-through" to second word.

(5A) The Data from the first word is transferred to second word. The first word is now empty as indicated by Input Ready HIGH.

(5B) If the second word is already full then the data remains at the first word. Since the FIFO is now full Input Ready remains low.

NOTE: Shift In pulses applied while Input Ready is LOW will be ignored (See Figure 4).

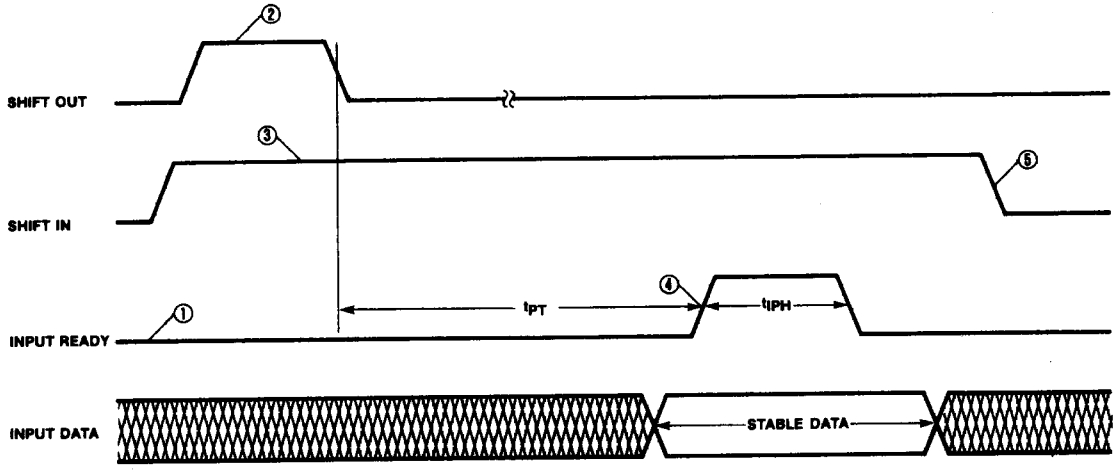
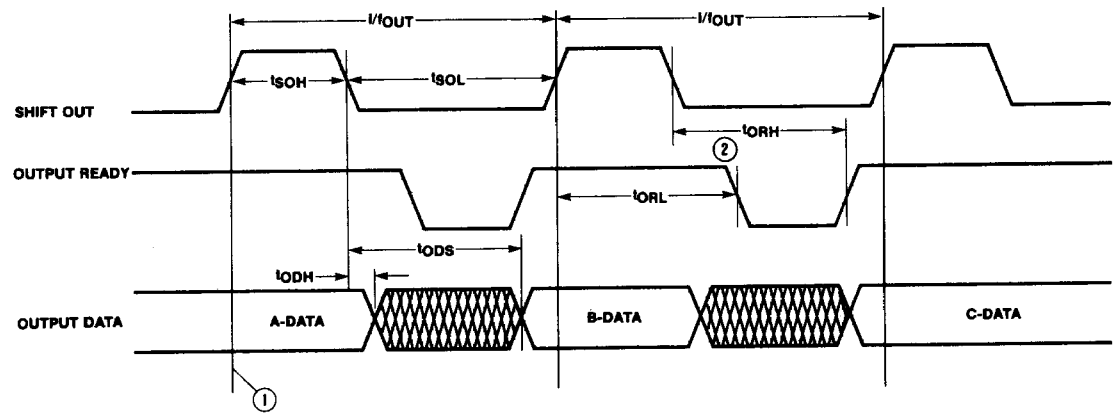


Figure 4. Data is Shifted in Whenever Shift In and Input Ready are Both HIGH

1. FIFO is initially full.
2. Shift Out pulse is applied. An empty location starts "bubbling" to the front.
3. Shift In is held HIGH
4. As soon as Input Ready becomes HIGH the Input Data is loaded into the first word.
5. The Data from the first word is released for "fall through" to second word.



1. The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.
2. Data is shifted out when Shift Out makes a HIGH to LOW transition.

Figure 5. Output Timing

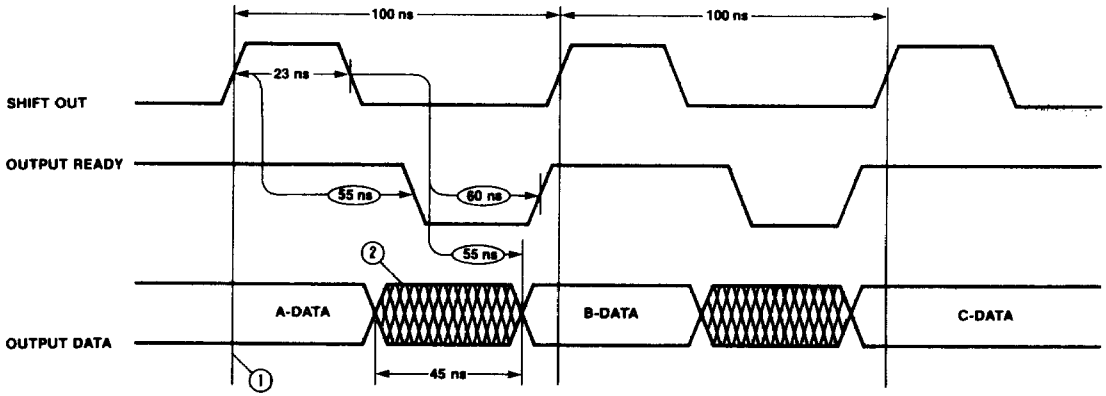


Figure 6. Typical Waveforms for 10 MHz Shift Out Data Rate

(1) The diagram assumes, that at this time, words 63, 62, 61 are loaded with A, B, C Data, respectively.

(2) Data in the crosshatched region may be A or B Data.

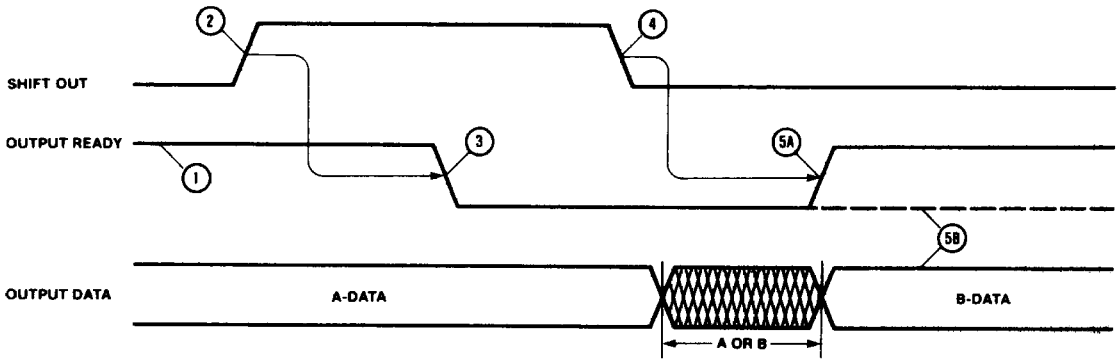


Figure 7. The Mechanism of Shifting Data Out of the FIFO.

(1) Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied.

(2) Shift Out goes HIGH causing the next step.

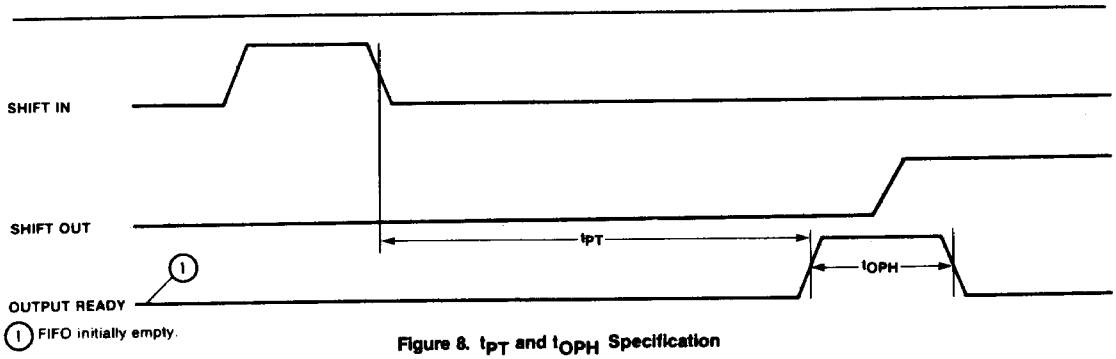
(3) Output Ready goes LOW.

(4) Contents of word 62 (B-DATA) is released for "fall through" to word 63.

(5A) Output Ready goes HIGH indicating that new data (B) is now available at the FIFO outputs.

(5B) If the FIFO has only one word loaded (A-DATA) then Output Ready stays LOW and the A-DATA remains unchanged at the outputs.

NOTE: Shift Out pulses applied when Output Ready is LOW will be ignored.



1 FIFO initially empty.

Figure 8. t_{PT} and t_{OPH} Specification

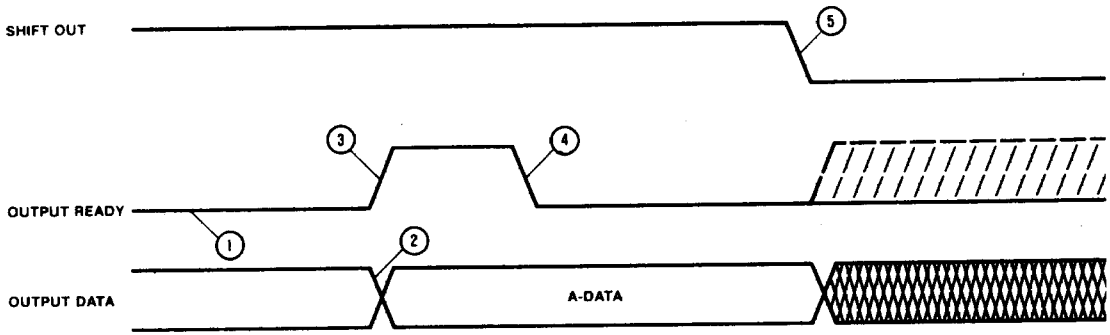
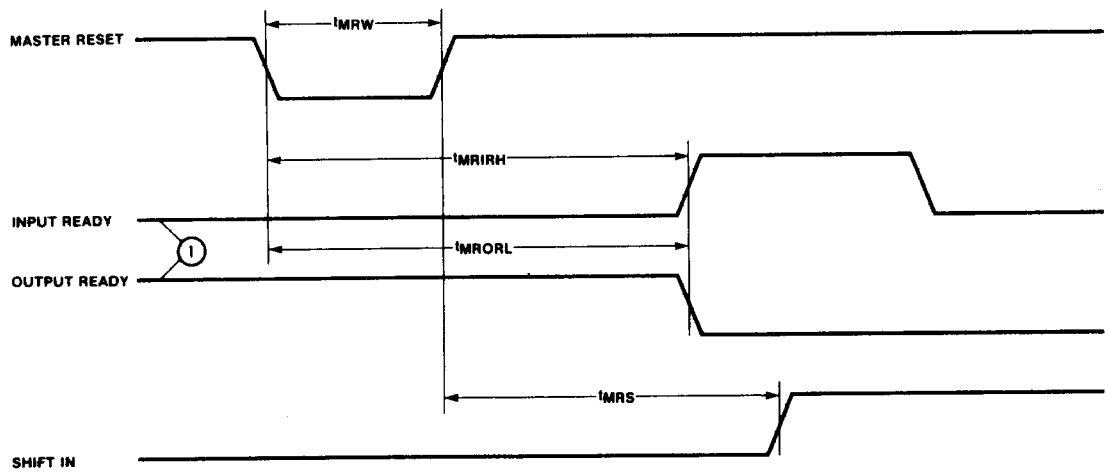


Figure 9. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH.

1. Word 63 is empty.
2. New data (A) arrives at the outputs (word 63).
3. Output Ready goes HIGH indicating the arrival of the new data.
4. Since Shift Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift Out goes LOW the Output Data is subject to change as shown by the dashed line on Output Ready.



1 FIFO initially full.

Figure 10. Master Reset Timing

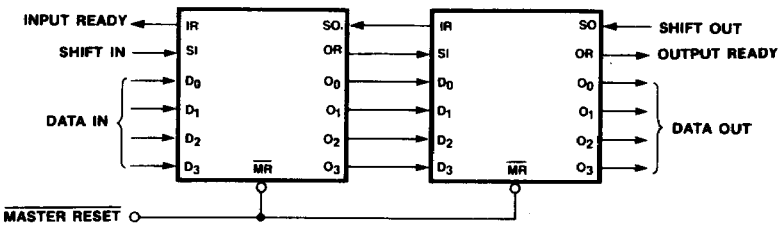


Figure 11. Cascading FIFOs to Form 128x4 FIFO with C5/C67401A/1

FIFOs can be easily cascaded to any desired depth. The handshaking and associated timing between the FIFOs are handled by the FIFOs themselves.

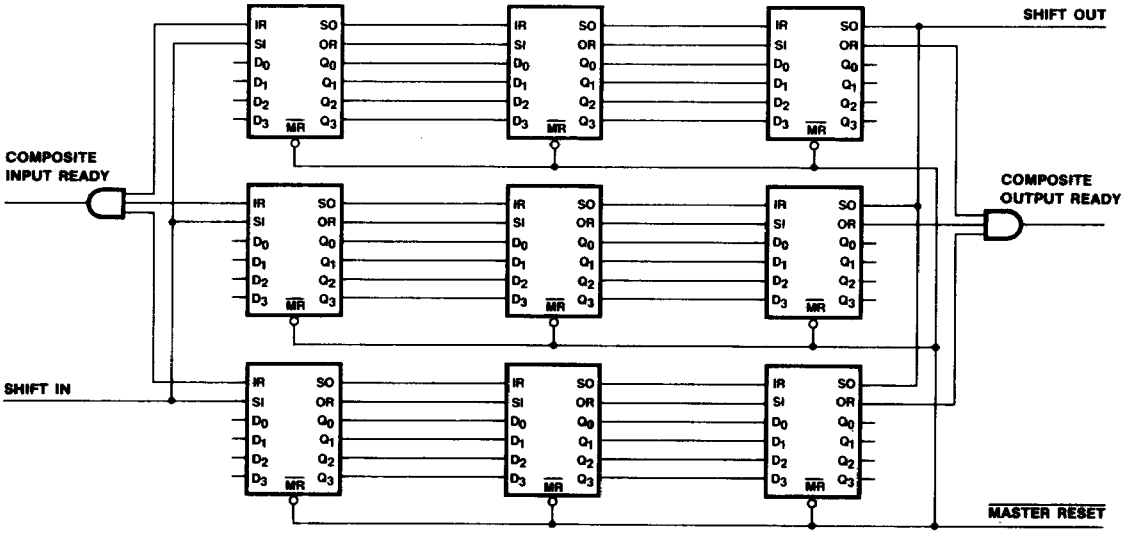
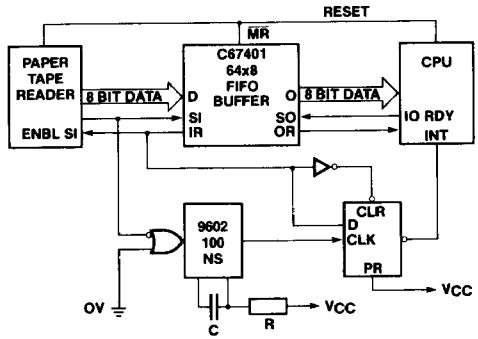


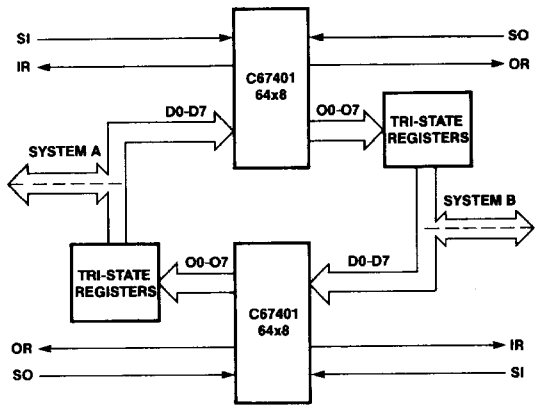
Figure 12. 192x12 FIFO with C5/C67401/1A

FIFOs are expandable in depth and width. However, in forming wider words two external gates are required to generate composite Input and Output Ready flags. This need is due to the different fall-through times of the FIFOs.



NOTE: The output of monostable holds off the "Buffer full" interrupt for 100ns. If 100ns after shift in, there has not been an input Ready to reset the "D Flip-flop" an interrupt is issued, as the FIFO is full. The CPU then empties the FIFO before the next character is output from the tape drive.

Figure 13. Slow Steady Rate to Fast "Blocked" Rate



NOTE: Both depth and width expansion can be used in this mode. The IR and OR signals are the anded versions of the individual IR and OR signals.

Figure 14. Bidirectional FIFO Application