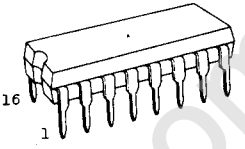
TC4076BP

C²MOS DIGITAL INTEGRATED CIRCUIT
SILICON MONOLITHIC

TC4076BP 4-BIT D-TYPE REGISTER

TC4076BP is the register which consists of four D type flip-flops having 3-stage outputs, and these four flip-flops are controlled by common CLOCK input and RESET input.
When both of INPUT DISABLE inputs G1 and G2 are at "L", data inputs D1 through D4 are stored in F/F's at the rising edge of CLOCK input, and with other combination of G1 and G2, the previous conditions of F/F's are retained even if the rising edge of CLOCK occurs. When both of OUTPUT DISABLE inputs M and N are at "L", the outputs of flip-flops appear at Q1 through Q4 outputs, and with any other combinations of M and N, the outputs have high impedance. RESET is active with "H" level.

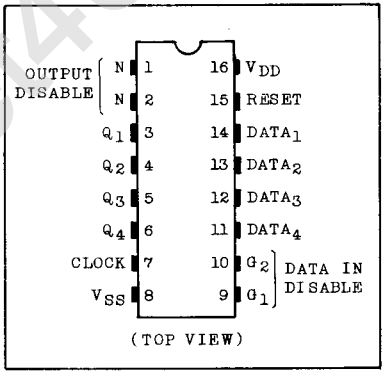


DIP 16(3D16A-P)

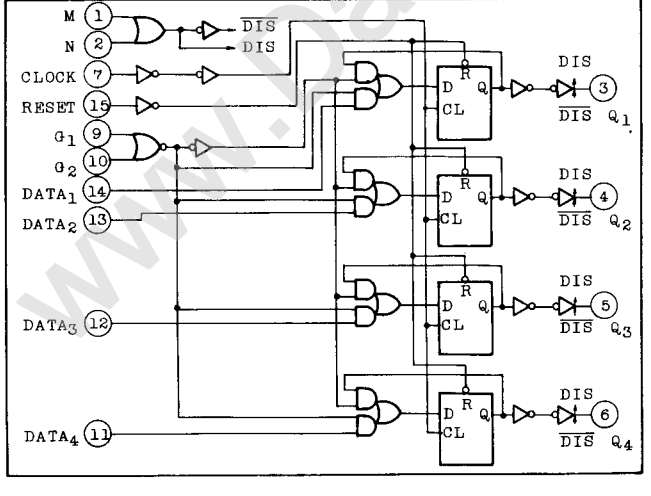
MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V_{DD}	V_{SS}-0.5 ~ V_{SS}+20	V
Input Voltage	V_{IN}	V_{SS}-0.5 ~ V_{DD}+0.5	V
Output Voltage	V_{OUT}	V_{SS}-0.5 ~ V_{DD}+0.5	V
DC Input Current	I_{IN}	±10	mA
Power Dissipation	P_D	300	mW
Operating Temperature Range	T_A	-40 ~ 85	°C
Storage Temperature Range	T_{stg}	-65 ~ 150	°C
Lead Temp./Time	T_{sol}	260°C · 10 sec	

PIN ASSIGNMENT



LOGIC DIAGRAM



TRUTH TABLE

RESET	CLOCK	DATA IN DISABLE G_1	DATA IN DISABLE G_2	DATA	OUTPUT DISABLE M	OUTPUT DISABLE N	Q_{n+1}
*	*	*	*	*	H	*	HZ
*	*	*	*	*	*	H	HZ
H	*	*	*	*	L	L	L
L	L	*	*	*	L	L	Q_n
L	↓	H	*	*	L	L	Q_n
L	↓	*	H	*	L	L	Q_n
L	↓	L	L	H	L	L	H
L	↓	L	L	L	L	L	L
L	H	*	*	*	L	L	Q_n
L	↓	*	*	*	L	L	Q_n

Q_{n+1} : NEXT STATE of Q_n
HZ : HIGH IMPEDANCE
* : Don't care

RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V_{DD}		3	-	18	V
Input Voltage	V_{IN}		0	-	V_{DD}	V

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{CC} (V)	-40°C MIN.	-40°C MAX.	25°C MIN.	25°C TYP.	25°C MAX.	85°C MIN.	85°C MAX.	UNIT
High-Level Output Voltage	V_{OH}	$\|I_{OUT}\|<1\mu A$	5	4.95	-	4.95	5.00	-	4.95	-	V
		$V_{IN}=V_{SS},V_{DD}$	10	9.95	-	9.95	10.00	-	9.95	-	
			15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage	V_{OL}	$\|I_{OUT}\|<1\mu A$	5	-	0.05	-	0.00	0.05	-	0.05	
		$V_{IN}=V_{SS},V_{DD}$	10	-	0.05	-	0.00	0.05	-	0.05	
			15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current	I_{OH}	V_{OH}=4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
		V_{OH}=2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
		V_{OH}=9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
		V_{OH}=13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Output Low Current	I_{OL}	V_{OL}=0.4V	5	0.61	-	0.51	1.5	-	0.42	-	
		V_{OL}=0.5V	10	1.5	-	1.3	3.8	-	1.1	-	
		V_{OL}=1.5V	15	4.0	-	3.4	15.0	-	2.8	-	
		$V_{IN}=V_{SS},V_{DD}$									
Input High Voltage	V_{IH}	V_{OUT}=0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
		V_{OUT}=1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
		V_{OUT}=1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
		$\|I_{OUT}\|<1\mu A$									
Input Low Voltage	V_{IL}	V_{OUT}=0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
		V_{OUT}=1.0V, 9.0V	10	-	3.0	-	4.5	3.0	-	3.0	
		V_{OUT}=1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
		$\|I_{OUT}\|<1\mu A$									
Input Current "H" Level	I_{IH}	V_{IH}=18V	18	-	0.1	-	10^{-5}	0.1	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	18	-	-0.1	-	-10^{-5}	-0.1	-	-1.0	

STATIC ELECTRICAL CHARACTERISTICS (V_{SS}=0V)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V_{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
3-State Output Leakage Current	"H" Level	I_{DH}	V_{OUT}=18V	18	-	0.4	-	10^{-4}	0.4	-	12	μA
	"L" Level	I_{DL}	V_{OUT}=0V	18	-	-0.4	-	-10^{-4}	-0.4	-	-12	
Quiescent Device Current		I_{DD}	V_{IN}=V_{SS}, V_{DD} *	5	-	5	-	0.005	5	-	150	μA
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

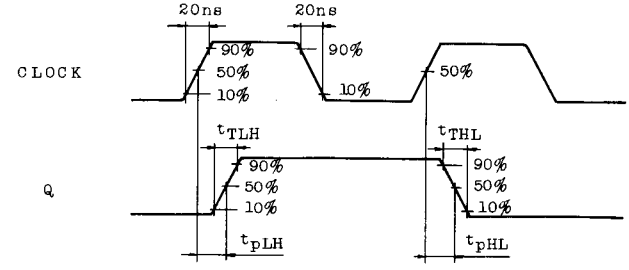
CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Output Transition Time (Low to High)	t_{TLH}		5	-	80	200	ns
			10	-	50	100	
			15	-	40	80	
Output Transition Time (High to Low)	t_{THL}		5	-	80	200	
			10	-	50	100	
			15	-	40	80	
Propagation Delay Time (CLOCK - Q)	t_{pLH} t_{pHL}		5	-	250	600	ns
			10	-	95	250	
			15	-	65	180	
Propagation Delay Time (RESET - Q)	t_{pHL}		5	-	230	460	ns
			10	-	90	200	
			15	-	60	150	
Three State Disable Time (OUTPUT DISABLE - Q)	t_{pHZ} t_{pLZ}	R_L=1kΩ	5	-	100	300	ns
			10	-	45	120	
			15	-	35	90	
Three State Disable Time (OUTPUT DISABLE - Q)	t_{pZH} t_{pZL}	R_L=1kΩ	5	-	110	300	
			10	-	40	150	
			15	-	30	120	
Max. Clock Frequency	f_{CL}		5	3	7	-	MHz
			10	6	21	-	
			15	8	24	-	

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, V_{SS}=0V, C_L=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V_{DD}(V)	MIN.	TYP.	MAX.	UNIT
Min. Clock Pulse Width	t_W		5	-	70	200	ns
			10	-	25	100	
			15	-	20	80	
Min. Pulse Width (RESET)	t_{WH}		5	-	100	200	ns
			10	-	40	80	
			15	-	30	60	
Max. Clock Input Rise Time. Max. Clock Input Fall Time.	t_{rCL} t_{fCL}		5	20	-	-	μs
			10	2.5	-	-	
			15	1.0	-	-	
Min. Set-up Time (DATA - CLOCK)	t_{SU}		5	-	75	150	ns
			10	-	30	60	
			15	-	20	40	
Min. Set-up Time (DATA INPUT DISABLE - CLOCK)	t_{SU}		5	-	100	200	ns
			10	-	40	80	
			15	-	25	50	
Min. Hold Time (DATA - CLOCK)	t_H		5	-	-	135	ns
			10	-	-	60	
			15	-	-	50	
Input Capacitance	C_{IN}			-	5	7.5	pF

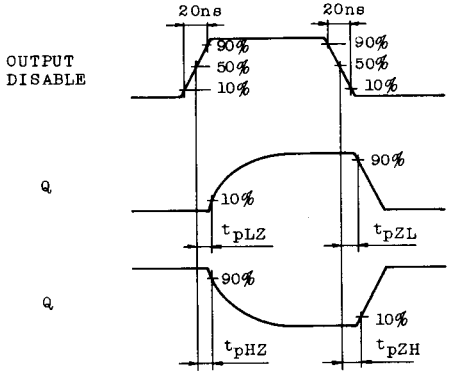
WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 1

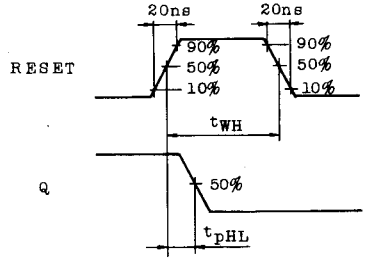


WAVEFORM FOR MEASUREMENT OF DYNAMIC CHARACTERISTICS

WAVEFORM 2



WAVEFORM 3



WAVEFORM 4