



# CAT28F001

1 Megabit CMOS Boot Block Flash Memory

Licensed Intel  
second source



## FEATURES

- Fast Read Access Time: 90/120 ns
- On-Chip Address and Data Latches
- Blocked Architecture
  - One 8 KB Boot Block w/ Lock Out
    - Top or Bottom Locations
  - Two 4 KB Parameter Blocks
  - One 112 KB Main Block
- Low Power CMOS Operation
- 12.0V ± 5% Programming and Erase Voltage
- Automated Program & Erase Algorithms
- High Speed Programming
- Commercial, Industrial and Automotive Temperature Ranges
- Deep Powerdown Mode
  - 0.05  $\mu\text{A}$   $I_{CC}$  Typical
  - 0.8  $\mu\text{A}$   $I_{PP}$  Typical
- Hardware Data Protection
- Electronic Signature
- 100,000 Program/Erase Cycles and 10 Year Data Retention
- JEDEC Standard Pinouts:
  - 32 pin DIP
  - 32 pin PLCC
  - 32 pin TSOP
- Reset/Deep Power Down Mode
- "Green" Package Options Available

## DESCRIPTION

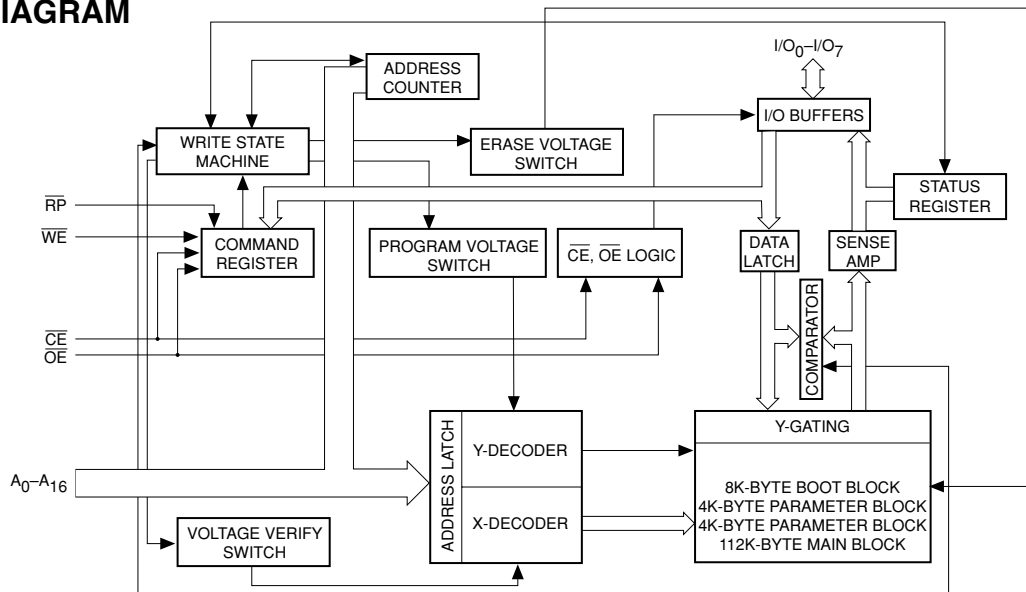
The CAT28F001 is a high speed 128K X 8 bit electrically erasable and reprogrammable Flash memory ideally suited for applications requiring in-system or after sale code updates.

The CAT28F001 has a blocked architecture with one 8 KB Boot Block, two 4 KB Parameter Blocks and one 112 KB Main Block. The Boot Block section can be at the top or bottom of the memory map and includes a reprogramming write lock out feature to guarantee data integrity. It is designed to contain secure code which will bring up the system minimally and download code to other locations of CAT28F001.

The CAT28F001 is designed with a signature mode which allows the user to identify the IC manufacturer and device type. The CAT28F001 is also designed with on-Chip Address Latches, Data Latches, Programming and Erase Algorithms.

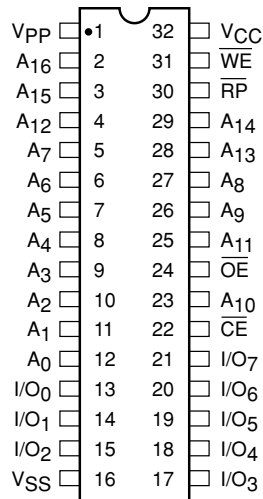
The CAT28F001 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles and has a data retention of 10 years. The device is available in JEDEC approved 32-pin plastic DIP, PLCC or TSOP packages.

## BLOCK DIAGRAM

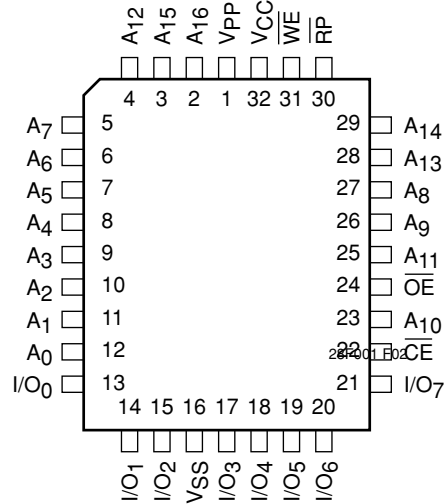


## PIN CONFIGURATION

**DIP Package (P, L)**



**PLCC Package (N, G)**



**TSOP Package (Standard Pinout) (T, H)**



## PIN FUNCTIONS

Pin Name	Type	Function
A <sub>0</sub> –A <sub>16</sub>	Input	Address Inputs for memory addressing
I/O <sub>0</sub> –I/O <sub>7</sub>	I/O	Data Input/Output
CE	Input	Chip Enable
OE	Input	Output Enable
WE	Input	Write Enable
V <sub>CC</sub>		Voltage Supply
V <sub>SS</sub>		Ground
V <sub>PP</sub>		Program/Erase Voltage Supply
RP	Input	Power Down

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	-55°C to +95°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground <sup>(1)</sup> .....	-2.0V to +V <sub>CC</sub> + 2.0V (Except A <sub>9</sub> , $\overline{RP}$ , $\overline{OE}$ , V <sub>CC</sub> and V <sub>PP</sub> )
Voltage on Pin A <sub>9</sub> , $\overline{RP}$ AND $\overline{OE}$ with Respect to Ground <sup>(1)</sup> .....	-2.0V to +13.5V
V <sub>PP</sub> with Respect to Ground during Program/Erase <sup>(1)</sup> .....	-2.0V to +14.0V
V <sub>CC</sub> with Respect to Ground <sup>(1)</sup> .....	-2.0V to +7.0V
Package Power Dissipation Capability (T <sub>A</sub> = 25°C) .....	1.0 W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(2)</sup> .....	100 mA

**\*COMMENT**

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units	Test Method
N <sub>END</sub> <sup>(3)</sup>	Endurance	100K		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(3)</sup>	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(3)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(3)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

**CAPACITANCE** T<sub>A</sub> = 25°C, f = 1.0 MHz

Symbol	Test	Limits		Units	Conditions
		Min	Max.		
C <sub>IN</sub> <sup>(3)</sup>	Input Pin Capacitance		8	pF	V <sub>IN</sub> = 0V
C <sub>OUT</sub> <sup>(3)</sup>	Output Pin Capacitance		12	pF	V <sub>OUT</sub> = 0V
C <sub>VPP</sub> <sup>(3)</sup>	V <sub>PP</sub> Supply Capacitance		25	pF	V <sub>PP</sub> = 0V

**Note:**

- (1) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> + 0.5V, which may overshoot to V<sub>CC</sub> + 2.0V for periods of less than 20ns.
- (2) Output shorted for no more than one second. No more than one output shorted at a time.
- (3) This parameter is tested initially and after a design or process change that affects the parameter.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> + 1V.

**D.C. OPERATING CHARACTERISTICS**

$V_{CC} = +5V \pm 10\%$ , unless otherwise specified

Symbol	Parameter	Limits			Test Conditions
		Min.	Max.	Unit	
$I_{LI}$	Input Leakage Current		$\pm 1.0$	$\mu A$	$V_{IN} = V_{CC}$ or $V_{SS}$ $V_{CC} = 5.5V$
$I_{LO}$	Output Leakage Current		$\pm 10$	$\mu A$	$V_{OUT} = V_{CC}$ or $V_{SS}$ , $V_{CC} = 5.5V$
$I_{SB1}$	$V_{CC}$ Standby Current CMOS		100	$\mu A$	$\overline{CE} = V_{CC} \pm 0.2V = \overline{RP}$ $V_{CC} = 5.5V$
$I_{SB2}$	$V_{CC}$ Standby Current TTL		1.5	mA	$\overline{CE} = \overline{RP} = V_{IH}$ , $V_{CC} = 5.5V$
$I_{PPD}$	$V_{PP}$ Deep Powerdown Current		1.0	$\mu A$	$\overline{RP} = GND \pm 0.2V$
$I_{CC1}$	$V_{CC}$ Active Read Current		30	mA	$V_{CC} = 5.5V$ , $\overline{CE} = V_{IL}$ , $I_{OUT} = 0mA$ , $f = 8 MHz$
$I_{CC2}^{(1)}$	$V_{CC}$ Programming Current		20	mA	$V_{CC} = 5.5V$ , Programming in Progress
$I_{CC3}^{(1)}$	$V_{CC}$ Erase Current		20	mA	$V_{CC} = 5.5V$ , Erase in Progress
$I_{PPS}$	$V_{PP}$ Standby Current		$\pm 10$	$\mu A$	$V_{PP} \leq V_{CC}$
			200	$\mu A$	$V_{PP} > V_{CC}$
$I_{PP1}$	$V_{PP}$ Read Current		200	$\mu A$	$V_{PP} = V_{PPH}$
$I_{PP2}^{(1)}$	$V_{PP}$ Programming Current		30	mA	$V_{PP} = V_{PPH}$ , Programming in Progress
$I_{PP3}^{(1)}$	$V_{PP}$ Erase Current		30	mA	$V_{PP} = V_{PPH}$ , Erase in Progress
$V_{IL}$	Input Low Level	-0.5	0.8	V	
$V_{OL}$	Output Low Level		0.45	V	$I_{OL} = 5.8mA$ , $V_{CC} = 4.5V$
$V_{IH}$	Input High Level	2.0	$V_{CC} + 0.5$	V	
$V_{OH}$	Output High Level	2.4		V	$I_{OH} = 2.5mA$ , $V_{CC} = 4.5V$
$V_{ID}$	$A_9$ Signature Voltage	11.5	13.0	V	$A_9 = V_{ID}$
$I_{ID}$	$A_9$ Signature Current		500	$\mu A$	$A_9 = V_{ID}$
$I_{CCD}$	$V_{CC}$ Deep Powerdown Current		1.0	$\mu A$	$\overline{RP} = GND \pm 0.2V$
$I_{CCES}$	$V_{CC}$ Erase Suspend Current		10	mA	Erase Suspended $\overline{CE} = V_{IH}$
$I_{PPES}$	$V_{PP}$ Erase Suspend Current		300	$\mu A$	Erase Suspended $V_{PP} = V_{PPH}$

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**SUPPLY CHARACTERISTICS**

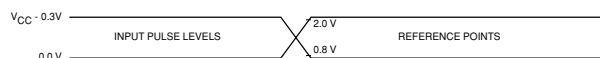
Symbol	Parameter	Limits		Unit
		Min	Max.	
V <sub>LKO</sub>	V <sub>CC</sub> Erase/Write Lock Voltage	2.5		V
V <sub>CC</sub>	V <sub>CC</sub> Supply Voltage	4.5	5.5	V
V <sub>PP</sub>	V <sub>PP</sub> During Read Operations	0	6.5	V
V <sub>PPH</sub>	V <sub>PP</sub> During Erase/Program	11.4	12.6	V
V <sub>HH</sub>	$\overline{RP}$ , $\overline{OE}$ Unlock Voltage	11.4	12.6	V

**A.C. CHARACTERISTICS, Read Operation**

V<sub>CC</sub> = +5V ±10%, unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	28F001-90 <sup>(7)</sup>		28F001-12 <sup>(7)</sup>		Units
			Min	Max	Min	Max	
t <sub>AVAV</sub>	t <sub>RC</sub>	Read Cycle Time	90		120		ns
t <sub>ELQV</sub>	t <sub>CE</sub>	$\overline{CE}$ Access Time		90		120	ns
t <sub>AVQV</sub>	t <sub>ACC</sub>	Address Access Time		90		120	ns
t <sub>GLQV</sub>	t <sub>OE</sub>	$\overline{OE}$ Access Time		35		50	ns
-	t <sub>OH</sub>	Output Hold from Address $\overline{OE}/\overline{CE}$ Change	0		0		ns
t <sub>GLQX</sub>	t <sub>OLZ</sub> <sup>(1)(6)</sup>	$\overline{OE}$ to Output in Low-Z	0		0		ns
t <sub>ELQX</sub>	t <sub>LZ</sub> <sup>(1)(6)</sup>	$\overline{CE}$ to Output in Low-Z	0		0		ns
t <sub>GHQZ</sub>	t <sub>DF</sub> <sup>(1)(2)</sup>	$\overline{OE}$ High to Output High-Z		30		30	ns
t <sub>EHQZ</sub>	t <sub>HZ</sub> <sup>(1)(2)</sup>	$\overline{CE}$ High to Output High-Z		35		55	ns
t <sub>PHQV</sub>	t <sub>PWH</sub>	$\overline{RP}$ High to Output Delay		600		600	ns

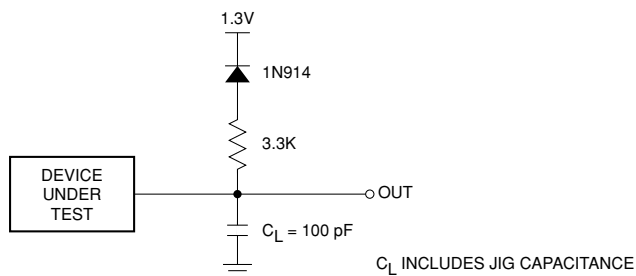
**Figure 1. A.C. Testing Input/Output Waveform<sup>(3)(4)(5)</sup>**



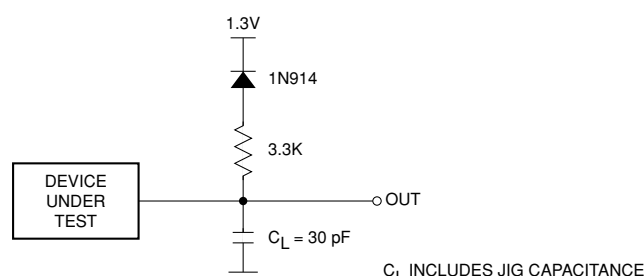
**Figure 2. Highspeed A.C. Testing Input/Output Waveform<sup>(3)(4)(5)</sup>**



**Testing Load Circuit (example)**



**Testing Load Circuit (example)**



Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) Output floating (High-Z) is defined as the state where the external data line is no longer driven by the output buffer.
- (3) Input Rise and Fall Times (10% to 90%) < 10 ns.
- (4) Input Pulse Levels = 0.45V and 2.4V. For High Speed Input Pulse Levels 0.0V and 3.0V.
- (5) Input and Output Timing Reference = 0.8V and 2.0V. For High Speed Input and Output Timing Reference = 1.5V.
- (6) Low-Z is defined as the state where the external data may be driven by the output buffer but may not be valid.
- (7) For load and reference points, see Fig. 1

## A.C. CHARACTERISTICS, Program/Erase Operation

 $V_{CC} = +5V \pm 10\%$ 

JEDEC Symbol	Standard Symbol	Parameter	28F001-90		28F001-12		Units
			Min	Max	Min	Max	
t <sub>AVAV</sub>	t <sub>WC</sub>	Write Cycle Time	90		120		ns
t <sub>AVWH</sub>	t <sub>AS</sub>	Address Setup to $\overline{WE}$ Going High	40		40		ns
t <sub>WHAX</sub>	t <sub>AH</sub>	Address Hold Time from $\overline{WE}$ Going High	10		10		ns
t <sub>DVWH</sub>	t <sub>DS</sub>	Data Setup Time to $\overline{WE}$ Going High	40		40		ns
t <sub>WHDX</sub>	t <sub>DH</sub>	Data Hold Time from $\overline{WE}$ Going High	10		10		ns
t <sub>ELWL</sub>	t <sub>CS</sub>	$\overline{CE}$ Setup Time to $\overline{WE}$ Going Low	0		0		ns
t <sub>WHEH</sub>	t <sub>CH</sub>	$\overline{CE}$ Hold Time from $\overline{WE}$ Going High	0		0		ns
t <sub>WLWH</sub>	t <sub>WP</sub>	$\overline{WE}$ Pulse Width	40		40		ns
t <sub>WHWL</sub>	t <sub>WPH</sub>	$\overline{WE}$ High Pulse Width	10		10		ns
t <sub>WHGL</sub>	—	Write Recovery Time Before Read	0		0		μs
t <sub>PHWL</sub>	t <sub>PS</sub> <sup>(1)</sup>	$\overline{RP}$ High Recovery to $\overline{WE}$ Going Low	480		480		ns
t <sub>PHHWH</sub>	t <sub>PHS</sub> <sup>(1)</sup>	$\overline{RP} V_{HH}$ Setup to $\overline{WE}$ Going High	100		100		ns
t <sub>VPWH</sub>	t <sub>VPS</sub> <sup>(1)</sup>	$V_{PP}$ Setup to $\overline{WE}$ Going High	100		100		ns
t <sub>WHQV1</sub>	—	Duration of Programming Operations	15		15		μs
t <sub>WHQV2</sub>	—	Duration of Erase Operations (Boot)	1.3		1.3		Sec
t <sub>WHQV3</sub>	—	Duration of Erase Operations (Parameter)	1.3		1.3		Sec
t <sub>WHQV4</sub>	—	Duration of Erase Operations (Main)	3		3		Sec
t <sub>QVVL</sub>	t <sub>VPH</sub> <sup>(1)</sup>	$V_{PP}$ Hold from Valid Status Reg Data	0		0		ns
t <sub>QVPH</sub>	t <sub>PHH</sub> <sup>(1)</sup>	$\overline{RP} V_{HH}$ Hold from Status Reg Data	0		0		ns
t <sub>PHBR</sub> <sup>(1)</sup>	—	Boot Block Relock Delay		100		100	ns
t <sub>GHHWL</sub>	—	$\overline{OE} V_{HH}$ Setup to $\overline{WE}$ Going Low	480		480		ns
t <sub>WHGH</sub>	—	$\overline{OE} V_{HH}$ Hold from $\overline{WE}$ High	480		480		ns

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

## ERASE AND PROGRAMMING PERFORMANCE

Parameter	28F001-90			28F001-12			Units
	Min	Typ	Max	Min	Typ	Max	
Boot Block Erase Time		2.10	14.9		2.10	14.9	Sec
Boot Block Program Time		0.15	0.52		0.15	0.52	Sec
Parameter Block Erase Time		2.10	14.6		2.10	14.6	Sec
Parameter Block Program Time		0.07	0.26		0.07	0.26	Sec
Main Block Erase Time		3.80	20.9		3.80	20.9	Sec
Main Block Program Time		2.10	7.34		2.10	7.34	Sec
Chip Erase Time		10.10	65		10.10	65	Sec
Chip Program Time		2.39	8.38		2.39	8.38	Sec

FUNCTION TABLE<sup>(1)</sup>

Mode	Pins						Notes
	RP	CE	OE	WE	VPP	I/O	
Read	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	D <sub>OUT</sub>	
Output Disable	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IH</sub>	X	High-Z	
Standby	V <sub>IH</sub>	V <sub>IH</sub>	X	X	X	High-Z	
Signature (MFG)	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	31H	A <sub>0</sub> = V <sub>IL</sub> , A <sub>9</sub> = 12V
Signature (Device)	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	X	94H-28F001T 95H-28F001B	A <sub>0</sub> = V <sub>IH</sub> , A <sub>9</sub> = 12V
Write Cycle	V <sub>IH</sub>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	X	D <sub>IN</sub>	During Write Cycle
Deep Power Down	V <sub>IL</sub>	X	X	X	X	HIGH-Z	

## WRITE COMMAND TABLE

Commands are written into the command register in one or two write cycles. Write cycles also internally latch addresses and data required for programming and erase operations.

Mode	First Bus Cycle			Second Bus Cycle			
	Operation	Address	D <sub>IN</sub>	Operation	Address	D <sub>IN</sub>	D <sub>OUT</sub>
Read Array/Reset	Write	X	FFH				
Program Setup/ Program	Write	A <sub>IN</sub>	40H 10H	Write	A <sub>IN</sub>	D <sub>IN</sub>	
Read Status Reg.	Write	X	70H	Read	X		St. Reg. Data
Clear Status Reg.	Write	X	50H				
Erase Setup/Erase Confirm	Write	Block ad	20H	Write	Block ad	D0H	
Erase Suspend/ Erase Resume	Write	X	B0H	Write	X	D0H	
Read Sig (Mfg)	Write	X	90H	Read	0000H		31H
Read Sig (Dev)	Write	X	90H	Read	0001H		94H-28F001T 95H-28F001B

Note:

(1) Logic Levels: X = Logic 'Do not care' (V<sub>IH</sub>, V<sub>IL</sub>, V<sub>PPL</sub>, V<sub>PPH</sub>)

## READ OPERATIONS

### Read Mode

The CAT28F001 memory can be read from any of its Blocks (Boot Block, Main Block or Parameter Block), Status Register and Signature Information by sending the Read Command Mode to the Command Register.

CAT28F001 automatically resets to Read Array mode upon initial device power up or after exit from deep power down. A Read operation is performed with both  $\overline{CE}$  and  $\overline{OE}$  low and with  $\overline{RP}$  and  $\overline{WE}$  high.  $V_{pp}$  can be either high or low. The data retrieved from the I/O pins reflects the contents of the memory location corresponding to the state of the 17 address pins. The respective timing waveforms for the read operation are shown in Figure 3. Refer to the AC Read characteristics for specific timing parameters.

### Signature Mode

The signature mode allows the user to identify the IC manufacturer and the type of the device while the device resides in the target system. This mode can be activated in either of two ways; through the conventional method of applying a high voltage (12V) to address pin A9 or by sending an instruction to the command register (see Write Operations).

The conventional method is entered as a regular read mode by driving the  $\overline{CE}$  and  $\overline{OE}$  low (with  $\overline{WE}$  high), and

applying the required high voltage on address pin A9 while the other address line are held at VIL.

A Read cycle from address 0000H retrieves the binary code for the IC manufacturer on outputs I/O<sub>7</sub> to I/O<sub>0</sub>:

Catalyst Code = 0011 0001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O<sub>7</sub> to I/O<sub>0</sub>:

CAT28F001T = 1001 0100 (94H)

CAT28F001B = 1001 0101 (95H)

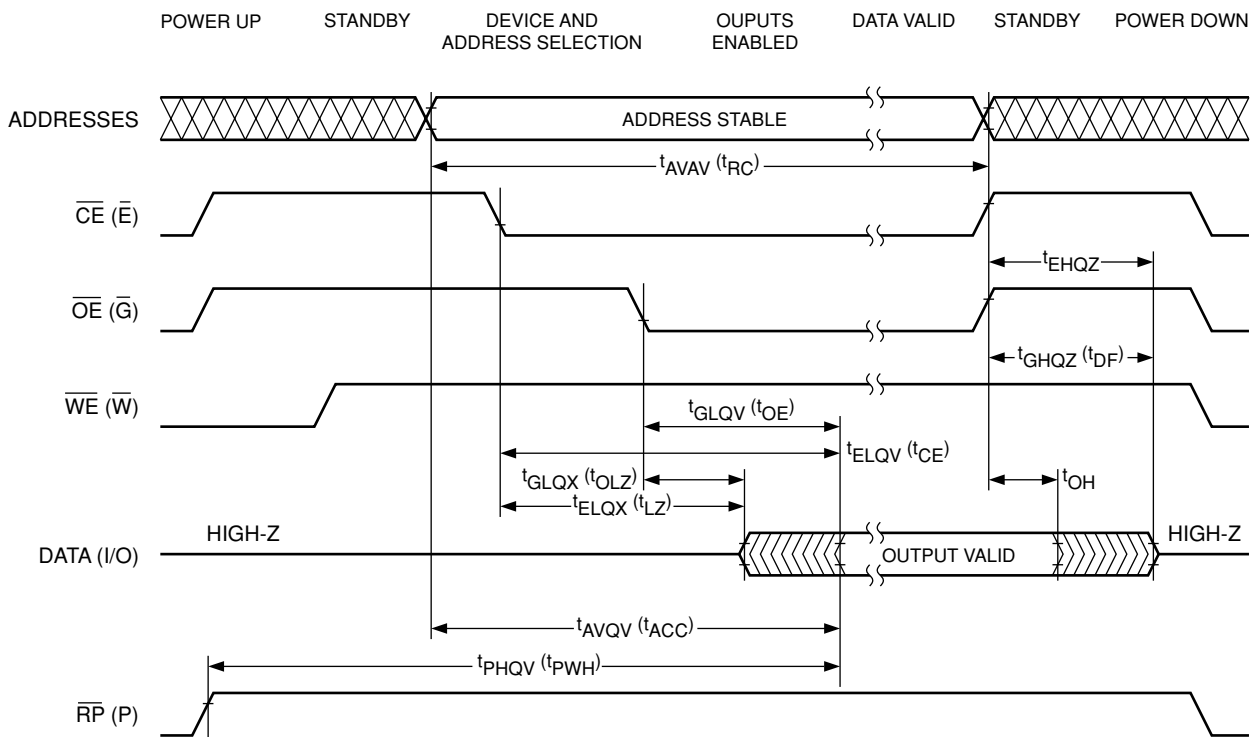
### Standby Mode

With  $\overline{CE}$  at a logic-high level, the CAT28F001 is placed in a standby mode where most of the device circuitry is disabled, thereby substantially reducing power consumption. The outputs are placed in a high-impedance state independent of the  $\overline{OE}$  status.

### Deep Power-Down

When  $\overline{RP}$  is at logic-low level, the CAT28F001 is placed in a Deep Power-Down mode where all the device circuitry are disabled, thereby reducing the power consumption to 0.25 $\mu$ W.

Figure 3. A.C. Timing for Read Operation





## WRITE OPERATIONS

The following operations are initiated by observing the sequence specified in the Write Command Table.

### Read Array

The device can be put into a Read Array Mode by initiating a write cycle with FFH on the data bus. The device is also in a standard Read Array Mode after the initial device power up and when comes out of the Deep Power-Down mode.

### Signature Mode

An alternative method for reading device signature (see Read Operations Signature Mode), is initiated by writing the code 90H into the command register. A read cycle from address 0000H with  $\overline{CE}$  and  $\overline{OE}$  low (and  $\overline{WE}$  high) will output the device signature.

Catalyst Code = Catalyst Code = 0011 0001 (31H)

A Read cycle from address 0001H retrieves the binary code for the device on outputs I/O<sub>7</sub> to I/O<sub>0</sub>:

CAT28F001T = 1001 0100 (94H)

CAT28F001B = 1001 0101 (95H)

To terminate the operations, it is necessary to write another valid command into the register.

## STATUS REGISTER

The 28F001 contains an 8-bit Status Register. The Status Register is polled to check for write or erase completion or any related errors. The Status Register may be read at any time by issuing a Read Status Register (70H) command. All subsequent read operations output data from the Status Register, until another valid command is issued. The contents of the Status Register are latched on the falling edge of  $\overline{OE}$  or  $\overline{CE}$ , whichever occurs last in the read cycle.  $\overline{OE}$  or  $\overline{CE}$  must be toggled to VIH before further reads to update the status register latch.

The Erase Status (SR.5) and Program Status (SR.4) are set to 1 by the WSM and can only be reset issuing Clear Status Register (50H). These two bits can be polled for failures, thus allowing more flexibility to the designer when using the CAT28F001. Also, VPP Status (SR.3) when set to 1 must be reset by system software before any further byte programs or block erases are attempted.

### ERASE SETUP/ERASE CONFIRM

Erase is executed one block at a time, initiated by a two cycle command sequence. The two cycle command sequence provides added security against accidental

block erasure. During the first write cycle, a Command 20H (Erase Setup) is first written to the Command Register, followed by the Command D0H (Erase Confirm). These commands require both appropriate command data and an address within Block to be erased. Also, Block erasure can only occur when VPP = VPPH.

Block preconditioning, erase and verify are all handled internally by the Write State Machine, invisible to the system. After receiving the two command erase sequence the CAT28F001 automatically outputs Status Register data when read (Fig.5). The CPU can detect the completion of the erase event by checking if the SR.7 of the Status Register is set.

SR.5 will indicate whether the erase was successful. If an erase error is detected, the Status Register should be cleared. The device will be in the Status Register Read Mode until another command is issued.

### ERASE SUSPEND/ERASE RESUME

The Erase Suspend Command allows erase sequence interruption in order to read data from another block of memory. Once the erase sequence is started, writing the Erase Suspend command (B0H) to the Command Register requests that the WSM suspend the erase sequence at a predetermined point in the erase algorithm. The CAT28F001 continues to output Status Register data when read, after the Erase Suspend command is written to it. Polling the WSM Status and Erase Suspend Status bits will determine when the erase operation has been suspended (both will be set to "1s").

The device may now be given a Read ARRAY Command, which allows any locations 'not within the block being erased' to be read. Also, you can either perform a Read Status Register or resume the Erase Operation by sending Erase Resume (D0H), at which time the WSM will continue with the erase sequence. The Erase Suspend Status and WSM Status bits of the Status Register will be cleared.

### PROGRAM SETUP/PROGRAM COMMANDS

Programming is executed by a two-write sequence. The program Setup command (40H) is written to the Command Register, followed by a second write specifying the address and data (latched on the rising edge of  $\overline{WE}$ ) to be programmed. The WSM then takes over, controlling the program and verify algorithms internally. After the two-command program sequence is written to it, the CAT28F001 automatically outputs Status Register data when read (see figure 4; Byte Program Flowchart). The CPU can detect the completion of the program event by analyzing the WSM Status bit of the Status Register. Only the Read Status Register Command is valid while programming is active.

<b>WSMS</b>	<b>ESS</b>	<b>ES</b>	<b>PS</b>	<b>VPPS</b>	<b>R</b>	<b>R</b>	<b>R</b>
<b>7</b>	<b>6</b>	<b>5</b>	<b>4</b>	<b>3</b>	<b>2</b>	<b>1</b>	<b>0</b>

SR.7 = WRITE STATE MACHINE STATUS  
 1 = Ready  
 0 = Busy  
 SR.6 = ERASE SUSPEND STATUS  
 1 = Erase Suspended  
 0 = Erase in Progress/Completed  
 SR.5 = ERASE STATUS  
 1 = Error in Block Erasure  
 0 = Successful Block Erase  
 SR.4 = PROGRAM STATUS  
 1 = Error in Byte Program  
 0 = Successful Byte Program  
 SR.3 = VPP STATUS  
 1 = V<sub>PP</sub> Low Detect; Operation Abort  
 0 = V<sub>PP</sub> Okay  
 SR.2 -SR.0 = RESERVED FOR FUTURE ENHANCEMENTS  
 These bits are reserved for future use and should be masked out when polling the Status Register.

NOTES:  
 The Write State Machine Status Bit must first be checked to determine program or erase completion, before the Program or Erase Status bits are checked for success. If the Program AND Erase Status bits are set to “1s” during an erase attempt, an improper command sequence was entered. Attempt the operation again.  
 If V<sub>PP</sub> low status is detected, the Status Register must be cleared before another program or erase operation is attempted.  
 The V<sub>PP</sub> Status bit, unlike an A/D converter, does not provide continuous indication of V<sub>PP</sub> level. The WSM interrogates the V<sub>PP</sub> level only after the program or erase command sequences have been entered and informs the system if V<sub>PP</sub> has not been switched on. The V<sub>PP</sub> Status bit is not guaranteed to report accurate feedback between V<sub>PLL</sub> and V<sub>PPH</sub>.

When the Status Register indicates that programming is complete, the Program Status bit should be checked. If program error is detected, the Status Register should be cleared. The internal WSM verify only detects errors for “1s” that do not successfully program to “0s”. The Command Register remains in Read Status Register mode until further commands are issued to it.

If erase/byte program is attempted while V<sub>PP</sub> = V<sub>PLL</sub>, the Status bit (SR.5/SR.4) will be set to “1”. Erase/Program attempts while V<sub>PLL</sub> < V<sub>PP</sub> < V<sub>PPH</sub> produce spurious results and should not be attempted.

**EMBEDDED ALGORITHMS**

The CAT28F001 integrates the Quick Pulse programming algorithm on-chip, using the Command Register, Status Register and Write State Machine (WSM). On-chip integration dramatically simplifies system software and provides processor-like interface timings to the Command and Status Registers. WSM operation, internal program verify, and V<sub>PP</sub> high voltage presence are monitored and reported via appropriate Status Register bits. Figure 4 shows a system software flowchart for device programming.

As above, the Quick Erase algorithm is now implemented internally, including all preconditioning of block data. WSM operation, erase verify and V<sub>PP</sub> high voltage presence are monitored and reported through the Status Register. Additionally, if a command other than Erase Confirm is written to the device after Erase Setup has been written, both the Erase Status and Program Status

bits will be set to “1”. When issuing the Erase Setup and Erase Confirm commands, they should be written to an address within the address range of the block to be erased. Figure 5 shows a system software flowchart for block erase.

The entire sequence is performed with V<sub>PP</sub> at V<sub>PPH</sub>. Abort occurs when  $\overline{RP}$  transitions to V<sub>IL</sub>, or V<sub>PP</sub> drops to V<sub>PLL</sub>. Although the WSM is halted, byte data is partially programmed or Block data is partially erased at the location where it was aborted. Block erasure or a repeat of byte programming will initialize this data to a known value.

**BOOT BLOCK PROGRAM AND ERASE**

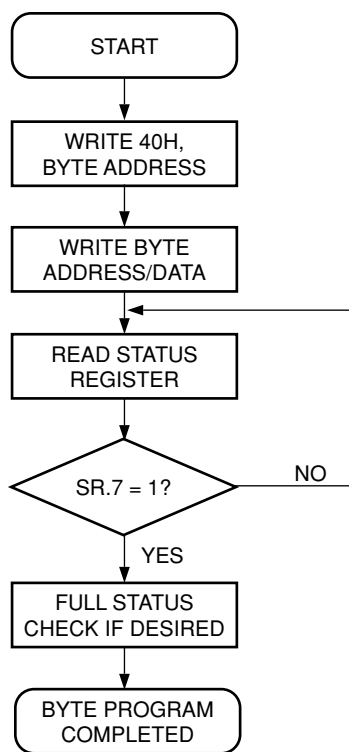
The boot block is intended to contain secure code which will minimally bring up a system and control programming and erase of other blocks of the device, if needed. Therefore, additional “lockout” protection is provided to guarantee data integrity. Boot block program and erase operations are enabled through high voltage V<sub>HH</sub> on either  $\overline{RP}$  or  $\overline{OE}$ , and the normal program and erase command sequences are used. Reference the AC Waveforms for Program/Erase.

If boot block program or erase is attempted while  $\overline{RP}$  is at V<sub>IH</sub>, either the Program Status or Erase Status bit will be set to “1”, reflective of the operation being attempted and indicating boot block lock. Program/erase attempts while V<sub>IH</sub> <  $\overline{RP}$  < V<sub>HH</sub> produce spurious results and should not be attempted.

### IN-SYSTEM OPERATION

For on-board programming, the  $\overline{RP}$  pin is the most convenient means of altering the boot block. Before issuing Program or Erase confirms commands,  $\overline{RP}$  must transition to  $V_{HH}$ . Hold  $\overline{RP}$  at this high voltage throughout the program or erase interval (until after Status Register confirm of successful completion). At this time, it can return to  $V_{IH}$  or  $V_{IL}$ .

**Figure 4 Byte Programming Flowchart**



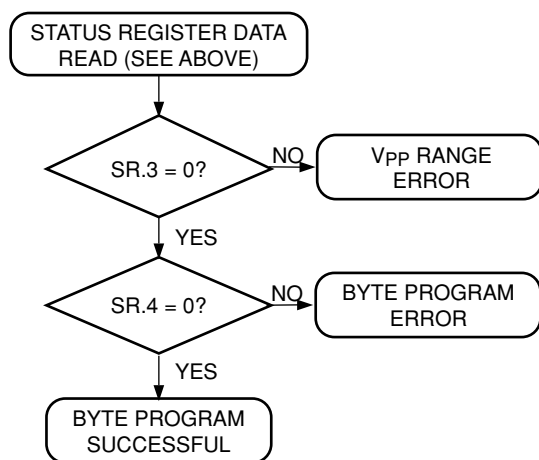
Bus Operation	Command	Comments
Write	Program Setup	Data = 40H Address = Bytes to be Programmed
Write	Program	Data to be programmed Address = Byte to be Programmed
Read		Status Register Data. Toggle OE or CE to update Status Register Check SR.7
Standby		1 = Ready, 0 = Busy

Repeat for subsequent bytes.

Full Status check can be done after each byte or after a sequence of bytes.

Write FFH after the last byte programming operation to reset the device to Read Array Mode.

#### FULL STATUS CHECK PROCEDURE



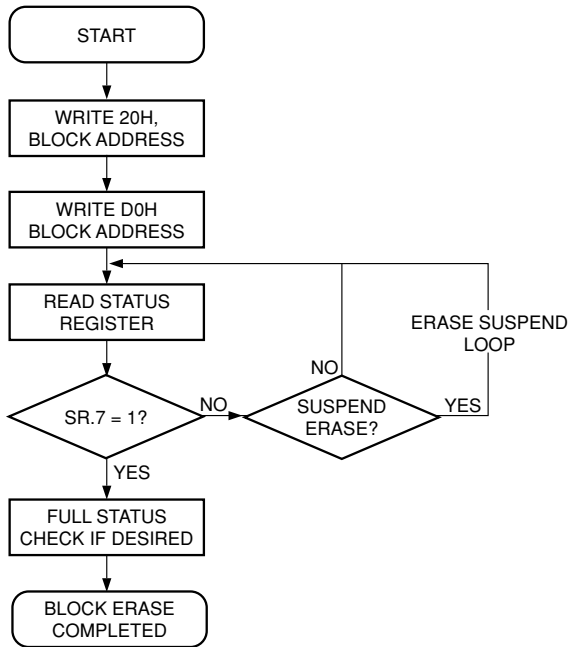
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V <sub>PP</sub> Low Detect
Standby		Check SR.3 1 = Byte Program Error

SR.3 MUST be cleared, if set during a program attempt, before further attempts are allowed by the Write State Machine.

SR.3 is only cleared by the Clear Status Register Command, in case where multiple bytes are programmed before full status is checked.

If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 5 Block Erase Flowchart



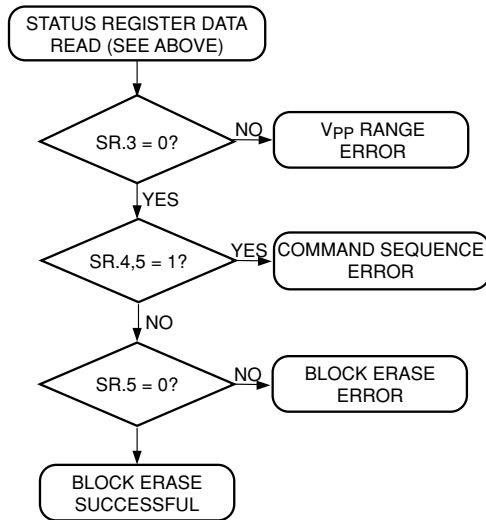
Bus Operation	Command	Comments
Write	Erase Setup	Data = 20H Address = Within Block to be erased
Write	Erase	Data - D0H Address = Within Block to be erased
Read		Status Register Data. Toggle OE or CE to update Status Register
Standby		Check SR.7 1 = Ready, 0 = Busy

Repeat for subsequent blocks.

Full Status check can be done after each block or after a sequence of blocks.

Write FFH after the last block erase operation to reset the device to Read Array Mode.

FULL STATUS CHECK PROCEDURE



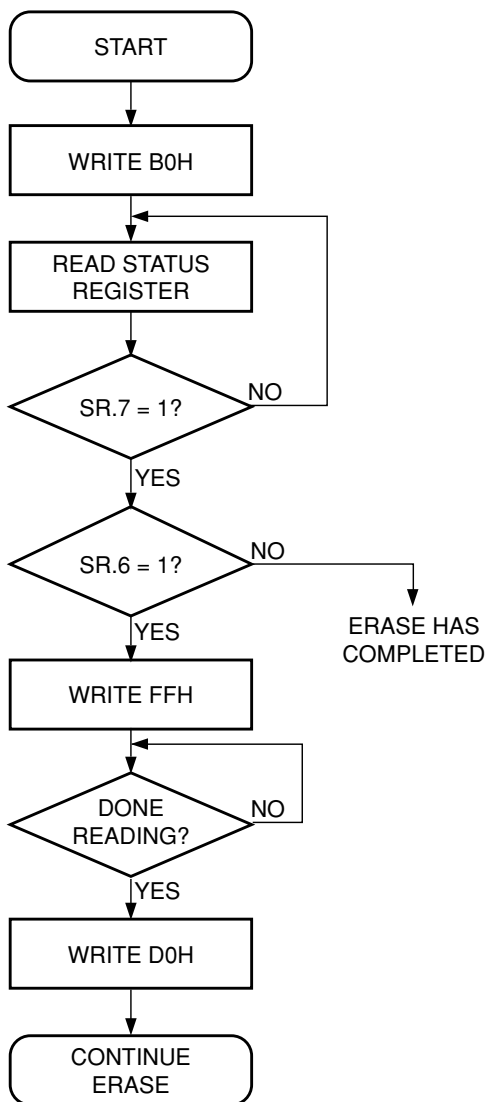
Bus Operation	Command	Comments
Standby		Check SR.3 1 = V <sub>PP</sub> Low Detect
Standby		Check SR.4 Both 1 = Command Sequence Error
Standby		Check SR.5 1 = Block Erase Error

SR.3 MUST be cleared, if set during a erase attempt, before further attempts are allowed by the Write State Machine.

SR.3 is only cleared by the Clear Status Register Command, in cases where multiple blocks are erased before full status is checked.

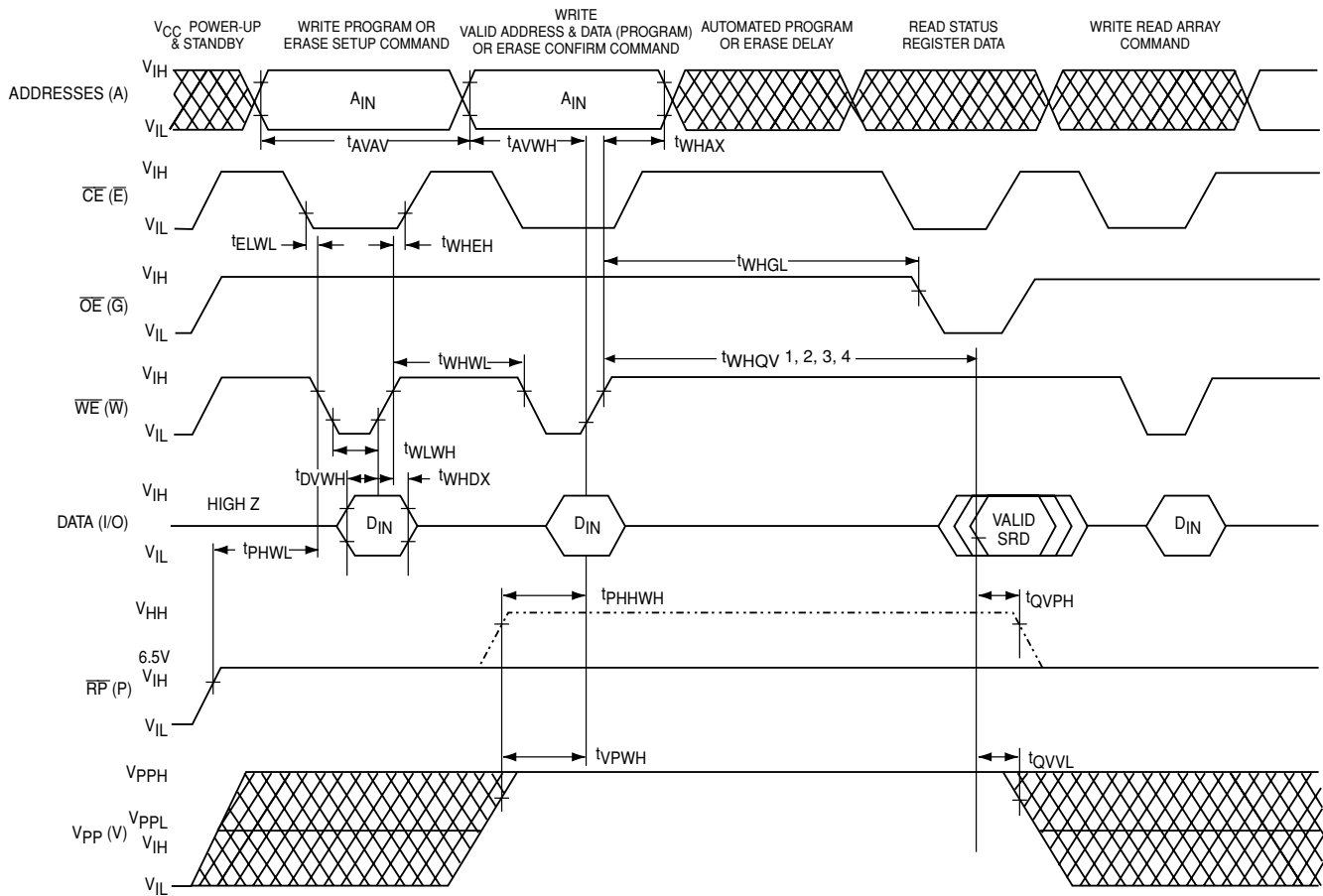
If error is detected, clear the Status Register before attempting retry or other error recovery.

Figure 6 Block Erase Suspend/Resume Flowchart



Bus Operation	Command	Comments
Write	Erase Suspend	Data = B0H
Standby/ Ready		Read Status Register Check SR.7 1 = Ready, 0 = Busy Toggle $\overline{OE}$ or $\overline{CE}$ to Update Status Register
Standby		Check SR.6 1 = Suspended
Write	Read Array	Data = FFH
Read		Read array data from block other than that being erased.
Write	Erase Resume	Data = D0H

Figure 7. A.C. Timing for Program/Erase Operation



### POWER UP/DOWN PROTECTION

The CAT28F001 offers protection against inadvertent programming during  $V_{PP}$  and  $V_{CC}$  power transitions. When powering up the device there is no power-on sequencing necessary. In other words,  $V_{PP}$  and  $V_{CC}$  may power up in any order. Additionally  $V_{PP}$  may be hardwired to  $V_{PPH}$  independent of the state of  $V_{CC}$  and any power up/down cycling. The internal command register of the CAT28F001 is reset to the Read Mode on power up.

### POWER SUPPLY DECOUPLING

To reduce the effect of transient power supply voltage spikes, it is good practice to use a 0.1 $\mu$ F ceramic capacitor between  $V_{CC}$  and  $V_{SS}$  and  $V_{PP}$  and  $V_{SS}$ . These high-frequency capacitors should be placed as close as possible to the device for optimum decoupling.

**ALTERNATE  $\overline{CE}$ -CONTROLLED WRITES**

$V_{CC} = +5V \pm 10\%$ , unless otherwise specified

JEDEC Symbol	Standard Symbol	Parameter	28F001-90		28F001-12		Units
			Min	Max	Min	Max	
tAVAV	tWC	Write Cycle Time	90		120		ns
tAVEH	tAS	Address Setup to $\overline{CE}$ Going High	40		40		ns
tEHAX	tAH	Address Hold Time from $\overline{CE}$ Going High	10		10		ns
tDVEH	tDS	Data Setup Time to $\overline{CE}$ Going High	40		40		ns
tEHDX	tDH	Data Hold Time from $\overline{CE}$ Going High	10		10		ns
tWLEL	tWS	$\overline{WE}$ Setup Time to $\overline{CE}$ Going Low	0		0		ns
tEHWH	tWH	$\overline{WE}$ Hold Time from $\overline{CE}$ Going High	0		0		ns
tELEH	tCP	$\overline{CE}$ Pulse Width	40		40		ns
tEHEL	tEPH	$\overline{CE}$ High Pulse Width	10		10		ns
tEHGL	—	Write Recovery Time Before Read	0		0		$\mu$ s
tPHEL	tPS <sup>(1)</sup>	$\overline{RP}$ High Recovery to $\overline{CE}$ Going Low	480		480		ns
tPHHEH	tPHS <sup>(1)</sup>	$\overline{RP}$ $V_{HH}$ Setup to $\overline{CE}$ Going High	100		100		ns
tVPEH	tVPS <sup>(1)</sup>	$V_{PP}$ Setup to $\overline{CE}$ Going High	100		100		ns
tEHQV1	—	Duration of Programming Operations	15		15		$\mu$ s
tEHQV2	—	Duration of Erase Operations (Boot)	1.3		1.3		Sec
tEHQV3	—	Duration of Erase Operations (Parameter)	1.3		1.3		Sec
tEHQV4	—	Duration of Erase Operations (Main)	3		3		Sec
tQVVL	tVPH <sup>(1)</sup>	$V_{PP}$ Hold from Valid Status Reg Data	0		0		ns
tQVPH	tPHH <sup>(1)</sup>	$\overline{RP}$ $V_{HH}$ Hold from Status Reg Data	0		0		ns
tPHBR <sup>(1)</sup>	—	Boot Block Relock Delay		100		100	ns
tGHHWL	—	$\overline{OE}$ $V_{HH}$ Setup to $\overline{WE}$ Going Low	480		480		ns
tWHGH	—	$\overline{OE}$ $V_{HH}$ Hold from $\overline{WE}$ High	480		480		ns

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

Figure 8. Alternate Boot Block Access Method Using  $\overline{OE}$

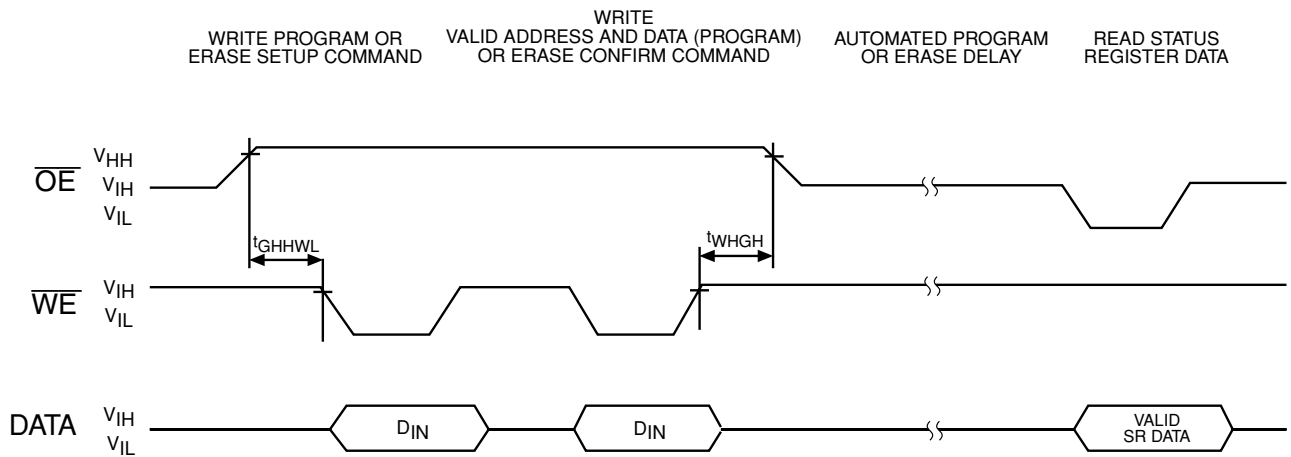
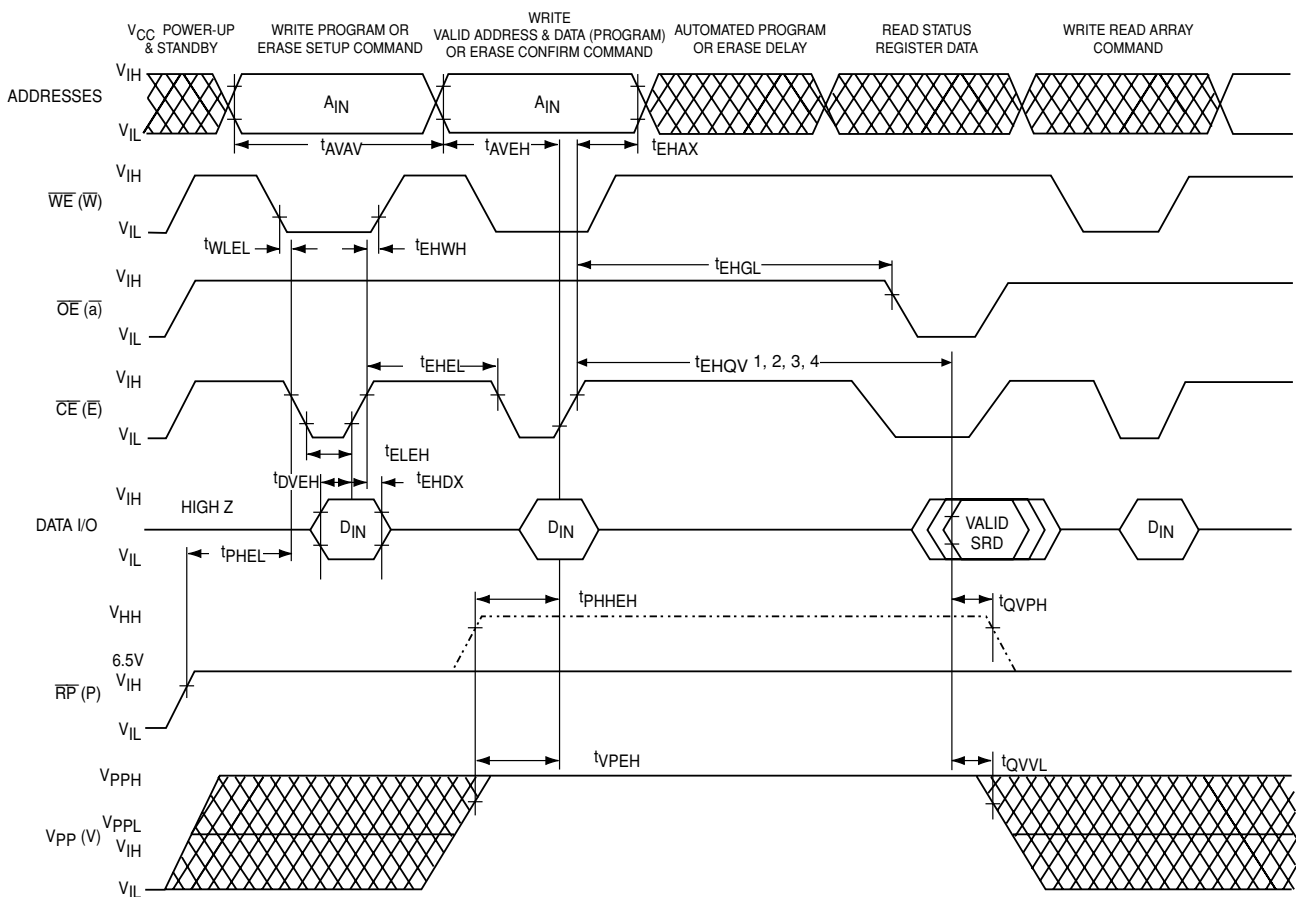
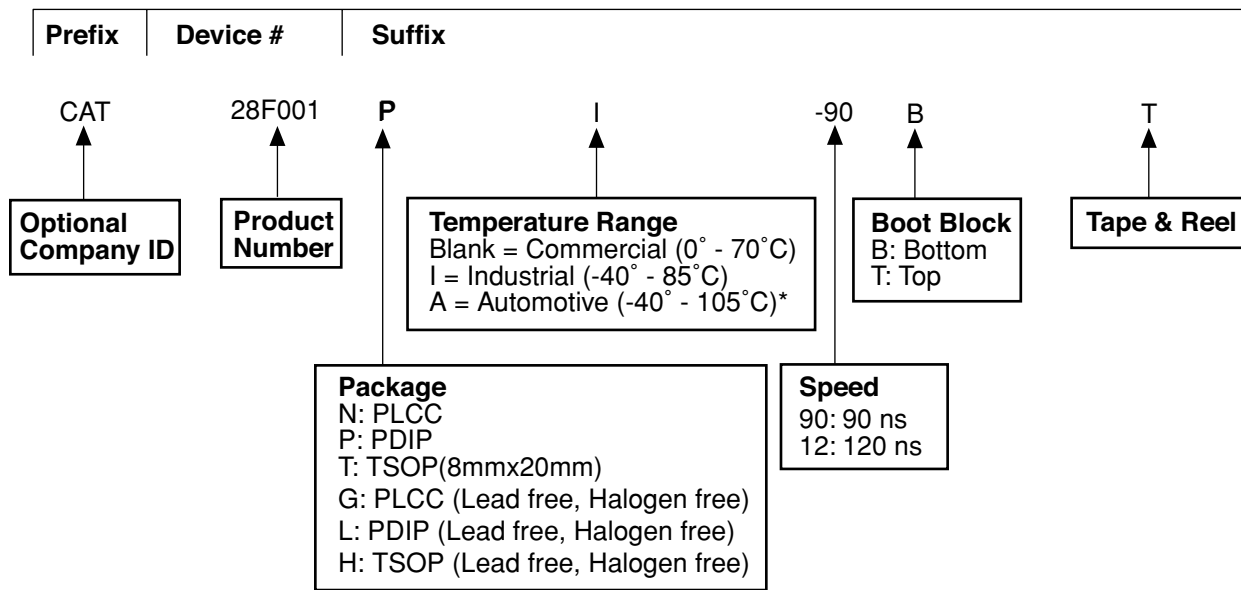


Figure 9. Alternate AC Waveform for Write Operations





## ORDERING INFORMATION



\* -40° to +125°C is available upon request

**Note:**

(1) The device used in the above example is a CAT28F001PI-90BT (PDIP, Industrial Temperature, 90ns access time, Bottom Boot Block, Tape & Reel)

## REVISION HISTORY

Date	Revision	Comments
04/20/04	G	Delete data sheet designation Update Features Update Pin Configuration Update Ordering Information Update A. C. Tables Update Erase Table Update Alternate Table Update Ordering Information Update Revision History Update Rev Number
09/21/04	H	Update Ordering Information
03/29/05	I	Update Ordering Information

---

### **Copyrights, Trademarks and Patents**

Trademarks and registered trademarks of Catalyst Semiconductor include each of the following:

DPP™ AE<sup>2</sup>™

Catalyst Semiconductor has been issued U.S. and foreign patents and has patent applications pending that protect its products. For a complete list of patents issued to Catalyst Semiconductor contact the Company's corporate office at 408.542.1000.

*CATALYST SEMICONDUCTOR MAKES NO WARRANTY, REPRESENTATION OR GUARANTEE, EXPRESS OR IMPLIED, REGARDING THE SUITABILITY OF ITS PRODUCTS FOR ANY PARTICULAR PURPOSE, NOR THAT THE USE OF ITS PRODUCTS WILL NOT INFRINGE ITS INTELLECTUAL PROPERTY RIGHTS OR THE RIGHTS OF THIRD PARTIES WITH RESPECT TO ANY PARTICULAR USE OR APPLICATION AND SPECIFICALLY DISCLAIMS ANY AND ALL LIABILITY ARISING OUT OF ANY SUCH USE OR APPLICATION, INCLUDING BUT NOT LIMITED TO, CONSEQUENTIAL OR INCIDENTAL DAMAGES.*

Catalyst Semiconductor products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the Catalyst Semiconductor product could create a situation where personal injury or death may occur.

Catalyst Semiconductor reserves the right to make changes to or discontinue any product or service described herein without notice. Products with data sheets labeled "Advance Information" or "Preliminary" and other products described herein may not be in production or offered for sale.

Catalyst Semiconductor advises customers to obtain the current version of the relevant product information before placing orders. Circuit diagrams illustrate typical semiconductor applications and may not be complete.

---



# CATALYST

Catalyst Semiconductor, Inc.  
Corporate Headquarters  
1250 Borregas Avenue  
Sunnyvale, CA 94089  
Phone: 408.542.1000  
Fax: 408.542.1200  
www.catalyst-semiconductor.com

Publication #: 1078  
Revision: I  
Issue date: 03/29/05