SYSTEM CAMERA DEVICE

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1. GENERAL DESCRIPTION

W99685BS is a high performance and highly-integrated system camera device that it can preview, capture, compress, store, and display the digital still images or playback a short period of live video. This chip provide 8 or 16 Bits Host interface and easy for base band platform(Host) to develop Camera function through Winbond CF Command set protocol that allow the development of products without knowing any W99685BS chip programming.

W99685BS Built-in 8-bit 8032 compatible uC with internal 16KB program RAM and 4K data RAM. Program can be down load from memory bus interface. This chip also Built-in 2M byte frame buffer for real-time video clip (MJPG) and burst snapshot. Support CCIR-656 8-bit YUV CMOS or CCD capture sensor interface.

W99685BS Support up to dual LCD Panels interface with MCU type interface. Support TFT-LCD, CSTN-LCD, STN-LCD Panel Types , If camera function is active, the host CPU can use W99685BS as the bridge (display controller) to LCM. And it can provide multiple display buffers. If camera function is disabled, the host CPU can use bypass mode to control the LCM directly for maximum power saving.

W99685BS Support dual video pipes and double buffering for real-time motion JPEG, Support smooth scaling-down of video pipes, different kinds of raw data formats for display, some popular image color effects (Black & White,Sepia,Negative,Solarize or Oil Painting), video rotation/mirror/flip for capture and playback,sticker maker, Comic Photo maker and smart frame rate control.

2. FEATURES

- **General**
  - 0.18um logic process
  - Core 1.8V
  - I/O 2.6V - 3.6V
  - Power consumption
    - < 23mA for 160x120 @ 15 fps, 2.8V preview mode
    - < 35mA for 160x120 @ 30fps, 2.8V preview mode
  - Support power-down mode
  - Support LCD bypass mode
  - Support GPIO pins for flash light control or else
  - Built-in smart processor to allow the development of products without knowing any W99685 chip programming. Minimum product design cycle time for fast time-to-market
  - Built-in 8-bit 8032 compatible uC with internal 16KB program RAM and 4K data RAM
  - Program can be down load from host interface.
  - Built-in 2M bytes frame buffer for real-time video clip (M-JPEG) and burst snapshot.
  - Support VGA/ Mega image resolution

- **Sensor Interface**
  - Support CCIR-656 8-bit YUV interface
  - Supports fast serial interface to program image sensor.
- **Host Interface**
  - 8/16 bits parallel Bus (Indirect access)
- **Easy for base band chip(Host) to develop Camera function through Command set protocol.**
- **LCD Display Interface**
  - Support up to dual LCD Panels interface
  - Supports **MCU type interface** LCD module
  - Supports 8/16/18-bit display data output to LCD Penal
  - Support 4 kinds of display data format out to LCD Penal
    - 256 colors (RGB-332)
    - 4096 colors (RGB-444)
    - 64k colors (RGB-565)
    - 256k colors (RGB-666)
  - Support LCD interface bypass mode
  - Support TFT-LCD, CSTN-LCD, STN-LCD Panel Types
  - If camera function is active, the host CPU can use W99685BS as the bridge (display controller) to LCM. And it can provide multiple display buffers.
  - If camera function is disabled, the host CPU can use bypass mode to control the LCM directly for maximum power saving.
- **JPEG CODEC for Image Compression and Decompression**
  - Fully compliant with ISO/IEC 10918-1 international JPEG standard
  - JPEG compression and decompression for still images
  - Real-time motion JPEG (M-JPEG) compression with advanced bit rate control for live video
  - JPEG baseline sequential mode in interleaved scan YcbCr(4:2:2) or YcbCr(4:2:0) format
  - Support adjustable quantization table for different compression ratio
  - Support smooth digital zoom
  - Support JPEG re-sizing and re-encoding

Operation Modes

- Preview ModeFrame rate up to 30 fps
- Single Snapshot Mode
- Burst Snapshot Mode
  - Support up to 10 frames burst snapshot at 1/30 sec interval
- Movie Mode (Motion JPEG)
  - About 15 seconds recording time with 800K bytes vedio buffer at 160x120 size @ 15 fps
- Playback Mode
- Comic Photo Mode
- Transfer Mode
- Still Image Size
  - 1280 x 960
  - 640 x 480 (VGA)
  - 320 x 240 (QVGA)
  - 160 x 120 (QQVGA)
  - Subject to change by request
- Video Clip Size
  - 160x120 (QQVGA)

Video Display Function

- Support high-color / OSD Video overlay function
- Support graphics/video blending
- Support image Rotation / Flip / Mirror
- Left 90 degree rotation
- Right 90 degree rotation
- 180 degree rotation
- Horizontal mirror
- Vertical flip
- Support image color effects
- Normal
- Black & white
- Sepia
- Negative
- Solarize / oil painting
- Support image sticker maker
- Support imprint of message photo

- Support comic photo maker
- Support OSD Video overlay function
- Support dual video pipes and double buffering for real-time Motion JPEG
- Support arbitrary N/M (=[0..255]) scaling-down of video pipes
- Support different kinds of raw data formats for display
- Support some popular image color effects
- Support smart frame rate control

❑ **Power Management**

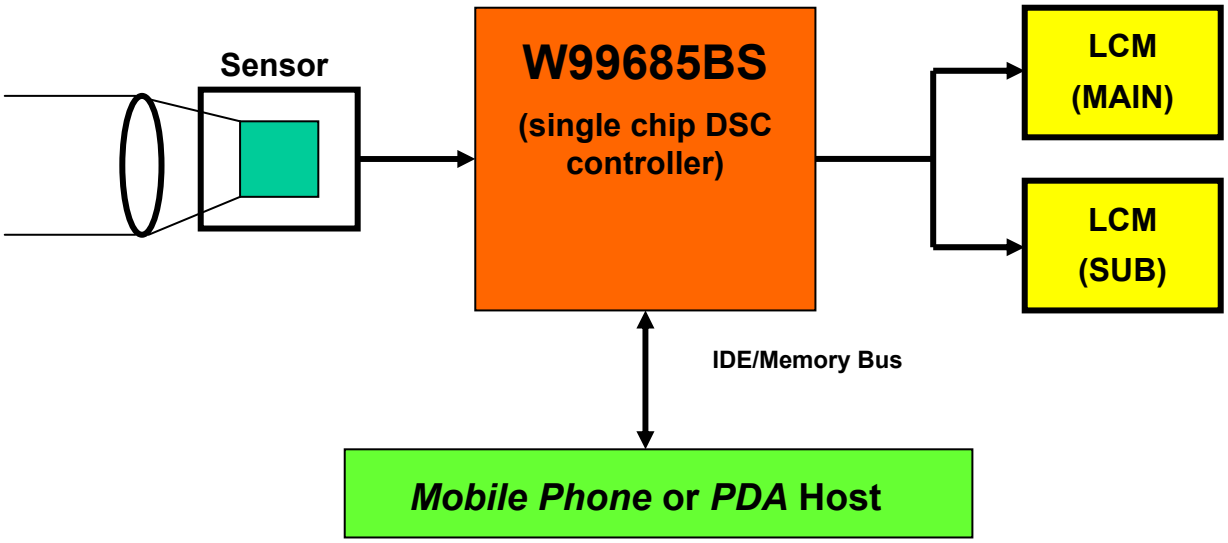
- Advanced power management including:
  - Power-down mode
  - Stand-by mode
  - Operating mode

❑ **Package:**

- **W99685BS**/ BGA 81-Balls package (8mm x 8mm)

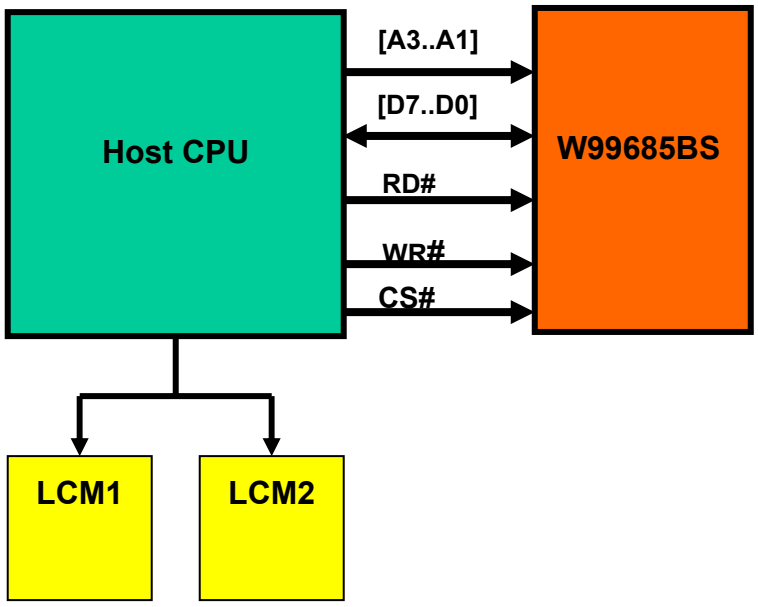
3. APPLICATION

3.1 System Overview

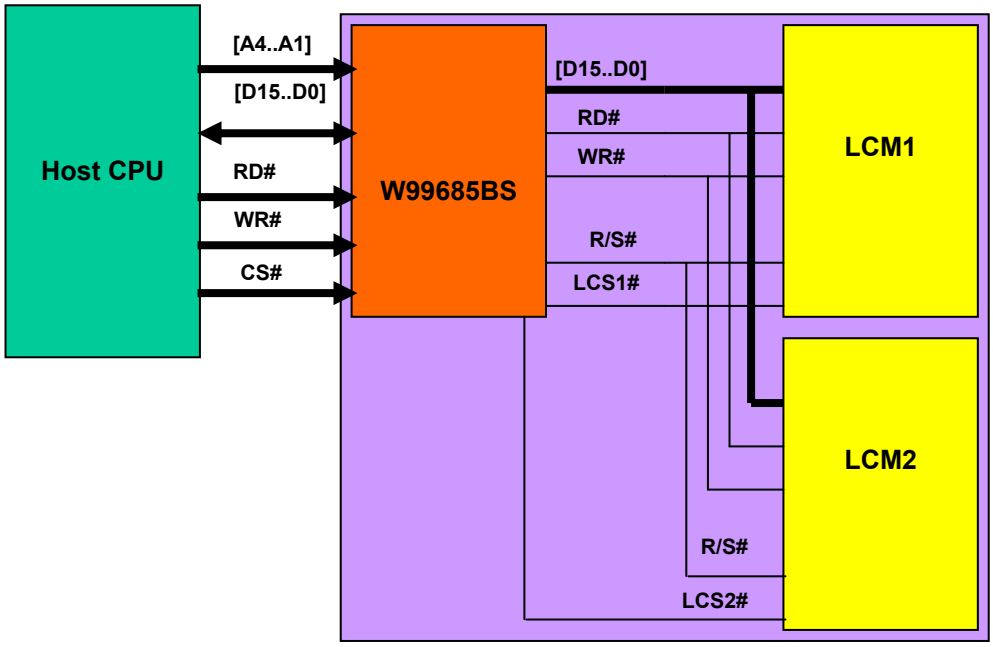


3.2 Host Interface

- **Host Interface IDE**
  - High speed parallel bus (8-bit or 16-bit)
  - Ideal attachable CF camera solution especially for PDA with CF slot
  - Ideal built-in camera solution
- **Host Interface IDE-1**



- Host Interface IDE-2



3.3 Camera Implementation

❑ **Preview Mode Features**

- Support raw data preview or JPEG preview
- Support video preview directly to LCM
- Support video rotation/flip/mirror
- Support live color effect and sticker display
- Support up to 30 fps preview depending on the sensor frame rate
- Support digital zoom

❑ **Snapshot Mode Features**

- Support encoding of different size of images
- Support image rotation/flip/mirror
- Support color effect and sticker functions

❑ **Burst Snapshot Mode Features**

- Extension to snapshot (single capture) mode
- Support up to 10 frames burst snapshot at 1/30 sec interval
- The encoded pictures are stored in W99685 frame buffer, the host can select the favorite ones for storage.

❑ **Movie Mode Features**

- Support real-time video clip encoding
- The video clip (dumb video) is stored in W99685 frame buffer, the duration depends on the frame rate and resolution
- Dumb Video Implementation
- Motion JPEG Movie Implementation

❑ **Playback Mode Features**

- Support still JPEG playback directly to LCD or raw data
- Support motion JPEG video playback direct to LCD or raw data
- Support image rotation/flip/mirror
- Support playback mode digital zoom in for 1.0x~2.0x to raw data or 1.0x~7.999x to LCD at small steps
- Support playback mode digital zoom out to LCD or raw data at N/M (=[0..255])
- Support pan/tilt control for LCD output at zoom in
- Support JPEG re-sizing and re-encoding

❑ **Comic Photo Mode Features**

- Support MxN grids of comic photo
- Each grid of comic photo can come either from a stored JPEG file or a captured video frame.

4. PIN DESCRIPTION

4.1 W99685BS Pin Definition (81 Balls, LFBGA Package)

The following signal types are used in these descriptions.

I Input pin
IS Input pin with Schmitt trigger
B Bi-directional input/output pin
BR Bi-directional input/output pin with repeater
BU Bi-directional input/output pin with internal pull-up
O Output pin
A Analog input/output pin
P Power supply pin
G Ground pin
Active low

UART Interface (2 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
TXD / P3[1]	J5	B	Serial Transmit Data Port-3 Bit-1
RXD / P3[0]	H5	B	Serial Receive Data Port-3 Bit-0

Sensor or Video Input Interface (14 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
SVID[9:0]	G7, A5, B5, C5, J8, H8, A6, B6, C6, H9	I	Sensor or Video Data Input SVID[9:0].
SPCLK	B4	I	Clock for Sensor or Video Data Input
SVS	H7	B	Vertical Sync Input. Programmable polarity.
SHS	J7	B	Horizontal Sync Input. Programmable polarity.
SCLK	A4	O	Clock Output to Sensor

LCD Digital Display Interface (19 pins) & Power on Setting (8 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
LA0(R/S)	D8	O	M-LCD: Address-0, for LCD Controller RS signal (CMD/DAT#)
LCD_CS0#	B7	O	M-LCD: LCD Chip Select 0 enable
LCD_WR#	A7	O	M-LCD: Write Enable
LDATA [7:0]/ Setting [7:0]	E7, D9, F7, C9, G8, F9, D7, E9	BU	Digital Display Output Data 8 bits Power On Setting [7:0]
LDATA [15:8]	B8, A8, A9, C8, E8, B9, G9, F8	BU	Digital Display Output Data [15:8]bits

Host Interface (23 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
FA0	B1	BR	Address-0
FA1	J6	BR	Address-1
FA2	C1	BR	Address-2
FIORD#	D2	BU	I/O Read Strobe
FIOWR#	E3	BU	I/O Write Strobe
FCE2# / LCD_CS#	E2	BR	Chip Select Signal – 2 LCD Function Selected
FCE1#	D1	BR	Chip Select Signal – 1
FD [15:0]	A2, A1, C2, J4, B2, C3, B3, A3, H3, H4, F2, E1, G3, G4, G5, F3	BR	Data Bus FD[15:0]

GPIO (6 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
GPIO0	J3	BU	General Purpose I/O [0]
GPIO1/ LCD_CS1#	G1	BU	General Purpose I/O [1] M-LCD: LCD Chip Select 1 enable
GPIO2/	D3	BU	General Purpose I/O [2]
GPIO3/ SCK	C4	BU	General Purpose I/O [3] Serial Interface Clock
GPIO4/ SDI/SDA	G6	BU	General Purpose I/O [4] Serial Interface Data Input/ Serial Data Acknowledge
GPIO5/ SDO/SDE	H6	BU	General Purpose I/O [5] Serial Interface Data Output / Serial Data Enable

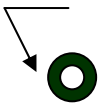
Miscellaneous (4 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
XIN	G2	I	Reference frequency input from ext. crystal or a clock source.
XOUT	F1	O	Oscillator output to a crystal. This pin is left unconnected if an external clock source is employed.
RESET	H1	IS	Reset In. This pin is active high to reset W99685 chip.
TME	J1	I	Test Mode Enable. Only for test, this pin must be connected to GND for normal operation.

Power and Ground (13 pins)

PIN NAME	PIN NUMBER	TYPE	DESCRIPTION
VDDB	C7, E6, J9	P	I/O Pad Buffer Power Supply. Provide isolated power to the I/O buffers for improved noise immunity. 2.6V~3.6 V.
GND	D4, D6, E5, F4, F6	G	I/O Pad Buffer Ground.
VDDI	D5, F5	P	Internal Core Logic Power Supply. 1.8 V .
AVDDP	J2	P	PLL Power Supply. 1.8 V .
AVSSP	H2	G	PLL Ground.
VDDFB	E4	P	Embedded Frame Buffer Power Supply. 2.6V~3.6 V.

4.2 W99685BS-81b Pin Assignment – Top View



	1	2	3	4	5	6	7	8	9
A	FD14	FD15	FD8	SCLK	SVID8	SVID3	LCD_WR #	LDAT14	LDAT13
B	FA0	FD11	FD9	SPCLK	SVID7	SVID2	LCD_CS0 #	LDAT15	LDAT10
C	FA2	FD13	FD10	GPIO3 / SCK	SVID6	SVID1	VDDB	LDAT12	LDAT4
D	FCE1#	FIORD#	GPIO2	GND	VDDI (1.8V)	GND	LDAT1	LA0(R/S)	LDAT6
E	FD4	FCE2#/ LCD_CS #	FIOWR#	VDDFB	GND	VDDB	LDAT7	LDAT11	LDAT0
F	XOUT	FD5	FD0	GND	VDDI (1.8V)	GND	LDAT5	LDAT8	LDAT2
G	GPIO1/ LCD_CS1 #	XIN	FD3	FD2	FD1	GPIO4 / SDA	SVID9	LDAT3	LDAT9
H	RESET	AVSSP (GND)	FD7	FD6	RXD / P_30	GPIO5 / SDO	SVS	SVID4	SVID0
J	TME	AVDDP (1.8V)	GPIO0	FD12	TXD /P_31	FA1	SHS	SVID5	VDDB

W99685BS 81 Ball Location List

LOCATION/ NUMBER	PIN NAME	LOCATION/ NUMBER	PIN NAME
C7 / (1)	VDDB(2.6V~3.6V)	E8 / (42)	LDAT11
D3 / (2)	GPIO2	C8 / (43)	LDAT12
D2 / (3)	FIORD#	A9 / (44)	LDAT13
E3 / (4)	FIOWR#	A8 / (45)	LDAT14
E2 / (5)	FCE2# / LCD_CS#	B8 / (46)	LDAT15
D1 / (6)	FCE1#	J9 / (47)	VDDB(2.6V~3.6V)
D4 / (7)	GND	D8 / (48)	LA0(R/S)
F3 / (8)	FD0	B7 / (49)	LCD_CS0#
G5 / (9)	FD1	A7 / (50)	LCD_WR#
G4 / (10)	FD2	F4 / (51)	GND
G3 / (11)	FD3	H9 / (52)	SVID0
E1 / (12)	FD4	C6 / (53)	SVID1
F2 / (13)	FD5	B6 / (54)	SVID2
H4 / (14)	FD6	A6 / (55)	SVID3
H3 / (15)	FD7	F6 / (56)	GND
J3 / (16)	GPIO0	H8 / (57)	SVID4
G2 / (17)	XIN	J8 / (58)	SVID5
F1 / (18)	XOUT	C5 / (59)	SVID6
G1 / (19)	GPIO1 / LCD_CS1#	B5 / (60)	SVID7
H2 / (20)	AVSSP(GND)	A5 / (61)	SVID8
J2 / (21)	AVDDP(1.8V)	G7 / (62)	SVID9
J1 / (22)	TME	B4 / (63)	SPCLK
H1 / (23)	RESET	H7 / (64)	SVS
H5 / (24)	RXD / P3_0	J7 / (65)	SHS
J5 / (25)	TXD / P3_1	A4 / (66)	SCLK
E6 / (26)	VDDB(2.6V~3.6V)	C4 / (67)	SCK / GPIO3
D6 / (27)	GND	G6 / (68)	SDA / GPIO4
D5 / (28)	VDDI(1.8V)	H6 / (69)	SDO / GPIO5
E5 / (29)	GND	A3 / (70)	FD8
E9 / (30)	LDAT0 / SET0	B3 / (71)	FD9

W99685BS 81 Ball Location List, continued

LOCATION/ NUMBER	PIN NAME	LOCATION/ NUMBER	PIN NAME
F5 / (31)	VDDI(1.8V)	C3 / (72)	FD10
D7 / (32)	LDAT1 / SET1	B2 / (73)	FD11
F9 / (33)	LDAT2 / SET2	J4 / (74)	FD12
G8 / (34)	LDAT3 / SET3	C2 / (75)	FD13
C9 / (35)	LDAT4 / SET4	A1 / (76)	FD14
F7 / (36)	LDAT5 / SET5	A2 / (77)	FD15
D9 / (37)	LDAT6 / SET6	B1 / (78)	FA0
E7 / (38)	LDAT7 / SET7	J6 / (79)	FA1
F8 / (39)	LDAT8	C1 / (80)	FA2
G9 / (40)	LDAT9	E4 / (81)	VDDFB(2.6V~3.6V)
B9 / (41)	LDAT10		

5. ELECTRICAL CHARACTERISTICS

5.1 Absolute Maximum Ratings

PARAMETER	MIN.	MAX.	UNIT
Ambient temperature	-20	70	°C
Storage temperature	-40	125	°C
DC supply voltage for core (1.8V) VDDI	0	2.0	V
DC supply voltage for I/O (2.8V) VDDB	0	3.6	V
I/O pin voltage with respect to V_{SS}	– 0.3	VDDB + 0.4	V

Table 5-1

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

5.2 D.C. Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DDB}	Power Supply for I/O Pads		2.6	2.8	3.6	V
A_{VDDP}	Power Supply for PLL Analog		1.70	1.8	1.90	V
V_{DDI}	Power Supply for Core		1.70	1.8	1.90	V
V_{IL}	Input Low Voltage		0		0.8	V
V_{IH}	Input High Voltage		2.0		VDDB	V
V_{OL}	Output Low Voltage	I_{OUT} = 2mA			VSS +0.4	V
V_{OH}	Output High Voltage	I_{OUT} = -2mA	VDDB * 0.8			V
V_{OH} (P30/P31)	Output High Voltage (Open Drain with Internal Pull-Up)	I_{OUT} = -2 mA			2.0	V
I_{IL}	Input Low Leakage Current	V_{IN} = 0.4V			10	μA
I_{IH}	Input High Leakage Current	V_{IN} = 2.4V			-10	μA
I_{UP}	Pull-up Current	V_{IN} = 0V			-500	μA
I_{PD}	Power Down Current (XIN=0, No Load)	Core V_{DDI}= 1.8V		20		μA
		I/O V_{DDB}= 2.8V		120		
I_{DD}	Active Current	160x120 preview at 15 fps CPU clock at 12 MHz Engine clock at 24 MHz		20	30	mA

Table 5-2

5.3 A.C. Characteristics

5.3.1 RESET A.C. Characteristics

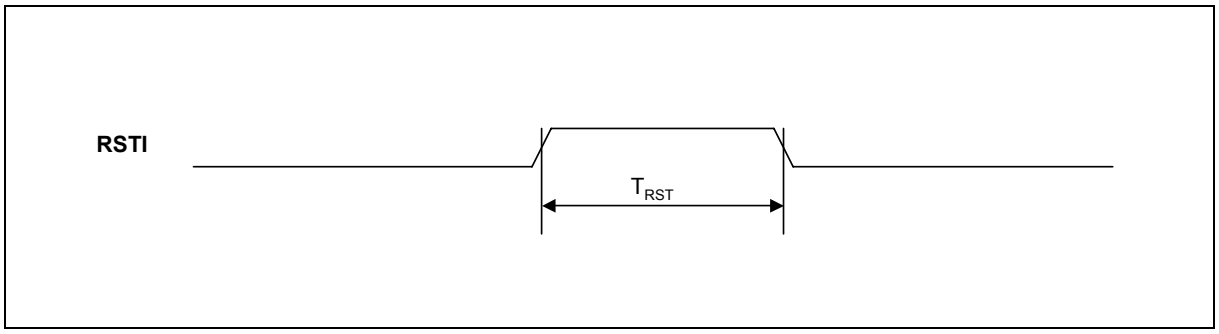


Figure 5.1 RESET Timing Diagram

RESET Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{RST}	Reset Pulse Width		1.0		mS

Table 5-3

5.3.2 Video Input A.C. Characteristics

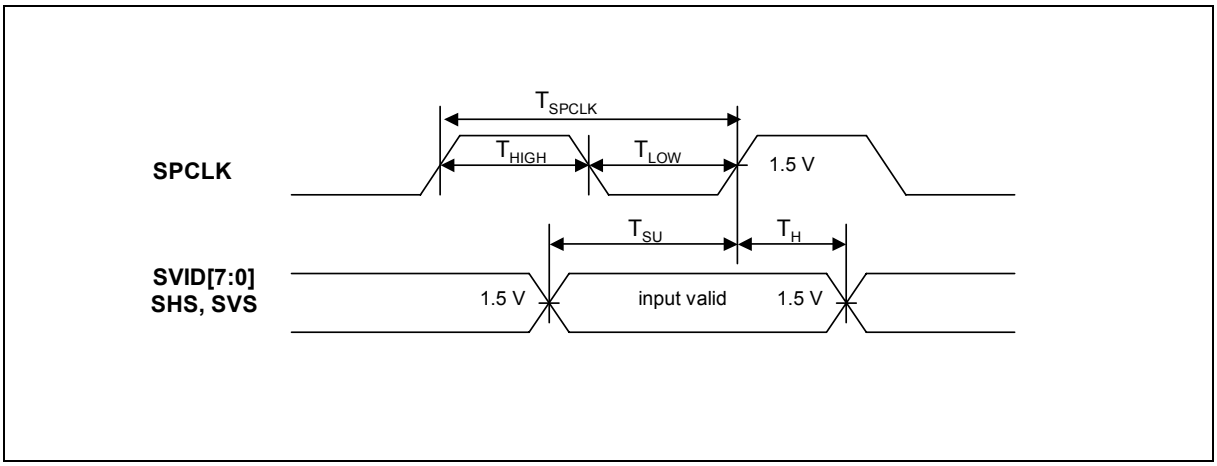


Figure 5.2 Input Video Timing Diagram

Input Video Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
F_{SPCLK}	SPCLK Frequency = 1 / T_{SPCLK}		5	48	MHz
T_{HIGH}	SPCLK Clock High Time		5		nS
T_{LOW}	SPCLK Clock Low Time		5		nS
T_{SU}	SVID[9:0], SHS, SVS Setup Time		6		nS
T_H	SVID[9:0], SHS, SVS Hold Time		4		nS

Table 5-4

5.3.3 Host Interface: CF-IDE Slave (Memory Bus) A.C. Characteristics

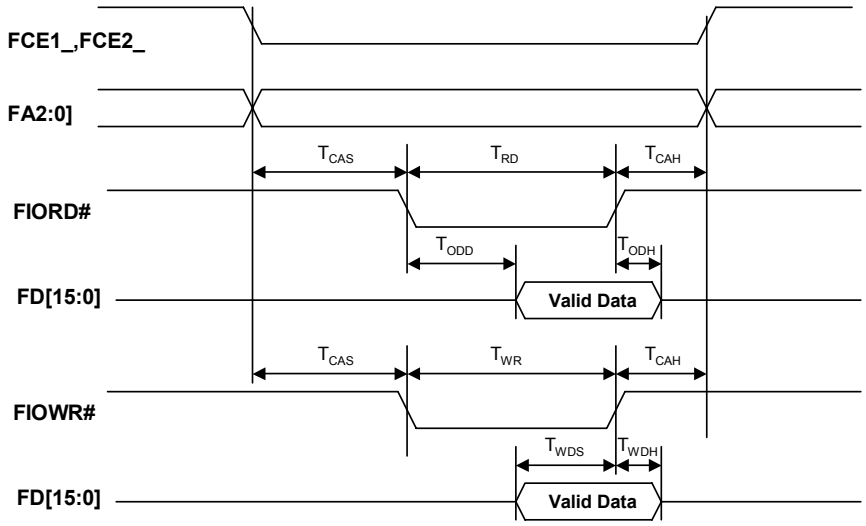


Figure 5.3 Host Interface: CF-IDE Slave (Memory Bus) Timing Diagram

Host Interface: CF_IDE Slave (Memory Bus) Timing

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{CAS}	Chip Select & Address Set-up Time		65	---	nS
T_{CAH}	Chip Select & Address Hold Time		5	---	nS
T_{ODD}	FIORD# Low to Data Valid Delay		---	$4T_{MCLK}$	nS
T_{ODH}	Read Data Output Hold Time		0	---	nS
T_{RD}	FIORD# Pulse Width		$*165/4T_{MCLK}$	---	nS
T_{WDS}	Write Data Input Setup Time		60	---	nS
T_{WDH}	Write Data Input Hold Time		2	---	nS
T_{WR}	WR# Pulse Width		$*165/4T_{MCLK}$	---	nS

Table 5-5

$165/4T_{MCLK}$: 165ns or 4 internal engine clock cycles

5.3.4 LCD Interface A.C. Characteristics

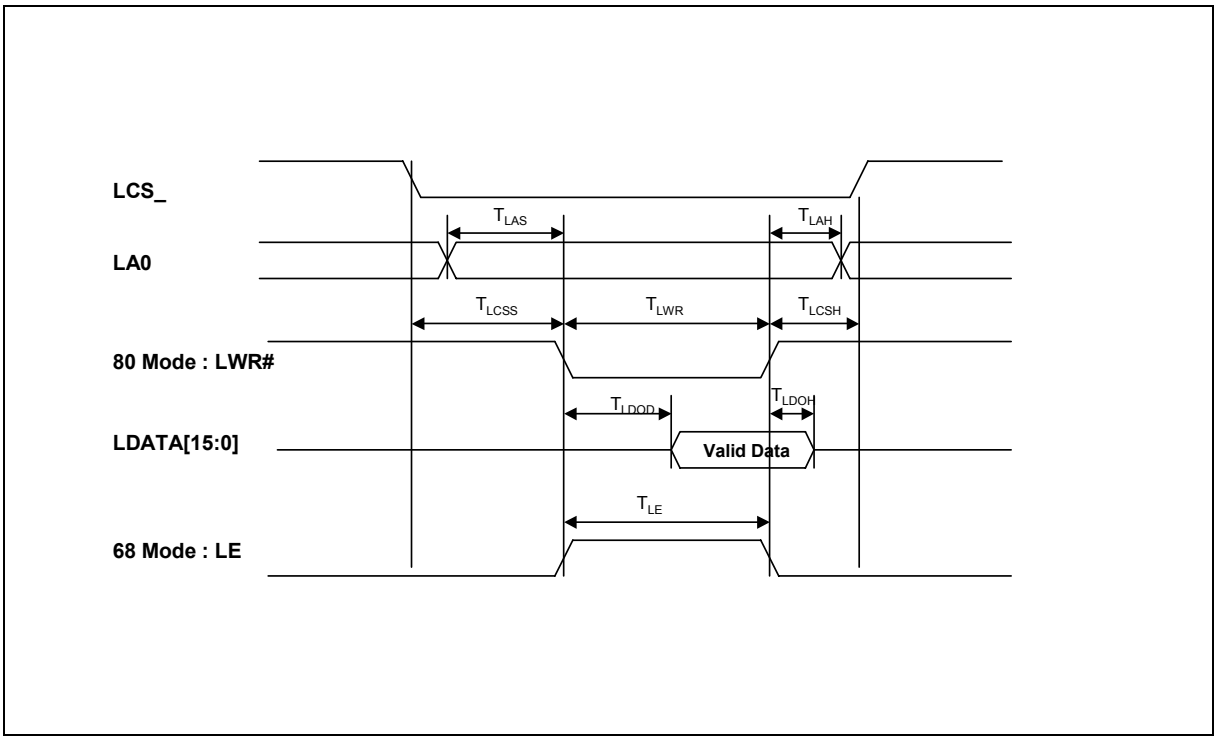


Figure 5.4 LCD Interface Timing Diagram

LCD Interface Timing

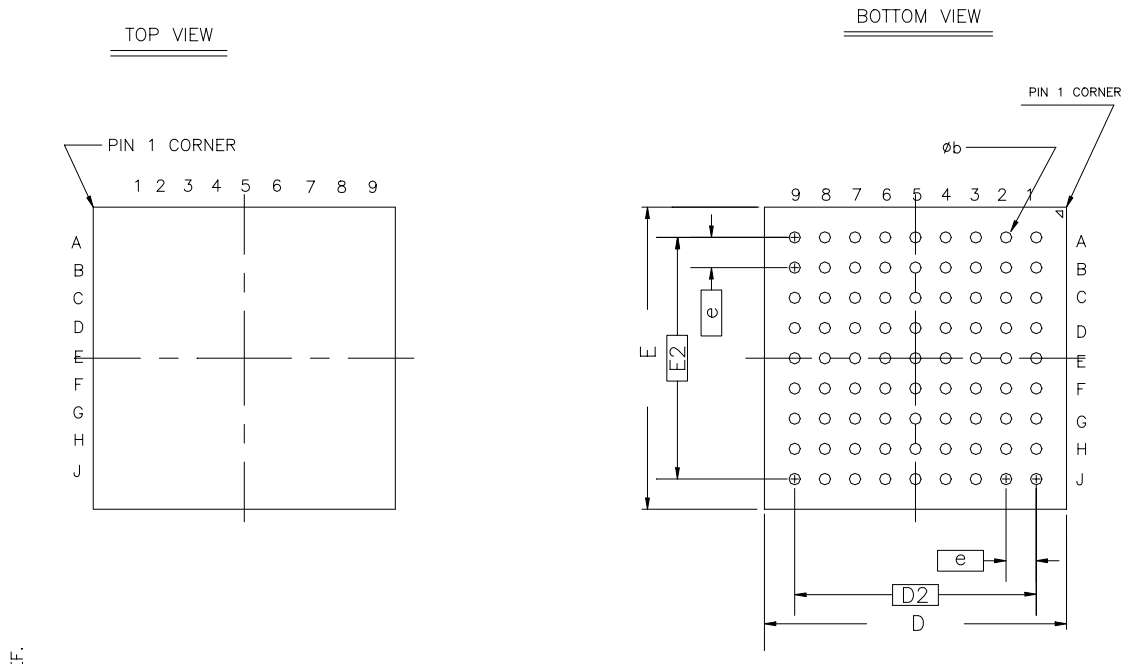
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
T_{LCSS}	Chip Select Set-up Time		0.5	---	PCLK
T_{LCSH}	Chip Select Hold Time		0.5	---	PCLK
T_{LAS}	Address Set-up Time		1	---	PCLK
T_{LAH}	Address Hold Time		1	---	PCLK
T_{LDOD}	Write Data Active Delay		5	---	nS
T_{LDOH}	Write Data Hold Time		0.5	---	PCLK
T_{LWR}	LWR# Pulse Width	80 Mode	0.5		PCLK
T_{LE}	LE Pulse Width	68 Mode	0.5		PCLK

Table 5-6

Note: PCLK => Engine Clock / 32

6. PACKAGE DIMENSION

6.1 81L LFBGA (8 x 8 mm, Ball pitch: 0.8 mm, Ø = 0.4 mm)



COTROL DIMENSIONS ARE IN MILLIMETERS.

SYMBOL	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	–	–	1.50	–	–	0.059
A1	0.27	–	0.37	0.011	–	0.015
D	7.95	8.00	8.05	0.313	0.315	0.317
D2	6.40 BASIC			0.252 BASIC		
E	7.95	8.00	8.05	0.313	0.315	0.317
E2	6.40 BASIC			0.252 BASIC		
y	0.08 BASIC			0.003 BASIC		
øb	0.37	–	0.47	0.015	–	0.019
e	0.80 BASIC			0.032 BASIC		

7. REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A1	June 28, 2004		Initial Issue
A2	Dec. 15, 2004	16	Revise Fspclk to 48 MHz
A3	Feb. 24, 2005	2, 4, 8	Update LCD I/F, JPEG Codec
A4	April 13, 2005	15	Update I_{PD}

Important Notice

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