DATA SHEET

Part No.	AN15865A
Package Code No.	*QFH080-P-1420H

SEMICONDUCTOR COMPANY
MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.

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Contents

AN15865A

The video switch IC including the synchronous separation function for TV

■ Overview

The AN15865A has the video switch portion which consists of a five-channel output in a ten-channel input, the synchronous separation function, the AFC function, and the format detection function. It contributes to the rationalization design of a television system.

■ Features

1. Support multi scan / Auto format identification 480i, 576i, 480P, 576P, 720P, 1080i, 1152i, 1152i/letter (both 50 Hz & 60 Hz)
2. Field 1 or 2 monitor out is available
3. Auto distinction in the selected input (Sync on CV/Y or Sync on SY or no input signal)
4. Dummy sync output 480i, 576i, 480P, 576P, 720P, 1080i (both 50 Hz & 60 Hz)
5. Sync separation with AFC w/o external x-tal or clock
6. 2 values, 3 values sync identification
7. RGB → YUV converter (CCIR standard, BTA standard, GBR matrix)
8. Each output can be switched between LPF (6 MHz) & through
9. Each output can be switched among 0 dB, 6 dB or mute
10. Macrovision
11. Comparators for Pin detection ×4 (Connected / Open)
12. Comparators for Aspect ratio ×4 (4:3 video / 4:3 letter box / 16:9 video)
13. High frequency (0 dB at 50 MHz)
14. Support the I^2C BUS
15. Various input mode can be selected by using flexible internal switch

INPUT

IN1	CV1		
IN2	CV2		
IN3	CV3		
IN4	CV4/SY4/SC4	Y7/U7/V7	
IN5	CV5/SY5/SC5	Y6/U6/V6	H6/V6
IN6	CV6/SY6/SC6	Y5/U5/V5	H5/V5
IN7	CV7/SY7/SC7	Y4/U4/V4	H4/V4
IN8		Y3(G3)/U3(B3)/V3(R3)	H3/V3
IN9		Y2(G2)/U2(B2)/V2(R2)	H2/V2
IN10		Y1(G1)/U1(B1)/V1(R1)	H1/V1

OUTPUT

OUT1	CV1-7/SY4-7/ SC4-7	
OUT2	CV1-7(SY4-7)/ SC4-7	
OUT3	CV1-7(SY4-7)/ SC4-7	
OUT4	G(Y1-6)(CV1-7)/B(U1-6)(SY4-7)/ R(V1-6)(SC4-7)	H1/V1 *1
OUT5	G(Y1-6)(CV1-7)/B(U1-6)(SY4-7)/ R(V1-6)(SC4-7)	H2/V2 *2

Note) *1: Independent HV only
*2: Independent HV or Sync-separated HV

■ Applications

- IC for Color TV

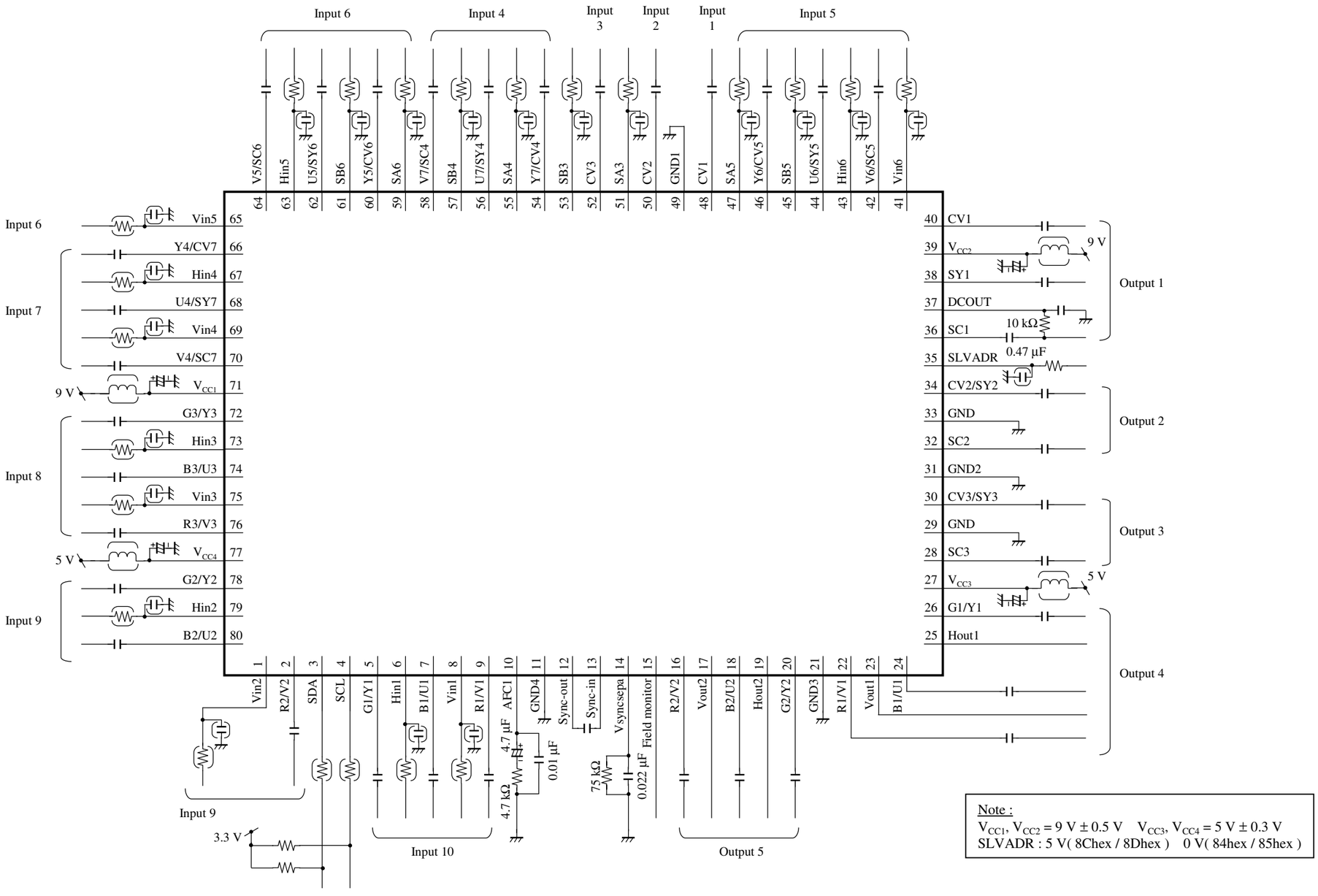
■ Package

- 80 Pin Plastic High Profile Quad Flat Package (QFP Type)

■ Type

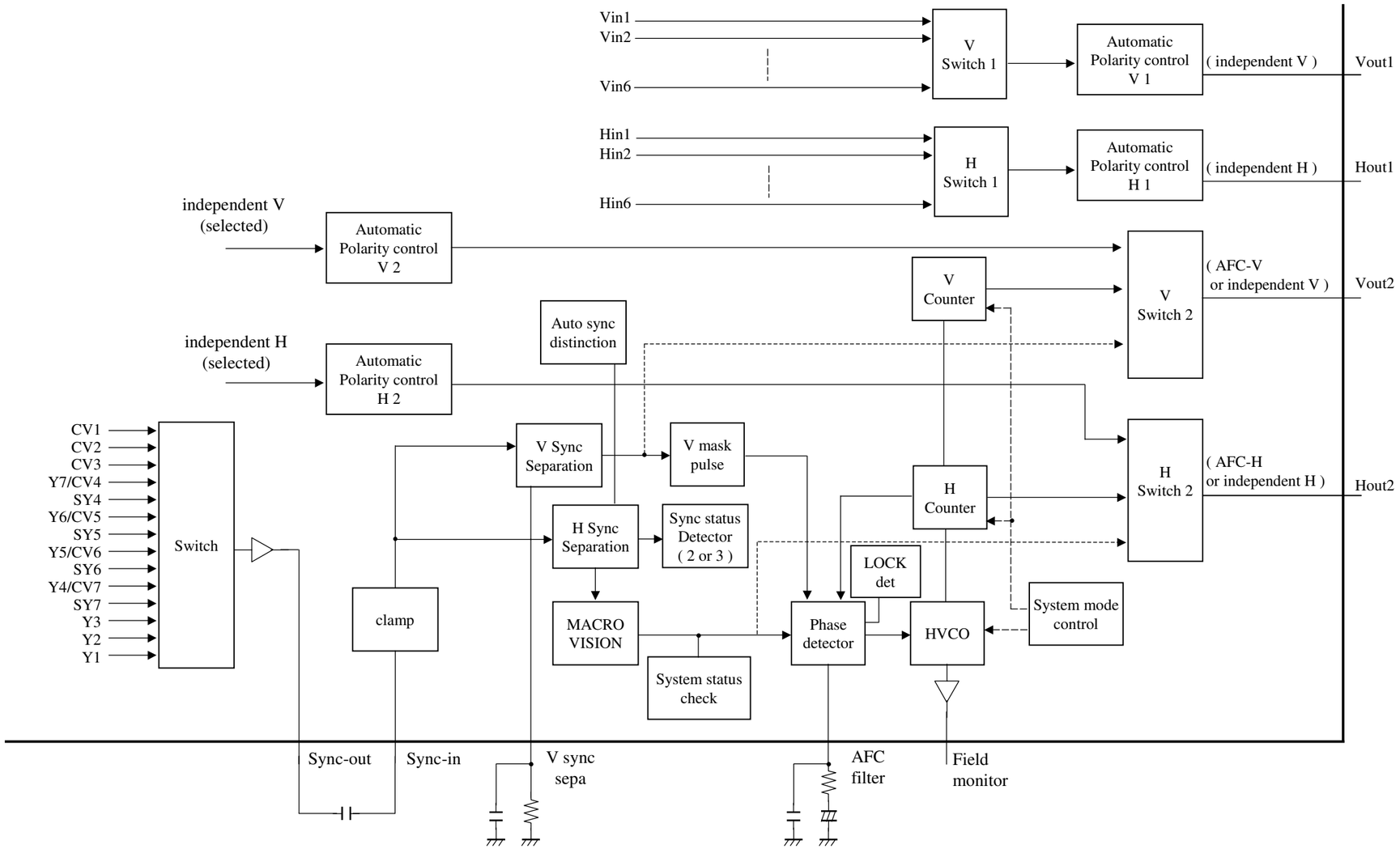
- Silicon Monolithic BICMOS IC

■ Application Circuit Example



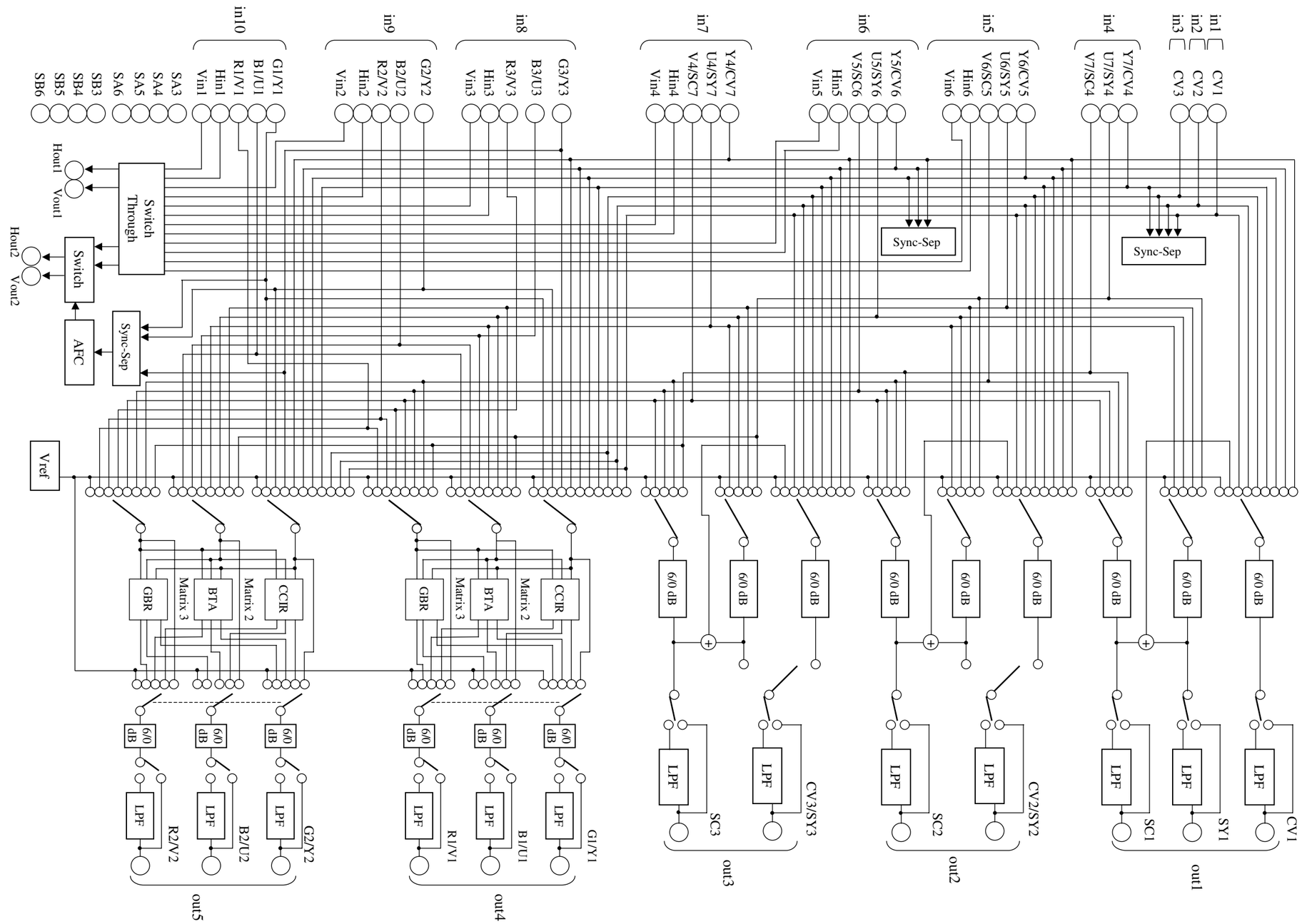
■ Block Diagram

(SYNC separation and AFC system)



■ Block Diagram (continued)

(Video-Switch)



■ Pin Descriptions

Pin No.	Pin name	Type	Description
1	Vin2	In	Independent V signal input 2
2	R2/V2	In	R2/V2 signal input
3	SDA	In / Out	I^2C bus data input
4	SCL	In	I^2C bus clock input
5	G1/Y1	In	G1/Y1 signal input
6	Hin1	In	Independent H signal input 1
7	B1/U1	In	B1/U1 signal input
8	Vin1	In	Independent V signal input 1
9	R1/V1	In	R1/V1 signal input
10	AFC1	In / Out	AFC filter
11	GND4	Ground	Ground
12	Sync-out	Out	Sync signal output for sync separation
13	Sync-in	In	Sync signal input for sync separation
14	V sync sepa	In / Out	V sync separation filter
15	Field monitor	Out	Field change signal output
16	R2/V2	Out	R2/V2 signal output
17	Vout2	Out	Independent V signal output 2
18	B2/U2	Out	B2/U2 signal output
19	Hout2	Out	Independent H signal output 2
20	G2/Y2	Out	G2/Y2 signal output
21	GND3	Ground	Ground
22	R1/V1	Out	R1/V1 signal output
23	Vout1	Out	Independent V signal output 1
24	B1/U1	Out	B1/U1 signal output
25	Hout1	Out	Independent H signal output 1
26	G1/Y1	Out	G1/Y1 signal output
27	V_{CC3}	Power supply	5.0 V power supply
28	SC3	Out	SC3 signal output
29	GND	Ground	Ground
30	CV3/SY3	Out	CV3/SY3 signal output
31	GND2	Ground	Ground
32	SC2	Out	SC2 signal output
33	GND	Ground	Ground
34	CV2/SY2	Out	CV2/SY2 signal output
35	SLVADR	In	Sets the I^2C bus slave address

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
36	SC1	Out	SC1 signal output
37	DCOUT	Out	Output DC voltage corresponding to S2
38	SY1	Out	SY1 signal output
39	V_{CC2}	Power supply	9.0 V power supply
40	CV1	Out	CV1 signal output
41	Vin6	In	Independent V signal input 6
42	V6/SC5	In	V6/SC5 signal input
43	Hin6	In	Independent H signal input 6
44	U6/SY5	In	U6/SY5 signal input
45	SB5	In	Pin status detection for input channel 5
46	Y6/CV5	In	Y6/CV5 signal input
47	SA5	In	Aspect ratio detection for input channel 5
48	CV1	In	CV1 signal input
49	GND1	Ground	Ground
50	CV2	In	CV2 signal input
51	SA3	In	Aspect ratio detection for input channel 3
52	CV3	In	CV3 signal input
53	SB3	In	Pin status detection for input channel 3
54	Y7/CV4	In	CV4 signal input
55	SA4	In	Aspect ratio detection for input channel 4
56	U7/SY4	In	SY4 signal input
57	SB4	In	Pin status detection for input channel 4
58	V7/SC4	In	SC4 signal input
59	SA6	In	Aspect ratio detection for input channel 6
60	Y5/CV6	In	Y5/CV6 signal input
61	SB6	In	Pin status detection for input channel 6
62	U5/SY6	In	U5/SY6 signal input
63	Hin5	In	Independent H signal input 5
64	V5/SC6	In	V5/SC6 signal input
65	Vin5	In	Independent V signal input 5
66	Y4/CV7	In	Y4/CV7 signal input
67	Hin4	In	Independent H signal input 4
68	U4/SY7	In	U4/SY7 signal input
69	Vin4	In	Independent V signal input 4
70	V4/SC7	In	V4/SC7 signal input

■ Pin Descriptions (continued)

Pin No.	Pin name	Type	Description
71	V_{CC1}	Power supply	9.0 V power supply
72	G3/Y3	In	G3/Y3 signal input
73	Hin3	In	Independent H signal input 3
74	B3/U3	In	B3/U3 signal input
75	Vin3	In	Independent V signal input 3
76	R3/V3	In	R3/V3 signal input
77	V_{CC4}	Power supply	5.0 V power supply
78	G2/Y2	In	G2/Y2 signal input
79	Hin2	In	Independent H signal input 2
80	B2/U2	In	B2/U2 signal input

■ Absolute Maximum Ratings

A No.	Parameter	Symbol	Rating	Unit	Note
1	Supply voltage	V_{CC1}, V_{CC2}	10.0	V	*1
		V_{CC3}, V_{CC4}	5.5		
2	Supply current	I_{CC1}, I_{CC2}	130	mA	
		I_{CC3}, I_{CC4}	23		
3	Power dissipation	P_D	773	mW	*2
4	Operating ambient temperature	T_{opr}	−20 to +75	°C	*3
5	Storage temperature	T_{stg}	−55 to +125	°C	*3

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

*2: The power dissipation shown is the value at T_a = 75°C for the independent IC package without a heat sink.
Refer to the package power dissipation prepared else and use under the condition not exceeding the allowable value.

*3: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.

■ Operating supply voltage range

Parameter	Symbol	Range	Unit	Note
Operating supply voltage range	V_{CC1}, V_{CC2}	8.5 to 9.5	V	—
	V_{CC3}, V_{CC4}	4.7 to 5.3		*

Note) *: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.

■ Electrical Characteristics at V_{CC1}, V_{CC2} = 9 V, V_{CC3}, V_{CC4} = 5 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Note
					Min	Typ	Max		
1	Quiescent Current	I_{CQ12}	1	No signal input V_{CC1}, V_{CC2}	109	118	127	mA	
2	Quiescent Current	I_{CQ34}	1	No signal input V_{CC3}, V_{CC4}	10	15	20	mA	
3	Video Gain	G_{V0}	1	f = 500 kHz, V_{IN} = 1 V[p-p] (except composite pass)	– 0.7	– 0.2	0.3	dB	
		G_{V6}	1		5.2	5.7	6.2	dB	
4	Video Frequency Response 1	f_{V1}	1	1.0 V[p-p] input at 30 MHz/500 kHz (during 6 dB output)(LPF OFF)	–1.5	—	1.0	dB	
5	Video Frequency Response 2	f_{V2}	1	1.0 V[p-p] input at 30 MHz/500 kHz (during 0 dB output) (composite in)	–1.5	—	1.0	dB	
6	Crosstalk	CT_V	1	1.0 V[p-p] input at 5 MHz Between contiguity channels	—	—	–50	dB	
7	Output DC level	dVD_O	1	Measure the difference from the Output DC level while in mute mode.	– 0.4	—	0.4	V	
8	LPF characteristic1	f_{LPF1}	1	1.0 V[p-p] input at 6 MHz/500 kHz (LPF ON)	– 6	–3	0	dB	
9	LPF characteristic2	f_{LPF2}	1	1.0 V[p-p] input at 10 MHz/500 kHz (LPF ON)	—	—	–25	dB	
[Hout items]									
10	Hout1/2 high level	H_{HI}	1		2.8	3.3	—	V	
11	Hout1/2 low level	H_{LO}	1		—	—	0.5	V	
12	Hout2 pulse width(1)	H_{WID1}	1	mode 480i, 576i	1.2	1.6	2.0	µs	
13	Hout2 pulse width(2)	H_{WID2}	1	mode 480p, 576p	0.6	1.0	1.4	µs	
14	Hout2 pulse width(3)	H_{WID3}	1	mode 1080i, 720p, 1152i, 1152i /letter	520	660	800	ns	
15	H pull in range upper	fH_{PULLUP}	1		700	—	—	Hz	
16	H pull in range lower	$fH_{PULLLOW}$	1		—	—	– 700	Hz	
17	Hout2 free-run Freq.1	fH_{FREE1}	1	mode 576i	15.53	15.62	15.72	kHz	
18	Hout2 free-run Freq.2	fH_{FREE2}	1	mode 576p, 1152i, 1152i/letter	31.06	31.25	31.43	kHz	
19	Hout2 free-run Freq.3	fH_{FREE3}	1	mode 1080i/50	28.00	28.17	28.34	kHz	
20	Hout2 free-run Freq.4	fH_{FREE4}	1	mode 720p/50	37.28	37.50	37.72	kHz	
21	Hout2 free-run Freq.5	fH_{FREE5}	1	mode 480i	15.65	15.75	15.84	kHz	

■ Electrical Characteristics (continued) at V_{CC1}, V_{CC2} = 9 V, V_{CC3}, V_{CC4} = 5 V

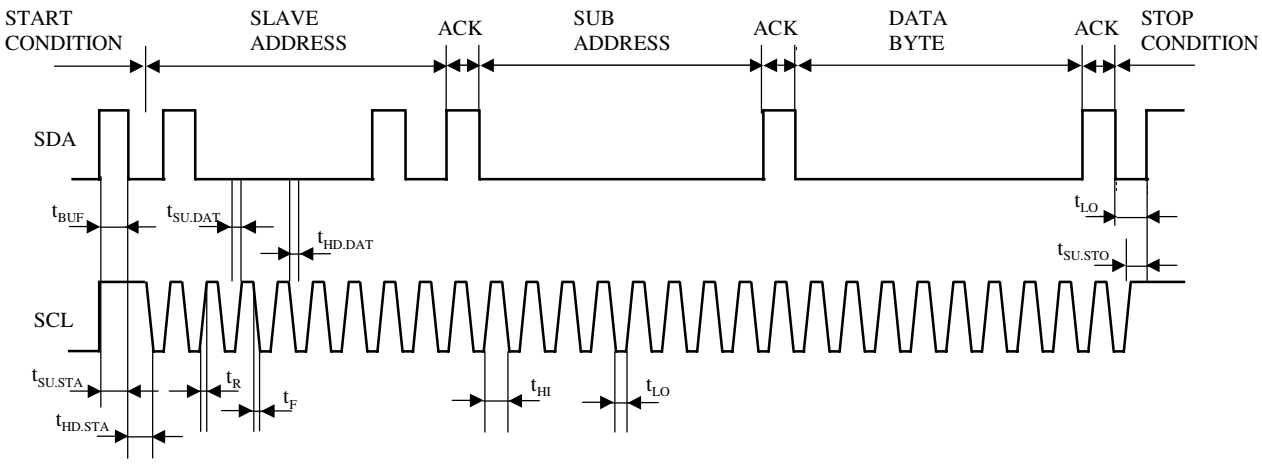
Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Note
					Min	Typ	Max		
22	Hout2 free-run Freq.6	fH_{FREE6}	1	mode 480p	31.23	31.41	31.60	kHz	
23	Hout2 free-run Freq.7	fH_{FREE7}	1	mode 1 080i/60	33.51	33.71	33.90	kHz	
24	Hout2 free-run Freq.8	fH_{FREE8}	1	mode 720p/60	44.84	45.11	45.38	kHz	
[Vout items]									
25	Vout1/2 high level	V_{HI}	1		2.8	3.3	—	V	
26	Vout1/2 low level	V_{LO}	1		—	—	0.5	V	
27	Vout2 pulse width(1)	V_{WID1}	1	AFC/free mode 480i, 480p, 1080i/60	—	6	—	H	
28	Vout2 pulse width(2)	V_{WID2}	1	AFC/free mode 576p, 1080i/50	—	6	—	H	
29	Vout2 pulse width(3)	V_{WID3}	1	AFC/free mode 1152i/letter	—	6	—	H	
30	Vout2 pulse width(4)	V_{WID4}	1	AFC/free mode 720p/60	—	5	—	H	
31	Vout2 pulse width(5)	V_{WID5}	1	AFC/free mode 576i, 720p/50	—	5	—	H	
32	Vout2 pulse width(6)	V_{WID6}	1	AFC/free mode 1152i	—	6	—	H	
[Address Pins]									
33	Address setting voltage (84/85hex)	V_{ADR1}	1		—	—	1.5	V	
34	Address setting voltage (8C/8Dhex)	V_{ADR2}	1		2.5	—	—	V	
[DCOUT]									
35	S2 compatible DC level L [00]	V_{DCL}	1		—	—	0.5	V	
36	S2 compatible DC level M [01]	V_{DCM}	1		1.4	—	2.8	V	
37	S2 compatible DC level H [11]	V_{DCH}	1		4.0	—	—	V	

■ Electrical Characteristics (continued) at V_{CC1}, V_{CC2} = 9 V, V_{CC3}, V_{CC4} = 5 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Limits			Unit	Note
					Min	Typ	Max		
[I²C Interface]									
38	Suction current during ACK	V_{ACK}	1	The pin voltage with Pin 3 suction current set to 3 mA during Ack.	—	—	0.4	V	
39	SCL, SDA signal input high level	V_{IHI}	1		3.0	—	5.5	V	
40	SCL, SDA signal input low level	V_{ILO}	1		0	—	1.5	V	
41	Max. frequency allowable to input	f_{imax}	1		100	—	—	Kbit/s	



Note) The above characteristics are reference values on IC designing and not guaranteed by shipping inspection.

■ Electrical Characteristics (Reference values for design) at V_{CC1}, V_{CC2} = 9 V, V_{CC3}, V_{CC4} = 5 V

Note) T_a = 25°C±2°C unless otherwise specified.

B No.	Parameter	Symbol	Test circuits	Conditions	Reference values			Unit	Note
					Min	Typ	Max		
42	Input Dynamic Range	V_{DYV}	1		2.4	—	—	V[p-p]	*1
43	Mute DC level	V_M	1		—	3.5	—	V	*1
44	Output pedestal level	V_{PED}	1	1.0 V[p-p] input 0 dB mode	—	3.5	—	V	*1
45	Output sync level	V_{SYNC}	1	1.0 V[p-p] input 0 dB mode	—	3.2	—	V	*1
[Hout items]									
46	H VCO osc. Chara.	B_H	1	Conversion by 6 MHz	—	–1.4	—	kHz/mV	*1
[Vout items]									
47	Vout2 free-run Freq.1	fV_{FREE1}	1	mode (V : 50 Hz)	—	50	—	Hz	*1
48	Vout2 free-run Freq.2	fV_{FREE2}	1	mode (V : 60 Hz)	—	60	—	Hz	*1
[SA SB Pins]									
49	Scart ident SA L	V_{SAL}	1		—	—	1.0	V	*1
50	Scart ident SA M	V_{SAM}	1		1.7	—	3.0	V	*1
51	Scart ident SA H	V_{SAH}	1		4.0	—	—	V	*1
52	Pin detect SB L	V_{SBL}	1		—	—	1.5	V	*1
53	Pin detect SB H	V_{SBH}	1		2.5	—	—	V	*1
[Others]									
54	Hin L	H_{SL}	1		—	—	1.5	V	*1
55	Hin H	H_{SH}	1		2.5	—	—	V	*1
56	Vin L	V_{SL}	1		—	—	1.5	V	*1
57	Vin H	V_{SH}	1		2.5	—	—	V	*1

Note) *1 : The characteristics listed above are logical values derived from the design, and as such, all of these cannot be guaranteed. If, in the unlikely case that problems do occur related to these parameters, Panasonic will negotiate in good faith with the customer on these matters.

■ I²C Bus Conditions

- The AN15865A in I²C bus control performs switch mode selection, matrix selection, gain selection, LPF selection, synchronous mode selection and freerun mode selection through a control register and detects the system status, aspect and pin information through a status register.
  The upper seven address bits are allocated to the slave address while the LSB is allocated to the R/W bit.
  The R/W bit corresponds to the control register with with the bit set to 0 and corresponds to the status register with the bit set to 1.

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
84/8C 85/8D	1	0	0	0	1/0	1	0	R/W

Note) The change of D3 data is performed by control of a SLVADR terminal

Control Register

- The AN15865A selects slave address 84 or 8C(hex) according to the status of the SLVADR pin.
  Address 84(hex) will be selected with the SLVADR pin grounded the the GND side. Address 8C(hex) will be selected with the pin grounded to the 5-V line.

S	Slave Address (84 or 8C)	AS	Sub Address (X)	AS	DATA (X)	AS	DATA (X + 1)	AS	DATA (X + 2)	continue

Note) AS = ACK from Slave

R/W = 0

Sub Address	D7	D6	D5	D4	D3	D2	D1	D0
00	OUT1signal select				OUT2 signal select			
01	OUT3 signal select				OUT4 signal select			
02	OUT5 sync distinction	00 : auto distinction 01 : sync on CV/Y use 10 : sync on SY use 11 : free-run	free-run priority 0 : fixing 1 : auto distinction use	OUT5 sync 0 : AFC 1 : independent	OUT5 signal select			
03	OUT4 matrix	00 : through 01 : CCIR standard 10 : BTA standard 11 : GBR matrix	OUT5 matrix	00 : through 01 : CCIR standard 10 : BTA standard 11 : GBR matrix	Dummy sync mode Control (When 02/D7, D6 = '11')	000 : 480i / 60 001 : 480p / 60 010 : 1 080i / 60 011 : 720p / 60	100 : 576i / 50 101 : 576p / 50 110 : 1 080i / 50 111 : 720p / 50	HVout2 polarity 0 : positive 1 : negative
04	CV1 GAIN 0 : 0 dB 1 : 6 dB	SY1/SC1 GAIN 0 : 0 dB 1 : 6 dB	CV2 GAIN 0 : 0 dB 1 : 6 dB	SY2/SC2 GAIN 0 : 0 dB 1 : 6 dB	CV3 GAIN 0 : 0 dB 1 : 6 dB	SY3/SC3 GAIN 0 : 0 dB 1 : 6 dB	OUT4 GAIN 0 : 0 dB 1 : 6 dB	OUT5 GAIN 0 : 0 dB 1 : 6 dB
05	OUT1 LPF 0 : through 1 : LPF ON	OUT2 LPF 0 : through 1 : LPF ON	OUT3 LPF 0 : through 1 : LPF ON	OUT4 LPF 0 : through 1 : LPF ON	OUT5 LPF 0 : through 1 : LPF ON	OUT1 DCOUT	00 : 0 V 01 : 1.9 V 10 : indefinite 11 : 4.5 V	Field monitor sel 0 : F1 / F2 out 1 : clock moni out
06	input4 U/SY sel 0 : SY select 1 : U select	input5 U/SY sel 0 : SY select 1 : U select	input6 U/SY sel 0 : SY select 1 : U select	input7 U/SY sel 0 : SY select 1 : U select	input8 BR/UV sel 0 : BR select 1 : UV select	input9 BR/UV sel 0 : BR select 1 : UV select	input10 BR/UV sel 0 : BR select 1 : UV select	Australia free-run 0 : except Australia 1 : Australia mode
07	test77	test76	test75	test74	test73	test72	test71	test70
08	test87	test86	test85	test84	test83	test82	test81	test80

Note) Please send data "00" to sub-address "07" and "08".

■ I²C Bus Conditions (continued)

OUT1 signal select

00/D7	00/D6	00/D5	00/D4	CV1 OUT1	SY1 OUT1	SC1 OUT1
0	0	0	0	CV1 IN1	DC	DC
0	0	0	1	CV2 IN2	DC	DC
0	0	1	0	CV3 IN3	DC	DC
0	0	1	1	CV4 IN4	SY4 IN4	SC4 IN4
0	1	0	0	SY4 + SC4 IN4 IN4	SY4 IN4	SC4 IN4
0	1	0	1	CV5 IN5	SY5 IN5	SC5 IN5
0	1	1	0	SY5 + SC5 IN5 IN5	SY5 IN5	SC5 IN5
0	1	1	1	CV6 IN6	SY6 IN6	SC6 IN6
1	0	0	0	SY6 + SC6 IN6 IN6	SY6 IN6	SC6 IN6
1	0	0	1	CV7 IN7	SY7 IN7	SC7 IN7
1	0	1	0	SY7 + SC7 IN7 IN7	SY7 IN7	SC7 IN7
1	0	1	1	DC	DC	DC
1	1	0	0	DC	DC	DC
1	1	0	1	DC	DC	DC
1	1	1	0	DC	DC	DC
1	1	1	1	DC	DC	DC *1

■ I²C Bus Conditions (continued)

OUT2 signal select

00/D3	00/D2	00/D1	00/D0	CV2/SY2 OUT2	SC2 OUT2
0	0	0	0	CV1 IN1	DC
0	0	0	1	CV2 IN2	DC
0	0	1	0	CV3 IN3	DC
0	0	1	1	CV4 IN4	SC4 IN4
0	1	0	0	SY4 IN4	SC4 IN4
0	1	0	1	SY4 + SC4 IN4 IN4	SC4 IN4
0	1	1	0	CV5 IN5	SC5 IN5
0	1	1	1	SY5 IN5	SC5 IN5
1	0	0	0	SY5 + SC5 IN5 IN5	SC5 IN5
1	0	0	1	CV6 IN6	SC6 IN6
1	0	1	0	SY6 IN6	SC6 IN6
1	0	1	1	SY6 + SC6 IN6 IN6	SC6 IN6
1	1	0	0	CV7 IN7	SC7 IN7
1	1	0	1	SY7 IN7	SC7 IN7
1	1	1	0	SY7 + SC7 IN7 IN7	SC7 IN7
1	1	1	1	DC	DC *1

■ I²C Bus Conditions (continued)

OUT3 signal select

01/D7	01/D6	01/D5	01/D4	CV3/SY3 OUT3	SC3 OUT
0	0	0	0	CV1 IN1	DC
0	0	0	1	CV2 IN2	DC
0	0	1	0	CV3 IN3	DC
0	0	1	1	CV4 IN4	SC4 IN4
0	1	0	0	SY4 IN4	SC4 IN4
0	1	0	1	SY4 + SC4 IN4 IN4	SC4 IN4
0	1	1	0	CV5 IN5	SC5 IN5
0	1	1	1	SY5 IN5	SC5 IN5
1	0	0	0	SY5 + SC5 IN5 IN5	SC5 IN5
1	0	0	1	CV6 IN6	SC6 IN6
1	0	1	0	SY6 IN6	SC6 IN6
1	0	1	1	SY6 + SC6 IN6 IN6	SC6 IN6
1	1	0	0	CV7 IN7	SC7 IN7
1	1	0	1	SY7 IN7	SC7 IN7
1	1	1	0	SY7 + SC7 IN7 IN7	SC7 IN7
1	1	1	1	DC	DC *1

■ I²C Bus Conditions (continued)

OUT4 signal select

01/D3	01/D2	01/D1	01/D0	G1/Y1 OUT4	B1/U1 OUT4	R1/V1 OUT4	HOUT1 OUT4	VOUT1 OUT4
0	0	0	0	CV1 IN1	DC	DC	indefinite	indefinite
0	0	0	1	CV2 IN2	DC	DC	indefinite	indefinite
0	0	1	0	CV3 IN3	DC	DC	indefinite	indefinite
0	0	1	1	Y7/CV4 IN4	U7/SY4 IN4	V7/SC4 IN4	indefinite	indefinite
0	1	0	0	Y6/CV5 IN5	U6/SY5 IN5	V6/SC5 IN5	Hin6 IN5	Vin6 IN5
0	1	0	1	Y5/CV6 IN6	U5/SY6 IN6	V5/SC6 IN6	Hin5 IN6	Vin5 IN6
0	1	1	0	Y4/CV7 IN7	U4/SY7 IN7	V4/SC7 IN7	Hin4 IN7	Vin4 IN7
0	1	1	1	G3/Y3 IN8	B3/U3 IN8	R3/V3 IN8	Hin3 IN8	Vin3 IN8
1	0	0	0	G2/Y2 IN9	B2/U2 IN9	R2/V2 IN9	Hin2 IN9	Vin2 IN9
1	0	0	1	G1/Y1 IN10	B1/U1 IN10	R1/V1 IN10	Hin1 IN10	Vin1 IN10
1	0	1	0	DC	DC	DC	indefinite	indefinite
1	0	1	1	DC	DC	DC	indefinite	indefinite
1	1	0	0	DC	DC	DC	indefinite	indefinite
1	1	0	1	DC	DC	DC	indefinite	indefinite
1	1	1	0	DC	DC	DC	indefinite	indefinite
1	1	1	1	DC	DC	DC *1	indefinite	indefinite

■ I²C Bus Conditions (continued)

OUT5 signal select

02/D3	02/D2	02/D1	012D0	G2/Y2 OUT5	B2/U2 OUT5	R2/V2 OUT5	HOUT2 OUT5	VOUT2 OUT5
0	0	0	0	CV1 IN1	DC	DC	*2	*2
0	0	0	1	CV2 IN2	DC	DC	*2	*2
0	0	1	0	CV3 IN3	DC	DC	*2	*2
0	0	1	1	Y7/CV4 IN4	U7/SY4 IN4	V7/SC4 IN4	*2	*2
0	1	0	0	Y6/CV5 IN5	U6/SY5 IN5	V6/SC5 IN5	*2	*2
0	1	0	1	Y5/CV6 IN6	U5/SY6 IN6	V5/SC6 IN6	*2	*2
0	1	1	0	Y4/CV7 IN7	U4/SY7 IN7	V4/SC7 IN7	*2	*2
0	1	1	1	G3/Y3 IN8	B3/U3 IN8	R3/V3 IN8	*2	*2
1	0	0	0	G2/Y2 IN9	B2/U2 IN9	R2/V2 IN9	*2	*2
1	0	0	1	G1/Y1 IN10	B1/U1 IN10	R1/V1 IN10	*2	*2
1	0	1	0	DC	DC	DC	*2	*2
1	0	1	1	DC	DC	DC	*2	*2
1	1	0	0	DC	DC	DC	*2	*2
1	1	0	1	DC	DC	DC	*2	*2
1	1	1	0	DC	DC	DC	*2	*2
1	1	1	1	DC	DC	DC *1	*2	*2

Note) *1 : 3.5 Vdc are outputted at the time of mute mode
*2 : It is based on a setup of sync distinction

■ I²C Bus Conditions (continued)

- The AN15865A selects slave address 85 or 8D(hex) according to the status of the SLVADR pin.
  Address 85(hex) will be selected with the SLVADR pin grounded the the GND side. Address 8D(hex) will be selected with the pin grounded to the 5-V line.

Status register

S	Slave Address (85 or 8D)	AM	DATA (X)	AM	DATA (X + 1)	AM	DATA (X + 2)	continue

Note) AM = Ack from Master

R/W = 1

	D7	D6	D5	D4	D3	D2	D1	D0
DATA0	Aspect ratio SA3	00 : 4:3 video signal 01 : 4:3 letter-box 10 : 16:9 video signal 11 : No use	Aspect ratio SA4	00 : 4:3 video signal 01 : 4:3 letter-box 10 : 16:9 video signal 11 : No use	Aspect ratio SA5	00 : 4:3 video signal 01 : 4:3 letter-box 10 : 16:9 video signal 11 : No use	Aspect ratio SA6	00 : 4:3 video signal 01 : 4:3 letter-box 10 : 16:9 video signal 11 : No use
DATA1	Pin detect SB3 0 : Open 1 : connect	Pin detect SB4 0 : Open 1 : connect	Pin detect SB5 0 : Open 1 : connect	Pin detect SB6 0 : Open 1 : connect	AFC-LOCK 0 : unlock 1 : lock	OUT5 System status	000 : 480i / 60 001 : 480p / 60 010 : 1 080i / 60 011 : 720p / 60	100 : 576i / 50 101 : 576p / 50 110 : 1 080i / 50 111 : 720p / 50
DATA2	Sync status 0 : 2 value 1 : 3 value	MACRO VISION detection (OUT5) 0 : normal signal 1 : macro vision signal	auto distinc. Result CVSYdet 0 : SY 1 : CV	auto distinc. Result sync fix 0 : continue 1 : fix	Australia interlace 0 : except Australia 1 : Australia	Australia format 0 : 1 152i 1 : 1 152i(letter)	Signal detect 0 : no signal 1 : signal input	0

Note) The default data at the time of power-on is 0.

■ I²C Bus Conditions (continued)

Description of Registers

1. Control Register

Out1 signal select : Selects the Input IN1 to IN7 for OUT1(CV1, SY1, SC1)
(Including Mute mode)

Out2 signal select : Selects the Input IN1 to IN7 for OUT2(CV2, SY2, SC2)
(Including Mute mode)

Out3 signal select : Selects the Input IN1 to IN7 for OUT3(CV3, SY3, SC3)
(Including Mute mode)

Out4 signal select : Selects the Input IN1 to IN10 for OUT4(G1/Y1, B1/U1, R1/V1, Hout1, Vout1)

Out5 Sync distinction : Switches the sync identification AFC circuit operating mode
0 = Automatic identification (with priority ranking)
(If input signal to both CV and SY, SY signal will be selected)
1 = Uses CV or Y input
2 = Uses SY input
3 = Free-run

Free-run priority : The priority of a free-run is changed
0 = Fixed mode
1 = Auto distinction will be started if a signal is inputted into a Sync block
While input signal is removed, return to free-run mode.
(Free-run priority only enabled when Out5 sync distinction = free-run)

Out5 Sync : Selects H, V signal of Hout2, Vout2 whether independent H and V or AFC H and V
0 = AFC H and V
1 = independent H and V

Out5 signal select : Selects the Input IN1 to IN10 for OUT5(G2/Y2, B2/U2, R2/V2, Hout2, Vout2)

Out4 matrix : Selects the type of matrix conversion of Out4
0 = Through
1 = CCIR protocol
2 = BTA protocol
3 = Convert GBR to YUV

Out5 matrix : Selects the type of matrix conversion of Out5
0 = Through
1 = CCIR protocol
2 = BTA protocol
3 = Convert GBR to YUV

Dummy sync mode control : Selects the type of output sync format of Out5
0 = 480i / 60
1 = 480p / 60
2 = 1080i / 60
3 = 720p / 60
4 = 576i / 50
5 = 576p / 50
6 = 1 080i / 50
7 = 720p / 50

HVout2 polarity : Select the polarity of HOUT2 and VOUT2 at AFC mode
0 = positive, Sync level is high
1 = Negative, Sync level is low

■ I²C Bus Conditions (continued)

CV1 GAIN : Select the gain of OUT1(CV1)
0 = 0 dB
1 = 6 dB

SY1/SC1 GAIN : Select the gain of OUT1(SY1, SC1)
0 = 0 dB
1 = 6 dB

CV2 GAIN : Select the gain of OUT2(CV2)
0 = 0 dB
1 = 6 dB

SY2/SC2 GAIN : Select the gain of OUT2(SY2, SC2)
0 = 0 dB
1 = 6 dB

CV3 GAIN : Select the gain of OUT3(CV3)
0 = 0 dB
1 = 6 dB

SY3/SC3 GAIN : Select the gain of OUT3(SY3, SC3)
0 = 0 dB
1 = 6 dB

OUT4 GAIN : Select the gain of OUT4(G1/Y1, B1/U1, R1/V1)
0 = 0 dB
1 = 6 dB

OUT5 GAIN : Select the gain of OUT5(G2/Y2, B2/U2, R2/V2)
0 = 0 dB
1 = 6 dB

OUT1 LPF : This switch selects LPF on/off of OUT1
0 = Through
1 = LPF ON

OUT2 LPF : This switch selects LPF on/off of OUT2
0 = Through
1 = LPF ON

OUT3 LPF : This switch selects LPF on/off of OUT3
0 = Through
1 = LPF ON

OUT4 LPF : This switch selects LPF on/off of OUT4
0 = Through
1 = LPF ON

OUT5 LPF : This switch selects LPF on/off of OUT5
0 = Through
1 = LPF ON

OUT1 DCOUT : Selects the DC level to OUT1(SC1) . This DC level corresponds to S2 standard.
0 = 0 V
1 = 1.9 V
2 = indefinite
3 = 4.5 V

Field monitor select : Selects the field distinction signal in interlace mode, or the oscillation clock of built-in VCO
0 = Field1/Field2 out (Field1 : Low Field2 : High)
1 = clock monitor out

INPUT4 U/SY select : The mode changeover switch of an incoming signal
0 : SY input select
1 : U input select

■ I²C Bus Conditions (continued)

INPUT5 U/SY select : The mode changeover switch of an incoming signal
0 : SY input select
1 : U input select

INPUT6 U/SY select : The mode changeover switch of an incoming signal
0 : SY input select
1 : U input select

INPUT7 U/SY select : The mode changeover switch of an incoming signal
0 : SY input select
1 : U input select

INPUT8 BR/UV select : The mode changeover switch of an incoming signal
0 : BR input select
1 : UV input select

INPUT9 BR/UV select : The mode changeover switch of an incoming signal
0 : BR input select
1 : UV input select

INPUT10 BR/UV select : The mode changeover switch of an incoming signal
0 : BR input select
1 : UV input select

Australia free-run : Set up, when you oscillate the free-run of the Australia signal
0 = except Australia
1 = Australia mode

2. Status Register

Scart Ident SA3 : Return the control voltage of SA3(Pin 51)
0 = less than 1 V
1 = 2 V or more to less than 3 V
2 = 4 V or more
3 = indefinite

Scart Ident SA4 : Return the control voltage of SA4(Pin 55)
0 = less than 1V
1 = 2 V or more to less than 3 V
2 = 4 V or more
3 = indefinite

Scart Ident SA5 : Return the control voltage of SA5(Pin 47)
0 = less than 1V
1 = 2 V or more to less than 3 V
2 = 4 V or more
3 = indefinite

Scart Ident SA6 : Return the control voltage of SA6(Pin 59)
0 = less than 1V
1 = 2 V or more to less than 3 V
2 = 4 V or more
3 = indefinite

Pin detect SB3 : Return the control voltage of SB3(Pin 53)
0 = 5 V(Open)
1 = 0 V(Connected)

Pin detect SB4 : Return the control voltage of SB4(Pin 57)
0 = 5 V(Open)
1 = 0 V(Connected)

■ I²C Bus Conditions (continued)

Pin detect SB5 : Return the control voltage of SB5(Pin 45)
0 = 5 V(Open)
1 = 0 V(Connected)

Pin detect SB6 : Return the control voltage of SB6(Pin 61)
0 = 5 V(Open)
1 = 0 V(Connected)

AFC-LOCK : Indicate the AFC lock status in the sync separation
0 = unlocked
1 = locked

OUT5 System status : Return the input signal format after sync separated
0 = 480i / 60 4 = 576i / 50
1 = 480p / 60 5 = 576p / 50
2 = 1080i / 60 6 = 1080i / 50
3 = 720p / 60 7 = 720p / 50

Sync status : Return of identifying whether the input is ternary sync
0 = Binary sync
1 = Tri-level sync

MACRO VISION : Indicate the whether to be a macro vision signal
0 = normal signal
1 = macro vision signal

Auto Distinction Result of CV/SY detection :
The detection result is indicated on which Sync shall have ridden between "CV" or "SY"
0 = SY
1 = CV

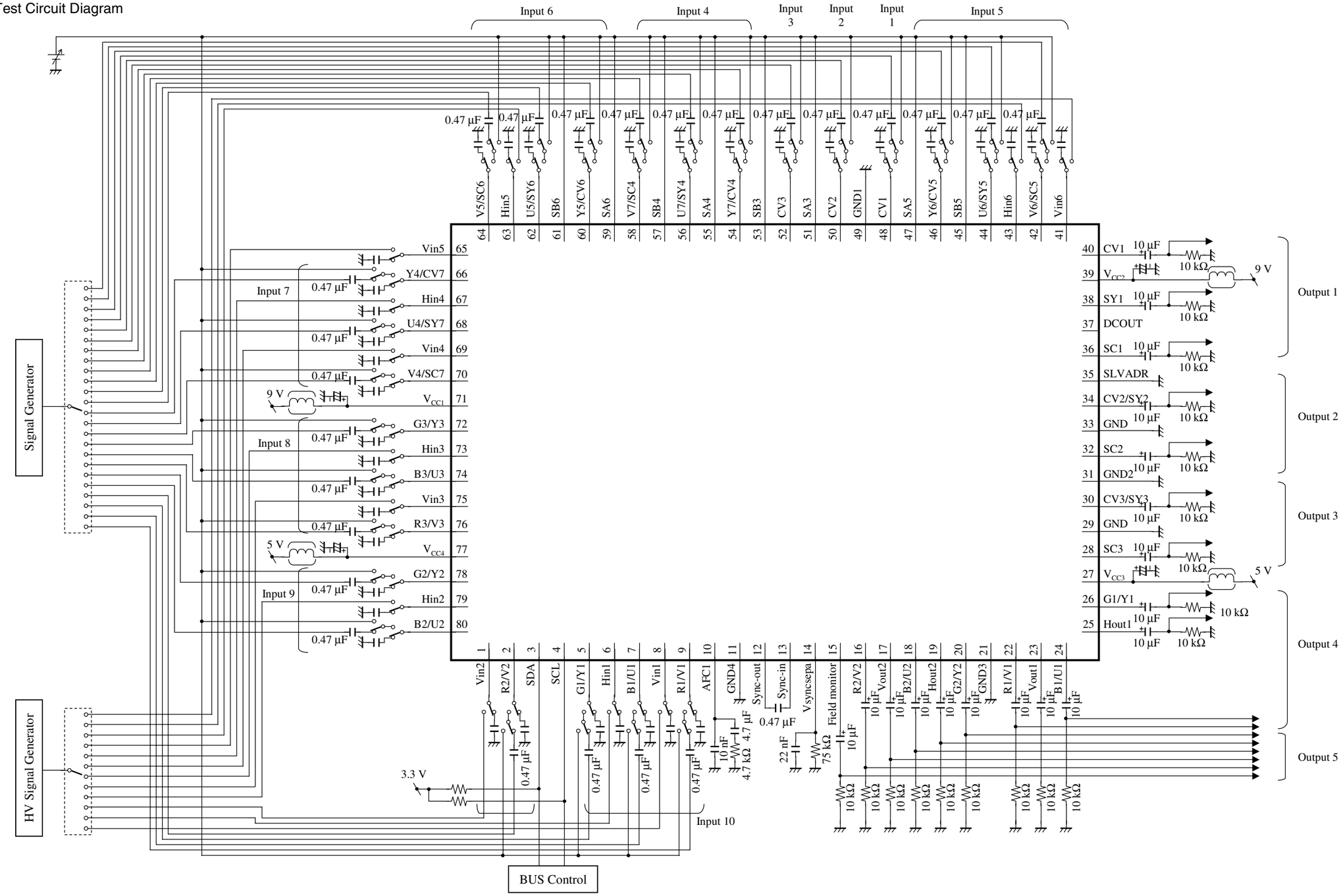
Auto Distinction Result of Sync fixing situation :
It indicates whether the detection result of Auto distinction fixed
0 = Under the check
1 = fixed

Australia interlace : It indicates whether the input signal is Australia format
0 = except Australia
1 = Australia

Australia format : It indicates the type of Australia format
0 = 1152i
1 = 1152i(litter)

Signal detect : It indicates whether there is input signal
0 = no signal
1 = Signal input

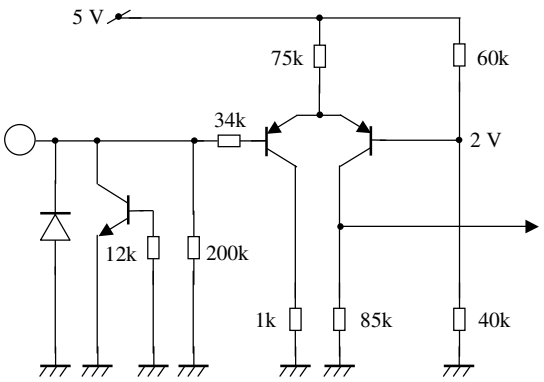
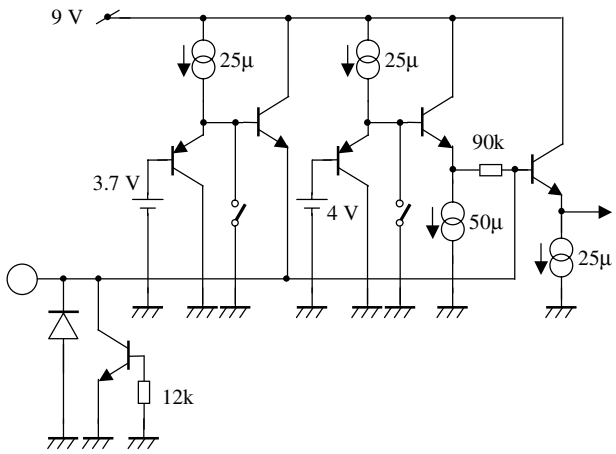
■ Test Circuit Diagram



■ Technical Data

1. Circuit diagrams of the input/output part and pin function descriptions

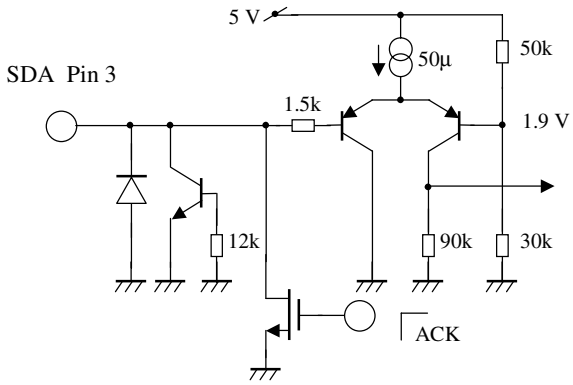
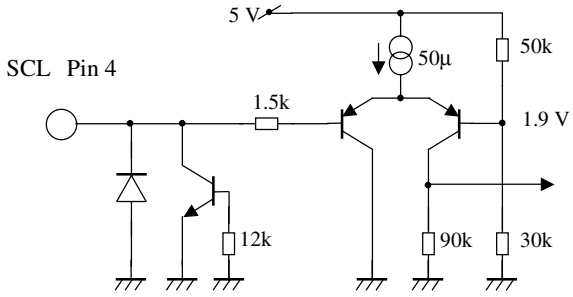
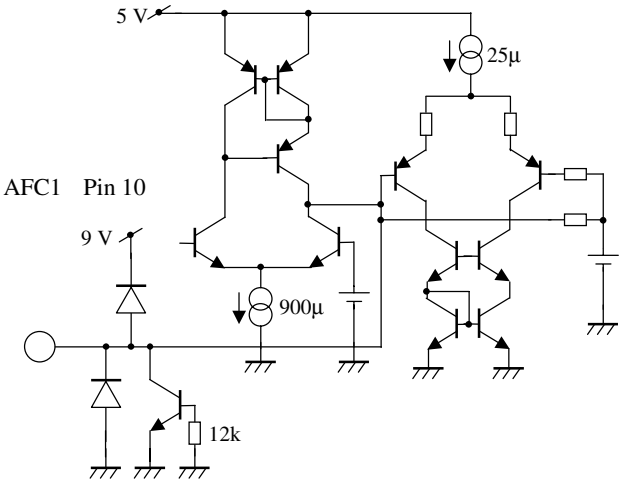
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Inner circuit	Description
1 6 8 41 43 63 65 67 69 73 75 79	V_{IN} Pin 1, 8, 41, 65, 69, 75 H_{IN} Pin 6, 43, 63, 67, 73, 79  	Independent H, V signal input pins.
2 5 7 9 44 46 48 50 52 54 56 60 62 66 68 72 74 76 78 80	G/Y Pin 5, 72, 78 B/U Pin 7, 74, 80 R/Y Pin 2, 9, 76 U/SY Pin 44, 56, 62, 68 Y/CV Pin 46, 48, 50, 52, 54, 60, 66  	G/Y, B/U, R/V, U/SY, Y/CV signal input pins.

■ Technical Data (continued)

1. Circuit diagrams of the input/output part and pin function descriptions

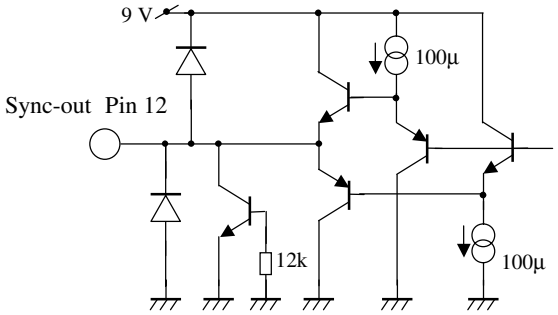
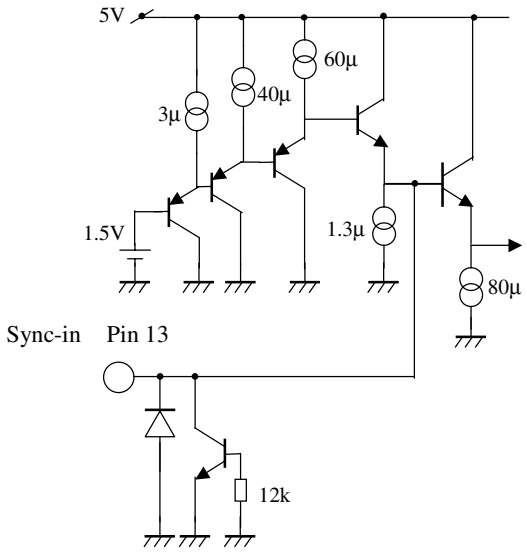
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Inner circuit	Description
3		I^2C bus data input pin.
4		I^2C bus clock input pin.
10		AFC filter pin.

■ Technical Data (continued)

1. Circuit diagrams of the input/output part and pin function descriptions (continued)

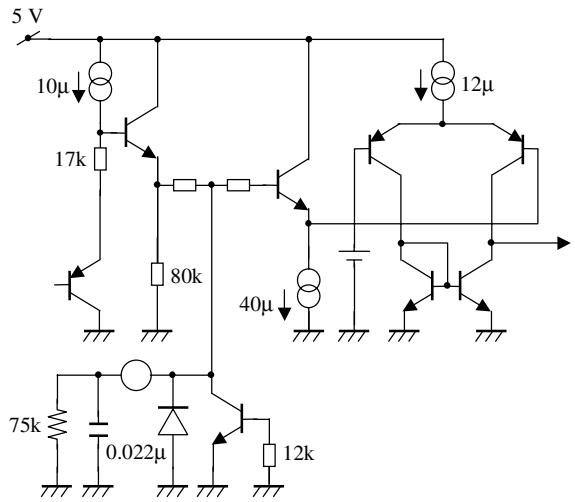
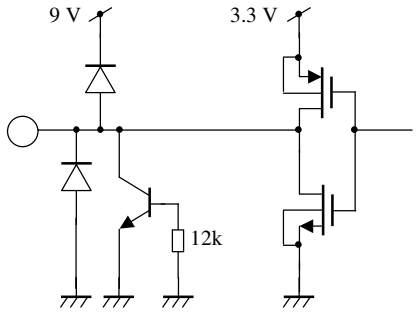
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Inner circuit	Description
11	GND4 Pin 11	5V system ground pin.
12		Sync signal output pin for sync separation.
13		Sync signal input pin for sync separation.

■ Technical Data (continued)

1. Circuit diagrams of the input/output part and pin function descriptions (continued)

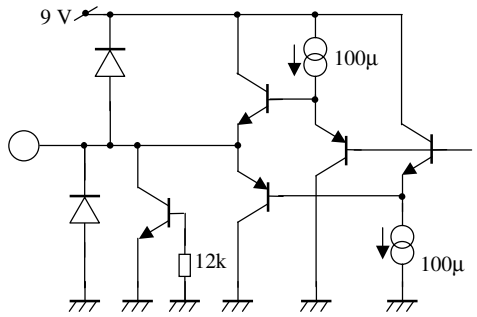
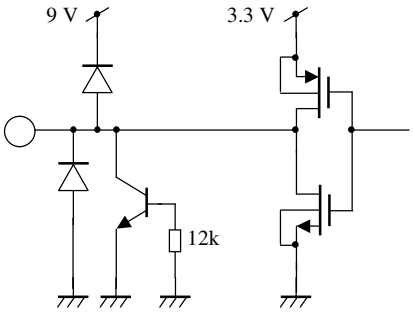
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Inner circuit	Description
14	V sync sepa Pin 14 	V sync separation filter pin.
15	Field monitor Pin 15 	Field change signal output pin.

■ Technical Data (continued)

1. Circuit diagrams of the input/output part and pin function descriptions (continued)

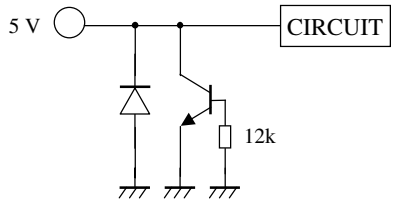
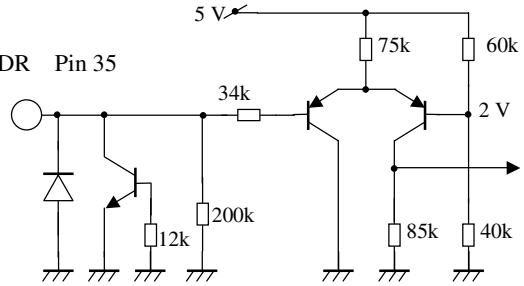
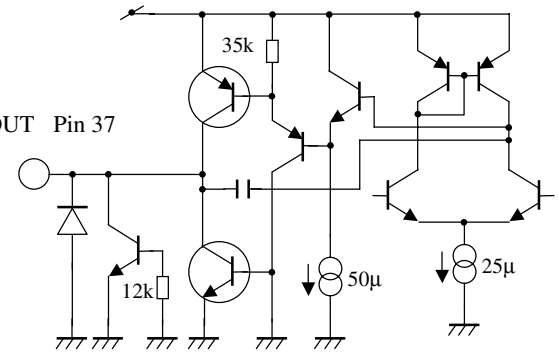
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Inner circuit	Description
16 18 20 22 24 26 28 30 32 34 36 38 40	G/Y Pin 20, 26 B/U Pin 18, 24 R/V Pin 16, 22 CV/SY Pin 30, 34, 38, 40 SC Pin 28, 32, 36 	G/Y, B/U, R/V, CV/SY, SC signal output pins.
17 19	Vout Pin 17, 23 Hout Pin 19, 25 	AFC or independent H, V signal output pins.
23 25		Independent H, V signal output pins
21	GND3 Pin 21	5 V system ground pin.

■ Technical Data (continued)

1. Circuit diagrams of the input/output part and pin function descriptions (continued)

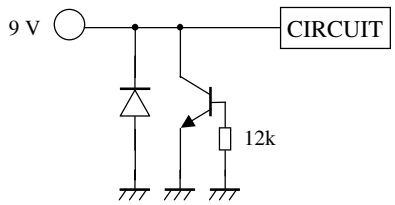
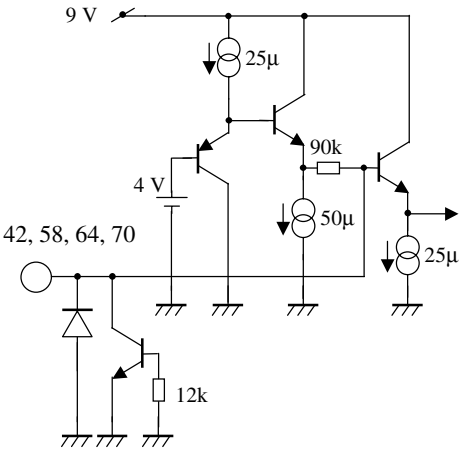
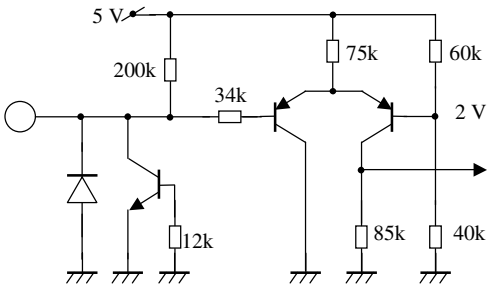
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

<table>
<tr><th>Pin No.</th><th>Inner circuit</th><th>Description</th></tr>
<tr><td>27</td><td>VCC3 Pin 27
 
</td><td>5 V system power supply pin.
• Apply 5 V.</td></tr>
<tr><td>29</td><td>GND Pin 29</td><td></td></tr>
<tr><td>31</td><td>GND2 Pin 31</td><td>9 V system ground pin.</td></tr>
<tr><td>33</td><td>GND Pin 33</td><td></td></tr>
<tr><td>35</td><td>SLVADR Pin 35
 
</td><td></td></tr>
<tr><td>37</td><td>DCOUT Pin 37
 
</td><td>Pin to output DC voltage corresponding to S2, which overlaps the SC1 signal on Output 1. The DC voltage varies with the setting in the control register.
<table><tr><th>05/D2</th><th>05/D1</th><th>DC value</th></tr><tr><td>0</td><td>0</td><td>0 V</td></tr><tr><td>0</td><td>1</td><td>1.9 V</td></tr><tr><td>1</td><td>0</td><td>indefinite</td></tr><tr><td>1</td><td>1</td><td>4.5 V</td></tr></table></td></tr>
</table>

■ Technical Data (continued)

1. Circuit diagrams of the input/output part and pin function descriptions (continued)

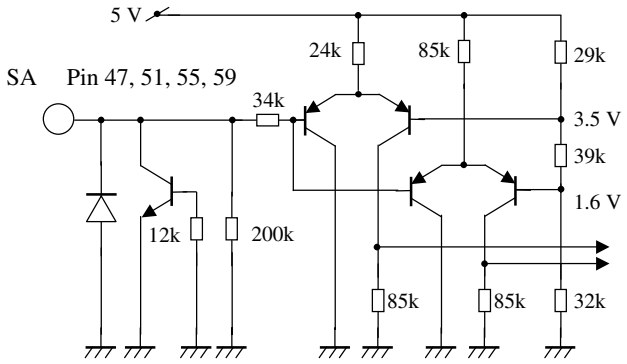
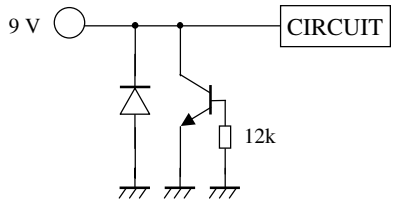
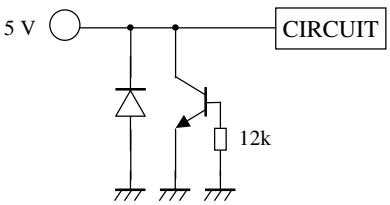
Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

Pin No.	Inner circuit	Description
39	VCC2 Pin 39 	9 V system power supply pin. • Apply 9 V.
42 58 64 70	V/SC Pin 42, 58, 64, 70 	V/SC signal input pins.
45 53 57 61	SB Pin 45, 53, 57, 61 	Pin status detection pins. Pin opened : No signal. Pin shorted : With signal. Status data is transferred to the microcomputer in serial.

■ Technical Data (continued)

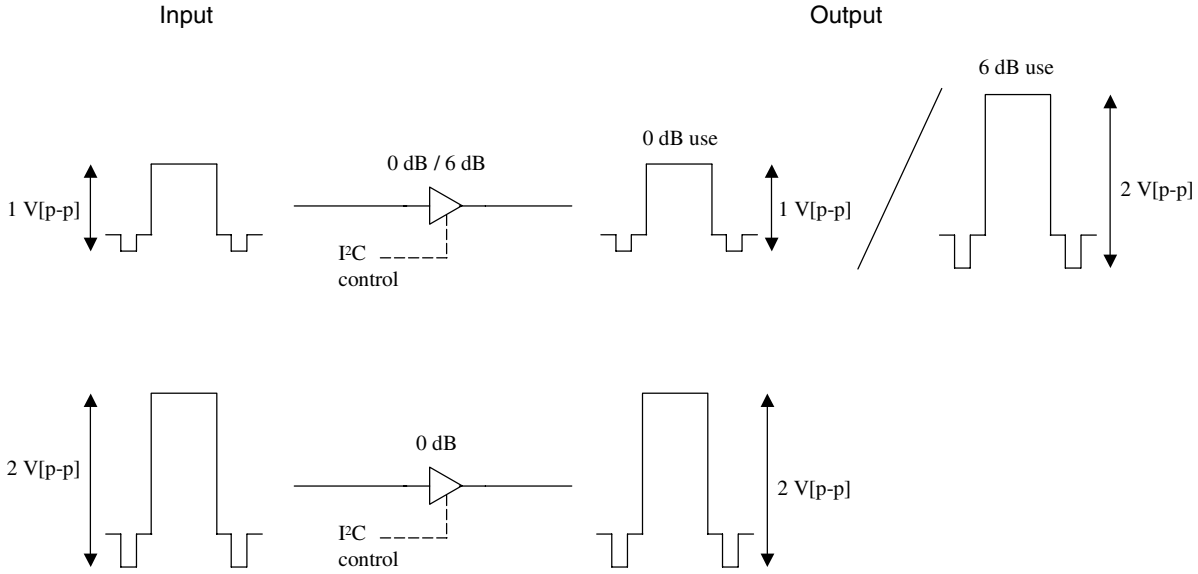
1. Circuit diagrams of the input/output part and pin function descriptions (continued)

Note) The characteristics listed below are reference values based on the IC design and are not guaranteed.

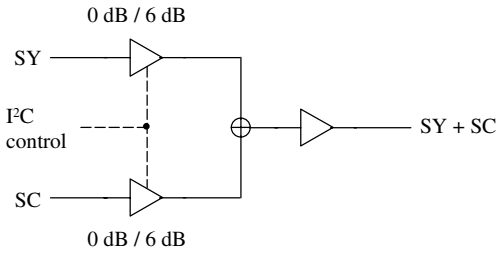
<table>
<tr><th>Pin No.</th><th>Inner circuit</th><th>Description</th></tr>
<tr><td>47
51
55
59</td><td>SA Pin 47, 51, 55, 59
 
</td><td>Aspect ratio detection pins.
<table>
<tr><th>Pin voltage</th><th>Aspect ratio</th></tr>
<tr><td>5.0 V to 4.0 V</td><td>16 : 9</td></tr>
<tr><td>3.0 V to 1.7 V</td><td>Letter-box</td></tr>
<tr><td>1.0 V to 0 V</td><td>4 : 3</td></tr>
</table></td></tr>
<tr><td>49</td><td>GND1 Pin 49</td><td>5 V system ground pin.</td></tr>
<tr><td>71</td><td>VCC1 Pin 71
 
</td><td>9 V system power supply pin.
• Apply 9 V.</td></tr>
<tr><td>77</td><td>VCC4 Pin 77
 
</td><td>5 V system power supply pin.
• Apply 5 V.</td></tr>
</table>

■ Technical Data (continued)

2. Notes on video gain



For 1 V[p-p] input signal, both 0 dB and 6 dB gain can be enabled. However, for 2 V[p-p] input signal, only 0 dB gain is allowed for normal operation.



The gain of SY + SC can be controlled by Control Register SY/SC GAIN.

SY/SC GAIN = 0 SY + SC = –6 dB

SY/SC GAIN = 1 SY + SC = 0 dB

please note that the gain of SY + SC is not controlled by Control Resister CV GAIN.

3. Other supplementary matters

- The remedy of APL change
  please attach resistance of 1 MΩ - 3 MΩ to each pin of CV and SY between opposite GND by carrying out that it is hard to receive APL change.
- How to output a synchronous separation output to Hout2 to Vout2
  Please choose "1" by test76(07/D6) and out5 sync(02/D4) in a control register, respectively.

■ Usage Notes

1. For use, voltages above 5.5 V should not be applied to the following pins.
   (Pin No. 15, 17, 19, 23, 25)

2. Pay enough attention to that following items when using the IC, otherwise the IC may break or give off smoke.
   - Do not insert the IC in the reverse direction.

3. Keep in mind the it may cause a latch-up by the following pins in the examination of the method of pulse current.

Pin number	Merit level (mA)
46	–100
47	–90
52	–80
53	–70
62	–80

   Be careful not to impress the pulse current more than the above.
   The current level is describing the merit value of the pulse current which a latch-up does not generate.
   However, in all pins, a latch-up is not caused by the examination of the CV method. (200pF 200V)

4. Purchase of Panasonic I^2C Components conveys a license under the Philips I^2C patent right to use these components in an I^2C systems, provided that the system conforms to the I^2C standard specifications as defined by Philips.

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(2) The technical information described in this material is limited to showing representative characteristics and applied circuits examples of the products. It neither warrants non-infringement of intellectual property right or any other rights owned by our company or a third party, nor grants any license.

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Even when the products are used within the guaranteed values, take into the consideration of incidence of break down and failure mode, possible to occur to semiconductor products. Measures on the systems such as redundant design, arresting the spread of fire or preventing glitch are recommended in order to prevent physical injury, fire, social damages, for example, by using the products.

(7) When using products for which damp-proof packing is required, observe the conditions (including shelf life and amount of time let standing of unsealed items) agreed upon when specification sheets are individually exchanged.