TA0102A

STEREO 150W (4Ω) CLASS-T DIGITAL AUDIO AMPLIFIER DRIVER USING DIGITAL POWER PROCESSING (DPP™) TECHNOLOGY

Technical Information **Revision 3.1 – June 2000**

GENERAL DESCRIPTION

The TA0102A is a 150W continuous average (4Ω), two channel Amplifier Driver Module which uses Tripath's proprietary Digital Power Processing (DPP™) technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

Applications

- Audio/Video
- Amplifiers/Receivers
- Pro-audio Amplifiers
- Automobile Power Amplifiers
- Subwoofer Amplifiers

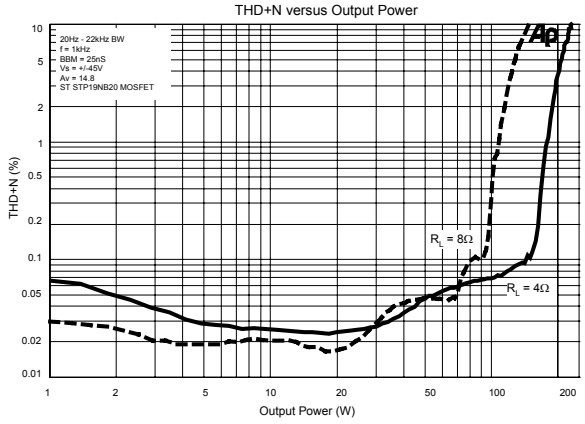
Benefits

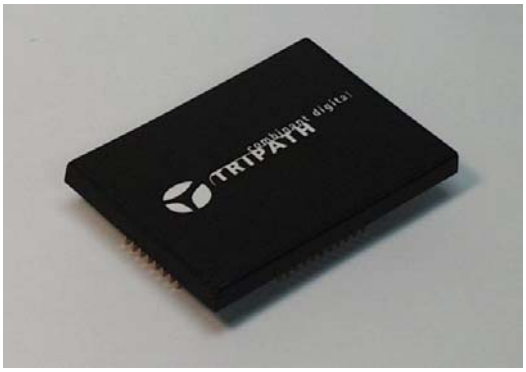
- Reduced system cost with smaller/less expensive power supply and heat sink
- Signal fidelity equal to high quality Class-AB amplifiers
- High dynamic range compatible with digital media such as CD and DVD

Features

- Class-T architecture
- Proprietary Digital Power Processing technology
- Supports wide range of output power levels
- "Audiophile" Quality Sound
  - 0.05% THD+N @ 20W, 8Ω
  - 0.03% IHF-IM @ 30W, 8Ω
  - 80W @ 8Ω, 0.1% THD+N, V_S = +/-45V
  - 150W @ 4Ω, 0.1% THD+N, V_S = +/-45V
- High Power
  - 100W @ 8Ω, 1% THD+N, V_S = +/-45V
  - 170W @ 4Ω, 1% THD+N, V_S = +/-45V
- High Efficiency
  - 90% @ 85W @ 8Ω, V_S = +/-33.75V
  - 88% @ 155W @ 4Ω, V_S = +/-33.75V
- Dynamic Range = 108 dB
- Requires only N-Channel MOSFET output transistors
- High power supply rejection ratio
- Mute input
- Outputs short circuit protected
- Over- and under-voltage protection
- Bridgeable, single-ended outputs
- 38-pin quad package
  Supports 100kHz BW of Super Audio CD and DVD-Audio (refer to Application Note for specifics)

Typical Performance





Absolute Maximum Ratings

SYMBOL	PARAMETER	VALUE	UNITS
V_S	Supply Voltage (V_{SPOS} & V_{SNEG})	+/-70	V
V5	Positive 5V Bias Supply	6	V
VN12	Supply Voltage: Nominal +12V referenced to V_{SNEG}	18	V
T_{STORE}	Storage Temperature Range	-40 to 150	°C
T_A	Operating Free-air Temperature Range	-20 to +80	°C

Notes: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Damage will occur to the device if VN12 is not supplied or falls below the recommended operating voltage when V_S is within its recommended operating range.

Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS
V_S	Supply Voltage (V_{spos} & V_{sneg})	+/-28		+/-49	V
V5	Positive 5V Bias Supply	4.5	5	5.5	V
VN12	Supply Voltage: Nominal +12V referenced to V_{SNEG}	10.8	12	13.2	V

Note: Operating Conditions indicate conditions for which the device is functional. See Electrical Characteristics for guaranteed specific performance limits.

Electrical Characteristics

Unless otherwise specified, T_A = 25°C. See Notes 1 & 2 for Operating Conditions and Test/Application Circuit Setup.

SYMBOL	PARAMETER		MIN.	TYP.	MAX.	UNITS
I_q	Quiescent Current	+33.75V		25	75	mA
	(no load, BBM0=BBM1=0)	-33.75V		30	50	mA
		+5V		45	65	mA
		VN12		110	160	mA
I_S	Source Current @ P_{OUT} = 150W, 4Ω	+33.75V		5.1		A
		-33.75V		5.2		A
I5	Source Current for 5V Bias Supply @ P_{OUT} = 150W, R_L = 4Ω			42		mA
IVN12	Source Current for VN12 Supply @ P_{OUT} = 150W, R_L = 4Ω			46		mA
V_U	Under Voltage (V_{spos} & V_{sneg})				+/-28	V
V_O	Over Voltage (V_{spos} & V_{sneg})		+/-49			V
V_{IH} - MUTE	High-level Input Voltage (MUTE)		3.5			V
V_{IL} - MUTE	Low-level Input Voltage (MUTE)				1	V
I_{DD}MUTE	Mute Supply Current	+33.75V		0.315	2	mA
	(no load, 145nS delay)	-33.75V		4	5	mA
		+5V		18	25	mA
		VN12		0.475	2	mA
V_{OH}	High-level Output Voltage (HMUTE & OVERLOADB)		3.5			V
V_{OL}	Low-level Output Voltage (HMUTE & OVERLOADB)				1	V
V_{TOC}	Over Current Sense Voltage Threshold		0.63	0.70	0.77	V
A_V	Gain Ratio V_O/V_I, R_{IN} = 0Ω			77		V/V
Voffset	Offset Voltage, no load, MUTE = Logic low (before nulling)				500	mV

Minimum and maximum limits are guaranteed but may not be 100% tested.

Performance Characteristics – Single Ended, Vs = ±45V

Unless otherwise specified, f = 1kHz, Measurement Bandwidth = 22kHz. T_A = 25°C.
See Notes 1 & 2 for Operating Conditions and Test/Application Circuit Setup.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (Continuous Average/Channel)	THD+N = 0.1%	R_L = 8Ω		80		W
			R_L = 4Ω		130		W
		THD+N = 1%	R_L = 8Ω		100		W
			R_L = 4Ω		170		W
THD + N	Total Harmonic Distortion Plus Noise	P_O = 20W/Channel, R_L = 8Ω			0.05		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 4Ω P_{OUT} = 30W/Channel			0.05		%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 88W/Ch, R_L = 8Ω			98.5		dB
CS	Channel Separation	0dBr = 30W, R_L = 8Ω			85		dB
PSRR	Power Supply Rejection Ratio	f = 120Hz, Vripple = 100 mV			67		dB
η	Power Efficiency	P_{OUT} = 230W/Channel, R_L = 4Ω			82		%
e_{NOUT}	Output Noise Voltage	A-Weighted, no signal, input shorted, DC offset nulled to zero			300		μV

Performance Characteristics – Single Ended, Vs = ±33.75V

Unless otherwise specified, f = 1kHz, Measurement Bandwidth = 22kHz. T_A = 25°C.
See Notes 1 & 2 for Operating Conditions and Test/Application Circuit Setup.

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNITS
P_{OUT}	Output Power (Continuous Average/Channel)	THD+N = 0.1%	R_L = 8Ω		47		W
			R_L = 4Ω		77		W
		THD+N = 1%	R_L = 8Ω		65		W
			R_L = 4Ω		110		W
THD + N	Total Harmonic Distortion Plus Noise	P_O = 20W/Channel, R_L = 8Ω			0.05		%
IHF-IM	IHF Intermodulation Distortion	19kHz, 20kHz, 1:1 (IHF), R_L = 4Ω P_{OUT} = 30W/Channel			0.03		%
SNR	Signal-to-Noise Ratio	A-Weighted, P_{OUT} = 47W/Ch, R_L = 8Ω			100		dB
CS	Channel Separation	0dBr = 20W, R_L = 8Ω			85		dB
PSRR	Power Supply Rejection Ratio	f = 120Hz, Vripple = 100 mV			67		dB
η	Power Efficiency	P_{OUT} = 85W/Channel, R_L = 8Ω			90		%
e_{NOUT}	Output Noise Voltage	A-Weighted, no signal, input shorted, DC offset nulled to zero			195		μV

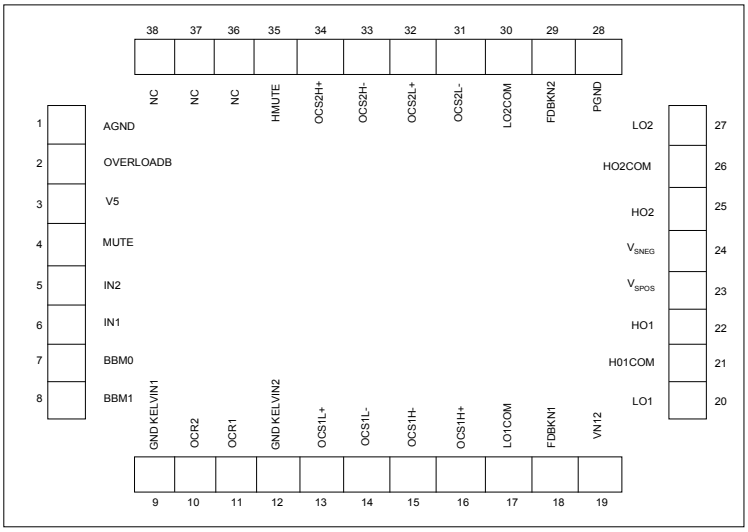
Minimum and maximum limits are guaranteed but may not be 100% tested.

Notes:

1. V5 = +5V, VN12 = +12V referenced to V_{SNEG}
2. Test/Application Circuit Values: D = MUR120T3 diodes, R_{IN} = 22.1KΩ
   R_D = 33Ω, R_S = 0.025Ω, R_G = 30Ω
   R_{OCR1} = R_{OCR2} = 0Ω, L_F = 18uH (Amidon core T200-2)
   C_F = 0.22uF, C_D = 0.1uF, C_{IN} = 1uF, C_{BY} = 0.1uF
   Power Output MOSFET, M = ST STP19NB20
   BBM0 =BBM1 = 1

Pin Description

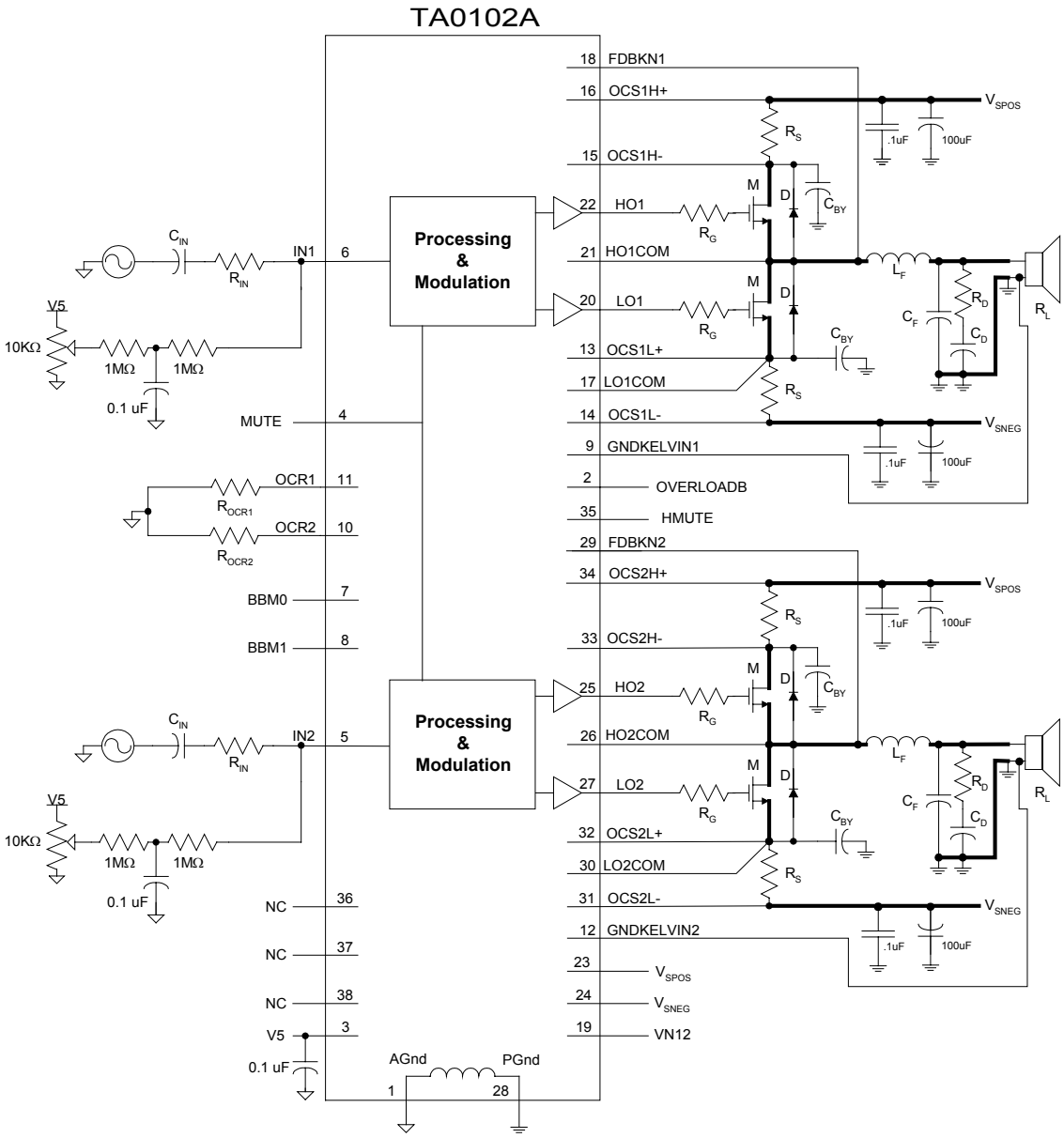
Pin	Function	Description
1	AGND	Analog Ground
2	OVERLOADB	Logic output. When low, indicates that the level of the input signal has overloaded the amplifier.
3	V5	Positive 5 Volts
4	MUTE	Logic input. When high, both amplifiers are muted. When low (grounded), both amplifiers are fully operational.
5, 6	IN2, IN1	Single-ended input (Channel 1 & 2)
7, 8	BBM0, BBM1	Break-before-make timing control
9, 12	GNDKELVIN1, GNDKELVIN2	Kelvin connection to speaker ground (Channel 1 & 2)
10, 11	OCR2, OCR1	Over-current threshold adjustment (Channel 1 & 2)
13, 14	OCS1L+, OCS1L-	Over Current Sense resistor, Channel 1 low-side
15, 16	OCS1H-, OCS1H+	Over Current Sense resistor, Channel 1 high-side
17, 30	LO1COM, LO2COM	Kelvin connection to source of low-side transistor (Channel 1 & 2)
18, 29	FDBKN1;FDBKN2	Feedback (Channel 1 & 2)
19	VN12	Voltage: +12 V from V_{SNEG}. Refer to Application Information section.
20, 27	LO1, LO2	Low side gate drive output (Channel 1 & 2)
21, 26	HO1COM, HO2COM	Kelvin connection to source of high-side transistor (Channel 1 & 2)
22, 25	HO1, HO2	High side gate drive output (Channel 1 & 2)
23	V_{SPOS}	Positive supply voltage
24	V_{SNEG}	Negative supply voltage
28	PGND	Power Ground
31, 32	OCS2L-, OCS2L+	Over Current Sense resistor, Channel 2 low-side
33, 34	OCS2H-, OCS2H+	Over Current Sense resistor, Channel 2 high-side
35	HMUTE	Logic output. When high, indicates that the output stages of both amplifiers are shut off and muted.
36, 37, 38	NC	Not Connected - Must Be Left Floating



38 PIN QUAD MODULE PIN OUT **TOP VIEW**

FIGURE 1

TEST/APPLICATION CIRCUIT



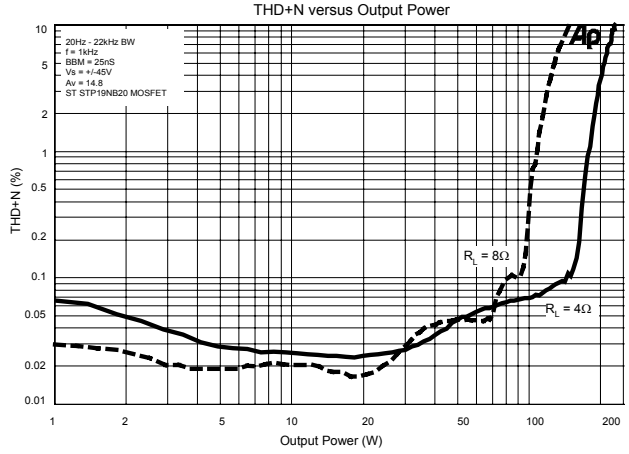
NC - Not Connected (Must Be Left Floating)

Note - Heavy Lines Indicate High-Current Paths

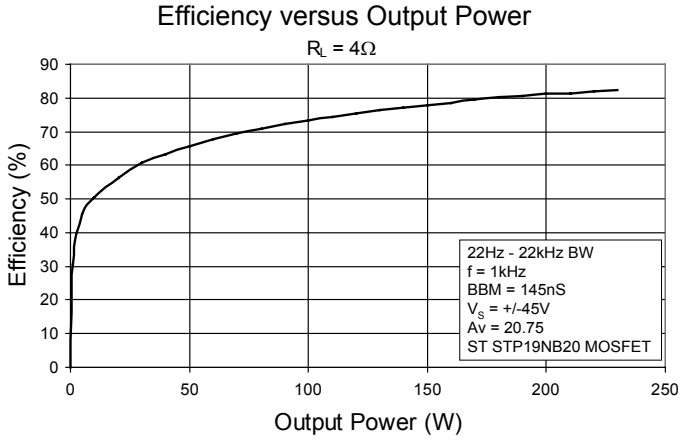
Figure 2

Typical Performance at Vs = +45V

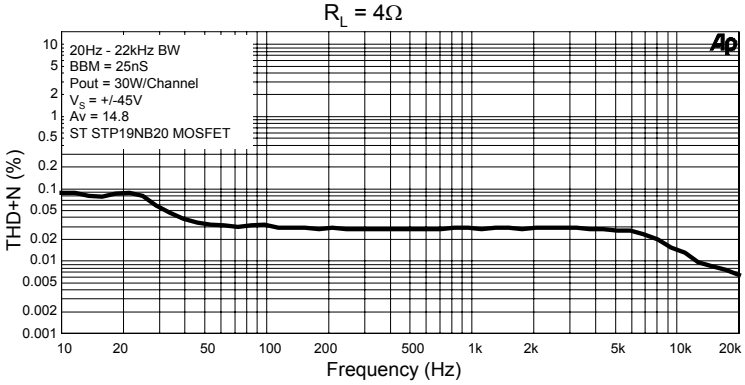
THD+N versus Output Power



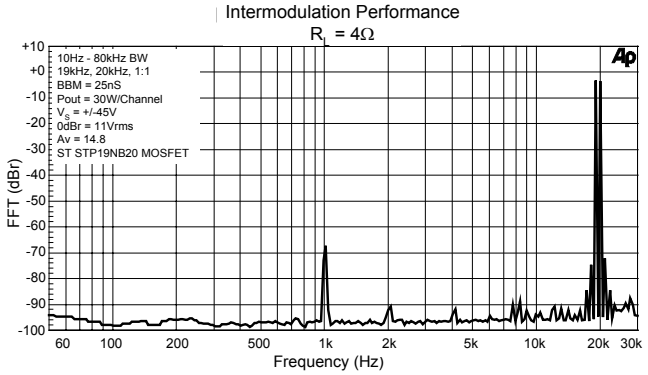
Efficiency versus Output Power



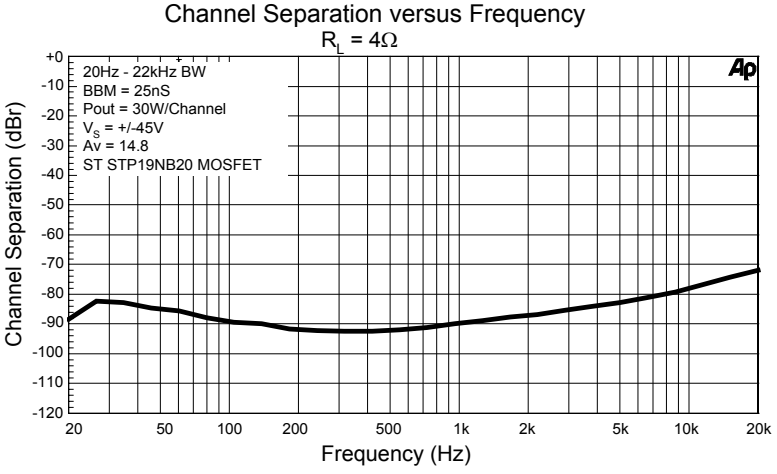
THD+N versus Frequency



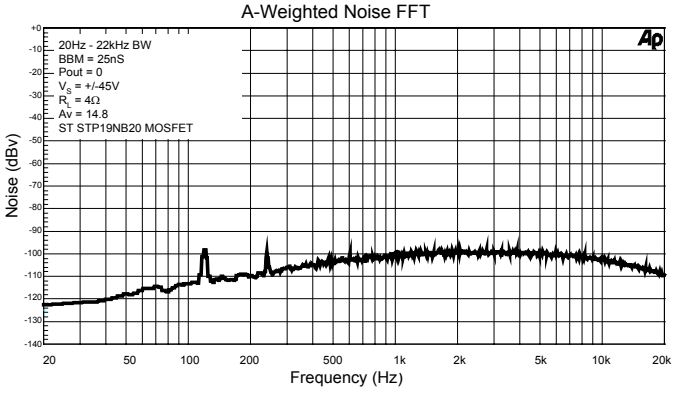
Intermodulation Performance



Channel Separation versus Frequency

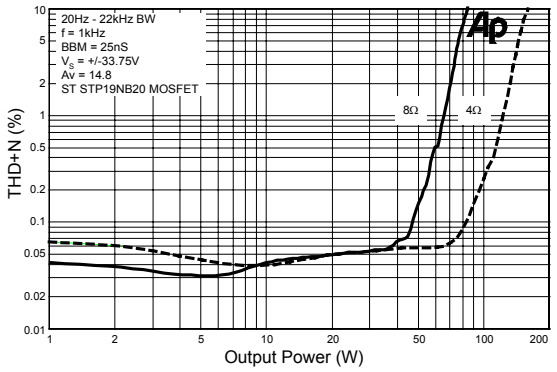


A-Weighted Noise FFT

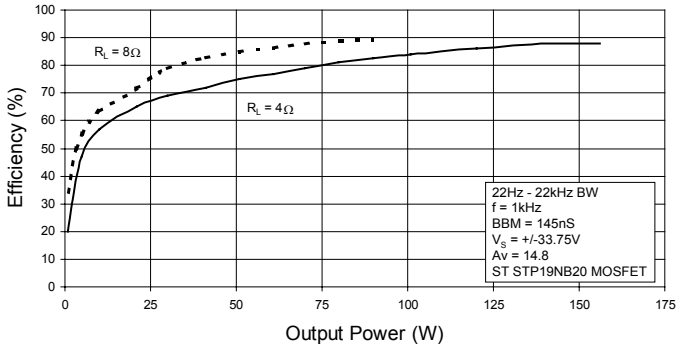


Typical Performance at Vs = +33.75V

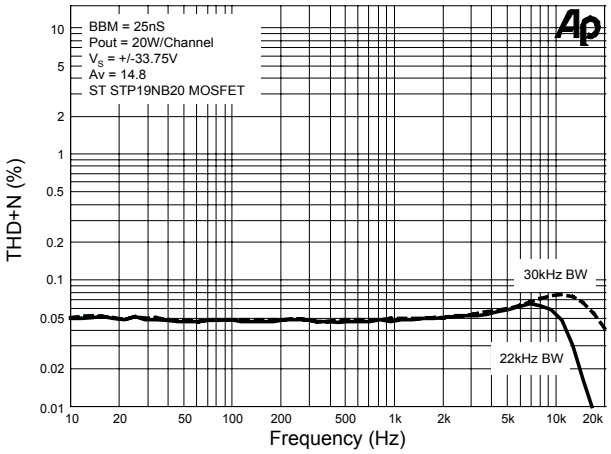
THD+N versus Output Power



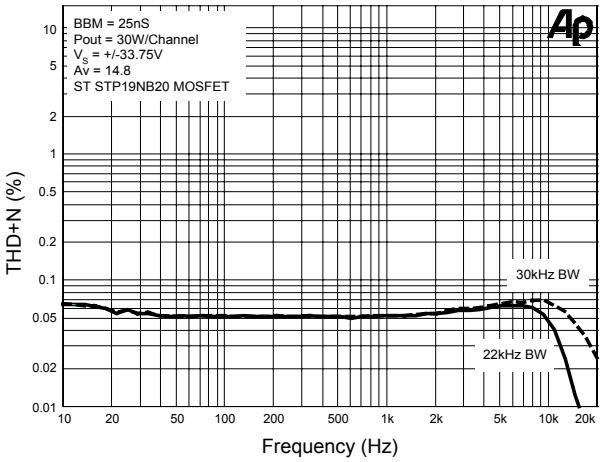
Efficiency versus Output Power



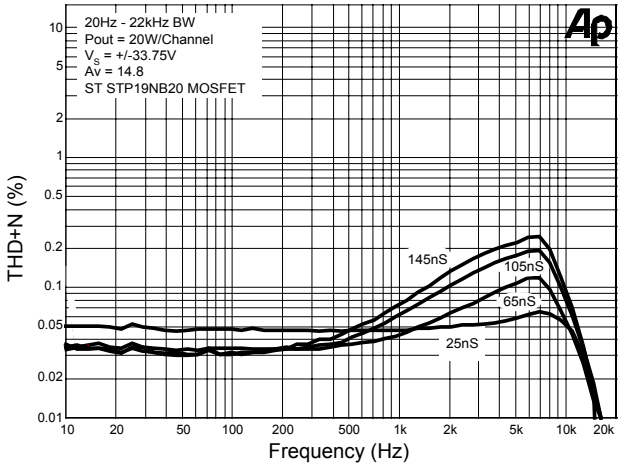
THD+N versus Frequency versus Bandwidth, R_L = 8Ω



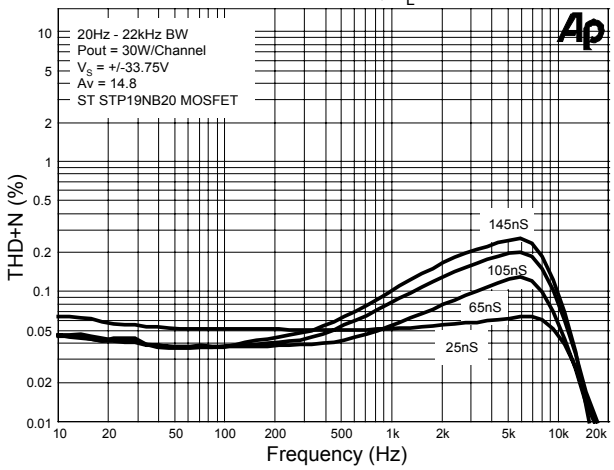
THD+N versus Frequency versus Bandwidth, R_L = 4Ω



THD+N versus Frequency versus Break Before Make, R_L = 8Ω

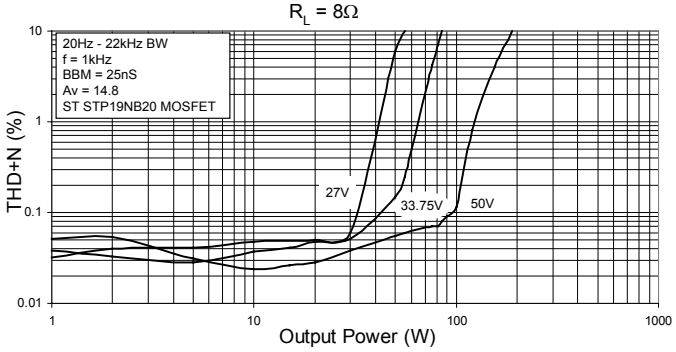


THD+N versus Frequency versus Break Before Make, R_L = 4Ω

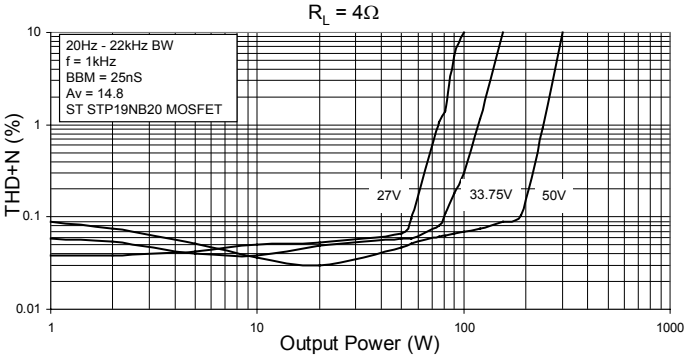


Typical Performance

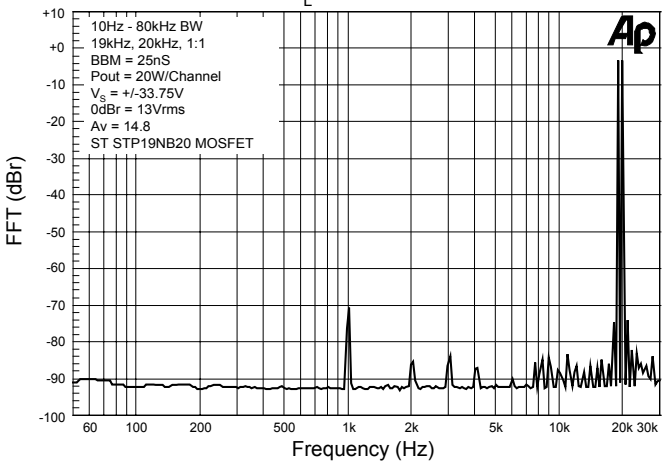
THD+N versus Output Power
versus Supply Voltage
$R_L = 8\Omega$



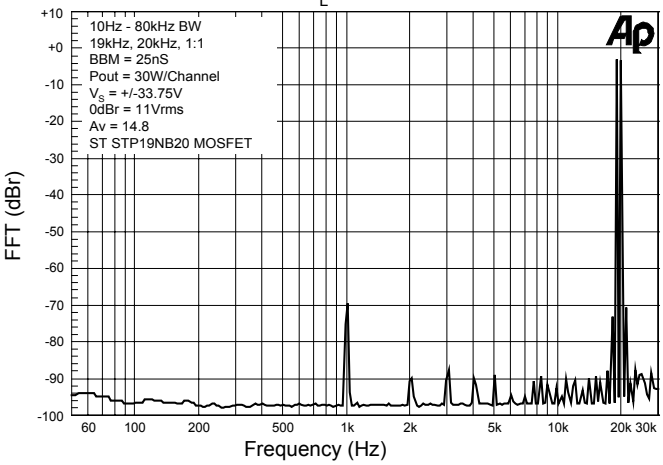
THD+N versus Output Power
versus Supply Voltage
$R_L = 4\Omega$



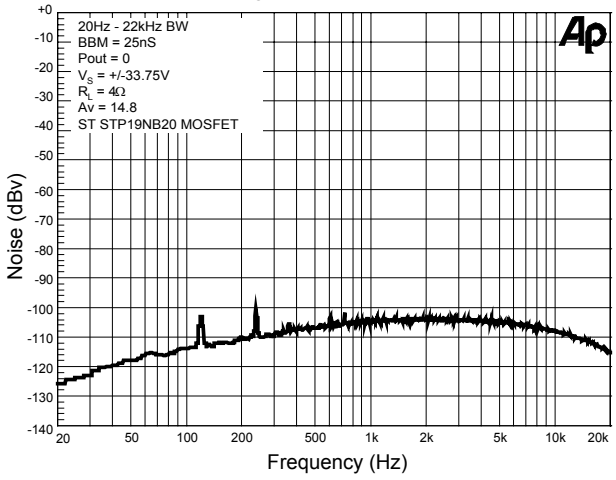
Intermodulation Performance
$R_L = 8\Omega$



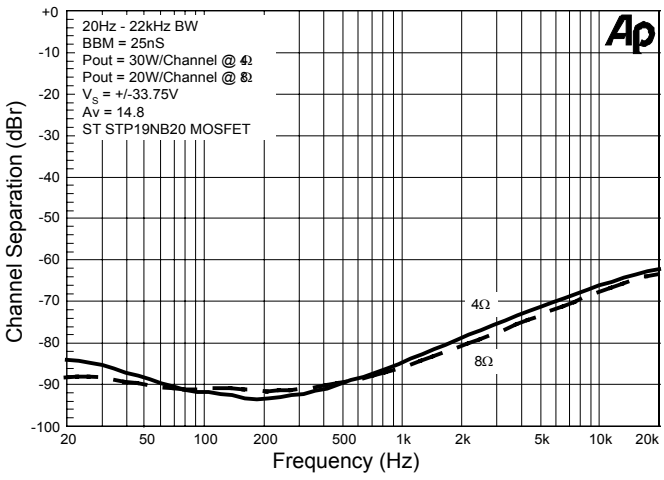
Intermodulation Performance
$R_L = 4\Omega$



A-Weighted Noise FFT



Channel Separation versus Frequency



Functional Description

TA0102A Amplifier Operation

Figure 3 is a simplified diagram of one channel (channel 1) of a TA0102A amplifier to assist in understanding its operation.

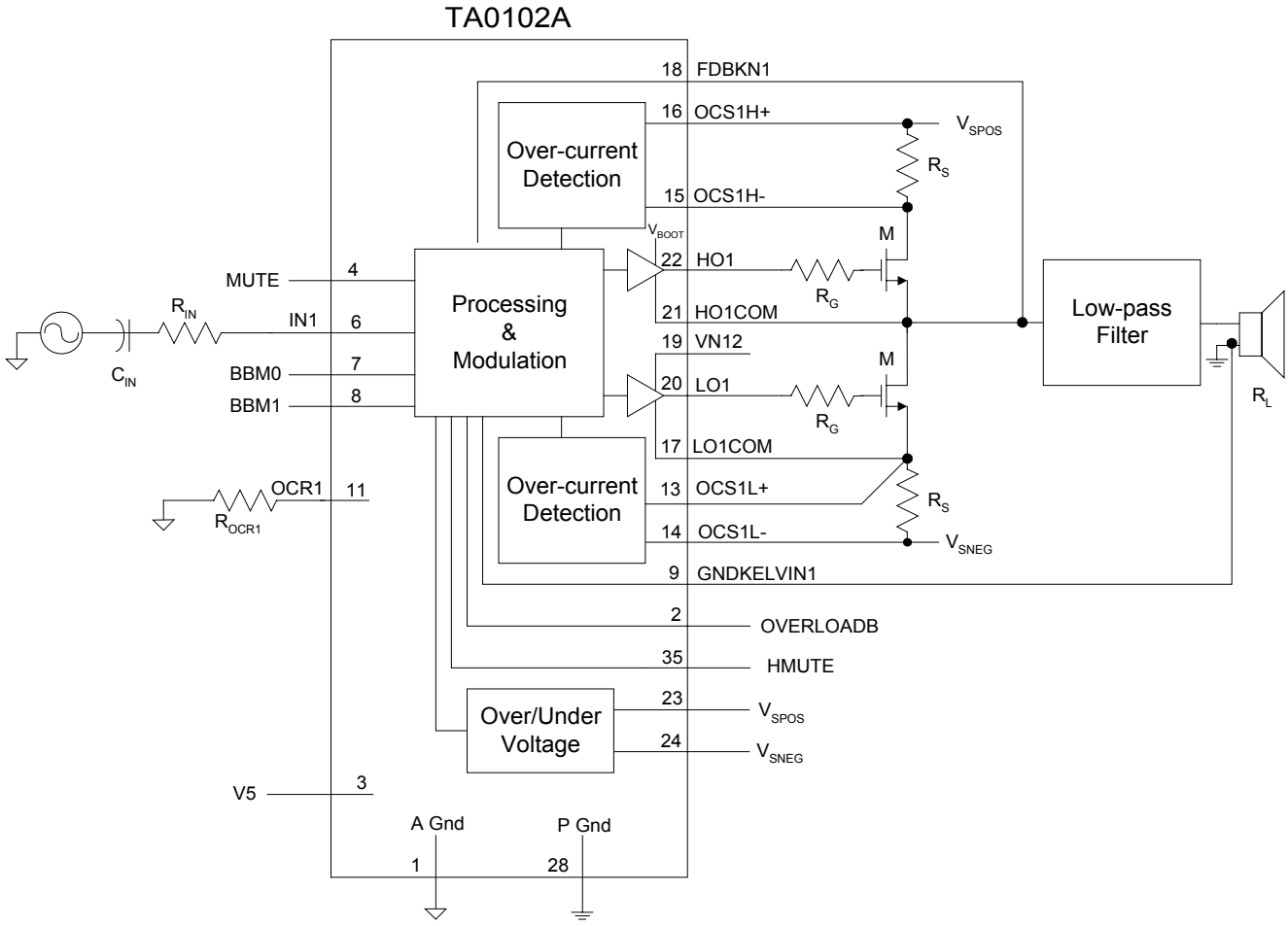


Figure 3. Simplified TA0102A Amplifier

The audio input signal (IN1) is fed into the processor internal to the TA0102A, where a modulation pattern is generated. This pattern is spread spectrum and varies between approximately 200kHz and 1.5MHz. Complementary copies of the switching pattern are level-shifted by the MOSFET drivers and output from the TA0102A where they drive the gates (HO1 and LO1) of external power MOSFETs that are connected as a half bridge. The output of the half bridge is a power-amplified version of the switching pattern that switches between V_{SPOS} and V_{SNEG}. This signal is then low-pass filtered to obtain amplified audio.

The processor portion of the TA0102A is operated from a 5-volt supply (between V5 and AGND). In the generation of the complementary modulation pattern for the output MOSFETs, the processor inserts a “break-before-make” dead time between when it turns one transistor off and it turns the other one on in order to minimize shoot-through currents in the MOSFETs. The dead time can be programmed by setting the break-before-make control bits, BBM0 and BBM1. Feedback information from the output of the half-bridge is supplied to the processor via FDBKN1. Additional feedback information to account for ground bounce is supplied via GNDKELVIN1.

The MOSFET drivers in the TA0102A are operated from voltages obtained from VN12 and LO1COM for the low-side driver, and V_{BOOT} (generated internal to the TA0102A) and HO1COM for the high-side. Only N-Channel MOSFETs are required for both the top and bottom of the half bridge. VN12 must be a stable 12V above V_{SNEG}. The gate resistors, R_G, are used to control MOSFET slew rate and thereby minimize voltage overshoots.

Over- and Under-Voltage Protection

The TA0102A senses the power rails through V_{SPOS} and V_{SNEG} for over- and under-voltage conditions. The over- and under-voltage limits are Vo and Vu respectively as specified in the Electrical Characteristics table. If the supply voltage exceeds Vo or drops below Vu, the TA0102A shuts off the output stages of the amplifiers and asserts a logic level high on HMUTE. The removal of the over-voltage or under-voltage condition returns the TA0102A to normal operation and returns HMUTE to a logic level low. Please note that the limits specified in the Electrical Characteristics table are at 25°C and these limits may change over temperature.

Over-current Protection

The TA0102A has over-current protection circuitry to protect itself and the output transistors from short-circuit conditions. The TA0102A uses the voltage across a resistor, R_S (measured via OCS1H+, OCS1H-, OCS1L+ and OCS1L-), that is in series with each output MOSFET to detect an over-current condition. R_S and R_{OCR} are used to set the over-current threshold. The OCS pins must be Kelvin connected for proper operation. See “Circuit Board Layout” in Applications Information for details. An over-current condition will cause the TA0102A to shut off the output stages of the amplifiers and supply a logic level high on HMUTE. The occurrence of an over-current condition is latched in the TA0102A and can be cleared by toggling the MUTE input or cycling power.

Overload

When logic low, the OVERLOADB pin indicates that the level of the input signal has overloaded the amplifier and that the audio output signal is starting to distort. The OVERLOADB signal is active only when an overload is present. The OVERLOADB signal can be used to control a distortion indicator light or LED through a simple buffer circuit.

Mute

When a logic high signal is supplied to MUTE, both amplifier channels are muted (both high- and low-side transistors are turned off) and a logic level high is output on the HMUTE pin. When a logic level low is supplied to MUTE, both amplifiers are fully operational and a logic level low is supplied on HMUTE. There is a delay of approximately 200 milliseconds between the de-assertion of MUTE and the un-muting of the TA0102A.

Application Information

Amplifier Gain and Input Resistor Selection

The value of the input resistor, R_{IN}, is based on the required voltage gain, A_V, of the amplifier according to:

$$A_V = 387 \times 10^3/(R_{IN} + 5000)$$

where R_{IN} = Input resistor value in ohms.

Input Capacitor Selection

C_{IN} can be calculated once a value for R_{IN} has been determined. C_{IN} and R_{IN} determine the input low-frequency pole. Typically this pole is set at 10Hz. C_{IN} is calculated according to:

$$C_{IN} = 1/((2\pi \times f_P)(R_{IN} + 5000))$$

where:
R_{IN} = Input resistor value in ohms.
f_P = Input low frequency pole (typically 10Hz).

DC Offset Adjust

While the DC offset voltages that appear at the speaker terminals of a TA0102A amplifier are typically small, Tripath recommends that any offsets during operation be nulled out of the amplifier with a circuit like the one shown connected to IN1 and IN2 in the Test/Application Circuit. Nulling should be performed with the inputs shorted to ground.

It should be noted that even after nulling, the DC voltage on the output of a TA0102A amplifier with no load in mute mode is approximately 2.5V. This offset does not need to be nulled. The output impedance of the amplifier in mute mode is approximately 10 KOhms. This means that the 2.5V drops to essentially zero when a typical load is connected.

Supply Voltage and Output Power

The relationship between the bipolar power supply voltage needed, V_S, for a given RMS output power, P_{OUT}, into a given load, R_L, at a given level of THD (total harmonic distortion) is approximated by:

$$V_S = (2 \times R_L \times P_{OUT})^{0.5}/(K \times R_L/(R_L + R_{ON} + R_S + R_{COIL}))$$

where:
R_{ON} = The at-temperature R_{DSON} of the output transistors, M.
R_{COIL} = Resistance of the output filter inductor.
R_S = Sense Resistor
K = THD Factor, a number fixed by the algorithms in the TA0102A's signal processor that provides the relationship between THD *at full output power* of the amplifier and V_S. K corresponds to THD at full output power as follows:

THD	K
0.1%	0.83
1%	0.95
10%	1.09

Typical measurement graphs of P_{OUT} versus supply voltage for various levels of THD are also included in this data sheet to help determine the supply voltage.

Bridged Operation

Note that the two channels of a TA0102A amplifier can be used to provide a single, bridged amplifier of almost four times the output power of one of the single-ended amplifier channels. To configure a bridged amplifier, the input to one TA0102A channel must be the inverted signal of the input to the other channel.

Low-frequency Power Supply Pumping

A potentially troublesome phenomenon in single-ended switching amplifiers is power supply pumping. This is caused by current from the output filter inductor flowing into the power supply output filter capacitors in the opposite direction as a DC load would drain current from them. Under certain conditions (usually low-frequency input signals), this current can cause the supply voltage to "pump" (increase in magnitude) and eventually cause over-voltage/under-voltage shut down. Moreover, since over/under-voltage are not "latched" shutdowns, the effect would be an amplifier that oscillates between on and off states. If a DC offset on the order of 0.3V is allowed to develop on the output of the amplifier (see "DC Offset Adjust"), the supplies can be boosted to the point where the amplifier's over-voltage protection triggers.

One solution to the pumping issue is to use large power supply capacitors to absorb the pumped supply current without significant voltage boost. The low frequency pole used at the input to the driver determines the value of the supply capacitor required. This works for AC signals only.

Another solution to the supply pumping problem uses the fact that music has low frequency information that is correlated in both channels (it is in phase). This information can be used to eliminate boost by putting the two channels of a TA0102A amplifier out of phase with each other. This works because each channel is pumping out of phase with the other, and the net effect is a cancellation of pumping currents. The phase of the audio signals needs to be corrected by connecting one of the speakers in the opposite polarity as the other channel.

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