SPF-3143Z

RoHS Compliant & Green Package

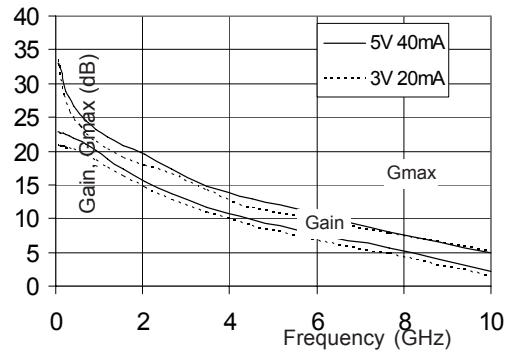
Low Noise pHEMT GaAs FET

Product Description

Sirenza Microdevices' SPF-3143Z is a high performance 0.5µm pHEMT Gallium Arsenide FET. This 600µm device is ideally biased at 3V, 20mA for lowest noise performance and battery powered requirements. At 5V, 40mA the device can deliver OIP3 of 32.5 dBm. It provides ideal performance as a driver stage in many commercial and industrial LNA applications.

The matte tin finish on Sirenza's lead-free package utilizes a post annealing process to mitigate tin whisker formation and is RoHS compliant per EU Directive 2002/95. This package is also manufactured with green molding compounds that contain no antimony trioxide nor halogenated fire retardants.

Typical Gain Performance



Product Features

- **Available in Lead free, RoHS compliant, & Green packaging**
- **DC-3.5 GHz Operation**
- **0.58 dB NF_{MIN} @ 2 GHz**
- **21 dB G_{MAX} @ 2 GHz**
- **+31 dBm OIP3 (5V,40mA)**
- **+17.7 dBm P1dB (5V,40mA)**
- **Low Current, Low Cost**
- **Apps circuits available for key bands**

Applications

- **Analog and Digital Wireless Systems**
- **3G, Cellular, PCS**
- **Fixed Wireless, Pager Systems**
- **Driver Stage for Low Power Applications**

Symbol	Parameters	Test Conditions V_{DS}=5V, I_{DQ}=40mA, 25C (unless otherwise noted)	Units	Test Frequency (GHz)	Min.	Typ.	Max.
G_{MAX}	Maximum Available Gain	$Z_S=Z_S^*$, $Z_L=Z_L^*$	dB	0.9		23.3	
				1.9		19.9	
NF_{MIN}	Minimum Noise Figure	$Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$	dB	0.9		0.36	
				1.9		0.58	
S_{21}	Insertion Gain	$Z_S=Z_L=50\Omega$	dB	0.9	18.2	19.7	21.2
NF	Noise Figure	Application Circuit	dB	1.9		0.8	1.0
Gain	Gain	Application Circuit	dB	1.9	14.1	15.6	17.1
OIP_3	Output Third Order Intercept Point	Application Circuit, Tone Spacing = 1MHz, Pout per tone = 0 dBm	dBm	1.9	30.5	32.5	
P_{1dB}	Output Power at 1dB Compression	Application Circuit		1.9	19.0	20.5	
V_P	Pinchoff Voltage	V_{DS} = 2V, I_{DS} = 0.6mA	V		-1.4	-1.0	-0.6
I_{DSS}	Saturated Drain Current	V_{DS} = 2V, V_{GS} = 0 V	mA			180	
g_m	Transconductance	V_{DS} = 2V, V_{GS} = 0 V	mS			210	
BVGSO	Gate-Source Breakdown Voltage	I_{GS}= 300 µA, drain open	V			-10	-7
BVGDO	Gate-Drain Breakdown Voltage	I_{GD}= 300 µA, source open	V			-12	-7
V_{DS}	Device Operating Voltage	drain-source	V				5.5
I_{DS}	Device Operating Current	drain-source	mA		38	40	42
R_{TH}, j-l	Thermal Resistance (junction - lead)	junction to lead	°C/W			200	

Junction Temperature Calculation

MTTF is inversely proportional to the device junction temperature. For junction temperature and MTTF considerations the device operating conditions should also satisfy the following expression:

$$P_{DC} < (T_J - T_L) / R_{TH}$$

where:

$P_{DC} = I_{DS} * V_{DS}$ (W)
T_J = Junction Temperature (C)
T_L = Lead Temperature (pin 2) (C)
R_{TH} = Thermal Resistance (C/W)

Biasing Details

The SPF-3143Z is a depletion mode FET and requires a negative gate voltage to achieve pinchoff. As such, power supply sequencing circuitry is strongly recommended to prevent damaging bias transients during turn-on. Active bias circuitry is also recommended to maintain a constant drain current from part-to-part.

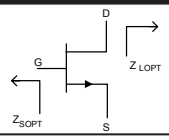
Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Current	I_{DSS}	180	mA
Forward Gate Current	I_{GSF}	600	µA
Reverse Gate Current	I_{GSR}	600	µA
Drain-to-Source Voltage	V_{DS}	7	V
Gate-to-Source Voltage	V_{GS}	<-3 OR >0	V
RF Input Power	P_{IN}	15	dBm
Storage Temperature Range	T_{stor}	-40 TO +150	C
Power Dissipation	P_{DISS}	325	mW
Junction Temperature	T_J	+150	C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page 1.

Peak RF Performance Under Optimum Matching Conditions

Freq (GHz)	V_{DS} (V)	I_{DQ} (mA)	NF_{MIN} [1] (dB)	Gmax (dB)	P1dB [2] (dBm)	OIP3 [3] (dBm)
0.90	3	20	0.25	21.5	15	29
	5	40	0.36	23.3	18	31
1.90	3	20	0.50	18.3	15	29
	5	40	0.58	19.1	18	31



[1] $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$, The input matching circuit losses have been de-emebedded.
[2] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$, where Z_{SOPT} and Z_{LOPT} have been tuned for max P1dB
[3] $Z_S=Z_{SOPT}$, $Z_L=Z_{LOPT}$, where Z_{SOPT} and Z_{LOPT} have been tuned for max OIP3
Note: Optimum NF, P1dB, and OIP3 performance cannot be achieved simultaneously.

Typical Performance - Noise Parameters

Freq (GHz)	V_{DS} (V)	I_{DS} (mA)	NF_{MIN} [4] (dB)	Γ_{OPT} Mag ∠ Ang	r_N	Gmax (dB)
0.90	3	20	0.25	0.70 ∠ 12.1	0.14	21.5
	5	40	0.36	0.66 ∠ 12.6	0.14	23.3
1.90	3	20	0.50	0.46 ∠ 26.4	0.13	18.3
	5	40	0.58	0.38 ∠ 28.1	0.13	19.1

[4] $Z_S=\Gamma_{OPT}$, $Z_L=Z_L^*$, NF_{MIN} is a noise parameter for which the input matching circuit losses have been de-emebedded. The device was mounted on a 0.010" PCB with plated-thru holes close to pins 2 and 4.

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed. ESD class rating 1B.

MSL (Moisture Sensitivity Level) **Rating: Level 1**

Pin Description

Pin #	Function	Description
1	Gate	RF Input / Gate Bias
2	Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output / Drain Bias
4	Source	No Connection / Recommend grounding pin

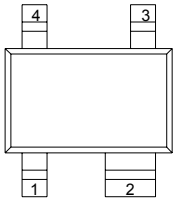
Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SPF-3143Z	7"	3000

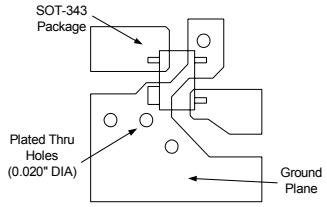
Part Symbolization

The part will be symbolized with the "F31Z" designator and a dot signifying pin 1 on the top surface of the package.

Pin Designation

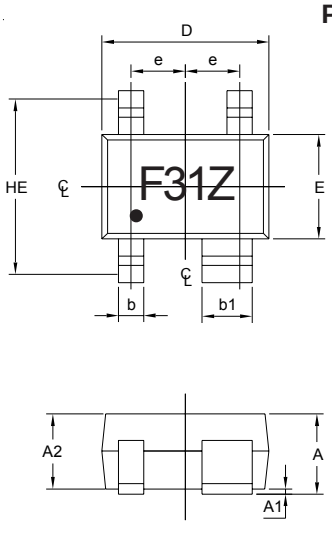


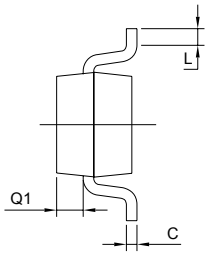
Recommended PCB Layout



Use multiple plated-through vias holes located close to the package pins to ensure a good RF ground connection to a continuous groundplane on the backside of the board.

Package Dimensions





NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. ALL SPECIFICATIONS COMPLY TO EIAJ SC70.
5. DIE IS FACING UP FOR MOLD AND FACING DOWN FOR TRIM/FORM. ie :REVERSE TRIM/FORM.
6. PACKAGE SURFACE TO BE MIRROR FINISH.

SYMBOL	NOM
E	1.25
D	2.05
HE	2.10
A	1.05
A2	0.90
A1	0.05
Q1	0.25
e	0.65
b	0.375
b1	0.675
c	0.14
L	0.20